A Scalable High-Frequency Noise Model for Bipolar Transistors with Application to Optimal Transistor Sizing for Low-Noise Amplifier Design

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Abstract—Fully scalable, analytical HF noise parameter equations for bipolar transistors are presented and experimentally tested on high-speed Si and SiGe technologies. A technique for extracting the complete set of transistor noise parameters from Y parameter measurements only is developed and verified. Finally, the noise equations are coupled with scalable variants of the HICUM and SPICE-Gummel–Poon models and are employed in the design of tuned low noise amplifiers (LNA’s) in the 1.9-, 2.4-, and 5.8-GHz bands.

Index Terms—Bipolar transistor, compact modeling, low noise, low-noise amplifier, low-noise transistor design, noise figure, noise matching, noise measurements, radio-frequency integrated circuit design, SiGe heterojunction bipolar transistor.

I. INTRODUCTION

The recent boom in wireless consumer applications has emphasized the requirement for low-cost, highly integrated RF parts. Steady improvement in transistor performance and desire for higher level of integration have led to the increased application of silicon technology. Since substrate and interconnect losses are significantly higher in Si than in GaAs, Si RF circuit design should target the optimization of the size of transistors in order to simplify matching, rather than design the matching circuit around a given transistor. Such an approach requires a physically based, scalable compact model for bipolar transistors [1], as well as accurate, closed-form noise parameter equations, suitable for circuit design.

In the first part, expressions for the four noise parameters of a bipolar transistor are derived. The accuracy of these equations is investigated using SPICE-Gummel–Poon (SGP) modeled and measured transistor noise data. Next, a technique is presented for extracting the complete set of noise parameters from measured Y parameters only. It avoids the inaccuracy of on-wafer noise parameter measurements which is especially severe for small geometry devices or devices biased in the sub-mA range. Finally, scalable variants of the SGP and HICUM models [2], in conjunction with the new noise parameter equations, are applied in the design of tuned low-noise amplifiers (LNA’s) in the 2–6 GHz band.

II. NOISE PARAMETER EQUATIONS AND MEASUREMENTS

A. Theoretical Background

Equations (1)–(3) define the noise resistance \( R_n \), optimum source admittance \( Y_{\text{SOP}} \), and minimum noise figure \( F_{\text{MIN}} \) of a two-port with respect to its noise correlation matrix entries \( C_{A11}, C_{A12}, \) and \( C_{A22} \) [3]–[4]. The latter, in turn, are expressed in (4)–(6) as functions of the input-referred noise voltage \( v_i^2 \) and noise current \( i_i^2 \) sources of the two-port, as well as of the \( Y \) parameters of the noise-free two-port

\[
R_n = C_{A11} \tag{1}
\]

\[
Y_{\text{SOP}} = C_{A22} + jB_{\text{SOP}} = \frac{C_{A22}}{C_{A11}} - \frac{\text{Im}(C_{A12})}{C_{A11}} \tag{2}
\]

\[
F_{\text{MIN}} = 1 + 2\text{Re}(C_{A12}) + C_{A11}G_{\text{SOP}} \tag{3}
\]

\[
C_{A11} = \frac{\langle v_i^2 \rangle}{4kT\Delta f} = \frac{4kT\Delta f |Y_{21}|^2}{\langle i_i^2 \rangle} + (r_E + r_B) \tag{4}
\]

\[
C_{A21} = C_{*A12} = \frac{\langle v_i^2 \rangle}{4kT\Delta f} = \frac{Y_{11} \cdot \langle i_i^2 \rangle}{4kT\Delta f |Y_{21}|^2} \tag{5}
\]

\[
C_{A22} = \frac{\langle i_i^2 \rangle}{4kT\Delta f} = \frac{|Y_{11}|^2 \cdot \langle v_i^2 \rangle}{4kT\Delta f} + \frac{\langle v_i^2 \rangle}{4kT\Delta f} \tag{6}
\]

Equation (3) is a recast of the original formula in [3]. Fig. 1 illustrates the simplified small-signal and noise equivalent circuit and the two-step approach used in the derivation of the noise parameters in the case of a bipolar transistor. The noise current sources \( i_i^2 \) represent the internal shot noise sources of the bipolar transistor. After substituting (4)–(6) into (1)–(3), (7)–(9) are obtained which describe the bipolar transistor noise parameters as functions of the internal shot noise current sources, transistor \( Y \) parameters, series emitter resistance \( r_E \), and total base resistance \( r_B \) in a manner similar to that employed for GaAs MESFET’s [5]. The bias current...
dependence of the noise parameters appears in explicit form via the $I_B$ and $I_C$ terms, and also implicitly in $r_B$ and in the $Y$ parameters. $V_T$ represents the thermal voltage. In the derivation of (7)–(9) it is assumed that the base and collector noise currents are uncorrelated. This is equivalent to neglecting the imaginary part of the transconductance $g_m e^{-j \omega \theta}$, a reasonable simplification up to frequencies approaching $f_T/2$ [6]. $\theta$ is the transconductance delay, typically 40–60% of the transit time [7]. Despite this assumption, the input-referred noise sources $\nu_n^2$ and $\nu_e^2$ remain correlated and are modeled accordingly [see (8) and (9) at the bottom of the page]

$$R_n = \frac{I_C}{2V_T |V_{21}|^2} + (r_e + r_B). \tag{7}$$

Similarly, Si MOSFET noise parameters can be obtained by making the following substitutions in (7)–(9):

$$\left( \frac{I_C}{2V_T} - \frac{2}{3} g_m \right); (I_B \rightarrow 0); (r_e + r_B) \rightarrow (R_S + R_C).$$

For the bias currents and frequency range used in wireless design, the bipolar transistor noise parameter equations can be recast in easy-to-interpret formats (10)–(13). These can be employed to tailor the device size—typically only the emitter length $L_E$—to achieve optimal low-noise matching at the desired frequency and input impedance. As indicated by (10) and (11), the noise resistance and optimum noise admittance scale as $I_E^{-1}$ and $I_C$, respectively. Alternatively, the real part of the optimum noise impedance $R_{SOPT}$, given by (12), scales as $I_E^{-1}$ and decreases with increasing frequency, $f$.

$$R_n \approx \frac{n^2 V_T}{2LC} + (r_e + r_B) \sim I_E^{-1} \tag{10}$$

$$Y_{SOPT} \approx \frac{f_T}{f}\left( \frac{I_C}{2V_T} \left( r_e + r_B \right) \left( 1 + \frac{f_T^2}{4\lambda_0^2} \right) \right) - \frac{n^2}{4} - \frac{j n}{2} \tag{11}$$

$$R_{SOPT} \approx \frac{R_n f_T}{f} \times \left( \frac{I_C}{2V_T} \left( r_e + r_B \right) \left( 1 + \frac{f_T^2}{4\lambda_0^2} \right) \right) + \frac{\nu_n^2}{4} + \frac{1}{4} \left( 1 + \frac{f_T^2}{4\lambda_0^2} \right) \tag{12}$$

where $\beta_0$ is the dc current gain. $n$ is the collector current ideality factor, approximately equal to one, except under high current injection bias when its value can exceed 1.2. As long as the length-to-width ratio ($L_E/w_E$) of the emitter stripe is larger than ten, $F_{MIN}$ remains invariant to changes in emitter length and increases almost linearly with frequency

$$F_{MIN} \approx 1 + \frac{n}{\beta_0} + \frac{f}{f_T} \times \sqrt{\frac{2I_C}{V_T} (r_e + r_B) \left( 1 + \frac{f_T^2}{4\lambda_0^2} \right) + \frac{n^2}{4} \left( 1 + \frac{f_T^2}{4\lambda_0^2} \right)}. \tag{13}$$

All noise parameters are nonlinear functions of emitter width $w_E$ via the $I_C(r_e + r_B)$ term.

### B. Experimental Validation

In order to verify the noise parameter equations, automated noise parameter measurements were carried out in the 2–6 GHz range using an NPS on-wafer measurement system from ATN Microwave Inc. Devices with variable widths, lengths, and with single- or multi-stripe geometries have been investigated in three technologies: 1) a single-poly BiCMOS...
Fig. 2. ATN-NP5, on-wafer measured minimum noise figure as a function of drain/collector current density for state-of-the-art Si MOSFET’s, Si BJT’s, and SiGe HBT’s with 0.5-μm minimum feature size. All measurements were performed at 1.6 GHz. The unit gate finger width of the multifinger MOSFET’s is 10 μm. The series and parallel parasitics associated with probing pads were not de-embedded. The drain current density in MOSFET’s is obtained as \( I_D/(W \times L) \).

Fig. 3. ATN-NP5 on-wafer measured minimum noise figure \( F_{\text{MIN}} \), optimum noise resistance \( R_{\text{opt}} \), and associated gain \( G_A \), as functions of emitter length for NT25 Si BJT’s with 0.5-μm emitter width biased at the minimum noise current density. All measurements were performed at 1.6 GHz. The series and parallel parasitics associated with probing pads were not de-embedded. Their contribution becomes comparable to the series base and emitter resistances of the transistor as the emitter length increases.

Fig. 4. ATN-NP5 on-wafer measured minimum noise figure \( F_{\text{MIN}} \), normalized to 50 Ω noise resistance \( R_{\text{ac}} \), and associated gain \( G_A \), as functions of emitter width for NT25 Si BJT’s with single-stripe 20-μm long emitters, two base, and two collector contacts, biased at the minimum noise current density. The series and parallel parasitics associated with probing pads were not de-embedded. The label nn122x200 represents the standard NT25 npn nomenclature, where the first digit represents the number of emitter stripes (one), the second digit describes the number of base metal contacts (two) and the third digit stands for the number of collector contacts (two). \( x \) describes the variable emitter width, whereas 200 stands for the emitter stripe length in tenths of micrometers (i.e., 20 μm in this case).

While noise parameters are available from the postprocessor of microwave circuit simulators such as HP-EESOF’s LIBRA, only equivalent noise voltages and currents can be modeled directly using SPICE-like simulators. To circumvent this problem, (7)–(9) were included in an HSPICE deck and, in conjunction with the MEASURE statement, were employed to simultaneously compute \( F_{\text{MIN}} \), \( f_T \), \( f_{\text{MAX}} \), \( R_{\text{in}} \), and \( Y_{\text{scp}} \) as functions of \( I_C \) in a single simulation run. The role of the simulator is to provide accurate, nonapproximated \( Y \) parameters and \( r_B(I_C) \) characteristics. The HSPICE-calculated noise parameters were found to agree within 0.25 dB, up to 10 GHz, with those generated by LIBRA.

Measured and SGP-modeled \( F_{\text{MIN}} \), associated power gain \( G_A \), \( f_T \), and \( f_{\text{MAX}} \) are compared in Fig. 5 as functions of the collector current for a 0.65 \( \times \) 25 μm\(^2\) single-poly bipolar transistor. The agreement is well within the typical on-wafer noise measurement error. The minimum noise current density is almost independent of \( V_{\text{CE}} \) and emitter length but increases
weakly with frequency. It is typically six to ten times smaller than the peak \( f_T \) current density. The simulation results were obtained with a set of SGP model parameters extracted from dc and \( S \) parameter measurements on the modeled device. No fitting of the noise measurement data was performed, thus confirming the accuracy of (7)–(9).

The measured and modeled frequency dependence of the noise parameters is plotted in Fig. 6 for a 0.5 \( \times \) 15 \( \mu \)m\(^2\) SiGe HBT biased close to the minimum noise current density \( J_C \). The rate of \( F_{\text{MIN}} \) degradation with frequency is inversely proportional to \( f_T \), highlighting the requirement for transistors with large cutoff frequencies if low noise operation at high frequency is desired. The scatter in the measured data is due to the fact that the current NP5 system is unable to provide a controlled number of high impedance source states in a specified region of the Smith chart, as required by a small device with typical optimum source reflection coefficients larger than 0.8. In general, noise parameter measurements are not sufficiently accurate to provide a reliable extraction of the base resistance. As described in the next section, this can be more readily achieved from \( Z \) parameter measurements.

### III. EXTRACTION OF TRANSISTOR NOISE PARAMETERS FROM \( Y \) PARAMETER MEASUREMENTS

Since noise-specific parameters are not present in (7)–(9), it follows that noise measurements are not necessary to obtain the transistor noise parameters. This remains valid even if correlation between the base and collector noise currents is considered [6]. Consequently, we propose to use (7)–(9) to determine the noise parameters of the transistor \( F_{\text{MIN}}, R_B, Y_{\text{SEP}} \), from measured \( Y \) parameters only, eliminating the need for lengthy and “noisy” on-wafer noise measurements. Such a possibility of measuring the 50-\( \Omega \) noise figure has been suggested earlier [11]. Here, it is extended to the complete set of noise parameters and it is verified in experiments. \( r_E \) and \( r_B(I_C) \), which are needed in addition to the \( Y \) parameters, are obtained as follows. \( r_E \) is determined from the frequency and collector current dependencies of the real part of the measured \( Z_{12}(I_C) \) characteristics, at low \( V_{CE} \) bias (<1 V) in order to avoid self-heating effects. First the real part of \( Z_{12}(I_C) \) is averaged over the 0.1 GHz ... 1 GHz range for each bias point \( I_C \). Then \( r_E \) is extracted by linear interpolation from the \( y \)-axis intercept of the averaged \( \text{Re}(Z_{12}) \) versus \( 1/I_C \) curve [12]. Similarly, the collector current-dependent base resistance \( r_B(I_C) \) is obtained from the real part of \( (Z_{11} - Z_{12}) \), averaged at frequencies below 1 GHz, where the impact of the substrate resistance is negligible. No model-related assumptions are made during the extraction about the shape of the \( r_B(I_C) \) characteristics. An ac-measured, model-independent, and noise-relevant \( r_B(I_C) \) is thus plugged in (7)–(9) to obtain the measured noise parameters.

This technique was implemented in HP-EESOF’s device characterization software package, ICCAP, and provides \( f_T, f_{\text{MAX}}, F_{\text{MIN}}, R_B, Y_{\text{SEP}} \), and \( G_A \) data from the same routine set of measured \( Y \) parameters. It also elegantly solves the nontrivial noise parameter de-embedding problem since the \( Y \) parameters have already been de-embedded using a conventional two-step shunt-series technique. Fig. 7 presents measured (from \( Y \) parameters) and modeled data for the SiGe HBT emphasizing the impact of the \( r_B(I_C) \) model on \( F_{\text{MIN}} \). The agreement between the \( Y \) parameter-derived noise measurements and the conventional noise measurements in Fig. 6 is very good and there is no measurement scatter.

Two base resistance models were considered in the simulated characteristics: a) the usual SGP base resistance model for the internal, bias-dependent base resistance term \( r_{\text{int}}(I_C) \) (with \( R_{\text{BM}}, R_B, \text{and } R_{\text{IRB}} \)) to which a constant external term \( R_{\text{BX}} \) is added (Fig. 8), and b) a constant resistance model with \( R_B = R_{\text{BM}}. \) In the case of the constant \( r_B \) model, the base resistance was set to more accurately reflect the value at large current bias (peak \( f_T \)). In the latter case, the predicted noise figure is optimistic for most of the bias current range. In the case of the bias-dependent SGP base-resistance model, the agreement with the measurements is excellent. The plots indicate that the impact of the base resistance model on the minimum noise figure is only significant at collector currents below the minimum noise current density, where the transistor noise is
Fig. 7. Measured (from Y parameters) versus SGP-modeled $f_T$, $f_{MAX}$, and $F_{MIN}$ versus $I_C$ characteristics for 0.5 × 15 μm² SiGe HBT, showing impact of the base resistance model on the minimum noise figure.

In this paper, the SGP base resistance model is obtained as follows: $R_B$ is analytically calculated from dc pinched-base resistance measurements and transistor geometry, $R_{BRM}$ is set to 0.001 Ω, while $R_{BR}$ and $R_{BX}$ are extracted from the $\Re\{Z_{11} - Z_{12}\}$ and $f_{MAX}(I_C)$ characteristics, as described above. This combined dc and ac-extraction technique, involving highly accurate measurements, appears to provide $r_{BP}(I_C)$ characteristics that, coupled with the appropriate distributed equivalent circuit (Fig. 8), match both the ac (i.e., $\Re\{Z_{11} - Z_{12}\}$, $f_{MAX}$) and the noise behavior of the transistor. The very same $R_B$ and $R_{BX}$ values are used in the HICUM model, but the $r_{BP}(I_C)$ dependence follows device physics more closely [2].

IV. SCALABLE MODEL IMPLEMENTATION AND VERIFICATION

The ability to predict the impact of (statistical) emitter width and length variations on the noise parameters depends on the availability of a physically based, scalable compact model. In this paper, geometry- and process-scalable variants of HICUM [1] and of the SGP models have been used. The scalable HICUM model has been recently described in detail [1]. In the case of the SGP model, the subcircuit presented in Fig. 8 was employed. In addition to the core vertical npn model, it uses external diodes, resistors, and capacitors to reflect the distributed nature of the base resistance and the physical partitioning of the base-emitter and base-collector capacitances [13]. The main features of the scalable SGP model are summarized below.

i) An external base-emitter diode is used to account for the different grading coefficients of the voltage dependence of the area and periphery components of the base-emitter capacitance.

ii) The part of the base-collector capacitance corresponding to the selectively implanted collector (SIC) region $\alpha_{bci} + \alpha_{bic}$ is captured in the internal transistor equivalent circuit whereas the epitaxial part of the collector capacitance $\alpha_{exc}$ is modeled using the external base-collector diode.

iii) The base resistance is split in a bias-dependent $r_{Bd}$ and a bias-independent term $R_{BX}$.

iv) In order to account for the series resistance $R_S$ associated with the collector-substrate region, and to allow for the physical partitioning of the collector resistance and collector-substrate capacitance, an external collector-substrate diode is employed. Even though the value of $R_S$ varies with the number and position of the substrate contacts, its accurate extraction is important as it affects $f_{MAX}$ and, depending on the extraction technique, $r_B$ and even $f_T$.

v) Bias-independent oxide capacitances associated with the emitter poly overlap of the base $C_{EOX}$ and with the base poly overlap of the field oxide $C_{OX}$ are deployed between the base and the emitter and between the base and the collector, respectively.

vi) The scaling of the low current transit time parameter $T_F$ with emitter size is implemented as in HICUM using (8) of [1].

vii) The large current transit time parameter $ITF$ is scaled with emitter area and also accounts for collector current spreading via the same function $f_{CS}$ as HICUM, described by (20) of [1].

viii) Weak avalanche multiplication is implemented using the same equation as in HICUM.

ix) Process scaling is achieved by physically relating area and periphery components of junction capacitances, saturation currents, transit time parameters, internal and external resistances to the pinched base resistance, SIC region resistance, poly sheet resistances, and oxide capacitances.
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Fig. 9. Measured (symbols) versus HICUM- (solid lines) and SGP- (dashed lines) modeled $f_T$ versus $I_C$ characteristics for “nominal” NT25 Si BJT’s biased at $V_{CE} = 1$ V.

x) All model parameters are derived as functions of emitter geometry and number of emitter, base, and collector contacts, and these functions are implemented as a preprocessor in HSPICE and ELDO decks.

Measured and HICUM- and SGP-modeled $f_T$ and $F_{MIN}$ characteristics are investigated in Figs. 9 and 10, respectively, for different transistor geometries on a “nominal” NT25 wafer at $V_{CE} = 1$ V. The error between measured and SGP and HICUM predicted characteristics is less than 7% over all geometries and over the entire bias current range up to more than two times the peak $f_T$ current density. Included in this error are random emitter width variations across the die, typically up to 5%, as well as measurement and de-embedding errors, estimated at 2–3%. This kind of accuracy is also obtained for other $V_{CE}$ bias values ranging from 0.5 V to 3.3 V. The SGP and HICUM model parameters were calculated from the same set of process and geometry data. There was no individual “tweaking” of the model parameters to better fit the characteristics of each transistor. In the low-noise regime, HICUM- and SGP-modeled transistor characteristics are practically indistinguishable. Because of the more sophisticated transit time model, HICUM is slightly more accurate than the SGP model with respect to $f_T$ scaling with transistor geometry at moderate and large currents. In the high-current regime, the dc characteristics are affected by self-heating effects, but the latter do not significantly impact $f_T$ versus $I_C$ characteristics. At present, self-heating effects are only accounted for in the HICUM model. The results in Figs. 9 and 10 establish the accuracy of the scalable HICUM and SGP models and demonstrate their applicability in a new bipolar circuit design philosophy where the transistor geometry becomes part of the design space.

V. APPLICATION TO LNA DESIGN

Finally, the noise parameter equations and the scalable SGP model are applied to the design of tuned LNA’s at 1.9, 2.4, and 5.8 GHz using Si and SiGe double-poly bipolar transistors. Present-day tuned LNA and mixer circuits for wireless systems often trade off noise and input impedance matching [14], [15]. This tradeoff is sometimes caused by the fact that the size of bipolar transistors is not traditionally considered as a design variable which can be continuously varied and optimized in a SPICE deck just like any other circuit element. In other situations, typical for GaAs-based technologies where the importance of optimal noise biasing and matching is well established [16]–[18], the lack of sufficiently accurate physical and scalable transistor models make such an approach unreliable. In the case of Si MOSFET’s, where transistor width is a ubiquitous design variable, high-frequency noise performance is at best poorly understood and modeled. To the best of these authors’ knowledge, an algorithmic design methodology with an optimal and unique solution to the noise- and input-impedance matching problem has not yet been developed. Instead, a passive network is designed around a given transistor in order to achieve noise matching and/or impedance matching [14], [15]. The passive network itself contributes losses and hence degrades the noise figure. The losses in the passive network increase as the network becomes more complicated and are particularly severe on silicon substrates. For this very reason, in Si RF IC’s the matching circuitry is typically left off-chip [15].

Examination of (11) shows that the optimum noise conductance $G_{SOPT}$ is different from the input conductance, whereas the optimum noise susceptance $B_{SOPT}$ is equal to the complex conjugate of the input susceptance of the device. This is a fundamental characteristic of both bipolar and field-effect transistors and underlies the requirement for separate treatment of matching the real part of the input impedance and the real part of the optimum noise impedance. The goal of the new design philosophy detailed below is to obtain simultaneous noise and input impedance matched circuits. It is applicable to both bipolar and FET circuits.

In order to minimize the losses in the passive network around the transistor, the size of the transistor is first designed so that the transistor becomes noise matched to the characteristic impedance of the system, typically 50 Ω, at the
desired frequency. Because the transistor is an active device, noise matching is achieved without losses and without noise figure degradation. Since the task of noise matching is removed from the passive network, the latter becomes simpler and less lossy. This can be labeled the low-noise-matched transistor design stage. Finally, to complete the circuit, a minimal passive network with two low-loss inductors is designed to provide input impedance matching with the lowest possible degradation of the overall noise figure. This corresponds to the passive matching network design stage.

A. Low-Noise-Matched Transistor Design

The transistor design stage first involves finding the optimal noise current density $J_C$ from (9) using the HSPICE deck, as shown in Fig. 11. As mentioned in Section II, the minimum noise figure and the optimum noise current density are practically independent of emitter length. The emitter length is then adjusted so that the optimum source resistance $R_{SOP}$ equals $Z_0$ (50 $\Omega$) at the minimum noise current density and at frequency $f$, as expressed in (12) and illustrated schematically in Fig. 12. After these two steps, the transistor size and its bias current are determined. The real part of the optimum noise impedance is now matched to 50 $\Omega$ without having degraded the minimum noise figure.

B. Passive Matching Network Design

An emitter inductor $L_E$ is added to match the real part of the input impedance to $Z_0$ [14], [18]  

$$L_E \approx \frac{Z_0}{2\pi f_T}. \quad (14)$$

It can be demonstrated using the theory of correlated noise sources in series-series feedback circuits [16] that, if lossless, $L_E$ does not change the value of $R_{SOP}$ but that it does affect the optimum source reactance $X_{SOP}$. For the combined transistor-emitter inductor structure, the latter becomes  

$$X_{SOP} \approx \frac{n R_{SOP} f_E}{2 X_T (r_E + r_B)} \left(1 + \frac{r_E}{X_T f_E^2}\right) + \frac{r_B}{X_T} \left(1 + \frac{r_B}{X_T f_B^2}\right)$$

Simultaneous noise and input impedance match is finally obtained by connecting an inductor $L_B$ in the base. It cancels out the reactance due to the input capacitance $C_{in}$ of the device, and, at the same time, it transforms the optimum noise reactance of the amplifier to 0 $\Omega$.  

$$L_B \approx \frac{1}{\omega^2 C_{in}} - L_E. \quad (16)$$

The matching network design stage is schematically shown in Fig. 13.

This design methodology guarantees optimal noise and input impedance match with the simplest matching network. An LNA design can be completed by adding a suitable matching network in the collector in order to maximize the power gain [18], [19]. Simulation results obtained with LIBRA are shown in Fig. 14. Table I illustrates several design examples at 1.9, 2.4, and 5.8 GHz. Ideal (lossless) inductors were assumed. As expected from the noise parameter equations, the optimal transistor size and bias current decrease with increasing frequency. At 5.8 GHz the SiGe HBT version is
predicted to have lower noise (mostly due to the higher $f_T$) and higher gain (because of higher $f_{MAX}$) while dissipating less power than the corresponding Si bipolar circuit.

Single transistor test structures with emitter inductors only, and with both base and emitter inductors, were fabricated in the NT25 Si bipolar process at 1.9, 2.4, and 5.8 GHz. The measured data confirmed the simultaneous noise and input impedance match. The input return loss was better than 19 dB in all cases. Fig. 15 shows the measured input impedance and associated gain for a single transistor structure with on-chip emitter and base inductors as a function of pinched-base resistance (PBR) for NT25 bipolar transistors.

VI. CONCLUSION

The capability of scalable variants of the SGP and HICUM models to accurately predict noise parameters was demonstrated using measurements and simulations on three different high-speed Si and SiGe technologies. A technique for extracting noise parameters from $S_{II}$ parameter measurements was described. Finally, a design methodology for low-noise amplifiers was illustrated with the goal of optimizing the
emitter geometry in order to minimize matching circuit losses and overall noise figure. In essence, this design methodology allows for the design of transistors that have the real part of the optimum noise impedance equal to 50 \( \Omega \) at the desired frequency of operation.

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From 1983 to 1993, he was with the Semiconductor Devices and Integrated Circuits Group at the Ruhr-University Bochum where his main activities included compact modeling and parameter extraction for high-speed bipolar transistors and development of a mixed-mode three-dimensional device simulator as well as a CAD tool for predictive circuit design and optimization. The work was financially supported by the German Research Society, Telefunken microelectronic (TEMIC), and Siemens. From 1993 to 1996, he was with Northern Telecom and BNR, Ottawa, ON, Canada, first as a Senior Member of Scientific Staff, and later as Team Leader and Advisor. He was responsible for bipolar transistor modeling, simulation, and parameter extraction. Also, in 1994, he was appointed Adjunct Research Professor at the Carleton University, Ottawa, where he gave a graduate course on bipolar transistor modelling for integrated circuit design in 1995 and 1996. In 1996, he joined Rockwell Semiconductor Systems, Newport Beach, CA, as a Group Leader. He has been responsible for establishing the RF Device Modelling Group which is responsible for developing compact models for semiconductor devices and related parameter extraction methodologies, including both bipolar and CMOS high-speed/high-frequency applications.

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Greg E. Babcock is completing the undergraduate degree in electrical engineering at Queen’s University, Kingston, ON, Canada.

In May 1996 he joined Nortel Technology, Ottawa, ON, for a 16-month internship, where he performed high-frequency (0.1–26.1 GHz) measurements on high-speed bipolar and FET technologies. In addition, he has aided in the parameter extraction and verification of the aforementioned technologies. During his stay with Nortel Technology he has fostered a strong interest in device physics, which he intends to apply towards RF circuit design.

David L. Harame (S’77–M’83) was born in Pocatello, ID, in 1948. He received the B.A. degree in zoology from the University of California, Berkeley, in 1971 and the M.S. degree in zoology from Duke University, Durham, NC, in 1973. He received the M.S. degree in electrical engineering from San Jose State University, San Jose, CA, in 1976, and the M.S. degree in materials science and the Ph.D. degree in electrical engineering, both from Stanford University, Stanford, CA, in 1986.

In 1986 he joined the Bipolar Technology Group at the IBM T.J. Watson Research Center, Yorktown Heights, NY, where he worked on a variety of projects related to fabrication and modeling of bipolar and BiCMOS integrated circuits. The primary focus of his work was the development of SiGe-base heterojunction bipolar and BiCMOS technology. Since 1994 he has been a Senior Engineer Manager of the SiGe Technology Group at the IBM Advanced Semiconductor Technology Center, Hopewell Junction, NY. In 1997, he moved to the IBM Essex Junction, VT, manufacturing site where he is a Senior Engineer Manager of the SiGe Manufacturing Product Engineering and Development group in IBM’s Microelectronic Division. His interests include Silicon and SiGe-channel FET transistors, NPN and PNP Bipolar Junction Transistors, NPN and PNP SiGe base heterojunction bipolar transistors, complementary bipolar technology, and BiCMOS technology. He has authored or coauthored over 100 publications. He is currently a member of the Bipolar/BiCMOS Technology Meeting Device Physics Subcommittee.

Peter Schvan (M’89) was born in Budapest, Hungary, in 1952. He received the M.S. degree in physics from Eotvos Lorand University, Budapest, in 1975 and the Ph.D. degree in electrical engineering from Carleton University, Ottawa, ON, Canada, in 1985.

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