A 4PAM/2PAM coaxial cable receiver analog front-end targeting 40Gb/s in 90-nm CMOS

by

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A thesis submitted in conformity with the requirements for the degree of Master of Applied Science
Graduate Department of Electrical and Computer Engineering
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Abstract

A 4-PAM/2-PAM receiver analog front-end (AFE) targeting 20GSymbol/s for use with coaxial cable channels is presented. Behavioral simulations incorporate a transmitter, scalable coaxial cable model, and the proposed receiver architecture, targeting cable loss of 32dB at 10GHz. To accommodate links of varying lengths, the AFE includes a variable-gain amplifier (VGA) and analog peaking equalizer. The input preamplifier is important for achieving the required input sensitivity. A DC bias current is introduced through the feedback resistor in a conventional shunt-shunt feedback nMOS transimpedance amplifier (TIA) to level-shift the output, obviating a following level-shifting stage. The fabricated AFE occupies 0.89mm$^2$ in a 90-nm CMOS process and dissipates 138mW from a 1.3V supply. The AFE amplifies and opens the eye pattern of a 20-Gb/s 2-PAM data stream transmitted over coaxial cable with 7.5dB loss at 10GHz.
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List of Acronyms

4-PAM  4-Level Pulse Amplitude Modulation
ADC   Analog-to-Digital Converter
AFE   Analog Front-End
AGC   Automatic Gain Control
BER   Bit Error Rate
BJT   Bipolar Junction Transistor
CDR   Clock and Data Recovery
CML   Current-Mode Logic
CMOS  Complementary Metal Oxide Semiconductor
DFE   Decision Feedback Equalizer
DFF   D Flip-Flop
DSP   Digital Signal Processing
FFE   Feed-Forward Equalizer
FIR   Finite Impulse Response
ISI   Intersymbol Interference
NF    Noise Figure
PWM   Pulse-Width Modulation
SNR   Signal-to-Noise Ratio
TIA   Transimpedance Amplifier
List of Acronyms

UI  Unit Interval
VGA  Variable-Gain Amplifier
VNA  Vector Network Analyzer
1 Introduction

1.1 Motivation

Multi-Gb/s transceivers including equalization is an area of ongoing research. A basic transceiver link is shown in Figure 1.1, where the channel is typically a backplane trace or coaxial cable. Due to frequency-dependent channel impairments such as skin-effect and dielectric loss, transmitter and/or receiver equalization becomes necessary. Signaling schemes other than binary (2-PAM) may also be beneficial. This thesis is part of a larger project targeting the design of a 40-Gb/s transceiver for a 40-m Belden 1694A coaxial cable having 50-dB of loss at 20 GHz (one-half of the bit rate). System simulations indicated that a combination of linear transmitter and receiver equalization with 4-level pulse amplitude modulation (4-PAM) signaling offered a possible solution to overcoming the large channel loss. The goal of this thesis project was to build the analog front-end (AFE) of a 4/2-PAM 20-GSymbol/s coaxial cable receiver in a 90-nm CMOS technology, with functionality including gain control and equalization. As part of this work, a broadband preamplifier topology was used that (to the author’s knowledge) had not previously been implemented in CMOS. Adaptation and clock recovery were beyond the scope of this work, but are to be included in the full transceiver.

![Figure 1.1: Basic transceiver link.](image-url)
A typical 4-PAM receiver is shown in Figure 1.2. The received signal is conditioned by the AFE, then sliced and decoded to recover the transmitted bits. The thresholds $+V_{\text{ref}}$, 0 and $-V_{\text{ref}}$ are used to slice the 4-PAM symbol by providing appropriate offsets for the following comparators. The decoder (DEC) then uses the comparator outputs to recover the originally transmitted bits. The decoder implementation depends on the line code used at the transmitter, where Gray-coded 2B1Q is a popular choice. Gray code has a number of advantages, including simplified decoder logic and support for both binary and 4-PAM signaling.

### 1.2 State of the Art

The following provides a survey of the current state of the art for 4-PAM transceivers and receivers in CMOS. To provide some context for the larger transceiver project goal in terms of speed and loss-compensation, current CMOS transceivers are also briefly described.

The 4-PAM transceiver in [FRYHL00] achieved 8 Gb/s in 0.3-μm CMOS, and im-
implemented 2-tap symbol-spaced finite impulse response (FIR) transmit and 1-tap 1/2-symbol-spaced FIR receive equalization.

The 4-PAM transceiver in [SWSW03] achieved 5 Gb/s in 0.25-µm CMOS using a FIR (3-tap + 1 long-latency tap) transmit equalizer with a slicing receiver, and an 8B5Q coding scheme meant to facilitate adaptive equalization and timing recovery.

The 4-PAM transceiver in [ZWS+03] achieved 10 Gb/s in 0.13-µm CMOS, and combined a 5-tap symbol-spaced FIR transmitter with a 5-tap decision feedback equalizer (DFE) at the receiver. Use of a DFE was motivated by the high-reflection backplane environment, and a loss of approximately 12-dB at 2.5 GHz was compensated.

The 4-PAM receiver AFE in [HMC+05] achieved 20 Gb/s in 0.18-µm CMOS, and used a 4-tap 1/3-symbol-spaced FIR equalizer with an LC-ladder delay line along with crosstalk cancellation. A loss of approximately 18-dB at 5 GHz was compensated.

The 4-PAM receiver in [TMR+06] achieved 22 Gb/s in 90-nm CMOS SOI. The equalization and slice level-shifting functions were combined into a single stage. This stage used a linear peaking equalizer implemented with capacitive source degeneration.

Regarding 4-PAM transmitters, the fastest reported CMOS implementation achieved 25 Gb/s in 90-nm SOI with 4-tap FIR preemphasis [MTR+05]. As part of the larger transceiver project mentioned in section 1.1, the Master’s thesis work of another student involved the design and fabrication of a 40-Gb/s 4-PAM transmitter in 0.13-µm CMOS with pulse-width modulation (PWM) pre-emphasis [Che08].

There are several examples of 2-PAM transceivers with equalization in CMOS up to 10 Gb/s using a combination of multi-tap feed-forward equalizer (FFE) at the transmitter and DFE at the receiver [KYMC+05], [PLB+05], [BSS+05], [BCC+05]. The 10-Gb/s 90-nm transceiver in [BMR+06] compensated the most loss (33.5 dB at 5 GHz), and utilized a 4-tap FFE at the transmitter and a 5-tap half-rate DFE at the receiver.

### 1.3 Linear vs. Non-Linear/Digital Techniques

The popularity of the transmitter FFE/receiver DFE combination in recent transceivers is due in part to the advantages of a DFE, which include the ability to compensate for post-cursor ISI and reflections without enhancing noise or crosstalk [BSS+05]. One
reported 4-PAM transceiver [ZWS+03] has also used this combination. In the early stages of this work, the signaling scheme had yet to be chosen. Both 40-Gb/s 2-PAM and 20-GSymbol/s 4-PAM signaling with a DFE were considered, but ruled out for the following reasons.

A 2-PAM DFE was ruled out, as it is unclear whether 40-Gb/s operation can be achieved in the target 90-nm CMOS technology. The first CMOS full-rate 40-Gb/s D flip-flop (DFF) was reported in [CYA+07], and required both low and high-V_t devices in a 90-nm process operating from a 1.2-V supply. However, successfully integrating the DFF in a full DFE would be a challenging task. The block diagram of a full-rate 1-tap loop-unrolled DFE (adapted from [BMR+06]) is shown in Figure 1.3. Note that unlike the 40-Gb/s DFF in [CYA+07], a DFE requires the DFF to be included in a feedback loop with a 2-to-1 multiplexer (MUX). Hence, the setup time and clock-to-Q delay of the DFF plus the delay through the MUX must all fit within one clock period (25 ps at 40 GHz). Furthermore, low-skew distribution of a 40-GHz clock to three DFFs would be required. A similar architecture was demonstrated at 40-Gb/s in a 160-GHz f_T, 0.18-µm SiGe BiCMOS process, operating from a 3.3-V supply [GCV06]. The fastest reported DFE receivers in 90-nm CMOS have operated at 10-Gb/s (with [BMR+06] and [ENVB+07] utilizing half-rate architectures with speculative feedback (loop-unrolling) for the first tap), meaning a 40-Gb/s 2-PAM DFE in 90-nm CMOS would require a 4x speed improvement over the state-of-the-art.

![Figure 1.3: 1-tap loop-unrolled 2-PAM DFE.](image)

A 4-PAM DFE was also ruled out due to the resulting complexity of the required
hardware. While the required speed would nominally be halved (to 20-Gb/s) as compared to the 2-PAM case, loop-unrolling would still likely be required for the first tap since even at 10-Gb/s, 90-nm CMOS DFEs in [BMR+06] and [ENVB+07] have used this technique. One possible implementation is shown in Figure 1.4, which is a 4-PAM version of the DFE in Figure 1.3. Note that there are four possible values of first post-cursor ISI denoted $V_1$, $V_2$, $-V_1$ and $-V_2$. Hence, a total of 12 comparators are required, greatly exacerbating the difficulties of clock distribution. The MUXs which are still in the critical feedback path are now 4-to-1 MUXs. Furthermore, the DEC would require significantly more gates (and have greater delay) than the corresponding blocks in the 2-PAM DFE, possibly limiting the achievable speed. Half-rate techniques could be applied to further reduce the required clock speed, at the cost of even more hardware. Due to the high comparator count and design issues related to the MUX, the 4-PAM DFE was not pursued.

![Figure 1.4: 1-tap loop-unrolled 4-PAM DFE.](image)

Note that the use of a 4-PAM DFE in [ZWS+03] and elsewhere has been motivated
by the high-reflection backplane environment, which has deep notches in the frequency response that cannot be compensated by linear equalization alone. In contrast, the target Belden coaxial cable has high loss but no nulls in the measured cable response, and hence provided less incentive to use a DFE.

An alternate approach to the receiver would involve directly digitizing and processing the channel output. One recent implementation of such a digital signal processing (DSP)-based receiver is the 65-nm CMOS 12.5-Gb/s serializer/deserializer (SERDES) reported in [HWS+07]. Two half-rate (6.25-GSample/s) flash analog-to-digital converters (ADCs) sampled the received data, and digital equalization (2-tap FFE + 5-tap DFE) was performed on the samples. Each lane (including transmitter, receiver and clock recovery blocks) consumed 330 mW and occupied 0.45 mm$^2$. While DSP-based receivers offer the possibility of sophisticated digital equalization, they were also ruled out due to the required ADC performance. For example, the 90-nm ADC in [SBF+08] used an interleaved architecture to achieve 24 GSamples/s, dissipated 1.2 W and occupied 16 mm$^2$. Recently reported CMOS flash ADCs have sampling frequencies in the 5-GSample/s range [WIL07], [PPF07], [PPR+06]. The 90-nm design in [PPR+06] had a sampling rate of 3.5 GSamples/s, dissipated 227 mW and occupied 0.658 mm$^2$. This suggested that a 40-Gb/s DSP-based solution was not feasible in 90-nm due to the speed, power and area requirements of the ADC (and subsequent DSP blocks).

For these reasons, signal processing with linear techniques was pursued over nonlinear (DFE) and DSP-based solutions. These techniques along with further justification for the choice of 4-PAM signaling will be given in Chapter 3, with later chapters presenting the design and measurement results of the receiver AFE.

1.4 Outline

Remaining chapters are organized as follows. Chapter 2 provides measurements of the target cable and describes the channel model used in system and circuit simulations. Chapter 3 presents various multilevel signaling and equalization methods, as well as system simulations of the chosen scheme. Chapter 4 details the circuit design of the receiver AFE. Chapter 5 describes the circuit layout and presents measurement results.
Chapter 6 concludes the thesis and gives suggestions for future work.
2 Channel Description

This chapter provides a description of the target Belden 1694A coaxial cable channel. Section 2.1 lists some important cable parameters and provides measurements of three cable lengths (10-m, 30-m and 50-m). Section 2.2 describes the channel model that was used in system and circuit simulations, including model verification and connector de-embedding.

2.1 Cable Description and Measurements

Belden 1694A is a low-loss serial digital coaxial cable constructed of a solid copper conductor, foamed high-density polyethylene (FHDPE) dielectric and an aluminum/copper shield. Some important data sheet parameters are reproduced in Table 2.1 [Bel06]. The nominal characteristic impedance of 75-Ω is common to audio-visual applications.

S parameters for 10-m, 30-m and 50-m cables were measured using a Hewlett-Packard HP 8510C 26.5-GHz Vector Network Analyzer (VNA) and converted from 50-Ω to 75-Ω reference impedance. The cables were supplied with crimped 75-Ω BNC (4-GHz BW) connectors, so BNC/SMA (8-GHz BW) and SMA/K (40-GHz BW) connectors were used to connect to the VNA. Figure 2.1 shows the measured $|S_{21}|$ for the three cable lengths. Measurements indicate a 50-m cable with connectors has approximately 65 dB of attenuation at 20 GHz.

2.2 Channel Model Description

Frequency-domain channel models are useful for simulation. The model should produce the desired loss vs. frequency characteristic, and phase information for use in the time-domain. For metallic conductors, as the operating frequency $f$ increases, the
Table 2.1: Belden 1694A coaxial cable data sheet parameters.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nominal Characteristic Impedance</td>
<td>75 Ω</td>
</tr>
<tr>
<td>Nominal Inductance</td>
<td>0.348 H/m</td>
</tr>
<tr>
<td>Nominal Capacitance - Conductor to Shield</td>
<td>53.1 pF/m</td>
</tr>
<tr>
<td>Nominal Velocity of Propagation</td>
<td>0.82(c)</td>
</tr>
<tr>
<td>Nominal Delay</td>
<td>4.07 ns/m</td>
</tr>
<tr>
<td>Nominal Conductor DC Resistance @ 20°C</td>
<td>21.0 mΩ/m</td>
</tr>
<tr>
<td>Nominal Shield DC Resistance @ 20°C</td>
<td>9.2 mΩ/m</td>
</tr>
<tr>
<td>Conductor Diameter ((d_1))</td>
<td>1.02 mm</td>
</tr>
<tr>
<td>Shield Inside Diameter ((d_2))</td>
<td>4.57 mm</td>
</tr>
</tbody>
</table>

Figure 2.1: Measured \(|S_{21}|\) for three coaxial cable lengths.
attenuation becomes dominated by skin-effect and dielectric losses. When measured in dB, skin-effect loss varies directly with $\sqrt{f}$, while dielectric loss varies directly with $f$. The channel model developed in [JG03] begins with standard transmission line expressions, then accounts for the frequency variation of the transmission line parameters themselves, modeling skin-effect and dielectric losses in addition to lower-frequency loss. The theory and implementation of the model are described below.

**Transmission Lines**

Assuming TEM propagation, transmission lines are characterized by their propagation coefficient ($\gamma$) and characteristic impedance ($Z_0$) [Poz05]:

$$
\gamma = \sqrt{(R + j\omega L)(G + j\omega C)}
$$

$$
Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}}
$$

where $R$ is series resistance (Ω/m), $L$ is series inductance (H/m), $G$ is shunt conductance (S/m) and $C$ is shunt capacitance (F/m). $R$ and $L$ include both the signal and return conductors.

**Transmission (ABCD) Matrices**

Transmission matrices (also called ABCD matrices) can be used to represent two-port networks, including transmission lines [Poz05]. In general, an ABCD matrix relates the terminal voltage and current phasors, shown in Figure 2.2, as follows:
2 Channel Description

\[
\begin{bmatrix}
V_1 \\
I_1
\end{bmatrix} = \begin{bmatrix}
A & B \\
C & D
\end{bmatrix} \begin{bmatrix}
V_2 \\
I_2
\end{bmatrix}
\] (2.3)

The ABCD matrix of a transmission line with length \( d \) is:

\[
\begin{bmatrix}
A & B \\
C & D
\end{bmatrix} = \begin{bmatrix}
\cosh(\gamma d) & Z_0 \sinh(\gamma d) \\
\frac{1}{Z_0} \sinh(\gamma d) & \cosh(\gamma d)
\end{bmatrix}
\] (2.4)

ABCD matrices are useful for representing a cascade of two-ports, since the matrix of the cascade is the product of the individual matrices. Hence, the ABCD matrix of the transmission line can be multiplied by the ABCD matrices of source and load impedances to generate the matrix of the terminated line. As it describes the network at a single frequency, a separate ABCD matrix is calculated for each frequency point within a desired range. Time-domain responses may then be generated through an IFFT.

2.2.1 Channel Model - Theory

The channel model that was used involves setting the parameters \( R, L, G \) and \( C \) such that the skin-effect and dielectric losses are modeled along with lower-frequency loss. The model development and notation of [JG03] is presented, but with a focus on modeling coaxial channels.

The model begins by choosing a frequency \( \omega_0 \) at which other frequency-dependent parameters are specified. It is recommended that \( \omega_0 \) be at a frequency much greater than the onset of skin-effect, but where all modes are still TEM, with a frequency near one-half the symbol frequency being ideal.

The expression for \( \gamma \) contains the square root of the product of two main terms. The term \( (R + jwL) \) contains all DC and AC series impedances. The term \( R \) is frequency-dependent and includes terms to model skin-effect.

\( R_0 \) is the skin-effect resistance at \( \omega_0 \), which can be derived from the equation for conductor skin-depth [Poz05]. For coaxial cable having inner and outer conductor diameters \( d_1, d_2 \) and conductivities \( \sigma_1, \sigma_2 \), respectively,
At high frequencies (well above the onset of skin-effect), the channel inductance is at a minimum as compared to lower frequencies. This minimum value is called the external inductance, $L_0$, while the additional inductance at lower frequencies is the internal inductance, $L_i$. It has been shown for round wires that $wL_i$ is equal to $R_0$, which allows these impedances to be written together in the form

$$R_{AC}(\omega) = R_0(1 + j)\sqrt{\frac{\omega}{\omega_0}} \, [\Omega/m] \quad (2.6)$$

where the $\sqrt{\omega/\omega_0}$ term creates the proper frequency dependence.

$R_{DC}$ is the total DC resistance per unit length of the channel. For coaxial cable,

$$R_{DC} = R_{DC,inner} + R_{DC,outer} \, [\Omega/m] \quad (2.7)$$

$R(\omega)$ is then found by combining $R_{DC}$ and $R_{AC}$:

$$R(\omega) = \sqrt{R_{DC}^2 + R_{AC}^2(\omega)} \, [\Omega/m] \quad (2.8)$$

The external inductance is found as

$$L_0 = \frac{Z_0}{v_0} \, [H/m] \quad (2.9)$$

where $Z_0$ is the characteristic impedance and $v_0$ is the propagation velocity, both evaluated at $\omega_0$.

The other main term in the expression for $\gamma$, $(G + jwC)$, contains all DC and AC shunt admittances. In this model, $G$ is taken as zero (essentially true for low-voltage coaxial cable), but $C$ is a complex-valued function of frequency. A real-valued conductance term is then created when the imaginary component of $C$ is multiplied by $jw$.

It has been shown that if a material is to have a dielectric-loss tangent $(\tan \theta)$ that
is constant over frequency, then the complex relative permittivity must have the form

\[ \epsilon_r(w) = ae^{-j\theta \omega^2} \]  

(2.10)

which for a given \( \omega_0 \) can be approximated as

\[ \epsilon_r(w) = \epsilon_r(\omega_0)\left(\frac{\omega}{\omega_0}\right)^{-\frac{\theta_0}{\pi}} \]  

(2.11)

leading to this expression for \( C(w) \):

\[ C(w) = C_0\left(\frac{\omega}{\omega_0}\right)^{-\frac{\theta_0}{\pi}} \quad \text{[F/m]} \]  

(2.12)

where \( C_0 \) is the capacitance at \( \omega_0 \):

\[ C_0 = \frac{1}{Z_0v_0} \quad \text{[F/m]} \]  

(2.13)

Further explanation as to why the expression for \( C(w) \) leads to a reasonable approximation of the conduction current is provided in [JG03].

With these expressions for \( R, L, G \) and \( C \), the expression for \( \gamma \) may be manipulated to derive the individual contributions of skin-effect and dielectric loss:

\[ \alpha_r = 4.34 \frac{R_0}{Z_0} \sqrt{\frac{\omega}{\omega_0}} \quad \text{[dB/m]} \]  

(2.14)

\[ \alpha_d = 4.34 \frac{\theta_0}{v_0} \left(\frac{\omega}{\omega_0}\right)^{-\frac{\theta_0}{\pi}} \quad \text{[dB/m]} \]  

(2.15)

These expressions confirm that when loss is measured in dB, skin-effect loss varies directly with \( \sqrt{f} \), while dielectric loss varies directly with \( f \). The resulting channel model can then be fit to measured data by using \( R_0 \) and \( \theta_0 \) as fitting parameters. An initial estimate of \( R_0 \) can be obtained from datasheet values and Equation 2.5, while \( \theta_0 \) may not be given on the datasheet but can be estimated from published values of the insulator loss tangent. The parameters are varied from their initial estimates, and the sum of squares error between the measured and modeled magnitude responses is minimized. This concludes the description of the model given in [JG03].
Time-domain responses such as the impulse response of the channel are available through an IFFT. The frequency response may be zero-padded prior to taking the IFFT to help achieve a desired time resolution, instead of increasing the upper limit of the frequencies used in the model. This can help avoid using the model outside of its appropriate frequency range, which may be an issue with shorter channels not having significant attenuation at the highest model frequency. In addition, the frequency resolution must be fine enough to avoid aliasing effects in the time domain.

### 2.2.2 Channel Model - Implementation

The channel model parameters for the Belden 1694A coaxial cable may now be found using the data in Table 2.1 and Table 2.2.

1. While not explicitly required for the channel model, the relative permittivity of the dielectric can be estimated. For non-magnetic media, $\mu_r = 1$, and so

$$v = \frac{c}{\sqrt{\varepsilon_r \mu_r}} = \frac{c}{\sqrt{\varepsilon_r}}$$  \hspace{1cm} (2.16)$$

Using the propagation velocity from Table 2.1, the relative permittivity of FDHPE, $\varepsilon_{r,FDHPE}$, is 1.49. This compares with published values near 2.4 [RBJK03].

2. Choose $\omega_0 = 2\pi \times 10$ GHz, half the intended symbol frequency of 20 GSymbol/s (and above the onset of skin-effect).

3. Find $Z_0$, the characteristic impedance at $\omega_0$. It is assumed that $Z_0$ has not changed significantly from its nominal value of 75 $\Omega$ at $\omega_0 = 2\pi \times 10$ GHz.

4. Find $v_0$, the propagation velocity at $\omega_0$. It is assumed that $v_0$ has not changed significantly from its nominal value of 0.82$c$ at $\omega_0 = 2\pi \times 10$ GHz.

5. $R_0 = 10.5$ $\Omega$/m (Equation 2.5).

6. $R_{DC} = 30.2e-3$ $\Omega$/m (Equation 2.7).

7. $L = L_0 = 0.306$ uH/m (Equation 2.9).
Table 2.2: Physical constants used in the channel model.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\sigma_{Cu}$</td>
<td>$5.80 \times 10^7 \text{ S/m}$</td>
</tr>
<tr>
<td>$\sigma_{Al}$</td>
<td>$3.54 \times 10^7 \text{ S/m}$</td>
</tr>
<tr>
<td>$\mu_0$</td>
<td>$4\pi \times 10^{-7} \text{ H/m}$</td>
</tr>
<tr>
<td>$\epsilon_0$</td>
<td>$8.85 \times 10^{-12} \text{ F/m}$</td>
</tr>
</tbody>
</table>

8. $C_0 = 54.24 \text{ pF/m}$ (Equation 2.13).

9. Initially estimate $\theta_0 = 0.0002$, as per published values of FHDPE loss tangent [RBJK03].

10. All terms in Equations 2.8, 2.9 and 2.12 have now been determined, and $\gamma$ may be found using Equation 2.1, since the model sets $G = 0$. The ABCD matrix of the transmission line with this propagation constant $\gamma$ can be generated using Equation 2.4.

11. The parameters $R_0$ and $\theta_0$ are now optimized to fit the channel model to measured data.

The relative contributions of skin-effect and dielectric loss may be estimated using the above values of $R_0$ and $\theta_0$. From Equation 2.14 and Equation 2.15, we have $\alpha_r = 0.86 \text{ dB/m}$ and $\alpha_d = 0.38 \text{ dB/m}$ at 20 GHz, indicating that about 70% of the loss is due to skin-effect at this frequency.

2.2.3 Connector De-embedding

The measured cable attenuation in Figure 2.1 includes any losses due to connectors with bandwidths lower than the VNA. However, if the channel bandwidth is severely limited by the connectors, it may be possible to replace them with different connectors offering better high-frequency performance. It is therefore desirable to de-embed the effect of the connectors in order to estimate the cable loss alone. A procedure for de-
embedding VNA measurements of a device under test (DUT) based on transmission lines is given in [Man05], and was adapted to de-embed the cable measurements.

The full de-embedding procedure involves using two pad-accessed transmission line test structures of different lengths for characterization, and using this information to de-embed them from the actual DUT measurement. In the case of the coaxial cable measurements, only the characterization portion of the procedure is necessary. Completing steps 1 through 3 of the procedure given in Section 4.3 of [Man05] with the 10-m and 50-m cables as test structures yields an ABCD matrix for a de-embedded cable of length \((50 - 10) = 40\) m.

Although the procedure is derived assuming the pads (or connectors, in this case) can be modeled as a lumped admittance, the size of the connectors used in the measurements approaches \(\lambda \approx 9.3\) mm at 26.5 GHz. Even so, it is shown in [Man05] that the resulting ABCD matrix will have the same A and D parameters as in the lumped admittance case, although all four parameters are used when the matrix is multiplied with the ABCD matrices of the source and load terminations.

### 2.2.4 Channel Model Results and Verification

The channel model was implemented in MATLAB, and initially optimized to the 50-m, non-de-embedded measurements. The final fitting parameters were \(\theta_0 = 0.00015\), \(R_0 = 11.55\ \Omega/m\). In order to verify the model, cable responses were then created for the 10-m and 30-m cables, keeping the fitting parameters unchanged from the 50-m values. The results are shown in Figure 2.3.

When fitted to the de-embedded 40-m data, the fitting parameters became \(\theta_0 = 0.00017\), \(R_0 = 10.5\ \Omega/m\). Note that for the de-embedded case, the final value of \(R_0\) was unchanged from its initial calculated value. The de-embedded measurements and fitted channel model are shown in Figure 2.4, and the corresponding 40-Gb/s binary pulse response is shown in Figure 2.5. Ideal matched source and load terminations were added after the de-embedding procedure, causing approximately 6 dB extra attenuation at all frequencies (including DC). This indicates that at 20 GHz, the attenuation due to the 40-m cable itself is approximately 50 dB. Interestingly, the connectors appear to have only contributed approximately 2 dB of loss at 20 GHz.
2.2.5 Non-TEM Modes

The channel model in [JG03] was derived under the assumption of TEM propagation. While only the TEM mode of the coaxial cable is meant to be excited, at sufficiently high frequencies non-TEM (waveguide) modes can propagate. While no signal power is lost, undesirable effects such as dispersion of rising/falling edges, ringing and overshoot can occur [JG03]. For the coaxial structure, $TE_{11}$ is the dominant waveguide mode with cutoff frequency $F_c = ck_c/(2\pi \sqrt{\epsilon_r, FHDPE})$, where $k_c \approx 4/(d_1 + d_2)$ [Poz05]. Using the values in Table 2.1 and taking $\epsilon_r, FHDPE = 1.49$, we have $F_c = 28$ GHz. This indicates that it is desirable to transmit signals without significant frequency content above approximately 28 GHz.

Figure 2.3: Channel model (dashed lines) and measurement (markers), with the same 50-m model fitting parameters used in the 10-m and 30-m models.
2 Channel Description

Figure 2.4: De-embedded measurements and model (40-m cable).

Figure 2.5: Pulse response (25-ps input pulse, 40-m cable model) shown with UI-spaced samples (markers).
3 Signaling and Equalization

This chapter presents the selected signaling format and equalization methods. Section 3.1 describes the benefits and drawbacks of some multilevel signaling formats, and explains why 4-PAM was chosen. Section 3.2 describes the transmitter and receiver equalization methods, and presents system-level simulation results.

3.1 Signaling Format

This section presents some of the advantages and disadvantages of multilevel signaling compared to 2-PAM, and describes why multilevel schemes were more suited to the target cable. A description of some multilevel formats and justification for the selection of 4-PAM are also presented.

3.1.1 Multilevel Signaling vs. 2-PAM

Although 2-PAM signaling is simple and robust, a larger signal bandwidth is required for a given bit rate compared to multilevel schemes. The 2-PAM signal will thus experience more attenuation and ISI due to frequency-dependent channel losses. While the 2-PAM receiver will have a larger noise bandwidth, the level-spacing will also be larger. With multilevel signaling, bandwidth requirements are lowered at the cost of reduced signal-to-noise ratio (SNR) [SDA05].

Transmitting 2-PAM at 40-Gb/s over the target cable would require compensating a loss of 50 dB at 20 GHz, which was deemed unfeasible for a number of reasons. The required performance would represent a 4x improvement in speed and 16.5 dB increase in loss compensation compared to the state-of-the-art transceiver in the same target 90-nm CMOS technology (and unlike [BMR+06], would not be able to use a DFE for
Figure 3.1: Multilevel signaling eye diagrams (with sampling phases shown): (a) duobinary, (b) 3-PAM, (c) 4-PAM.

the reasons given in section 1.3). A practical reason for not using 2-PAM was the swing limitation of the transmitter. For example, assuming that a 40-Gb/s 2-PAM CMOS transmit driver could achieve a swing of 1.6-V_{pp} single-ended (as in [Che08], where breakdown voltage was the limiting factor), a toggling 1010 pattern would experience 50 dB of loss through the target cable and be attenuated to approximately 5 mV_{pp}. Assuming a receiver noise bandwidth of 40 GHz, source impedance of 75 Ω and a temperature of 290 K, a bit error rate (BER) of 10^{-12} (Q of 7.035) would require the noise figure (NF) of the entire broadband receiver (up to the decision circuit) to be less than approximately 10 dB. This would be difficult to achieve, as a differential broadband preamplifier alone designed for low-noise operation had a (single-ended) NF near 10 dB at 10 GHz in 90-nm CMOS [DYC+06]. Note that this example did not use the worst-case sequence, and ignored any attenuation due to linear equalization. This motivated exploring multilevel alternatives to 2-PAM.

3.1.2 Selection of 4-PAM

The following provides a brief description of various multilevel signaling schemes, and justification for the selection of 4-PAM.
Duobinary

Duobinary is a special case of partial-response signaling, where a controlled amount of ISI remains after equalization and is removed through decoding. This can reduce the amount of equalization that would otherwise be required, leading to a simpler equalizer and less noise enhancement. The $Z$-transform of the equalized channel is ideally $X(z) = 1 + z^{-1}$, corresponding to one term of ISI with amplitude equal to the main pulse. The resulting eye diagram will have three levels as shown in Figure 3.1(a), and is sliced by two comparators with appropriate thresholds.

Depending on the channel response, duobinary can yield potentially larger eye-openings than 4-PAM [YSK05], but a number of implementation issues exist. For example, duobinary symbols must be transmitted at full rate (as in 2-PAM), and fractionally-spaced FIR transmitter equalization may be required for best performance ([SDA05], [YSK05]). Given CMOS speed and swing limitations, the transmitter would likely require significant multiplexing and multiple clock phases, complicating the design compared to a 4-PAM transmitter. The receiver would have to latch 40-Gb/s data, but due to the difficulty of implementing a DFF at this speed (as described in section 1.3), a half-rate architecture would be preferred resulting in four 20-Gb/s DFFs, yielding comparable hardware to the basic 4-PAM receiver in Figure 1.2 which requires three such DFFs.

Due to the required transmitter and receiver complexity, duobinary was not used. The current fastest reported CMOS duobinary transceiver achieved 20 Gb/s in 90-nm CMOS, dissipated 195 mW and occupied 0.32 mm$^2$ [LCW08].

3-PAM

An alternate multilevel scheme is three-level pulse amplitude modulation (3-PAM), with a typical eye diagram as shown in Figure 3.1(b). While requiring larger (> 30%) bandwidth than 4-PAM, the simplest receiver would need only two comparators and a decoder.

The main challenge would be devising and implementing a low-overhead line code in order to transmit at a symbol rate significantly less than the bit rate. For example,
3B2T would allow transmission at \((2/3) \times 40 = 26.7\) GSymbol/s, while 8B6T would require a rate of \((3/4) \times 40 = 30\) GSymbol/s. This leads to increased transmitter complexity, since each bit-grouping maps to at least two consecutive ternary symbols. Furthermore, a corresponding frame aligner and decoder would be required at the receiver.

Due to uncertainties related to the line code, 3-PAM was not used. It should be noted that 3-PAM is much less common in current literature than duo-binary and 4-PAM.

### 4-PAM

The main advantage of 4-PAM is the 2x reduction in bandwidth (and hence, reduced channel loss at relevant frequencies) compared to 2-PAM. A typical 4-PAM eye diagram is shown in Figure 3.1(c). A common criterion for considering 4-PAM is when the channel loss difference between the 4-PAM and 2-PAM Nyquist frequencies exceeds 10 dB, due to the 4-PAM level-spacing being \(1/3\) (or -9.5 dB) that of a 2-PAM eye for a fixed transmit swing [ZWS+03]. For 40-Gb/s, the 2-PAM and 4-PAM Nyquist frequencies are 20 GHz and 10 GHz, respectively. While this is only a rough guideline, the channel response of the target 40-m Belden 1694A coaxial cable (in Figure 2.4) has a loss difference of 18 dB between 10 GHz and 20 GHz, showing the potential benefit of 4-PAM. Note that the amount of loss at the 4-PAM Nyquist frequency (32 dB at 10 GHz) has been compensated by previously reported (2-PAM) transceivers and equalizers (at data rates of 10 Gb/s [BMR+06] and 5 Gb/s [SKVN06]).

Disadvantages compared to 2-PAM include increased susceptibility to crosstalk and reflections due to the decreased level-spacing [ZWS+03], and more receiver complexity. However, as was noted in section 1.3, measurements indicated that reflections are not of major concern.

The decision to use 4-PAM with the target cable was motivated mainly by the significantly lower channel loss and symbol rate. It was expected that the transmitter design would be simplified as compared to other multilevel schemes, but the receiver design potentially more complex. Other signaling schemes (such as \(M\)-PAM, \(M > 4\)) were not considered.
3 Signaling and Equalization

3.2 Equalization Method

System simulations of the transmitter and receiver were done with the target cable model (presented in section 2.2) to see how the equalization could be partitioned. This section describes the equalization methods used by the transmitter and receiver, and presents the system simulations.

3.2.1 Transmitter Equalization

The PWM technique was chosen over common 2-tap symbol-spaced FIR equalization because it provided greater high-frequency boost [SKVN06], with a frequency response that better approximated the inverse of the target cable [Che08]. Figure 3.2 shows example 2-PAM PWM pulses for various pulse widths. In particular, [SKVN06] reported 33-dB loss compensation at the 2-PAM Nyquist frequency using PWM alone, comparable to the 4-tap FFE/5-tap DFE transceiver in [BMR+06]. The target 40-m coaxial cable had similar loss at the 4-PAM Nyquist frequency, which provided motivation for combining the PWM technique with 4-PAM. Simulated 40-m cable pulse responses for 25 ps and 50 ps UIs are shown in Figure 3.3(a) and Figure 3.3(b), respectively, for various PWM settings.

As was mentioned in section 1.2, the Master’s thesis work of another student involved implementing a 40-Gb/s 4-PAM transmitter in 0.13-µm CMOS with adjustable PWM pre-emphasis [Che08]. The transmitter was designed to have a swing of 0.4 - 1.6 Vpp, single-ended on a doubly-terminated 75-Ω (37.5-Ω effective) load.

3.2.2 Receiver Equalization

The majority of CMOS linear receiver equalizers at or above 10 Gb/s have been implemented as peaking equalizers or continuous-time FIR filters. Peaking equalizers have commonly been used to compensate notch-free, low-pass channels, and tend to have simpler implementations while providing the appropriate frequency response. Continuous-time FIR equalizers using $LC$ delay lines can achieve high speed with low power (such as the 30-Gb/s 90-nm CMOS equalizer in [SC06]), but require large area,
3 Signaling and Equalization

Figure 3.2: Transmitted 2-PAM PWM pulses.

Figure 3.3: Simulated 40-m Belden 1694A coaxial cable pulse responses for (a) 25-ps and (b) 50-ps input pulses.
3 Signaling and Equalization

and were not considered due to the need for precise passive device modeling. Instead, a peaking equalizer was used to complement the equalization done at the transmitter.

Generally, a large amount of peaking is desired so that more loss can be compensated. However, in this work the transmitter is meant to provide significant equalization, and system simulations indicated that only about 5 dB of peaking at the receiver would be required for the target cable. Hence, this was the targeted total peaking for the receiver AFE, with the majority of the equalization to be provided by the transmitter. The moderate amount of peaking meant that multiple equalizer stages could be avoided, thus ameliorating the attendant noise enhancement.

What follows is a brief description and analysis of the main peaking equalizer circuit topologies, and the reasons for selecting the implemented topology.

**Peaking Equalizer Topologies**

Capacitive degeneration is commonly used to provide a peaked response, and is implemented as shown in Figure 3.4. The location of the peak is set by the degeneration devices. The basic cell in Figure 3.4 has been used (with additional bandwidth-enhancement techniques) to achieve equalization up to 20-Gb/s in 0.13-µm CMOS [Lee06]. In [TKO+05], the basic cell was cascaded with a transimpedance stage to generate increased peaking, compensating up to 20-dB loss at 5 GHz for 10-Gb/s operation in 0.11-µm CMOS. Alternatively, the weighted sum of low-pass and high-pass paths can create a peaked response, as shown in Figure 3.5, where the weighting parameter determines the peak location. The 10-Gb/s BiCMOS cable equalizer in [ZG05] used this structure, with a simplified CMOS version shown in Figure 3.6, where the weighting is set by the \( g_m \) of transistors M3 and M4. The equalizer in [ZG05] used an inductor to create the high-pass path, while the split-path equalizer in [GR07] instead employed the cell shown in Figure 3.4 for the same purpose.

The gain of the capacitively degenerated stage in Figure 3.4 is given by

\[
A_{cap-degen}(s) = \frac{\Delta_{out}}{\Delta_{in}} = \frac{g_m R_1}{1 + g_m R_s} \cdot \frac{1}{1 + \frac{s C_s R_s}{1 + g_m R_s}} = A_{DC} \cdot \frac{1 + \frac{s}{\omega_{z1}}}{1 + \frac{s}{\omega_{p1}}} \tag{3.1}
\]

where \( A_{DC} = \frac{g_m R_1}{1 + g_m R_s} \), \( \omega_{z1} = \frac{1}{C_s R_s} \) and \( \omega_{p1} = \frac{1 + g_m R_s}{C_s R_s} \).
3 Signaling and Equalization

Figure 3.4: Basic peaking stage using capacitive degeneration.

Figure 3.5: Basic split-path equalizer model.

Figure 3.6: Example split-path equalizer circuit.
The gain of the split-path equalizer in Figure 3.6 is given by

\[ A_{\text{split-path}}(s) = \frac{\Delta \text{out}}{\Delta \text{in}} = g_{m1}g_{m3}R_1R_3 \cdot \frac{1 + \frac{sL}{R_2} (1 + \frac{g_{m4}g_{m2}R_2}{g_{m3}g_{m1}R_1})}{1 + \frac{s}{\omega_p}} = A_{\text{DC}} \cdot \frac{1 + \frac{s}{\omega_p}}{1 + \frac{s}{\omega_z}} \]  

(3.2)

where \( A_{\text{DC}} = g_{m1}g_{m3}R_1R_3 \), \( \omega_z = \frac{R_2}{L(1 + \frac{g_{m4}g_{m2}R_2}{g_{m3}g_{m1}R_1})} \) and \( \omega_p = \frac{R_2}{L} \).

Equations 3.1 and 3.2 show that the equalizers in Figure 3.4 and Figure 3.6 have similar (single-zero/pole) transfer functions. These first-order equations ignore drain parasitic capacitance (which could be mitigated with shunt-peaking inductors) and gate capacitance. The finite transistor output impedance (\( r_o \)) is also ignored. In the case of the capacitively degenerated stage, equation 3.1 shows that the zero and pole locations vary with the product \( C_s R_s \) and have a fixed separation factor of \( (1 + g_{m1}R_s) \). Similarly, in the case of the split-path equalizer, equation 3.2 shows that the zero and pole locations depend on \( \frac{R_2}{L} \) and are separated by a factor of \( (1 + \frac{g_{m4}g_{m2}R_2}{g_{m3}g_{m1}R_1}) \). However, in this case the pole is located at \( \omega_p = \frac{R_2}{L} \) independent of where the zero is placed. This implies potentially greater frequency peaking, since the zero may be placed at lower frequencies while the pole remains fixed. One disadvantage of this topology is that the DC gain \( (A_{\text{DC}}) \) in equation 3.2 will tend to drop more quickly than in 3.1, as increased equalization requires raising \( g_{m4} \) while lowering \( g_{m3} \), with \( g_{m3} \) directly scaling \( A_{\text{DC}} \).

Split-path equalization was selected over capacitive degeneration for the implemented AFE. In addition to the potentially greater single-stage peaking, the lack of varactor models in the target CMOS design kit coupled with prior experience in inductor modeling made the inductor-based split-path equalizer of Figure 3.6 a more desirable choice in this case.

### 3.2.3 System Simulation

System simulations were done for the chosen signaling and transmitter/receiver equalization methods. In these simulations, the 4-PAM transmitter provided PWM equalization and a maximum swing of 1.6-V_{pp} single-ended. For the receiver split-path equalizer, the low-pass path was implemented as a low-pass filter with 30-GHz bandwidth, while
the high-pass path was implemented as the intrinsic high-pass path in Figure 3.6 (i.e. $A_{HP}(s) = g_{m2} \cdot \frac{sL}{1+sL}$, with $g_{m2} = 0.013 \text{ A/V}$, $R_2 = 82 \Omega$ and $L = 1 \text{ nH}$) followed by another 30-GHz low-pass filter. The weighting factor was denoted $G_1$ as depicted in Figure 3.5.

The transmitter and receiver equalizer settings were swept together in order to minimize the percentage of remaining ISI compared to the height of the main pulse at 40-Gb/s (20-Gsymbol/s), resulting in a PWM setting of 52.5%, and a peaking setting $G_1$ of 0.48. The transmitted 40-Gb/s 4-PAM eye and split-path equalizer transfer functions corresponding to these optimized PWM and $G_1$ settings are shown in Figure 3.7(a) and Figure 3.7(b), respectively. Note that in Figure 3.7(a), the maximum transmitted swing is doubled since the loss due to double-termination is accounted for in the channel model. Also shown are the channel eye diagrams simulated with the target 40-m cable model for the optimized settings, with transmitter equalization only (Figure 3.8(a)), and with both transmitter and receiver equalization enabled (Figure 3.8(b)). These simulations did not include noise or jitter.
Figure 3.7: Transmitter and receiver equalization: (a) 40-Gb/s 4-PAM transmitted eye diagram (PWM = 52.5%), (b) Receiver split-path peaking equalizer transfer functions ($G_1 = 0.48$).

Figure 3.8: Simulated 40-Gb/s 4-PAM equalized 40-m cable eye diagrams (Gray-coded $2^{10} - 1$ PRBS sequence, 1.6-V$_{pp}$ single-ended transmitted swing): (a) with transmitter PWM only, (b) with transmitter PWM and receiver equalization.
4 Circuit Design and Simulation

This chapter details the circuit design of the 4/2-PAM 20-GSymbol/s receiver AFE. Section 4.1 gives a top-level summary of the AFE blocks. The circuit design of each block is described and simulation results are presented, including transient simulations of cable equalization in the 2-PAM and 4-PAM modes.

4.1 Circuit Description

This section presents the design and simulation of the receiver blocks along with full AFE simulations. A block diagram of the AFE annotated with key simulated results is shown in Figure 4.1. The signal swings shown are for a 60-mV$_{pp}$ single-ended input with maximum equalization and VGA gain, corresponding to the 40-m target cable case with maximum transmitter PWM equalization applied (as described in section 3.2).

4.1.1 Device and Design Description

This section describes the process technology used to implement the AFE, including transistor biasing and sizing choices. Design considerations such as general AFE specifications and sizing of stages are also described.

Design Technology

The 90-nm CMOS design kit from STMicroelectronics was used to implement the design. The process offered 7 metal levels with 2 thick upper layers. The reported $f_T$ of a 90-nm CMOS process is approximately 120 GHz [DYC+06].
Transistor Biasing

For a number of CMOS processes (including 90-nm), the nMOS bias current densities for peak $f_T$ ($J_{pT}$), peak $f_{MAX}$ ($J_{pMAX}$) and optimum $NF_{MIN}$ ($J_{OPT}$) have been reported as 0.3 mA/µm, 0.2 mA/µm and 0.15 mA/µm, respectively [DYC+06]. Since both speed and noise were important considerations in this work, a bias current density of at least 0.15 mA/µm was used for signal-path transistors wherever possible. If higher gain was required, a lower current density was used.

Transistor Dimensions

All nMOS transistors were built from a unit cell having 1-µm finger width ($W_f$), which was chosen based on simulations of $f_T$, $f_{MAX}$ and $NF_{MIN}$ vs. $W_f$. All pMOS transistors were built from a unit cell having 2-µm finger width. All signal-path transistors used minimum gate length.

Simulation Corners

The simulation corners used were TT/80°C, SS/100°C and FF/20°C. Transistor current densities were maintained over corners by manually setting control and reference voltages. This approach was taken since it maintains transistor performance across
temperature and process [DYC+06]. All reported results refer to post-layout simulations.

**General AFE Specifications**

General target specifications of the AFE are described below.

- **Input matching:** $|S_{11}| < -15 \text{ dB}$ from DC to 10 GHz (i.e. one-half the symbol rate) was targeted.

- **Frequency peaking:** Approximately 5 dB of peaking at 10 GHz was targeted (as described in section 3.2).

- **Dynamic range:** The minimum expected input swing obtained from system simulations of the target 40-m cable was 60 mV<sub>pp</sub> single-ended (as described in section 3.2). For shorter cables, larger input swings must be accommodated. Hence, a 1-dB gain compression point ($P_{1\text{dB}}$) of 100 mV<sub>pp</sub> single-ended was targeted.

- **Output swing:** The output swing was set by the swing required at the input to the slicers that would follow the AFE (see Figure 1.2). An output swing of 300-400 mV<sub>pp</sub> differential was chosen, assuming some adjustment of slicer threshold levels is possible.

- **Sensitivity:** An initial noise target was obtained for the 40-m cable case in the following manner. Assuming the AFE output is well-equalized and achieves the minimum targeted 150 mV<sub>pp</sub> single-ended output swing, each 4-PAM eye opening would be approximately 50 mV<sub>pp</sub>. Selecting an RMS noise level at least 15 times smaller gives a maximum output noise of 3.3 mV<sub>rms</sub>, and dividing this by the mid-band gain gives an estimate of the corresponding input-referred noise voltage. The 60 mV<sub>pp</sub> and 150 mV<sub>pp</sub> input and output swings correspond to a (single-ended) mid-band gain of 2.5, so the targeted maximum input-referred noise voltage is 1.3 mV<sub>rms</sub>. Note that impairments such as sampling jitter and residual ISI were ignored in this sensitivity estimate.
Supply voltage: If the slicing and digital decoding blocks had been implemented along with the AFE, current-mode logic (CML) gates incorporating three stacked transistors would likely have been required. It was uncertain whether this could be done with a standard 90-nm supply voltage, so a VDD of 1.3 V was used to accommodate the future addition of these digital back-end circuits.

Stage Sizing

The broadband preamplifier was sized to reduce noise. The following differential stage was sized to avoid excessive loading of the preamplifier, and subsequent input/output capacitances were roughly maintained up to the output driver. However, in an integrated receiver not requiring an output driver, reverse scaling could potentially be used to extend the AFE bandwidth [Sac05].

4.1.2 Broadband Preamplifier

The first stage of the receiver AFE is the broadband preamplifier. To maximize sensitivity, it is generally desirable for the first stage of a receiver to provide high gain and low noise, which can be seen from Friis’ equation for the NF of a cascade of stages:

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1G_2} + \cdots$$  \hspace{1cm} (4.1)

where $F_n$ and $G_n$ are the $n^{th}$-stage noise factor and gain, respectively. NF and F are related as NF = 10log$_{10}$F. Ideally, the first-stage gain is high enough such that the NF (and input-referred noise) of the receiver approaches the NF (and input-referred noise) of the first stage. However, the maximum gain is limited by other system specifications such as dynamic range.

In optical receivers, the first stage is typically a transimpedance amplifier (TIA) that amplifies the small photodiode current into a voltage for further processing. The majority of recent TIAs use the shunt-feedback structure shown in Figure 4.2(a), which has input impedance.
Figure 4.2: Shunt-feedback TIA: (a) driven by a photodiode, and (b) as a broadband preamplifier.

\[
R_{in} = R_f \frac{1}{1 - A} \quad (4.2)
\]

and DC transimpedance gain

\[
Z_{T, DC} = R_f \frac{A}{1 - A} \quad (4.3)
\]

where the voltage gain \( A < 0 \). In Figure 4.2(a), \( I_{pd} \) and \( C_{pd} \) are the photodiode current and capacitance, respectively. This structure provides low input impedance, low noise and high transimpedance gain, all of which are beneficial in an optical receiver application [Sac05]. Increasing \( R_f \) improves noise and transimpedance, but also increases the input time constant \( R_{in} C_{pd} \). As the input pole is usually dominant due to the large value of \( C_{pd} \), the bandwidth is reduced unless \( A \) is also increased to keep \( R_{in} \) constant. Large values of \( R_f \) and \( A \) are therefore desired.

While widely used in conjunction with photodiodes, the shunt-feedback TIA has also been used as a low-noise broadband preamplifier as shown in Figure 4.2(b) [SVC06]. MOS differential pairs preceded by on-chip termination resistors have also been used as broadband preamplifiers, but it has been shown that the shunt-feedback topology is preferred in terms of noise, power and bandwidth [DYC+06], [VDC+05]. When operated as a broadband preamplifier, the desired values of various TIA parameters differ than when operated with a photodiode. For instance, equation 4.2 is used to create a broadband input match by setting \( R_{in} \) to the source impedance \( R_s \), instead of reducing \( R_{in} \) to make the input pole formed by \( R_{in} \) and \( C_{pd} \) non-dominant. In addition,
the voltage gain $\frac{V_o}{V_i}$ is ideally equal to $A$, whereas the transimpedance gain $Z_{T,DC}$ is relatively independent of $A$ (for $|A|$ sufficiently large). The value of $A$ is an important parameter when the TIA is used as a broadband preamplifier because it directly sets the gain, as opposed to an optical application where the precise value of $A$ is less critical.

**Preamplifier Specifications**

This section gives the target specifications of the input preamplifier.

- **Input matching:** $|S_{11}| < -15$ dB from DC to 10 GHz (one-half of the symbol rate) was desired.

- **$A_{DC}$:** A single-ended gain near 7 dB was targeted to realize the signal swings shown in Figure 4.1 for the 40-m cable case.

- **$BW$:** A bandwidth near 20 GHz was targeted in order to accommodate the subsequent peaking equalization occurring in the 10-15 GHz range.

- **Linearity:** As an initial specification, a 10-GHz $P_{1dB}$ approximately 3 dB greater than the maximum expected input swing was chosen. From the general AFE specifications, the assumed maximum input swing of 100 mV$_{pp}$ gave a target of $P_{1dB} \geq 140$ mV$_{pp}$ single-ended.

- **Noise:** The targeted maximum input-referred noise for the full AFE was 1.3 mV$\text{rms}$ (equivalent to a 2-PAM input sensitivity of 21 mV$_{pp}$ for a BER of $10^{-15}$). Half of this was allocated to the input preamplifier, and with an assumed preamplifier noise bandwidth of 30 GHz, source impedance of 75 Ω and temperature of 290 K, this gave a target of $NF < 16.7$ dB across the band.

- **Output common-mode (CM) level:** The preamplifier output CM level must be high enough to drive the following DC-coupled stage, in this case a differential pair. In order to allow the input transistors of the differential pair to be biased at a current density of at least 0.15 mA/µm, an output CM of at least 750 mV was targeted.
Topography Selection and Design

This section compares a number of TIA topologies for use as a broadband preamplifier in the receiver front-end. Throughout this section, it is assumed that the preamplifier is followed by an nMOS-input differential pair, so the preamplifier’s output CM level must be compatible with this.

Figure 4.3: TIA topologies: (a) RGC input stage, (b) nMOS TIA with feedback SF, (c) CMOS TIA with CS, (d) nMOS TIA with CS, (e) nMOS TIA with passive bias and (f) nMOS TIA with active bias.
RGC Input Stage

In optical applications, the regulated cascode (RGC) stage in Figure 4.3(a) is often used to buffer the TIA from the photodiode in order to lessen the dependence of the TIA bandwidth on the large $C_{pd}$. In [PY04] it is shown that the low input impedance of the RGC ($R_{in}$) can make the pole associated with $R_{in}$ and $C_{pd}$ non-dominant, at the cost of the additional noise contributed by this stage. Since this work uses the TIA as a broadband preamplifier (as in Figure 4.2(b)), $C_{pd}$ is replaced by an input pad capacitance $C_{pad}$ that is approximately 10 times smaller than $C_{pd}$, and $R_{in}$ must be set to $R_s$ for impedance matching. Hence, there is little incentive to use the RGC input stage, and it was not considered further.

nMOS TIA with Feedback SF

Figure 4.3(b) shows a single-ended version of a TIA topology common in BJT realizations [DBV05], and also implemented in CMOS [MdMHBL00]. Here, a source-follower (SF) is used in the feedback path. A higher supply voltage would be needed to accommodate the SF [HC06], and so this topology was not used.

CMOS TIA with CS

The TIA in Figure 4.3(c) uses a CMOS inverter for the voltage-gain stage, and has recently been used as a broadband preamplifier [DYC+06]. Note that the CM voltage at the output of the inverter would be too low to drive the following nMOS differential pair directly. Therefore, a common-source (CS) stage follows the CMOS inverter to level-shift the signal higher and provide additional gain. Figure 4.3(c) differs from the TIA described in [DYC+06] in that a current source ($M_{2P}$) is used to set the bias current density and provide power supply rejection. However, accommodating the current source while biasing the TIA at $J_{OPT}$ would require either a higher supply voltage ($VDD \approx 1.4 \text{ V}$) or a very wide tail current device ($W \approx 1.5 \text{ mm with } V_{eff} \approx 120 \text{ mV}$), so this topology was not used.
nMOS TIA with CS

The TIA in Figure 4.3(d) uses a CS amplifier with active load for the voltage-gain stage, followed by another CS stage to provide more gain and level-shifting (as with the CMOS TIA). This topology has recently been used as a broadband preamplifier ([DYC+06], [SVC06]). One possible issue with this topology is the output swing being limited on the low side due to $M_1$ being diode-connected at DC.

nMOS TIA with Passive Bias

The TIA in Figure 4.3(e) is a simplified version of a topology commonly used in discrete realizations (pp. 395-406, [Lee04b]). It is similar to the nMOS TIA with CS but uses passive biasing ($R_1$) to raise the output CM, so the level-shifting CS stage is not required. One disadvantage is that if $R_1$ is not sufficiently large, the input match, and therefore the gain of the TIA when driven with a non-zero source impedance (as in Figure 4.2(b)), will be degraded [Lee04b]. Instead, a topology using active devices for biasing was considered.

nMOS TIA with Active Bias

The TIA in Figure 4.3(f) is similar to that of Figure 4.3(e), but the higher output resistance of $M_3$ compared to $R_1$ improves input matching and gain. One disadvantage is the noise contributed by $M_3$, which appears directly at the input. Suggestions for reducing the extra noise, and expressions for estimating the TIA bandwidth, are given in Appendix B. To the author’s knowledge, this topology (nMOS TIA with active bias) has not previously been implemented in CMOS, either as a broadband preamplifier or photodiode TIA.

The preamplifier topologies were thus narrowed down to two possibilities: the nMOS TIA with CS and the nMOS TIA with active bias. The following section presents a simulation comparison between the two, and describes the final design.
Preamplifier Design and Comparison

The design procedure given in [DYC+06] for the nMOS TIA with CS topology was followed, resulting in the circuit shown in Figure 4.4(a). Transistor $M_1$ was biased near the optimum $NF_{MIN}$ current density (0.15 mA/$\mu$m), corresponding to a gate-source voltage of 0.56 V. The width of $M_{1P}$ ($W_{1P}$) was made double the width of $M_1$ ($W_1$). To first order, the choice of current density sets the gain $A$ (from $V_i$ to the drain of $M_1$) since

$$A = g_{m1}(r_{ol}|r_{o1P}) = g_{m1}r_o$$  \hspace{1cm} (4.4)$$

where $g_{m1} \propto W_1$ and $r_o \propto \frac{1}{W_1}$ for a given current density, making $A$ independent of $W_1$. The approximate value of $R_f$ required to set $R_{in}$ to the desired 75 $\Omega$ source impedance was found from equation 4.2. The width $W_1$ was chosen to make the optimal source impedance $Z_{S,OPT}$ of the stage also near 75 $\Omega$. Inductor $L_f$ extends bandwidth and reduces the input-referred noise of $R_f$ [TPM+04]. The CS transistor $M_2$ was sized half as large as $M_1$ as was done in [DYC+06], and load resistor $R_l$ was chosen to make the CS stage gain near 0 dB. This was done so that the gains of both TIAs under consideration would be the same (and approximately equal to the gain targeted in Figure 4.1).

The design of the nMOS TIA with active bias in Figure 4.4(b) is very similar to the nMOS TIA with CS, apart from the addition of $M_3$ and the removal of the CS stage. In order to source the extra DC current flowing through $R_f$ and $M_3$ while maintaining the same current density of $M_1$, $W_{1P}$ was increased by 20%.

For both TIA topologies, the simulated AC gain, $|S_{11}|$, NF and gain compression at 10 GHz are shown in Figure 4.5(a)-Figure 4.5(d), with the results summarized in Table 4.1. The simulations included 30 fF of capacitance at the input and output nodes. The AC response and input match were essentially the same for both topologies. However, the 10-GHz NF and $P_{1dB}$ of the nMOS TIA with active bias were 0.5 dB lower and 50% higher, respectively, indicating slightly lower noise and greater output swing. Note that by increasing the value of $R_l$, the nMOS TIA with CS can have significantly larger gain than the nMOS TIA with active bias and would, therefore, tend to lower the
Figure 4.4: Broadband preamplifiers used for simulation comparison: (a) nMOS TIA with CS, (b) nMOS TIA with active bias.

The schematic of the implemented nMOS TIA with active bias is shown in Figure 4.6. Approximately 1 mA of bias current drawn by $M_3$ flows through $R_f$ at DC. By using

\begin{table}[h]
\centering
\begin{tabular}{|c|c|c|}
\hline
TIA topology comparison results. & nMOS TIA: CS & Active Bias \\
\hline
$A_{DC}$ (dB) & 8.4 & 8.4 \\
$BW$ (GHz) & 13.4 & 13.4 \\
$S_{11} < -15$ dB up to: (GHz) & 17.6 & 17.2 \\
NF @ 10 GHz (dB) & 6.2 & 5.7 \\
$P_{1dB}$ @ 10 GHz ($V_{pp}$) & 0.28 & 0.42 \\
\hline
\end{tabular}
\end{table}
Figure 4.5: Simulation comparison between nMOS TIA with active bias (solid) and nMOS TIA with CS (dashed): (a) AC gain, (b) $|S_{11}|$, (c) NF and (d) gain compression at 10 GHz.
M₃ instead of a resistor, the current source output resistance was increased (≈ 1 kΩ versus 0.5 kΩ). Inductors $L_p$ and $L_g$ were added to improve matching and provide bandwidth extension [HC06]. Although the input is single-ended, a dummy stage was used to provide power supply rejection at the expense of higher power and noise.

**Simulation Results**

The AC gain is shown in Figure 4.7(a), with and without inductors $L_p$ and $L_g$. These inductors improved high-frequency matching and NF, but caused gain peaking near 30 GHz. This was left unchanged because the peaking occurred well above the target symbol frequency of 20 GHz, and was removed by the finite bandwidth of later stages. The DC gain of 7.5 dB drops by 3 dB at 11.6 GHz. The $|S_{11}|$, NF and NF$_{MIN}$ are shown in Figure 4.7(b), with $|S_{11}|$ less than -15 dB up to 16.6 GHz, and NF of 5.8 dB at 10 GHz. Gain compression as a function of single-ended input swing at 10 GHz is shown in Figure 4.8, with a corresponding input-referred $P_{1dB}$ of 470 mV$_{pp}$. A summary of simulation results is given in Table 4.2.
Figure 4.7: TIA: (a) AC gain and (b) |S_{11}|, NF and NF_{MIN}.

Figure 4.8: TIA: Gain compression as a function of single-ended input swing at 10 GHz.

Table 4.2: Broadband preamplifier simulation summary.

<table>
<thead>
<tr>
<th>Corner</th>
<th>TT/80°C</th>
<th>SS/100°C</th>
<th>FF/20°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>A_{DC} (dB)</td>
<td>7.5</td>
<td>8.2</td>
<td>5.9</td>
</tr>
<tr>
<td>BW (GHz)</td>
<td>11.6</td>
<td>8.2</td>
<td>13.4</td>
</tr>
<tr>
<td>S_{11} &lt; -15 dB up to: (GHz)</td>
<td>16.6</td>
<td>14.7</td>
<td>17.2</td>
</tr>
<tr>
<td>NF @ 10 GHz (dB)</td>
<td>5.8</td>
<td>6.1</td>
<td>5.2</td>
</tr>
<tr>
<td>P_{1dB} @ 10 GHz (V_{pp})</td>
<td>0.47</td>
<td>0.46</td>
<td>0.53</td>
</tr>
</tbody>
</table>
4.1.3 Single-ended to Differential Stage (S2D)

The cable output is single-ended, and the first-stage broadband preamplifier does not provide any CM rejection. However, later blocks are operated differentially, so a single-ended to differential conversion stage (S2D) follows the preamplifier. Transformer-based methods have been used to create differential clock signals from single-ended sources [DBV05], but are less suitable for broadband data with significant low-frequency content. Another conversion method involves driving one side of a differential pair, as shown in Figure 4.9(a). This method was used in this work, with the unused side biased by the dummy preamplifier stage. An equivalent decomposition of Figure 4.9(a) is shown in Figure 4.9(b), where half of the input signal appears as a CM component, and the other half appears differentially (pp. 116, [Raz01]). The S2D should therefore significantly reject CM inputs, and provide at least 6 dB of differential gain if it is desired to keep the output swing (peak-peak, per side) equal to the input swing (peak-peak, single-ended).

S2D Specifications

This section gives the target specifications of the S2D.

- **CM gain:** As an initial specification, $A_{CM} < 20$ dB from DC to 10 GHz (one-half of the symbol rate) was targeted. Note that all stages following the S2D are differential, providing further CM attenuation.

- **$A_{DC}$:** A differential gain of at least 6 dB was desired, which would maintain the output swing (peak-peak, per side) equal to the input swing (peak-peak, single-ended).

- **$BW$:** A bandwidth near 20 GHz was targeted in order to accommodate the peaking equalization occurring in the 10-15 GHz range.

- **Linearity:** A $P_{1dB}$ 3 dB greater than the maximum expected S2D input swing was targeted (as with the preamplifier), giving $P_{1dB} \geq 330$ mV$_{pp}$ single-ended.
Figure 4.9: Differential pair: (a) with single-ended input, and (b) equivalent decomposition into differential and common-mode inputs.

**Circuit Design**

The schematic of the S2D is shown in Figure 4.10. Three stages were used to ensure sufficient rejection of the large effective CM input. The current density of the first differential pair was made lower than in the subsequent stages to accommodate the output CM of the broadband preamplifier. Unlike all subsequent blocks, minimum-length transistors were used for the S2D tail current sources since capacitance at the common source node of the differential pair limits CM rejection at 10 GHz.

**Simulation Results**

The AC responses (with single-ended input) are shown in Figure 4.11(a), and the CM response is shown in Figure 4.11(b). The S2D has a differential-output DC gain \( A_{DC} \) of 8.3 dB with 19 GHz bandwidth, and \( A_{CM} \) of -21.5 dB at 10 GHz. Since mismatch in differential pairs can create differential outputs from CM inputs, \( A_{CM-DM} \) due to mismatch was simulated. A histogram of \( A_{CM-DM} \) at 10 GHz is shown in Figure 4.12, with a mean value of -52.2 dB and standard deviation of 5.0 dB for \( N = 50 \) runs. Gain compression as a function of single-ended input swing at 10 GHz is shown in Figure 4.13, with a corresponding \( P_{1dB} \) of 370 mV_{pp}. A summary of simulation results is given in Table 4.3.
Figure 4.10: S2D: Schematic.

Figure 4.11: S2D: (a) AC gain (single-ended input), and (b) CM gain.
Figure 4.12: S2D: Histogram of $A_{CM-DM}$ due to mismatch at 10 GHz.

Figure 4.13: S2D: Gain compression as a function of single-ended input swing at 10 GHz.

Table 4.3: S2D simulation summary.

<table>
<thead>
<tr>
<th>Corner</th>
<th>TT/80°C</th>
<th>SS/100°C</th>
<th>FF/20°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_{DC}$ (dB)</td>
<td>8.3</td>
<td>7.1</td>
<td>9.3</td>
</tr>
<tr>
<td>$BW$ (GHz)</td>
<td>19.0</td>
<td>17.2</td>
<td>22.8</td>
</tr>
<tr>
<td>$A_{CM}$ @ 10 GHz (dB)</td>
<td>-21.5</td>
<td>-16.3</td>
<td>-20.5</td>
</tr>
<tr>
<td>Mean $A_{CM-DM}$ @ 10 GHz (dB)</td>
<td>-52.2</td>
<td>-48.7</td>
<td>-54.5</td>
</tr>
<tr>
<td>$P_{1dB}$ @ 10 GHz ($V_{pp}$)</td>
<td>0.370</td>
<td>0.410</td>
<td>0.324</td>
</tr>
</tbody>
</table>
4.1.4 Analog Equalizer

An equalizer was included to compensate for ISI remaining after transmitter equalization. The reasons for using the inductor-based split-path peaking topology of Figure 3.6 were presented in section 3.2, along with system simulation results that indicated about 5 dB of peaking (in combination with transmitter equalization) would be sufficient for the target cable.

Analog Equalizer Specifications

This section gives the target specifications of the analog equalizer.

- **Peaking**: At least 5 dB of peaking at 10 GHz was targeted, with any additional peaking desirable in order to compensate for possible bandwidth limitations in other AFE blocks.

- **$A_{DC}$ range**: This equalizer decreases the DC gain as the amount of equalization is increased (see section 3.2). As an initial specification, a minimum DC gain of -6 dB was targeted.

- **Linearity**: A $P_{1dB}$ 3 dB greater than the maximum expected equalizer input swing was targeted, giving $P_{1dB} \geq 860 \text{ mV}_{pp}$ differential.

Circuit Design

The schematic of the equalizer is shown in Figure 4.14. The low-pass and high-pass paths are formed by transistors $M_{1,2}$ and $M_{3,4}$, respectively. The outputs of these paths are summed by $M_{5}-M_{8}$ with a weighting set by $eq_{ctlp}$ and $eq_{ctln}$. Simple gain expressions for this topology were given in section 3.2. Re-stating equation 3.2 for this equalizer gives

$$A_{equalizer}(s) = g_{m1,2}g_{m5,6}R_{1,2}R_{5,6}\cdot \frac{1 + \frac{sL_{3,4}}{R_{5,6}}}{1 + \frac{sL_{3,4}}{R_{5,6}}} = A_{DC} \cdot \frac{1 + \frac{s}{\omega_{z1}}}{1 + \frac{s}{\omega_{p1}}}$$ (4.5)
where $A_{DC} = g_{m1,2}g_{m5,6}R_{1,2}R_{5,6}$, $\omega_{z1} = \frac{R_{3,4}}{L_{3,4}(1+\frac{2g_{m7,8}g_{m3,4}R_{3,4}}{g_{m5,6}g_{m1,2}R_{1,2}})}$ and $\omega_{p1} = \frac{R_{3,4}}{L_{3,4}}$.

As a starting point, identical sizing and geometry of $M_1$-$M_4$ and $R_1$-$R_4$ was used to ensure equal low-pass and high-pass output CM levels going into the summing stage. The output CM levels of the low-pass and high-pass paths (nodes $lpp/lpn$ and $hpp/hpn$, respectively) were raised to 1 V to increase the control range of the equalization control signals $eq_{ctlp}$ and $eq_{ctln}$. The output CM of the summing stage was lowered to 0.95 V which was more suitable for the following AFE block, and allowed increasing $R_{5,6}$ and hence $A_{DC}$ in equation 4.5.

If the pole and zero frequency are kept constant, increasing $L_{3,4}$ allows proportional increases in $R_{3,4}$ and $R_{1,2}$, hence, in the equalizer’s DC gain, $A_{DC}$. For this design, an inductance of 1 nH was used. With the geometry described in Appendix A, this value could be realized with an SRF $> 50$ GHz, well above the targeted peaking frequencies. The location of $\omega_{p1}$ was set at $2\pi \cdot 13$ GHz (65% of the symbol rate), resulting in a $R_{1,2}$ and $R_{3,4}$ of 82 $\Omega$. The values of $R_{1}-R_{4}$ along with the target output CM of 1 V determined the tail currents for the low-pass and high-pass paths, and the desired bias current density determined the widths of $M_1$-$M_4$. The range of control signals $eq_{ctlp}$ and $eq_{ctln}$ was chosen so that all transistors remained in the saturation region, and adjusted to keep the equalizer output CM constant. While both control signals were applied manually, adaptive equalization would be simplified if the control signal pair could be generated from a single input. A circuit that performed this function was used by the split-path equalizer in [GR07]. Note that a smaller value of $L_{3,4}$ could have been used without changing the equalizer transfer function if different widths for $M_{1,2}$ and $M_{3,4}$ had been considered, at the cost of increased power dissipation. For example, if $R_{3,4}$ had been halved, $L_{3,4}$ would be halved as well. If the tail current and width of $M_{3,4}$ had been doubled, $g_{m3,4}$ would also have doubled. Under these conditions, the transfer function in equation 4.5 would remain the same, permitting a smaller inductor at the cost of more power.
Simulation Results

The AC responses of the low-pass \((A_{LP} = \frac{\Delta in}{\Delta out})\) and high-pass \((A_{HP} = \frac{\Delta hp}{\Delta in})\) equalizer paths are shown in Figure 4.15(a) and Figure 4.15(b). The low-pass path has a DC gain of 1.3 dB and bandwidth of 33.8 GHz. The high-pass path has a maximum gain of 0.3 dB at approximately 20 GHz. The overall equalizer AC responses \((A_{EQ} = \frac{\Delta out}{\Delta in})\) for various equalizer settings are shown in Figure 4.16(a) and Figure 4.16(b). The equalizer has a DC gain range of -8.6 to 0.3 dB, and maximum peaking of 8.6 dB. Gain compression as a function of input swing at 10 GHz is shown in Figure 4.17, with a corresponding \(P_{1dB}\) of 668 mV_{pp}, about 20% less than the targeted value. The target could have been met by including degeneration resistors in the differential pair stages, at the cost of lower gain. However, the required resistances were on the order of 30 Ω, and would have occupied significant area (≈ 350 µm² each, assuming the same unit finger size as in the load resistors), so the lower \(P_{1dB}\) was tolerated in order to reduce area. Equalizer transient simulations were done with 40-Gb/s 4-PAM data and the 40-m cable model described in section 2.2. The channel output (i.e. input to the equalizer) is shown in Figure 4.18(a), where a transmitter PWM setting of 52.5% was used as in the system simulations of section 3.2. The equalized output is shown in Figure 4.18(b). A summary of simulation results is given in Table 4.4.

<table>
<thead>
<tr>
<th>Corner</th>
<th>TT/80°C</th>
<th>SS/100°C</th>
<th>FF/20°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>(A_{DC}) (dB)</td>
<td>-8.6 to 0.3</td>
<td>-3.3 to -0.6</td>
<td>-7.7 to 0.9</td>
</tr>
<tr>
<td>Max. Peaking (dB)</td>
<td>8.6</td>
<td>4.1</td>
<td>8.5</td>
</tr>
<tr>
<td>Min. (P_{1dB})</td>
<td>0.668</td>
<td>0.805</td>
<td>0.625</td>
</tr>
<tr>
<td>LP Path Gain (dB)</td>
<td>1.3</td>
<td>1.0</td>
<td>1.4</td>
</tr>
<tr>
<td>LP Path BW (GHz)</td>
<td>33.8</td>
<td>32.7</td>
<td>36.3</td>
</tr>
<tr>
<td>Max. HP Path Gain (dB)</td>
<td>0.3</td>
<td>-0.1</td>
<td>0.5</td>
</tr>
<tr>
<td>((eq_p, eq_n)) @ Min. EQ (V)</td>
<td>(0.39, 0.60)</td>
<td>(0.48, 0.70)</td>
<td>(0.27, 0.55)</td>
</tr>
<tr>
<td>((eq_p, eq_n)) @ Max. EQ (V)</td>
<td>(0.66, 0.27)</td>
<td>(0.70, 0.48)</td>
<td>(0.55, 0.27)</td>
</tr>
</tbody>
</table>
Figure 4.14: Equalizer: Schematic.
Figure 4.15: Equalizer: AC gains of the LP and HP paths on (a) linear and (b) log scales.

Figure 4.16: Equalizer: AC gains for various equalizer settings on (a) linear and (b) log scales.
Figure 4.17: Equalizer: Gain compression as a function of differential input swing at 10 GHz for the worst-case (maximum equalization) setting.

Figure 4.18: Equalizer: Transient simulation with 40-Gb/s 4-PAM data and the 40-m cable model ($2^{10} - 1$ PRBS input applied differentially and scaled by the gain of the previous stages): (a) equalizer input (with 52.5% PWM transmitter equalization), and (b) equalizer output.
4.1.5 Variable-Gain Amplifier (VGA)

A variable-gain amplifier (VGA) follows the equalizer, and was used to compensate for the low-frequency equalizer losses that increase with the amount of peaking applied. The unit gain control cell was a differential pair degenerated with a variable resistor, implemented as a triode-region nMOS device.

VGA Specifications

This section gives the target specifications of the VGA.

- $A_{DC}$ range: As the VGA was intended mainly to compensate for losses due to the equalizer (see Table 4.4), a minimum differential gain range of 0 to 6.5 dB was desired.

- $BW$: A minimum bandwidth near 20 GHz (at the maximum gain setting) was targeted in order to accommodate the peaking equalization occurring in the 10-15 GHz range.

- Linearity: A $P_{1dB}$ 3 dB greater than the maximum expected VGA input swing was targeted, giving $P_{1dB} \geq 565$ mV$_{pp}$ differential.

Circuit Design

The schematic of the VGA is shown in Figure 4.19. Three source-degenerated differential pairs were cascaded to achieve the desired gain range. Splitting the tail current sources into halves meant no DC current flowed through the degeneration resistors, which relaxed headroom constraints and allowed for fixed output CM levels independent of the variable degeneration resistor values. In adaptive designs the MOS resistor is often placed in parallel with a passive resistor to set a maximum allowable resistance, which aids adaptation but reduces the gain tuning range [CHJ04]. In order to increase the gain range of this block, a passive resistor was not included. The input CM was lowered by 50 mV in the first unit cell and maintained throughout the VGA. This was done to increase the achievable gain of each unit cell, and to lower the drain and source
voltages of the nMOS resistors in order to maintain a linear resistor characteristic by increasing the gate-source voltage. Due to the higher input CM, the first unit cell was biased at a higher current density in order to match the drain and source voltages of the nMOS resistor to those in the following cells. The signal $r_{\text{ctl}}$ controls the VGA gain, with a nominal range of 0.7 to 1.3 V.

**nMOS Resistor**

An nMOS transistor in the triode region behaves as a voltage-controlled resistor with $R_{on} = \frac{|\mu_n|C_{ox} W}{L} (V_{GS} - V_T)$ if $V_{DS} \ll 2(V_{GS} - V_T)$ (pp. 18, [Raz01]). From simulation, the maximum expected value of $V_{DS}$ across any nMOS resistor was approximately 50 mV. With $V_S = 250$ mV (set by the input CM and unit cell bias current density) and threshold voltage $V_T = 280$ mV, the condition $V_{DS} \ll 2(V_{GS} - V_T)$ gives $V_G \gg 0.555$ V, so a minimum $V_G$ (or $r_{\text{ctl}}$ in Figure 4.19) of 0.7 V was chosen. The nMOS resistors had double the minimum gate length as simulations indicated this would lower $V_T$, increasing the allowable range of $r_{\text{ctl}}$.

**Simulation Results**

The AC responses for various gain-control settings ($r_{\text{ctl}}$) are shown in Figure 4.20. The VGA has a gain range of 0 to 6.5 dB and a minimum bandwidth of 19.6 GHz. Gain compression as a function of input swing at 10 GHz is shown in Figure 4.21, with a corresponding minimum $P_{1dB}$ of 553 mV$_{pp}$. The resistance of the nMOS resistors in Figure 4.19 as a function of $V_{DS}$ for various values of $r_{\text{ctl}}$ is shown in Figure 4.22. As $V_{DS}$ increases from 0 to 50 mV (the maximum expected value), across the range of $r_{\text{ctl}}$ the resistance changes by a maximum of +3.8%. A summary of simulation results is given in Table 4.5.

**4.1.6 Output Driver**

An output driver was used to provide appropriate termination and signal swing to the 50-Ω testing environment. This stage was required solely for testing, as a fully integrated receiver (as in Figure 1.2) would slice the AFE output on-chip.
Figure 4.19: VGA: Schematic.

Figure 4.20: VGA: AC gain for various gain control settings ($r_{ctl}$).
Figure 4.21: VGA: Gain compression as a function of differential input swing at 10 GHz.

Figure 4.22: Resistance of triode-region nMOS (W/L = 46/0.2) vs. $V_{DS}$ for various values of $r_{ctl}$.

Table 4.5: VGA simulation summary.

<table>
<thead>
<tr>
<th>Corner</th>
<th>TT/80°C</th>
<th>SS/100°C</th>
<th>FF/20°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_{DC}$ (dB)</td>
<td>0 to 6.5</td>
<td>0.8 to 5.4</td>
<td>0.5 to 6.8</td>
</tr>
<tr>
<td>Min. $BW$ (GHz)</td>
<td>19.6</td>
<td>17.9</td>
<td>23.9</td>
</tr>
<tr>
<td>$P_{1dB}$ @ 10 GHz, Min. Gain (V$_{pp}$)</td>
<td>0.777</td>
<td>0.823</td>
<td>0.585</td>
</tr>
<tr>
<td>$P_{1dB}$ @ 10 GHz, Max. Gain (V$_{pp}$)</td>
<td>0.553</td>
<td>0.675</td>
<td>0.432</td>
</tr>
<tr>
<td>$\Delta R_{triode}$ @ $V_{DS} = 50$ mV (%)</td>
<td>3.8</td>
<td>2.4</td>
<td>5.4</td>
</tr>
</tbody>
</table>
Output Driver Specifications

This section gives the target specifications of the output driver.

- $A_{DC}$: A gain of approximately 0 dB with the doubly-terminated 50-Ω (25-Ω effective) output load was targeted in order to drive the test equipment with sufficient swing.

- $BW$: As with previous blocks, a bandwidth of at least 20 GHz was targeted in order to preserve the AFE frequency peaking in the 10-15 GHz range.

- Linearity: A $P_{1dB}$ 3 dB greater than the maximum expected output driver input swing was targeted, giving $P_{1dB} \geq 565 \text{ mV}_{pp}$ differential.

Circuit Design

The schematic of the output driver is shown in Figure 4.23. Two stages were used to relax the gain-bandwidth requirements of each stage. The current density of the final differential pair was lowered in order to achieve the desired gain with the (relatively low) doubly-terminated load. The maximum possible output swing is given by the product of the final-stage tail current and load, i.e. $14 \text{ mA} \times 25 \Omega = 350 \text{ mV}_{pp}$ per side, large enough to accommodate the expected range of AFE inputs and gains.

Simulation Results

The AC response is shown in Figure 4.24. The output driver has a DC gain of 0.4 dB with 25.6 GHz bandwidth. Gain compression as a function of differential input swing at 10 GHz is shown in Figure 4.25, with a corresponding $P_{1dB}$ of 618 mV$_{pp}$. A summary of simulation results is given in Table 4.6.

4.1.7 AFE Simulations

This section presents simulation results of the full AFE. A summary of main simulated results is given in Table 4.7, and compared with target AFE specifications as applicable.
Figure 4.23: Output driver: Schematic.

Figure 4.24: Output driver: AC gain.

Table 4.6: Output driver simulation summary.

<table>
<thead>
<tr>
<th>Corner</th>
<th>TT/80°C</th>
<th>SS/100°C</th>
<th>FF/20°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>$A_{DC}$ (dB)</td>
<td>0.4</td>
<td>-0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>$BW$ (GHz)</td>
<td>25.6</td>
<td>23.5</td>
<td>29.5</td>
</tr>
<tr>
<td>$P_{1dB}$ @ 10 GHz ($V_{pp}$)</td>
<td>0.618</td>
<td>0.722</td>
<td>0.507</td>
</tr>
</tbody>
</table>
The single-ended $|S_{21}|$ and NF for maximum and minimum VGA gains across equalizer setting are shown in Figure 4.26(a)-Figure 4.26(d) and Figure 4.27(a)-Figure 4.27(b), with frequency peaking and NF (each at 10 GHz) of 4.6 dB and 12.9 dB, respectively.

The single-ended available input-referred and differential output-referred noise spectra at the limits of VGA and equalizer control settings are shown in Figure 4.28(b)-Figure 4.28(a). The corresponding RMS noise voltages are shown in Table 4.7, where the output noise was integrated from 10 kHz-100 GHz, and the input-referred RMS noise was defined as the differential output-referred RMS noise divided by the differential mid-band gain. At the maximum EQ/maximum VGA setting (the setting appropriate for long cables), the differential output and input-referred noise voltages were 2.0 mV$_{rms}$ and 0.36 mV$_{rms}$, respectively.

The simulated gain compression at the limits of VGA and equalizer control settings as a function of single-ended input swing at 10 GHz is shown in Figure 4.29, with the corresponding $P_{1dB}$ values shown in Table 4.7. At the maximum EQ/maximum VGA setting, $P_{1dB}$ was 68 mV$_{pp}$, while at the minimum EQ/minimum VGA setting, $P_{1dB}$ was 82 mV$_{pp}$. Assuming the 4-PAM transmitter has an adjustable swing of 0.4 - 1.6 V$_{pp}$, system modeling predicted the allowable range of cable lengths to be between 20 m to 40 m. Cable lengths below 20 m would cause the input swing to be too large for the AFE. Note that the original desired input swing of up to 100 mV$_{pp}$ was not reached despite the $P_{1dB}$ targets of the individual blocks being met (with the
The output driver was responsible for a significant portion of the degradation, but would not be required in an integrated receiver. Accordingly, the $P_{1dB}$ values excluding the output driver are also shown in Table 4.7, where the 100 mV$_{pp}$ target is met for the minimum VGA settings.

Transient AFE simulations were done for a variety of channel and transmitter equalization settings. The 4-PAM eye diagrams in Figure 4.31(a)-Figure 4.31(b) and Figure 4.31(c)-Figure 4.31(d) are for a 0-m cable with no transmitter equalization (and transmitter swing below 0.4 V$_{pp}$) at 33.3 Gb/s and 40 Gb/s, respectively. The 4-PAM eye diagrams in Figure 4.32(a)-Figure 4.32(b) are for a 40-m cable at 33.3 Gb/s with 55% PWM transmitter equalization, representing the maximum bit rate for the target cable length. The 40-m cable model had 28.5 dB of loss at 8.3 GHz. The 4-PAM eye diagrams in Figure 4.32(c)-Figure 4.32(d) are for a 30-m cable at 40 Gb/s again with 55% PWM transmitter equalization, representing the maximum cable length for the target bit rate. The 30-m cable model had 23.9 dB of loss at 10 GHz.

Transient simulations were also done in 2-PAM mode. The 2-PAM eye diagrams in Figure 4.33(a)-Figure 4.33(b) and Figure 4.33(c)-Figure 4.33(d) are for a 15-m cable with no transmitter equalization at 16.6 Gb/s and 20 Gb/s, respectively. The 15-m cable model had 10.7 dB of loss at 8.3 GHz, and 12.0 dB of loss at 10 GHz. The simulated 2-PAM results may be compared to the measured results in Chapter 5. The frequency responses of all cable models that were used in these simulations are shown in Figure 4.30.

Note that the effects of (and circuit techniques to handle) offsets due to mismatch were not considered in this work, but should be in practice.

### 4.2 Conclusion

This chapter has described the circuit design of each block of the 4/2-PAM 20-GSymbol/s receiver AFE. Simulation results have been presented, showing the expected performance of the fabricated AFE. Measured results are given in Chapter 5.
Figure 4.26: AFE: Simulated single-ended $|S_{21}|$ for ((a),(b)) maximum and ((c),(d)) minimum VGA gains across equalizer setting (linear and log frequency scales).
Figure 4.27: AFE: Simulated single-ended NF for (a) maximum and (b) minimum VGA gains across equalizer setting.

Figure 4.28: AFE: Simulated noise voltages at the limits of VGA and equalizer control settings (75-Ω source impedance): (a) differential output noise and (b) single-ended available input-referred noise.
Figure 4.29: AFE: Simulated gain compression at the limits of VGA and equalizer control settings, as a function of single-ended input swing at 10 GHz.

Figure 4.30: Cable model frequency responses used in AFE transient simulations.
Figure 4.31: AFE: Simulated 4-PAM single-ended input and differential output eye diagrams (no transmitter equalization): ((a),(b)) 0-m cable at 33.3 Gb/s and ((c),(d)) 0-m cable at 40 Gb/s.
Figure 4.32: AFE: Simulated 4-PAM single-ended input and differential output eye diagrams (55% PWM transmitter equalization): ((a),(b)) 40-m cable at 33.3 Gb/s and ((c),(d)) 30-m cable at 40 Gb/s.
Figure 4.33: AFE: Simulated 2-PAM single-ended input and differential output eye diagrams (no transmitter equalization): ((a),(b)) 15-m cable at 16.6 Gb/s and ((c),(d)) 15-m cable at 20 Gb/s.
Table 4.7: AFE Simulation Summary.

<table>
<thead>
<tr>
<th></th>
<th>Target</th>
<th>TT/80°C</th>
<th>SS/100°C</th>
<th>FF/20°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_{11} &lt; -10 , \text{dB}$ up to:</td>
<td>10 GHz</td>
<td>19.8 GHz</td>
<td>17.4 GHz</td>
<td>22.4 GHz</td>
</tr>
<tr>
<td>$S_{11} &lt; -15 , \text{dB}$ up to:</td>
<td>10 GHz</td>
<td>14.9 GHz</td>
<td>12.9 GHz</td>
<td>16.5 GHz</td>
</tr>
<tr>
<td>$</td>
<td>S_{21}</td>
<td>$ Peaking @ 10 GHz</td>
<td>5 dB</td>
<td>4.6 dB</td>
</tr>
<tr>
<td>Gain Control Range</td>
<td>6.5 dB</td>
<td>6.8 dB</td>
<td>4.5 dB</td>
<td>6.3 dB</td>
</tr>
<tr>
<td>$P_{1dB}$ @ 10 GHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>min EQ, min VGA</td>
<td>&gt; 100 mV&lt;sub&gt;pp&lt;/sub&gt;</td>
<td>82 mV&lt;sub&gt;pp&lt;/sub&gt;</td>
<td>115 mV&lt;sub&gt;pp&lt;/sub&gt;</td>
<td>58 mV&lt;sub&gt;pp&lt;/sub&gt;</td>
</tr>
<tr>
<td>max EQ, min VGA</td>
<td>93 mV&lt;sub&gt;pp&lt;/sub&gt;</td>
<td>118 mV&lt;sub&gt;pp&lt;/sub&gt;</td>
<td>68 mV&lt;sub&gt;pp&lt;/sub&gt;</td>
<td></td>
</tr>
<tr>
<td>min EQ, max VGA</td>
<td>54 mV&lt;sub&gt;pp&lt;/sub&gt;</td>
<td>89 mV&lt;sub&gt;pp&lt;/sub&gt;</td>
<td>39 mV&lt;sub&gt;pp&lt;/sub&gt;</td>
<td></td>
</tr>
<tr>
<td>max EQ, max VGA</td>
<td>&gt; 60 mV&lt;sub&gt;pp&lt;/sub&gt;</td>
<td>68 mV&lt;sub&gt;pp&lt;/sub&gt;</td>
<td>95 mV&lt;sub&gt;pp&lt;/sub&gt;</td>
<td>46 mV&lt;sub&gt;pp&lt;/sub&gt;</td>
</tr>
<tr>
<td>(Excluding output driver)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>min EQ, min VGA</td>
<td>&gt; 100 mV&lt;sub&gt;pp&lt;/sub&gt;</td>
<td>105 mV&lt;sub&gt;pp&lt;/sub&gt;</td>
<td>141 mV&lt;sub&gt;pp&lt;/sub&gt;</td>
<td>75 mV&lt;sub&gt;pp&lt;/sub&gt;</td>
</tr>
<tr>
<td>max EQ, min VGA</td>
<td>108 mV&lt;sub&gt;pp&lt;/sub&gt;</td>
<td>140 mV&lt;sub&gt;pp&lt;/sub&gt;</td>
<td>83 mV&lt;sub&gt;pp&lt;/sub&gt;</td>
<td></td>
</tr>
<tr>
<td>min EQ, max VGA</td>
<td>87 mV&lt;sub&gt;pp&lt;/sub&gt;</td>
<td>128 mV&lt;sub&gt;pp&lt;/sub&gt;</td>
<td>66 mV&lt;sub&gt;pp&lt;/sub&gt;</td>
<td></td>
</tr>
<tr>
<td>max EQ, max VGA</td>
<td>&gt; 60 mV&lt;sub&gt;pp&lt;/sub&gt;</td>
<td>98 mV&lt;sub&gt;pp&lt;/sub&gt;</td>
<td>130 mV&lt;sub&gt;pp&lt;/sub&gt;</td>
<td>74 mV&lt;sub&gt;pp&lt;/sub&gt;</td>
</tr>
<tr>
<td>NF @ 10 GHz</td>
<td></td>
<td>12.9 dB</td>
<td>13.3 dB</td>
<td>11.2 dB</td>
</tr>
<tr>
<td>Differential Output Noise</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>min EQ, min VGA</td>
<td>- 1.6 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
<td>1.4 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
<td>1.7 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
<td></td>
</tr>
<tr>
<td>max EQ, min VGA</td>
<td>- 1.3 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
<td>1.3 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
<td>1.3 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
<td></td>
</tr>
<tr>
<td>min EQ, max VGA</td>
<td>- 3.0 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
<td>2.1 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
<td>3.0 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
<td></td>
</tr>
<tr>
<td>max EQ, max VGA</td>
<td>&lt;6.6 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
<td>2.0 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
<td>1.8 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
<td>2.2 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
</tr>
<tr>
<td>Input-Reflected Noise</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>min EQ, min VGA</td>
<td>- 0.22 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
<td>0.23 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
<td>0.20 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
<td></td>
</tr>
<tr>
<td>max EQ, min VGA</td>
<td>- 0.49 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
<td>0.28 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
<td>0.43 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
<td></td>
</tr>
<tr>
<td>min EQ, max VGA</td>
<td>- 0.18 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
<td>0.20 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
<td>0.18 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
<td></td>
</tr>
<tr>
<td>max EQ, max VGA</td>
<td>&lt;1.3 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
<td>0.36 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
<td>0.24 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
<td>0.35 mV&lt;sub&gt;rms&lt;/sub&gt;</td>
</tr>
</tbody>
</table>
5 Layout and Measurements

This chapter presents the layout and measurement results of the 4/2-PAM receiver AFE fabricated in the 90-nm CMOS design kit from STMicroelectronics. Section 5.1 describes the AFE layout. Section 5.2 presents the equipment setup and measurement results of the S parameter, linearity and transient tests.

5.1 Circuit Layout

The die photo of the AFE is shown in Figure 5.1. Multiple power and ground pads were used to reduce IR drop and electromigration. The references $bias_n$ and $bias_p$ set bias levels in the broadband preamplifier. The controls $eq_{ctln}$ and $eq_{ctlp}$ determined the equalization setting, and $r_{ctl}$ set the VGA gain. The reference $vref$ set the tail currents for all differential stages. The fabricated AFE occupies an area of 1.33 mm x 0.67 mm = 0.89 mm$^2$ and dissipates 138 mW from a 1.3 V supply.

Figure 5.1: AFE die photo.
5.2 Measurements

This section presents the equipment setup and measurement results for S parameter, linearity and transient testing of the AFE. All signals were applied and measured single-endedly through wafer probing.

5.2.1 Test Equipment and Setup

A list of all test equipment used is given below. The two 67-GHz probes were used to probe the AFE input and output, while the two DC probes provided bias and control signals. A block diagram of the measurement setup is shown in Figure 5.2. The National Instruments (NI) PCI-6733 board was used with the NI BNC-2110 Shielded Connector Block (capable of outputting eight analog signals with 16-bit accuracy) to provide all DC bias/control to the AFE, except for the supply voltage.

Equipment List

- 2x 67-GHz GSGSG Probes
- 2x DC GPPGPPGPPG Probes
- NI PCI-6733 Board (8x 16-bit analog output channels controlled by PC) with NI BNC-2110 Shielded Connector Block
- HP 8510C 26.5-GHz VNA
- HP 83650B Synthesized Swept Signal Generator (10 MHz - 50 GHz)
- HP 8565E Spectrum Analyzer (30 Hz - 50 GHz)
- Centellax Pattern Generator (OTB3P1A 10-Gb/s PRBS, UXC40M Divider, MS4S1M 4-to-1 Multiplexer)
- Agilent 86100C Infinium DCA-J Wideband Oscilloscope
Figure 5.2: Block diagram of measurement setup (S parameter, linearity and transient).
5.2.2 S parameters

S parameters were measured using a HP 8510C 26.5-GHz VNA with the setup shown in Figure 5.2. Since the target cable channel is 75-Ω, all S parameters were converted from a 50-Ω to 75-Ω/50-Ω input/output port environment using the expressions in [Dob91]. The measured and simulated single-ended $|S_{11}|$ and $|S_{22}|$ are shown in Figure 5.3, with $|S_{11}|$ and $|S_{22}|$ below -10 dB up to 16 GHz and 20 GHz, respectively. The measured and simulated single-ended $|S_{21}|$ for various equalizer and VGA settings are shown in Figure 5.4(a), with the measurements re-plotted on a log frequency scale in Figure 5.4(b). The upper plot in Figure 5.4(a) is for minimum equalization and swept VGA settings, displaying 6 dB of gain variation (versus the targeted 6.5 dB) and minimum single-ended gain-bandwidth product (GBW) of 147 GHz. The lower plot in Figure 5.4(a) is for minimum VGA and swept equalizer settings, displaying maximum peaking of 6.5 dB at 8 GHz (versus the targeted 5 dB at 10 GHz).

The measured gains were much higher than expected from the simulated TT/80°C corner, with approximately 10-15 dB higher gain (and lower bandwidth). The extra gain may have caused the peaking frequency to be lower than the targeted 10 GHz. The disparity between measured and simulated results is investigated in section 5.2.4.

![Figure 5.3: Measured and simulated $|S_{11}|$ and $|S_{22}|$.](image-url)
Figure 5.4: Measured and simulated $|S_{21}|$: (a) minimum equalization and various VGA settings (top), minimum VGA and various equalizer settings (bottom) (b) measurements re-plotted on a log frequency scale.

### 5.2.3 Linearity

Linearity measurements were done using a HP 83650B 50-GHz signal generator and HP 8565E 50-GHz spectrum analyzer with the setup shown in Figure 5.2. Measured and simulated (TT/80°C) single-ended gain compression data for various equalizer and VGA settings are shown in Figure 5.5(a) and Figure 5.5(b) at 1 GHz and 7 GHz (i.e. at low frequency and near the measured maximum peaking frequency), respectively, with the corresponding $P_{1dB}$ values shown in Table 5.1. The test cable and probe losses were de-embedded from the measurements. The corresponding total harmonic distortion (THD) was calculated using the following equation:

$$THD = \frac{H_2 + H_3 + \cdots + H_n}{H_1} \times 100\% \quad (5.1)$$

where $H_n$ is the power (W) in the $n^{th}$ harmonic. Referring to Figure 5.5(a), the THD for a -40-dBm, 1-GHz input at the (no EQ, min VGA), (no EQ, max VGA) and (max...
EQ, max VGA) settings were 0.01%, 0.19% and 0.03%, respectively. Since measured harmonics had to be above the noise floor, only \( H_2 \) and \( H_3 \) were used in the calculation. With 7-GHz input, the harmonics were not in-band, so THD was not measured for the 7-GHz input.

As was the case with the measured S parameters, in Figure 5.5(a) and Figure 5.5(b) there is a large discrepancy between the measured and simulated results, with the corresponding \( P_{1dB} \) linearity values in Table 5.1 much lower than expected. This difference is also likely related to the extra measured gain, and is addressed in section 5.2.4.

![Graphs showing measured and simulated \( P_{1dB} \) linearity data at 1 GHz and 7 GHz for various equalizer (EQ) and VGA settings.](image)

5.2.4 Measurement and Simulation Disparity

This section presents a possible cause for the differences between measured and expected results, and attempts to verify it through simulation. Since the AFE comprises ten cascaded differential pair stages (excluding the preamplifier), it was suspected that the large excess \(|S_{21}|\) gain (and reduced \( P_{1dB} \) linearity) could be due to the accumulation of smaller excess gain in every stage. Since the differential pairs are passively loaded, larger-than-expected load resistors (implemented in polysilicon) could account
for the increased gain. Also, given the lower-than-expected total DC current drawn, the on-chip temperature could be significantly lower than 80°C.

DC measurements were used to estimate the temperature and process conditions of the AFE. The measured DC current drawn by the AFE was 106 mA, 8.6% lower than the expected 116 mA for the TT/80°C corner. Also accessible as a test structure was the diode-connected NMOS with series resistor shown in Figure 5.6, used for external equalizer control (in Figure 4.14). Here, the measured current was approximately 15% lower than expected for a given applied voltage. For each of the five process corners available (TT/SS/FF/FS/SF), the simulation temperature was set to 30°C and 80°C, with the resistor values either nominal or increased by 20% (resistor values were nominally independent of the selected corner in the design kit used). Of the twenty resulting corner/temperature settings, the TT/30°C/R_+20% most closely matched the AFE and test structure DC current measurements, with a maximum error of 4.8% from the measured values.

In order to further verify this process and temperature setting, the $|S_{21}|$ gain and $P_{1dB}$ linearity were re-simulated under these conditions. The re-simulated and measured $|S_{21}|$ for various equalizer and VGA settings are shown in Figure 5.7, with improved agreement compared to those in Figure 5.4(a). Similarly, the re-simulated and measured gain compression data for various equalizer and VGA settings are shown in Figure 5.8(a) and Figure 5.8(b) at 1 GHz and 7 GHz, respectively, with improved
agreement compared to those in Figure 5.5(a) and Figure 5.5(b). The corresponding improved match in $P_{1dB}$ is shown in Table 5.2, compared to the original results in Table 5.1. The improved agreement between DC current, gain and linearity indicates the fabricated AFE had lower temperature ($\approx 30^\circ$C) and higher resistors ($\approx 20\%$) than expected, with most of the excess gain due to the increased resistance.

5.2.5 Transients

Transient measurements were done using a HP 83650B 50-GHz signal generator and Centellax boards (OTB3P1A 10-Gb/s PRBS, UXC40M divider and MS4S1M 4-to-1 multiplexer) to generate 2-PAM input patterns of up 20.4-Gb/s, and an Agilent 86100C

Figure 5.6: On-chip structure used to estimate temperature and process conditions.

Figure 5.7: Re-simulated (TT/30°C/R$_{+20\%}$) and measured $|S_{21}|$. 

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Figure 5.8: Re-simulated (TT/30°C/R+20%) and measured \( P_{1dB} \) linearity data at (a) 1 GHz and (b) 7 GHz for various equalizer and VGA settings.

Table 5.2: Re-simulated (TT/30°C/R+20%) and measured \( P_{1dB} \) at 1 GHz and 7 GHz for various equalizer and VGA settings.

<table>
<thead>
<tr>
<th>EQ, VGA setting</th>
<th>Measured ( P_{1dB} )</th>
<th>Simulated ( P_{1dB} ) (TT/30°C/R+20%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 GHz, no EQ, min VGA</td>
<td>-30.8 dBm</td>
<td>-32.4 dBm</td>
</tr>
<tr>
<td>1 GHz, no EQ, max VGA</td>
<td>-39.8 dBm</td>
<td>-39.8 dBm</td>
</tr>
<tr>
<td>1 GHz, max EQ, max VGA</td>
<td>-36.8 dBm</td>
<td>-34.3 dBm</td>
</tr>
<tr>
<td>7 GHz, no EQ, min VGA</td>
<td>-31.6 dBm</td>
<td>-31.0 dBm</td>
</tr>
<tr>
<td>7 GHz, no EQ, max VGA</td>
<td>-38.6 dBm</td>
<td>-37.0 dBm</td>
</tr>
<tr>
<td>7 GHz, max EQ, max VGA</td>
<td>-35.6 dBm</td>
<td>-33.5 dBm</td>
</tr>
</tbody>
</table>
wideband oscilloscope with the setup shown in Figure 5.2. The equipment required for 4-PAM signal generation at 40 Gb/s was unavailable at the time of testing, so only 2-PAM results are available. The unexpectedly large gain (and low linearity) of the measured AFE would pose a challenge for transient measurements. In order to facilitate testing, the bias currents of all blocks following the broadband preamplifier were lowered to reduce the AFE gain. This was done by raising the reference voltage $v_{\text{ref}}$ in Figure C.1 from 0.6 V to 0.7 V, as simulations of the TT/30°C/R+20% corner showed that this would bring $|S_{21}|$ closer to what was originally targeted and improve $P_{\text{dB}}$ by up to 6 dB. In this mode, the measured power dissipated by the AFE was 125 mW (versus the original measured 138 mW). Note that all eye diagrams presented in this section are single-ended.

The Centellax board setup was used to generate a 2-PAM 508-bit input pattern for use with the pattern-locking oscilloscope. Basic AFE functionality and VGA control were initially verified at 10-Gb/s, 16.25-Gb/s and 20.4-Gb/s with a clean input signal (i.e. 0-m cable channel) having 30 mVpp swing. At 10-Gb/s, AFE operation with low VGA gain is shown by the output eye diagram and bathtub curve in Figure 5.9(a) and Figure 5.9(b), respectively, while operation with high VGA gain is shown by the eye diagram and bathtub curve in Figure 5.9(c) and Figure 5.9(d). The eye amplitudes in Figure 5.9(a) and Figure 5.9(c) indicate approximately 6.5 dB of gain variation, comparable to what was obtained from S parameter measurements. Similarly, the AFE output eye diagrams and bathtub curves for both low and high VGA gain settings are shown for 16.25-Gb/s input in Figure 5.10(a)-Figure 5.10(d), and 20.4-Gb/s in Figure 5.11(a)-Figure 5.11(d). The specific cause of the oscilloscope reporting the bathtub graph data as questionable in Figure 5.11(d) is not known, but likely due to the measurement setup. For all bit rates tested, the timing margin indicated by the bathtub curves was reduced at higher VGA gain due to the attendant bandwidth reduction.

With basic functionality and VGA control verified, the equalization function was tested at 16.25 Gb/s and 20.4 Gb/s using the same 508-bit input pattern and a 9-ft SMA cable (made from three 3-ft sections.) For the 16.25-Gb/s input, the frequency response $|S_{21}|$ of the 9-ft SMA cable section having 5.7 dB of loss at 8.125 GHz is
shown in Figure 5.12(a), with the corresponding eye diagram shown in Figure 5.12(b). The equalized AFE output eye diagram and bathtub curve are shown in Figure 5.12(c) and Figure 5.12(d), respectively. The input swing was 40 mV<sub>pp</sub>, while the output swing was 225 mV<sub>pp</sub> per side with a maximum RMS jitter of 2.5 ps. Similarly for the 20.4-Gb/s input, Figure 5.13(a) shows that the 9-ft SMA cable section has 7.5 dB of loss at 10.2 GHz, with the corresponding eye diagram shown in Figure 5.13(b). The equalized AFE output eye diagram and bathtub curve are shown in Figure 5.13(c) and Figure 5.13(d), respectively. Note that as with the previous 20.4-Gb/s measurement, the oscilloscope reports the bathtub graph data as questionable. The input swing was 40 mV<sub>pp</sub>, while the output swing was 225 mV<sub>pp</sub> per side with a maximum RMS jitter of 2.7 ps. For both data rates, the amount of loss equalized exceeded the system-level target (given in section 3.2) of 5 dB of peaking at one-half the symbol rate.

### 5.3 Measurement Summary

This section presented S parameter, linearity and transient measurement results of the 4/2-PAM receiver AFE fabricated in the 90-nm CMOS design kit from STMicroelectronics. Operation in 2-PAM mode at 10-Gb/s, 16.25-Gb/s and 20.4-Gb/s was demonstrated, as was equalization of a 9-ft SMA cable. A summary of main measurement results is given in Table 5.3.
Figure 5.9: AFE single-ended output eye diagrams and bathtub curves for 10-Gb/s 2-PAM 508-bit input pattern (no cable channel): ((a), (b)) low VGA gain and ((c),(d)) high VGA gain.
Figure 5.10: AFE single-ended output eye diagrams and bathtub curves for 16.25-Gb/s 2-PAM 508-bit input pattern (no cable channel): ((a), (b)) low VGA gain and ((c), (d)) high VGA gain.
Figure 5.11: AFE single-ended output eye diagrams and bathtub curves for 20.4-Gb/s 2-PAM 508-bit input pattern (no cable channel): ((a), (b)) low VGA gain and ((c),(d)) high VGA gain.
Figure 5.12: Cable loss, single-ended eye diagrams and bathtub curve for 16.25-Gb/s 2-PAM 508-bit input pattern: ((a),(b)) $|S_{21}|$ of a 9-ft SMA cable section (5.7-dB loss at 8.125 GHz) with corresponding AFE input eye diagram; ((c),(d)) equalized AFE output eye diagram and bathtub curve.
Figure 5.13: Cable loss, single-ended eye diagrams and bathtub curve for 20.4-Gb/s 2-PAM 508-bit input pattern: ((a),(b)) $|S_{21}|$ of a 9-ft SMA cable section (7.5-dB loss at 10.2 GHz) with corresponding AFE input eye diagram; ((c),(d)) equalized AFE output eye diagram and bathtub curve.
Table 5.3: Measurement Summary.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>90-nm CMOS</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>1.3 V</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>138 mW</td>
</tr>
<tr>
<td>Area</td>
<td>0.89 mm$^2$</td>
</tr>
<tr>
<td>$</td>
<td>S_{11}</td>
</tr>
<tr>
<td></td>
<td>$&lt;-15$ dB up to 10 GHz</td>
</tr>
<tr>
<td>$</td>
<td>S_{22}</td>
</tr>
<tr>
<td></td>
<td>$&lt;-15$ dB up to 11 GHz</td>
</tr>
<tr>
<td>$</td>
<td>S_{21}</td>
</tr>
<tr>
<td></td>
<td>6.5 dB @ 8 GHz</td>
</tr>
<tr>
<td>Gain Control Range</td>
<td>6.0 dB</td>
</tr>
<tr>
<td>GBW Product</td>
<td>$\geq 294$ GHz (differential)</td>
</tr>
<tr>
<td>$P_{1dB}$ @ 1 GHz</td>
<td></td>
</tr>
<tr>
<td>(no EQ, min VGA)</td>
<td>-30.75 dBm (18.4 mV$_{pp}$)</td>
</tr>
<tr>
<td>(no EQ, max VGA)</td>
<td>-39.75 dBm (6.5 mV$_{pp}$)</td>
</tr>
<tr>
<td>(max EQ, max VGA)</td>
<td>-36.75 dBm (9.2 mV$_{pp}$)</td>
</tr>
<tr>
<td>$P_{1dB}$ @ 7 GHz</td>
<td></td>
</tr>
<tr>
<td>(no EQ, min VGA)</td>
<td>-31.6 dBm (16.6 mV$_{pp}$)</td>
</tr>
<tr>
<td>(no EQ, max VGA)</td>
<td>-38.6 dBm (7.4 mV$_{pp}$)</td>
</tr>
<tr>
<td>(max EQ, max VGA)</td>
<td>-35.6 dBm (10.5 mV$_{pp}$)</td>
</tr>
<tr>
<td>THD (-40-dBm, 1-GHz input)</td>
<td>$\leq 0.19%$</td>
</tr>
</tbody>
</table>

16.25 Gb/s 2-PAM Input

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>9-ft SMA Cable Loss @ 8.125 GHz</td>
<td>5.7 dB</td>
</tr>
<tr>
<td>Input Swing</td>
<td>40 mV$_{pp}$ (single-ended)</td>
</tr>
<tr>
<td>Output Swing</td>
<td>225 mV$_{pp}$ (single-ended)</td>
</tr>
<tr>
<td>RMS Jitter</td>
<td>2.5 ps</td>
</tr>
<tr>
<td>Timing Margin (BER = $10^{-12}$)</td>
<td>0.58 UI</td>
</tr>
</tbody>
</table>

20.4 Gb/s 2-PAM Input

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>9-ft SMA Cable Loss @ 10.2 GHz</td>
<td>7.5 dB</td>
</tr>
<tr>
<td>Input Swing</td>
<td>40 mV$_{pp}$ (single-ended)</td>
</tr>
<tr>
<td>Output Swing</td>
<td>225 mV$_{pp}$ (single-ended)</td>
</tr>
<tr>
<td>RMS Jitter</td>
<td>2.7 ps</td>
</tr>
<tr>
<td>Timing Margin (BER = $10^{-12}$)</td>
<td>0.32 UI (validity uncertain)</td>
</tr>
</tbody>
</table>
6 Conclusion

6.1 Summary

The design of a 4-P AM/2-P AM receiver AFE targeting 40 Gb/s in 90-nm CMOS has been investigated for incorporation into a transceiver for a 40-m Belden 1694A coaxial cable having 50 dB of loss at 20 GHz. This included measurement and modeling of the target cable, and consideration of possible transceiver signaling and equalization methods. This resulted in the decision to use 4-P AM with PWM equalization at the transmitter [Che08] and analog peaking equalization at the receiver. The main functional blocks of the AFE were the broadband preamplifier, analog (split-path) peaking equalizer and VGA. To the author’s knowledge, the nMOS TIA with active bias used as the broadband preamplifier had not previously been implemented in CMOS. The AFE provided a broadband match with $|S_{11}| < -10$ dB up to 16 GHz, with maximum peaking of 6.5 dB at 8 GHz and VGA range of 6.0 dB. A 9-ft SMA cable was equalized in 2-P AM mode at 16.25 Gb/s (5.7 dB loss at 8.125 GHz) and 20.4 Gb/s (7.5 dB loss at 10.2 GHz). Implemented in 90-nm CMOS, the fabricated AFE occupies an area of 0.89 mm$^2$ and dissipates 138 mW from a 1.3 V supply. The receiver AFE is compared with other reported equalizers and CMOS amplifiers in Table 6.1 and Table 6.2, respectively. Although measurements were not done with 4-P AM inputs, a comparison with other CMOS 4-P AM systems is given in Table 6.3 to provide a summary of (and comparison with) the state of the art.

6.2 Future Work

Although the AFE was intended for both 4-P AM and 2-P AM operation, a suitable 4-P AM transmitter was not available during the measurement period. However, the
40-Gb/s transmitter in [Che08] is in the process of being packaged, and should allow for both circuits to be tested together.

Other areas of future work include lessening the AFE sensitivity to resistor variation (a method for which is given in [TMR+06] and [WSJ06], utilizing digitally programmable resistors) and increasing the maximum tolerable signal swing in order to handle a wider range of cable lengths.

In order to develop a complete transceiver, future work includes integration of the 4-PAM latches and decoding logic with the AFE, equalizer adaptation at the transmitter and receiver and clock recovery.

Table 6.1: Comparison with other equalizers. (Loss refers to channel loss compensated at one-half the symbol rate. SP, SF, CD and CH refer to split-path, sum-feedback, capacitive-degeneration and Cherry-Hooper topologies, respectively).

<table>
<thead>
<tr>
<th>Reference</th>
<th>Symbol Rate (GS/s)</th>
<th>Loss (dB)</th>
<th>Modulation</th>
<th>Supply (V)</th>
<th>EQ Power (mW)</th>
<th>Adaptive</th>
<th>Type</th>
<th>Process</th>
<th>Area (mm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ZG05</td>
<td>10</td>
<td>13</td>
<td>2-PAM</td>
<td>3.3</td>
<td>151</td>
<td>YES</td>
<td>SP</td>
<td>0.18-um</td>
<td>0.705</td>
</tr>
<tr>
<td>CHL06</td>
<td>10</td>
<td>8.5</td>
<td>4-PAM</td>
<td>1.8</td>
<td>121</td>
<td>YES</td>
<td>SF</td>
<td>0.18-um</td>
<td>1.259</td>
</tr>
<tr>
<td>HMC+05</td>
<td>10</td>
<td>18</td>
<td>4-PAM</td>
<td>1.8</td>
<td>–</td>
<td>NO</td>
<td>4-FIR</td>
<td>0.18-um</td>
<td>–</td>
</tr>
<tr>
<td>GLTR05</td>
<td>10</td>
<td>9.5</td>
<td>2-PAM</td>
<td>1.2</td>
<td>7.3</td>
<td>YES</td>
<td>CD</td>
<td>0.13-um</td>
<td>0.162 (CORE)</td>
</tr>
<tr>
<td>Lee06</td>
<td>20</td>
<td>20</td>
<td>2-PAM</td>
<td>1.5</td>
<td>25</td>
<td>YES</td>
<td>CD+</td>
<td>0.13-um</td>
<td>0.2 (CORE)</td>
</tr>
<tr>
<td>TKO+05</td>
<td>10</td>
<td>14.5</td>
<td>2-PAM</td>
<td>1.2</td>
<td>60</td>
<td>YES</td>
<td>3-FIR</td>
<td>0.11-um</td>
<td>0.004 (EQ)</td>
</tr>
<tr>
<td>SC06</td>
<td>40</td>
<td>10</td>
<td>2-PAM</td>
<td>1.2</td>
<td>13.2</td>
<td>YES</td>
<td>5-FIR</td>
<td>90-nm</td>
<td>0.3 (EQ)</td>
</tr>
<tr>
<td>LL08b</td>
<td>49</td>
<td>7.5</td>
<td>2-PAM</td>
<td>1</td>
<td>25</td>
<td>NO</td>
<td>5-FIR</td>
<td>90-nm</td>
<td>0.359</td>
</tr>
<tr>
<td>This Work</td>
<td>40</td>
<td>20.4</td>
<td>4/2-PAM</td>
<td>1.3</td>
<td>58</td>
<td>YES</td>
<td>SP+CD</td>
<td>90-nm</td>
<td>0.891</td>
</tr>
</tbody>
</table>

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Table 6.2: Comparison with other CMOS amplifiers. (CGS and DA refer to cascaded gain stage and distributed amplifier topologies, respectively).

<table>
<thead>
<tr>
<th>Reference</th>
<th>[GR04]</th>
<th>[SSH+04]</th>
<th>[CL07]</th>
<th>[WSJ06]</th>
<th>[LL08a]</th>
<th>[LWL+05]</th>
<th>[TWKC05]</th>
<th>This Work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Symbol Rate (GS/s)</td>
<td>40</td>
<td>40</td>
<td>40</td>
<td>40</td>
<td>N/A</td>
<td>N/A</td>
<td>20.4</td>
<td></td>
</tr>
<tr>
<td>Supply (V)</td>
<td>2.2</td>
<td>1.8</td>
<td>2.8</td>
<td>1</td>
<td>1.2</td>
<td>2.4</td>
<td>1.3</td>
<td></td>
</tr>
<tr>
<td>Power (mW)</td>
<td>190</td>
<td>140</td>
<td>250</td>
<td>80</td>
<td>75</td>
<td>4.5</td>
<td>122</td>
<td>138</td>
</tr>
<tr>
<td>Diff. Gain (dB)</td>
<td>15</td>
<td>4</td>
<td>20</td>
<td>20</td>
<td>26</td>
<td>7.4</td>
<td>31.2</td>
<td>7</td>
</tr>
<tr>
<td>BW (GHz)</td>
<td>22</td>
<td>39</td>
<td>39</td>
<td>23</td>
<td>22</td>
<td>80</td>
<td>70</td>
<td>8.1</td>
</tr>
<tr>
<td>GBP (GHz)</td>
<td>124</td>
<td>62</td>
<td>301</td>
<td>230</td>
<td>144</td>
<td>188</td>
<td>155</td>
<td>294</td>
</tr>
<tr>
<td>VGA</td>
<td>NO</td>
<td>NO</td>
<td>NO</td>
<td>YES</td>
<td>YES</td>
<td>NO</td>
<td>YES</td>
<td></td>
</tr>
<tr>
<td>Type</td>
<td>CGS</td>
<td>DA</td>
<td>DA</td>
<td>CGS</td>
<td>CGS</td>
<td>DA</td>
<td>CGS</td>
<td></td>
</tr>
<tr>
<td>Process</td>
<td>0.18-um CMOS</td>
<td>0.18-um CMOS</td>
<td>90-nm CMOS</td>
<td>90-nm CMOS</td>
<td>90-nm CMOS</td>
<td>90-nm CMOS</td>
<td>90-nm CMOS</td>
<td></td>
</tr>
<tr>
<td>Area (mm²)</td>
<td>0.5</td>
<td>3.3</td>
<td>2.24</td>
<td>0.633 (CORE)</td>
<td>0.56</td>
<td>0.72</td>
<td>0.72</td>
<td>0.891</td>
</tr>
</tbody>
</table>

Table 6.3: Comparison with other 4-PAM systems. (Loss refers to channel loss compensated at one-half the symbol rate. SP and CD refer to split-path and capacitive-degeneration topologies, respectively. Note that 2-PAM performance is quoted under ‘This Work’).

<table>
<thead>
<tr>
<th>Reference</th>
<th>[FRYHL00]</th>
<th>[SWSW03]</th>
<th>[ZWS+03]</th>
<th>[TMR+06]</th>
<th>This Work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Symbol Rate (GS/s)</td>
<td>4</td>
<td>2.5</td>
<td>5</td>
<td>11</td>
<td>20.4</td>
</tr>
<tr>
<td>Loss (dB)</td>
<td>10</td>
<td>12</td>
<td>7.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply (V)</td>
<td>3</td>
<td>2.5/3.3</td>
<td>1.1</td>
<td>1.3</td>
<td></td>
</tr>
<tr>
<td>Power (mW)</td>
<td>1100</td>
<td>1000</td>
<td>400</td>
<td>227</td>
<td>138</td>
</tr>
<tr>
<td>Adaptive</td>
<td>NO</td>
<td>YES</td>
<td>NO</td>
<td>NO</td>
<td></td>
</tr>
<tr>
<td>VGA</td>
<td>NO</td>
<td>NO</td>
<td>NO</td>
<td>NO</td>
<td></td>
</tr>
<tr>
<td>TX Type</td>
<td>2-FIR</td>
<td>4-FIR</td>
<td>5-FIR</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>RX Type</td>
<td>1-FIR</td>
<td>Slicer</td>
<td>5-DFE</td>
<td>CD</td>
<td></td>
</tr>
<tr>
<td>Process</td>
<td>0.3-um CMOS</td>
<td>0.25-um CMOS</td>
<td>0.13-um CMOS</td>
<td>90-nm CMOS</td>
<td>90-nm CMOS</td>
</tr>
<tr>
<td>Area (mm²)</td>
<td>4</td>
<td>17</td>
<td>1</td>
<td>0.12 (CORE)</td>
<td>0.891</td>
</tr>
</tbody>
</table>
A Inductors

Inductor Design and Model

All inductors were designed using ASITIC [Nik]. The majority of the inductors were implemented as 3-dimensional (multi-layer) structures as shown in Figure A.1. The parameters of the double-π model in Figure A.2 were fit to the two-port parameters from ASITIC for use in circuit simulation. This model includes capacitances and losses due to skin-effect [DLB+05]. Table A.1 gives the geometry and fitted double-π parameters for all inductors used. The fit was done after the entry and exit metals were extended outward by approximately the inductor diameter, as this was the desired separation from other circuit elements. All inductors were square, had uniform metal width and spacing, and began from the top metal layer. The ASITIC and fitted double-π models of $L_{EFF}$ and $Q$ for the largest-valued inductor (1 nH with 50-GHz SRF) are shown in Figure A.3(a) and Figure A.3(b), respectively.

Figure A.1: 3-dimensional (multi-layer) inductor.
A Inductors

Figure A.2: Equivalent double-π model of an inductor.

Table A.1: Inductor dimensions and fitted double-π parameters ($l$, $w$ and $s$ are defined as in Figure A.1).

<table>
<thead>
<tr>
<th></th>
<th>125 pH</th>
<th>150 pH</th>
<th>200 pH</th>
<th>350 pH</th>
<th>400 pH</th>
<th>500 pH</th>
<th>1.0 nH</th>
</tr>
</thead>
<tbody>
<tr>
<td>$l$ ($\mu$m)</td>
<td>20</td>
<td>30</td>
<td>19.5</td>
<td>23.5</td>
<td>24</td>
<td>32</td>
<td>26.5</td>
</tr>
<tr>
<td>$w$ ($\mu$m)</td>
<td>2</td>
<td>4</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>$s$ ($\mu$m)</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Turns</td>
<td>2.5</td>
<td>1.25</td>
<td>2</td>
<td>2.5</td>
<td>2.5</td>
<td>2</td>
<td>3</td>
</tr>
<tr>
<td>Layers</td>
<td>1</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>3</td>
</tr>
</tbody>
</table>

<p>| | | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{s22}$ (fF)</td>
<td>0.262</td>
<td>1.590</td>
<td>1.734</td>
<td>3.466</td>
<td>0.823</td>
<td>2.547</td>
</tr>
<tr>
<td>$C_{s11}$ (fF)</td>
<td>0.255</td>
<td>1.510</td>
<td>0.609</td>
<td>0.120</td>
<td>0.100</td>
<td>0.975</td>
</tr>
<tr>
<td>$R_{\text{sub}22}$ (kΩ)</td>
<td>11.360</td>
<td>5.990</td>
<td>5.110</td>
<td>1.808</td>
<td>0.486</td>
<td>2.861</td>
</tr>
<tr>
<td>$R_{\text{sub}11}$ (kΩ)</td>
<td>8.960</td>
<td>6.110</td>
<td>12.953</td>
<td>4.286</td>
<td>4.400</td>
<td>4.948</td>
</tr>
<tr>
<td>$C_{oxx22}$ (fF)</td>
<td>0.355</td>
<td>3.980</td>
<td>2.716</td>
<td>2.700</td>
<td>1.880</td>
<td>9.227</td>
</tr>
<tr>
<td>$C_{oxx11}$ (fF)</td>
<td>0.406</td>
<td>3.710</td>
<td>1.095</td>
<td>0.390</td>
<td>0.369</td>
<td>4.383</td>
</tr>
<tr>
<td>$L_f$ (nH)</td>
<td>0.025</td>
<td>0.010</td>
<td>0.041</td>
<td>0.059</td>
<td>0.054</td>
<td>0.089</td>
</tr>
<tr>
<td>$R_f$ (Ω)</td>
<td>2.244</td>
<td>1.000</td>
<td>2.585</td>
<td>3.662</td>
<td>3.584</td>
<td>11.662</td>
</tr>
<tr>
<td>$R_m$ (Ω)</td>
<td>1.869</td>
<td>1.425</td>
<td>2.505</td>
<td>4.096</td>
<td>4.526</td>
<td>3.091</td>
</tr>
<tr>
<td>$L$ (nH)</td>
<td>0.107</td>
<td>0.144</td>
<td>0.179</td>
<td>0.332</td>
<td>0.351</td>
<td>0.536</td>
</tr>
<tr>
<td>$C_p$ (fF)</td>
<td>0.100</td>
<td>0.817</td>
<td>3.650</td>
<td>6.320</td>
<td>6.540</td>
<td>10.000</td>
</tr>
</tbody>
</table>

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A Inductors

Figure A.3: ASITIC and fitted double-π models for the 1-nH inductor: (a) \( L_{EFF} \) and (b) \( Q \).
B Broadband Preamplifier

Noise and Bandwidth Expressions

Figure B.1: nMOS TIA with active bias: (a) driven by an input source and (b) the corresponding circuit for open-circuit time constant calculations.

In the nMOS TIA with active bias, the noise due to the current source $M_3$ may be estimated as follows. Referring to Figure B.1(a), the noise power due to $M_3$ referred to the input source $V_s$ is given by

$$v_{n,s}^2(f) = [4kT\gamma g_{m3} + \frac{K_N}{C_{ox}W_3L_3f}g_{m3}^2]R_s^2$$

(B.1)

indicating that to reduce the noise contribution of $M_3$, $g_{m3}$ should be minimized while the product $W_3L_3$ should be maximized.
The bandwidth of a lower-order circuit is often estimated using the open-circuit time constant (OCTC) method [Lee04a]. Although inductors are used throughout the TIA, they are ignored in this OCTC calculation as only an identification of possible limiting nodes is desired. The open-circuit time constants for the capacitances identified in Figure B.1(b) are given by

\[
\tau_1 = C_1 \left( \frac{1}{R_s || R_f || r_o} + \frac{(r_o1 || r_o1P || R_f) (g_m1 R_f - 1)}{R_f^2} \right) \tag{B.2}
\]

\[
\tau_2 = C_2 (R_f || (R_s || r_o3) + (R_s || r_o3) (r_o1 || r_o1P) g_m1 + (r_o1 || r_o1P)) \tag{B.3}
\]

\[
\tau_3 = C_3 \left( \frac{1}{R_f || r_o1 || r_o1P} + \frac{(R_s || R_f || r_o3) (g_m1 R_f - 1)}{R_f^2} \right) \tag{B.4}
\]

with the bandwidth estimate \( f_H \) given by

\[
2\pi f_H = (\tau_1 + \tau_2 + \tau_3)^{-1} \tag{B.5}
\]

Once all device sizes and component values are known, equations B.2-B.5 may be used to help judge the impact of each node on the bandwidth. While \( \tau_2 \) might be expected to dominate due to Miller multiplication, a calculation with the final device values indicates that \( \tau_3 \) can be larger, due to the relatively high value of \( C_{db} \) versus \( C_{gd} \) and the input capacitance of the following stage. Note that equations B.2-B.5 may also be applied to the first stage of the nMOS TIA with CS (see Figure 4.3(d)) by neglecting terms related to \( M_3 \).
C Bias Distribution

Bias Current Generation

Bias currents were generated as shown in Figure C.1 and shipped to the appropriate circuit blocks. The voltage $v_{ref}$ was supplied off-chip.

Figure C.1: Bias current generation.
References


[KYMC+05] Kannan Krishna, David A. Yokoyama-Martin, Aaron Caffee, Chris Jones, Mat Loikkanen, James Parker, Ross Segelken, Jeff L. Sonntag,


References


