Development of Al₂O₃ Gate Dielectrics for Organic Thin-film Transistors

By

Gordon Yip

A Thesis submitted in conformity with the requirements for the degree of Master of Applied Science, in the Department of Materials Science and Engineering, in the University of Toronto

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Gordon Yip
Graduate Department of Materials Science and Engineering
University of Toronto

ABSTRACT

The focus of this thesis is on radio frequency magnetron sputtered aluminum oxide thin films developed for use as the gate dielectric for organic thin film transistors. The effect of top metal electrodes on the electrical characteristics of aluminum oxide metal-insulator-metal capacitors has been studied to determine an optimum material combination for minimizing the leakage current, while maximizing the breakdown field. The leakage current and breakdown characteristics were observed to have a strong dependence on the top electrode material. Devices with Al top electrodes exhibited significantly higher breakdown voltages compared to devices with Au, Ni, Cu and Ag electrodes. Introducing an Al diffusion barrier dramatically increased the breakdown field and reduced the leakage current for capacitors with Ag, Au and Cu top electrodes. The electrical characteristics were found to relate well to material properties, of the contacting metals, such as ionization potential and diffusion coefficient.
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# Table of Contents

1  INTRODUCTION ................................................................................................. 1

1.1  Organic Thin Film Transistors ........................................................................... 1
    1.1.1  Device and Operation ............................................................................. 1
    1.1.2  Research Motivation ............................................................................. 3
    1.1.3  Charge Injection ..................................................................................... 4
    1.1.4  Present Status of Technology ............................................................... 7

1.2  Gate Insulator Requirements for OTFT Devices .............................................. 10
    1.2.1  Low Thermal Budget ........................................................................... 10
    1.2.2  Uniformity in thickness ........................................................................ 10
    1.2.3  Low Leakage Current ......................................................................... 10
    1.2.4  High Breakdown Strength ..................................................................... 11
    1.2.5  Low Surface Roughness ...................................................................... 11

1.3  Ultra High Vacuum Systems ........................................................................... 12

1.4  Thesis Objective ............................................................................................. 13

2  TFT DESIGN .................................................................................................... 16

2.1  TFT Substrate Selection ................................................................................ 16
    2.1.1  Silicon Substrates ................................................................................. 16
    2.1.2  Plastic Substrates ................................................................................. 17
    2.1.3  Glass Substrates .................................................................................. 17

2.2  TFT Patterning: ............................................................................................. 18
    2.2.1  Photolithography ................................................................................. 18
    2.2.2  Shadow Mask ...................................................................................... 19

2.3  TFT Mask Design and Fabrication: ............................................................... 20
    2.3.1  TFT Shadow Mask Design ................................................................... 20
    2.3.2  TFT Shadow Mask Fabrication ............................................................ 22

2.4  TFT Structure: ............................................................................................... 24
    2.4.1  Bottom Gate Top Contact ................................................................... 24
    2.4.2  Top Gate Top Contact ........................................................................ 25
    2.4.3  Bottom Gate Bottom Contact ............................................................. 25
    2.4.4  Top Gate Bottom Contact ................................................................... 26

2.5  Organic Semiconductor Material Selection .................................................. 26

2.6  Initial OTFT Experiments .............................................................................. 27
    2.6.1  OTFT Device Fabrication ..................................................................... 28
    2.6.2  Experimental Results ......................................................................... 29

2.7  Chapter Summary .......................................................................................... 31

3  Al₂O₃ GATE INSULATOR CHARACTERIZATION .............................................. 34
3.1 Experiments ................................................................. 34
3.1.1 Metal Insulator Metal Capacitor Devices ...................... 34
3.1.2 Fabrication and Measurement Procedure ...................... 36
3.2 Results and Discussion .................................................. 37
3.2.1 Surface Roughness ..................................................... 37
3.2.2 Thickness Uniformity .................................................. 38
3.2.3 MIM Capacitors with Al Electrodes .............................. 39
3.2.4 Effects of Annealing ................................................... 41
3.3 Chapter Summary .......................................................... 44

4 EFFECTS OF CONTACTS ON Al₂O₃ MIM DEVICES ............... 46
4.1 Requirements for OTFT contacts ....................................... 46
4.2 Experiments ................................................................. 47
4.2.1 Metal Insulator Metal Capacitor Devices ...................... 47
4.2.2 Fabrication and Measurement Procedure ...................... 47
4.3 Results and Discussion .................................................. 49
4.3.1 Effects of Bottom Contact Material ............................... 49
4.3.2 Effects of Top Contact Material ..................................... 50
4.3.3 Effects of Polarity ....................................................... 53
4.3.4 Electric Field Enhanced Cation Diffusion ....................... 55
4.3.5 Effects of a Diffusion Barrier ....................................... 58
4.4 Chapter Summary .......................................................... 60

5 CONCLUSIONS ............................................................... 63

A. LASER MICROMACHINING ............................................. 65
A.1 Guide to Laser Micromachining ....................................... 65
A.1.1 Background Information on Laser Micromachining .......... 65
A.1.2 Overview of Laser Micromachining Process at IOS .......... 66
A.2 G-Code Examples .......................................................... 67

B. EXPERIMENTAL RESULTS ............................................... 69
B.1 Lithium Fluoride OTFT Devices ...................................... 69
B.2 Parylene OTFT Devices .................................................. 71
B.3 Aluminum Oxide MIM Capacitor Devices ........................... 73

C. MATERIALS CHARACTERIZATION ..................................... 76
C.1 X-Ray Photoelectron Spectroscopy Results ....................... 76
C.2 Profilometer Measurement Results ................................... 77
C.3 Scanning Electron Microscopy Results .............................. 78
List of Figures

Figure 1.1 Cross sectional schematic of OTFT device ................................................................. 1
Figure 1.2 Plot of drain to source current versus gate voltage for a CuPc OTFT.
Adapted from Reference [7], with permission from Elsevier ................................................... 2
Figure 1.3 Conceptual drawing of potential roll-up display fabricated on plastic.
Reprinted by permission from Macmillan Publishers Ltd: Nature, [9], copyright 2004 ................................ ......................................................................................................................... 4
Figure 1.4 Energy level diagram of charge injection into organic semiconductors [16] ........... 6
Figure 1.5 Comparison between metal work functions and HOMO and LUMO positions, of various organic materials. Adapted from reference [20] ......................... 7
Figure 1.6 Schematic view of bottom gate bottom contact OTFT device .. .................. 11
Figure 1.7 OLED Cluster Tools in the Lu Group ................................................................. 12
Figure 2.1 AutoCAD schematic of TFT mask design .......................................................... 20
Figure 2.2 TFT Structure: (a) Top view of TFT, (b) cross-sectional view ...................... 21
Figure 2.3 Optical micrographs of (a) Au patterned through the shadow mask shown in (b) and shadow mask test patterns corresponding to (c) 30 µm and (d) 40 µm. Each minor division on the scale shown represents 10 µm .................................................. 23
Figure 2.4 Schematic cross-sectional diagram of (a) bottom gate top contact, (b) top gate top contact, (c) bottom gate bottom contact, (d) top gate bottom contact structures ......................................................................................................................................................................................... 24
Figure 2.5 Chemical structure of copper phthalocyanine. Reprinted from Reference [15], with permission from Elsevier ................................................................. 27
Figure 2.6 Plot of current for CuPc OTFT: (a) W/L = 500µm/500µm, (b) W/L = 500µm/400µm ................................ ................................................................................. 29
Figure 2.7 Picture of (a) fabricated CuPc OTFT device and (b) optical micrograph showing localized dielectric breakdown at the Au source contact .................. 30
Figure 3.1 Schematic (a) cross-section and (b) top view of MIM test devices .......... 35
Figure 3.2 AFM image of a 220 nm thin film of RF magnetron sputtered Al₂O₃ on a Corning 1737 glass substrate [2]. ................................................................. 37
Figure 3.3 Plot of dielectric constant of Al₂O₃ vs. spatial position ....................... 38
Figure 3.4 Plot of leakage current for Al/Al₂O₃/Al capacitor structure .................. 40
Figure 3.5 Plot of leakage current density for different annealing conditions ........... 42
Figure 4.1 Plot of leakage current for Cr and Al bottom electrodes ...................... 49
Figure 4.2 Plot of leakage current for different top electrode metals .................. 51
Figure 4.3 (a) Optical microscope images of Au MIM devices before and after breakdown and (b) scanning laser confocal microscope profile of crater shaped defect in Au MIM devices ......................................................................................................................... 52
Figure 4.4 Plot of leakage current for different polarities of applied fields .......... 53
Figure 4.5 Plot of leakage current for different polarities of applied fields for Ag/Al₂O₃/Al devices with both Ag as the bottom electrode and top electrode ...... 54
Figure 4.6 Plot of (a) ionization energy and (b) logarithmic diffusion coefficient at 1473 K of various cations and metals respectively vs. typical breakdown field of MIM capacitors with corresponding top electrode metals [19] .................. 57
Figure 4.7 Plot of leakage current for different top contacts with an Al barrier layer .. 58
Figure B.1  Schematic (a) cross sectional view and (b) top view of fabricated OTFT device with LiF as the gate insulator layer.......................................................... 69
Figure B.2  Plot of current versus gate voltage sweep of LiF OTFT device ............ 70
Figure B.3  Schematic (a) cross sectional view and (b) top view of fabricated OTFT device with parylene C as the gate insulator layer material...................................... 71
Figure B.4  Plot of current versus gate voltage sweep of parylene OTFT device ...... 73
Figure B.5  Plot of leakage current for Al/Al₂O₃/Al capacitor structure............... 74

Figure C.1  Plot of the XPS spectrum from the surface of an RF magnetron sputtered aluminum oxide film.......................................................... 76
Figure C.2  Tencor Alpha-step profilometer calibration measurement for Al₂O₃ ...... 77
Figure C.3  SEM images of Al₂O₃ film.......................................................... 78
List of Tables

Table 4.1  Relationship between typical breakdown field and the work function of different top electrode metals in Al₂O₃ MIM devices with Al bottom electrodes [13]................................................................................................................................. 55
1 INTRODUCTION

This chapter will provide an introduction on OTFT technology and ultra-high vacuum systems, before concluding by presenting the thesis objective.

1.1 Organic Thin Film Transistors

The first Organic thin-film transistor (OTFT) was reported in 1986 and had a polythiophene polymer film electrochemically grown as the thin film semiconductor layer [1]. Since then, significant advancements have been made in the development of OTFT technology [2-4]. This section will provide an introduction on understanding the operation of OTFT devices, OTFT charge injection, motivations for pursuing this technology, as well as information on the current status of OTFT technology.

1.1.1 Device and Operation

An OTFT is a transistor device consisting of a thin film organic layer as the semiconductor layer, a gate insulator and three electrical terminals. Commonly used OTFT substrates are silicon, glass or plastic [5]. A cross sectional schematic of an OTFT device with a bottom gate bottom contact structure is shown in Figure 1.1.

![Cross sectional schematic of OTFT device](image)

Figure 1.1 Cross sectional schematic of OTFT device

The resistance of the organic semiconductor layer, between the source and drain contacts, is modulated by the applied voltage to the gate electrode during operation. A simple way to understand the operation of an OTFT is to consider it operating, in digital mode, as a switch. When an appropriate gate voltage is applied to switch the device on, a significant increase in the conductivity of the channel region occurs due to an
accumulation [6] of majority charge carriers at the insulator organic interface, caused by the induced electric field in the gate insulator. In contrast, when an appropriate voltage is applied to switch the device off, a significant decrease in the conductivity of the channel region occurs due to a depletion [6] of majority charge carriers at the insulator organic interface, caused by the induced electric field in the gate insulator.

![Plot of drain to source current versus gate voltage for a CuPc OTFT.](image)

Figure 1.2 Plot of drain to source current versus gate voltage for a CuPc OTFT.

Adapted from Reference [7], with permission from Elsevier.

To illustrate the device operation, Figure 1.2 shows a typical plot of the electrical characteristics of a copper phthalocyanine OTFT device [7], where the gate voltage is swept and the source to drain voltage is held constant. The plot corresponds to a $p$-type device with a maximum on voltage of about $-40$ V, and a turn off voltage of about $15$ V. In the plot of the square root of the drain to source current in Figure 1.2, the slope of the dotted line of best fit is directly proportional to the field effect mobility of the OTFT device and the intersection of the extrapolated one to the x-axis represents the threshold voltage of the device, which is approximately $-6$ V in this case. Another common figure of merit is the on/off current ratio which is the ratio of the maximum and
minimum drain to source current values achievable at a given drain to source voltage. In this case, the on/off current ratio is approximately $10^2$.

### 1.1.2 Research Motivation

Organic thin film transistors (OTFTs) are currently being developed as an alternative to hydrogenated amorphous silicon (a-Si:H) based TFTs for use in applications such as sensors, e-paper, RF ID tags, smart cards and flat-panel displays [8]. OTFT technology is very promising because there is a tremendous potential for low cost large area fabrication [2] using methods such as spin coating, ink-jet printing or roll-to-roll processing. An OTFT fabricated using roll-to-roll processing can potentially allow for very high manufacturing throughput [9]. An OTFT driven OLED display made in Kyushu University has been demonstrated using spin coating to deposit the organic layer to fabricate the transistor devices [10]. Fabrication of OTFTs by ink-jet printing methods have also been demonstrated [11]. Due to the intrinsic low mobility of organic semiconductor materials compared to inorganic semiconductors such as Si and Ge, OTFT devices are not intended to compete with existing technologies for use in applications where high switching speeds are required [2].

One advantage of OTFTs, over silicon based TFTs, is that they are compatible with flexible substrates. This is possible because organic molecules are held together by weak van der Waals forces as opposed to strong chemical bonds [12]. OTFT devices fabricated using a low temperature process have been demonstrated on flexible low-cost transparent plastic substrates [13]. Two of the most promising types of plastic substrates for OTFT fabrication, as discussed in section 2.1.2, are polyethylenenapthalate (PEN) and polyester (PET) [14]. By fabricating OTFTs on flexible plastic substrates, there is a potential in the future for producing roll-up displays that can be integrated into a small device such as a pen. A conceptual drawing by Universal Display Corporation of such a roll-up display is shown in Figure 1.3.
OTFT technology has tremendous potential from a fundamental research standpoint and a practical standpoint. Some of the companies and research institutions that have been actively conducting research in this field include IBM, Lucent, Sony, Samsung, Infineon, Phillips, Hitachi, Pioneer Corp., Toshiba, Universal Display Corp., Plastic Logic, NHK, 3M, AU Optronics, Sarnoff, Xerox, Mitsubishi Chemical and Dupont. Some universities currently with well-established OTFT research include Massachusetts Institute of Technology, Stanford, University of Cambridge, Berkeley, University of Tokyo, Kyushu University, University of Chicago, Princeton University, Pennsylvania State University, University of Michigan, Seoul National University, and Cornell University. The ultimate goal of this project is to lay the groundwork for sustained OTFT research at the University of Toronto.

1.1.3 Charge Injection

The device physics of silicon based field effect transistors (FETs) has been extensively studied mainly arising from the needs of the lucrative silicon-based semiconductor electronics market [5]. Fundamental research on the device physics of organic based FETs is also gaining significant interest in recent years, due to increasing interest in promising emerging technologies such as organic thin film transistors (OTFTs), Organic light emitting diodes (OLEDs), as well as organic photovoltaics [15]. The aim of this section is to provide the reader with a brief background on charge injection in OTFT devices, while highlighting the key differences between organic electronic devices and their inorganic counterparts.
The Concept of n-type and p-type Organic Semiconductors:

Unlike silicon based electronics, n-type and p-type organic semiconductor devices are not doped with impurities. Electron and hole mobility values vary for different organic molecules. An organic molecule that has high electron mobility and low hole mobility is defined as an n-type organic semiconductor. Similarly, an organic molecule that has a high hole mobility and a low electron mobility is defined as an p-type organic semiconductor. For example, in an n-type OTFT, n-type behaviour is based on both the electron mobility of the organic material and the electron injection efficiency [16]. Poor electron injection will result in injection limited current resulting in a poor n-type device. Poor electron mobility will result in bulk limited current resulting in poor n-type device. Thus in order to achieve good n-type OTFT characteristics, good charge injection and high electron mobility are both required. Similarly, for a p-type OTFT, p-type behaviour is based on both the hole mobility of the organic material and the hole injection efficiency at the source and drain contacts.

OTFT Charge Injection:

In organic semiconductors, the lowest unoccupied molecular orbital (LUMO) level is analogous to conduction band in inorganic semiconductors. Similarly, the highest occupied molecular orbital (HOMO) level is analogous to valence band. Since organic molecules are undoped [17], charge carriers are injected into the conduction channel from the source and drain electrode contacts. As shown in the diagram in Figure 1.4, in p-type OTFTs, holes are injected into the HOMO level, while in n-type OTFTs, electrons are injected into the LUMO level.
The Schottky contact between the metal electrode and the organic semiconductor material can have a very high resistance due to the potential barrier present between the undoped semiconductor and metal [18]. By selecting proper electrode materials based on their work function to lower the barrier height, the contact resistance can be minimized. High work function metals such as Au are used for efficient hole injection, while lower work function metals such as Al are used for efficient electron injection.

To better illustrate charge injection during OTFT operation, an example of an OTFT with a pentacene organic layer and Au source and drain contacts is considered [19]. Figure 1.5 shows a comparison between metal work functions and HOMO and LUMO positions, of various organic materials [20], where the zero of the energy scale represents a common vacuum level. Considering a grounded source electrode of the OTFT, when a positive bias is applied to the gate, an accumulation of electrons occurs at the insulator-semiconductor interface. Since the fermi level of Au is far away from the LUMO level of pentacene as indicated in Figure 1.5, a significant energy barrier exists, thus electron injection is highly unlikely. When a negative bias is applied to the gate, an accumulation of holes occurs at the insulator-semiconductor interface. Holes are easily injected into the channel since the fermi level of Au is close to the HOMO level of pentacene and hole current will flow between the source and drain contacts if a separate bias is applied to the drain contact. \textit{n}-type OTFTs operate in a similar manner, with the exception that the fermi level of the metal electrode should be close to the LUMO level of the organic semiconductor and positive voltage is applied to the gate to increase the channel conductivity for negative charges.
1.1.4 Present Status of Technology

To illustrate the current status of OTFT technology, one should first understand that a fully mature OTFT technology would ideally have most of the following features:

- A carrier mobility at least greater than 1 cm²/Vs, that of a-Si:H
- A reliable gate insulator compatible with low-cost plastic substrates
- $n$-type and $p$-type transistors for CMOS capability
- Stable under exposure to air or moisture
- Be solution processed and not require ultra high vacuum deposition
- Have minimal threshold voltage variation and instability
- Have ohmic contacts
- Exhibit spatial uniformity in performance for large area applications
• Have low driving voltages
• Have a high tolerance for temperature variation during operation
• Be compatible with patterning using photolithography
• Have single crystal order to maximize mobility and achieve reproducibility

At present, many of these features have been demonstrated individually. OTFT devices have been fabricated with pentacene and rubrene and reported to have mobilities that exceed that of a-Si:H [21]. $p$-type [22] and $n$-type [23] air stable OTFTs have been reported. OTFTs with low driving voltages using high-$k$ dielectric materials have been demonstrated [24]. Contact resistance has been minimized with the use of contact materials based on their work function for efficient charge injection [19]. Photolithographic patterning of OTFTs has been demonstrated [25]. A solution-processed derivative of pentacene exhibiting a field effect mobility of 1 cm$^2$/Vs has been reported [26]. Single crystal OTFTs fabricated with rubrene and CuPc have also been reported [21].

Despite all of these promising results, a major challenge is to integrate all of these technological advances together in one OTFT device. At present, this is not possible. Single crystal OTFTs exhibiting the highest performance, in terms of field effect mobility, are currently fabricated by physical vapor transport, which is a slow process and is not compatible with large scale manufacturing [21]. OTFTs fabricated with solution processed organic layers generally exhibit large non-uniformities in mobility and threshold voltage from one device to the next on the same sample. Due to the incompatibility of organic materials with solvents used for photolithography, the bottom gate bottom contact structure is generally implemented, where the organic layer is deposited at the last step [26]. This structure suffers from large contact resistance, due to damage at the edges of the chemically etched source and drain contacts and low effective charge injection area. Air-stable organic semiconductors generally have poor performance in terms of mobility and non-uniformity in mobility is another major issue [23]. Many reported results from OTFT experiments use crystalline Si substrates with a thermally grown oxide, which is a highly reliable but impractical gate insulator [2]. Thus despite many proof-of-concept experiments which demonstrate the potential of
OTFT technology, much improvement is still necessary, before OTFT technology can be widely commercialized.

Other major challenges include finding a stable and reliable gate insulator that can be deposited at low temperatures, as will be detailed in the following section, and more advanced issues such as temperature dependence and minimizing threshold voltage shifts over the lifetime of an OTFT device. Near the end of the OTFT development cycle, additional concerns such as production yield will arise.

Due to the interdisciplinary nature of OTFT technology and development, research is generally conducted by individuals with diverse backgrounds including physics, chemistry, materials science and electrical engineering. The compounded problems of OTFT technology present a great challenge to researchers, but also serve to keep research in this field exciting since as innovative solutions to problems continue to be reported on a frequent basis.
1.2 Gate Insulator Requirements for OTFT Devices

Currently, one of the major challenges of fabricating OTFT devices while taking advantage of its costs savings is to have a reliable good gate insulator that can be deposited at low temperatures. This section will present the requirements for a good OTFT gate insulator.

1.2.1 Low Thermal Budget

A low thermal budget is required during gate insulator deposition in order for OTFT fabrication to be compatible with low cost glass or plastic substrates. This requirement is one of the key limiting factors for fabricating reliable gate insulators for OTFT devices on flexible plastic substrates. Traditional methods for fabricating gate insulators on amorphous silicon TFTs such as plasma enhanced chemical vapor deposition are not compatible with plastic substrates due to the high temperature processing required. The beneficial effects of high temperature annealing to improve the electrical characteristics and thermal stability of the oxide [27] also cannot be realized given the limited thermal budget.

1.2.2 Uniformity in thickness

Uniformity in thickness is especially important for large area applications. In the case of large area active matrix organic light emitting diode (OLED) televisions driven by current programming, non-uniformities in insulator thickness over a large area will directly result in variations in pixel brightness due to variations in the transistor drive current under the same operating conditions [28].

1.2.3 Low Leakage Current

The main output of a transistor device is the drain to source current, as indicated by $I_{DS}$ in Figure 1.6 for an OTFT in the bottom gate bottom contact configuration. If the sum of the gate leakage currents $I_{GS}$ and $I_{GD}$ is larger than or comparable in magnitude to that of the drain to source current, the drain to source current will be masked and the
device will not function as intended. In the case of OTFTs, low gate leakage current is especially important since the field effect mobility of organic materials can be quite low, thus resulting in a low value for the drain to source current. As discussed in the section 1.2.4, high driving voltages are generally required for OTFTs, thus further contributing to a large gate leakage current.

![Schematic view of bottom gate bottom contact OTFT device](image)

**Figure 1.6** Schematic view of bottom gate bottom contact OTFT device

### 1.2.4 High Breakdown Strength

Although high operating voltages are not ultimately practical, at present, they are necessary in order to study OTFT devices, especially those using newly discovered organic semiconductor molecules, whose processing conditions have yet to be optimized to realize their maximum field effect mobility.

For many OTFT studies, upwards of 100 V of applied voltage at the gate-source and drain-source contacts [29-31] is required in order to overcome the low field effect mobility of many organic molecules.

### 1.2.5 Low Surface Roughness

It is also desirable to minimize the roughness at the OTFT semiconductor-insulator interface in order to achieve higher field effect mobility, especially in the case of bottom gate configurations. It has been reported that most of the charge carriers flowing from the source to drain are concentrated at the first several monolayers from the organic-insulator interface [19]. Significant roughness of the gate insulator will impede the path of the charge flow at the insulator-organic interface, thus reducing the observed field effect mobility of the device.
1.3 Ultra High Vacuum Systems

With the exception of the material parylene, material deposition for all experiments discussed in this thesis was performed in an ultra high vacuum (UHV) environment inside the OLED Cluster Tools in the Lu Group as shown in Figure 1.7. UHV systems allow monolayer control over the growth of thin films with an extremely high chemical purity and structural precision [15]. The quality of the vacuum greatly affects the amount of impurities that are adsorbed onto the substrate surface. The typical base pressure, during experiments was ~10^{-8} Torr.

OTFT devices fabricated in UHV systems have been reported to exhibit field effect mobilities comparable to or exceeding that of a-Si TFTs [32]. UHV systems offer the advantages of high purity, monolayer thickness control and excellent reproducibility [15].
1.4 Thesis Objective

The objective of this work is to design a platform for thin film transistor (TFT) fabrication utilizing the existing organic light emitting diode (OLED) Cluster Tools and facilities in the Lu Group. The developed platform will be designed such that it can be compatible with a wide range of semiconductor materials. One of the ultimate goals of this work is to eventually allow for the fabrication of OLED displays that can be driven by OTFTs as the switching element in pixel circuits.

Chapter 2 provides an overview of the TFT design methodology and based on initial OTFT experiments, the performance of the gate insulator is identified as a major limitation for fabricating OTFTs. In chapter 3, radio frequency (RF) magnetron sputtered aluminum oxide is characterized in terms of surface roughness, thickness uniformity, and breakdown strength as a candidate OTFT gate insulator material. The main novelty of this work is contained in Chapter 4, where results showing a strong dependence of the electrical characteristics of RF magnetron sputtered aluminum oxide on the contact material is presented and discussed. A possible mechanism for the observed behavior is proposed and a method to minimize the contact material dependence by applying a diffusion barrier is presented. Conclusions and future directions are presented in Chapter 5.
References


2 TFT DESIGN

The TFT design process includes the following steps. First, the type of substrate is chosen, based on the ultimate goal of the research project. An appropriate patterning method is selected. Masks are designed for patterning the device. Finally, once masks have been made, the device can be made in one of four possible structures as highlighted in section 2.3.

2.1 TFT Substrate Selection

Organic thin film transistors (OTFTs) are generally fabricated on silicon, glass or plastic substrates. This section will highlight the advantages and disadvantages of each of these types of substrates and highlight the reasoning behind the selection of glass substrates for this project.

2.1.1 Silicon Substrates

Crystalline silicon substrates have been used extensively in research environments for OTFT studies involving the testing of new potential organic semiconductor materials [1], self assembled monolayers [2,3], and charge transport [4]. Heavily doped n+ or p+ silicon substrates are generally used for OTFT fabrication so that the entire wafer is highly conductive and thus, can serve as the bottom gate electrode. Silicon substrates have a very high thermal budget. Hence, the major advantage of using a silicon substrate is that a very reliable and robust SiO$_2$ gate insulator layer can be thermally grown directly on the substrate, leaving the source and drain metal patterning and organic layer deposition as the only remaining steps of OTFT fabrication process. Due to the robust SiO$_2$ gate insulator, OTFT testing can commonly be performed using applied voltages of up to 100 V [1], which can be necessary in the case of OTFTs due to the inherent low field effect mobility of most organic semiconductor materials. Since silicon substrates offer the advantages of simple processing, excellent reproducibility and compatibility with high voltage testing, they are very well suited for fundamental research studies involving OTFTs.
From a practical perspective, fabricating OTFTs on silicon substrates has little merit. The major motivation for pursuing OTFT technology compared to other more mature TFT technologies, such as hydrogenated (a-Si:H) and polycrystalline silicon, is that they can be potentially compatible with low-cost, large area applications. Single crystal silicon substrates fabricated by Czochralski growth are not compatible with large area applications and are very expensive compared to substrates such as glass or plastic [5]. Since the substrate itself is used as the gate electrode, silicon substrates are only compatible with bottom gate configurations. High parasitic capacitance is also an issue, since the overlap area between the gate and source/drain contacts is essentially, the entire area of the source/drain contacts.

2.1.2 Plastic Substrates

From a purely practical perspective, plastic substrates represent the ideal substrates for OTFT fabrication. The cost of plastic substrates is very low and they are flexible, thus making them suitable for potential applications such as roll-up displays and flexible displays utilizing OTFTs as switching elements. Other potential applications include RF identification tags and smart cards.

The most promising plastic substrates to date are polyethylenenaphthalate (PEN) and polyester (PET), since they are inexpensive, transparent, have a moderate coefficient of thermal expansion, have good chemical resistance and have moderate moisture absorption [6]. The major limitation of plastic substrates is that the continuous use temperature is about 120 °C and 150 °C, for PET and PEN substrates respectively, and the major challenge is to find a reliable gate insulator that can be deposited at such low temperatures.

2.1.3 Glass Substrates

Glass substrates offer the advantages of good mechanical stability, transparency, and low surface roughness and low impurity concentrations in the case of display quality glass. They are compatible with large area applications and the cost of glass substrates is relatively low compared to crystalline silicon. Bottom or top gate OTFT
structures can be fabricated on glass substrates. Practical applications involving OTFTs on glass substrates include large area flat panel displays, such as OLED televisions. Currently, large area LCD and plasma televisions are fabricated on glass substrates.

Glass substrates were chosen as the starting substrate material for making OTFTs in this project since they provide good mechanical stability and are compatible with OLED fabrication, thus allowing for the potential demonstration of OTFT driven OLED displays in the future. Corning 1737 alkaline earth boro-aluminosilicate glass was selected as the substrate material for this project since it has low surface roughness, low impurity concentrations and has a higher strain point compared to standard Corning 7059 borosilicate glass substrates. The slightly higher strain point allows for potential annealing at higher temperatures for possible improvement of the gate insulator characteristics.

2.2 TFT Patterning:

The patterning of TFT devices are commonly accomplished by either photolithography or patterning through a shadow mask. The advantages and disadvantages of each method will be highlighted in this section.

2.2.1 Photolithography

Photolithography is the preferred technique used for advanced OTFT fabrication since micron-sized resolution is generally achievable in a clean room environment. Photolithography is a patterning process that involves using light to transfer a pattern from a photomask onto a substrate that is coated with photoresist, a chemical that is sensitive to light. In the case of positive photoresist, the areas exposed to typically UV light are made soluble in a developer solution and are later removed during the developing process. In the case of negative photoresist, the areas exposed to UV light are made insoluble in the developer solution and the areas that are not exposed to light are later removed during the developing process. With the overlying photoresist layer acting as a protective coating, wet or dry etching is performed in order to pattern the underlying substrate material. Selective etching is generally employed to ensure that the desired pattern is only transferred to a particular layer during the etching process.
As the final step to the patterning of the single layer, the resist is removed and a new layer can be deposited on top of the existing layer and patterned in the same manner. Excellent alignment of less than 1 micron can be readily achieved if proper alignment marks are designed on a series of photomask patterns and careful alignment is performed on an alignment station, under a microscope.

One of the major disadvantages of photolithography for fabricating OTFTs is that it is very difficult to remove traces of resist after patterning. The solvents are also harmful to organic layers and as a result, it is difficult to achieve reproducible results. In order to achieve successful photolithographic patterning, a clean room environment is essential since airborne contaminants can dramatically reduce the yield of the fabricated devices. Proper selection of the type of resist, developer and etchant is also necessary. It is also necessary to carefully optimize the UV exposure time to the resist, the exact development time and the exact etching time in addition to conditions such as temperature, in order to achieve micron sized features.

2.2.2 Shadow Mask

Shadow mask patterning involves the patterning of thin film layers on sample by depositing the material through a patterned shadow mask to achieve a desired pattern. The major advantage of shadow mask patterning over patterning by photolithography is that ultra-high vacuum (UHV) deposition with clean shadow masks result in high purity materials and reproducible results [7].

In this work, shadow masks will be used for patterning instead of conventional photolithography in an attempt to keep the organic and insulator layers as free from chemical contamination as possible. Some promising organic materials for OTFT fabrication such as C₆₀ are extremely sensitive to moisture and oxygen degradation. Shadow mask patterning of all layers, allows for fabrication of the OTFT device to occur in UHV conditions from the time the glass substrate is loaded into the cluster tool, until the encapsulated OTFT device is finally removed from the system. Since the OLED cluster tools in the Lu Group are designed for patterning OLEDs with shadow masks, shadow mask patterning is also consistent with the existing fabrication
techniques currently employed during OLED fabrication. Some of the disadvantages of shadow mask patterning are larger feature sizes and lower alignment resolution.

2.3 TFT Mask Design and Fabrication:

Shadow masks will be fabricated for the purpose of patterning the various layers of an OTFT device. This section will detail the shadow mask design and fabrication process.

2.3.1 TFT Shadow Mask Design

Shadow masks were designed in AutoCAD. The final pattern is to be transferred onto stainless steel shadow masks for OTFT layer patterning. Figure 2.1 shows an AutoCAD schematic of the mask design. The dimensions of the large square is 2” x 2”
and represents the area of the glass substrate. Figure 2.2 shows a schematic (a) top view and (b) cross-sectional view of a single OTFT device in the bottom contact bottom gate configuration. A total of four masks are required in order to pattern a TFT. The gate metal and data metal masks for patterning the gate and source/drain contacts respectively, the organic mask and the insulator mask. Four OTFT devices are made on one sample, with the limitation on smaller dimensions arising from the following issues:

1) Shadowing effect of the sputtered chromium gate contact pads, of about 300 µm.
2) Misalignment during mask fabrication
3) Misalignment during device fabrication
4) Limitation of the Nd:YAG laser (20 µm resolution)
5) Limitation of the stainless steel etching process (150 µm minimum feature size)
6) Robustness of the mask for fine patterns

![TFT Structure: (a) Top view of TFT, (b) cross-sectional view](image)

Sputtered chromium was chosen as the material used for contact pads/gate metal due to its excellent adhesion to glass. Pads were designed to be 0.1 inch x 0.1 inch with a separation of 0.15 inch. Organic islands are separated for each device to prevent crosstalk or effects from other floating electrodes. In this design, the worse case misalignment tolerated is approximately 1 mm, which corresponds to the gate/source or gate/drain overlap. Having too much overlap between the gate/source and gate/drain
contacts is undesirable since the overlap area is proportional to the parasitic capacitance between these contacts and lead to increased gate leakage current. However, some overlap between these contacts is necessary in order to account for possible misalignment during either device fabrication or mask fabrication. During device fabrication, misalignment can occur due to either the mask being shifted relative to the sample, or due to the sample shifting relative to the mask during the sample transfer steps. Sources for misalignment during mask fabrication will be discussed in section 2.3.2. In the worst case, if the misalignment is greater than the source/gate or drain/gate overlap distance, the gate electrode may no longer overlap the entire active channel region of the TFT device and the transistor will not function as intended.

In terms of transistor sizing, in the current design, the channel width is fixed at 500 µm, and the gate lengths are 500 µm, 400 µm, 200 µm and 150 µm for the four devices. A 500 µm wide and 150 µm long channel region in the shadow mask requires a thin metal line on the shadow mask with dimensions of 500 µm and 150 µm. The dimensions chosen in this first design are mainly done to test the design limits of the current process, with respect to minimum transistor sizes attainable. Future designs for different gate widths and lengths require only fabricating a single new mask, the data metal mask.

### 2.3.2 TFT Shadow Mask Fabrication

The gate and source/drain masks were patterned professionally, by photolithography and chemical etching, by the company Microphoto Inc. due to the need for strict alignment between the two masks. An AutoCAD schematic was sent to the company and based on the design, a photo mask was made. Subsequently, stainless steel shadow masks, of dimensions 137.8 mm by 97.52 mm and 0.127 mm thick were patterned by chemical etching. Due to the one time cost associated with making the photo mask, the cost per mask decreases substantially as the quantity of same mask ordered increases. A total of 5 masks were purchased for both the gate and data metal masks.
Figure 2.3 Optical micrographs of (a) Au patterned through the shadow mask shown in (b) and shadow mask test patterns corresponding to (c) 30 µm and (d) 40 µm. Each minor division on the scale shown represents 10 µm.

On each mask, additional test patterns with a gate width of 500 µm and gate lengths between 100 µm and 10 µm were designed in the region outside of the sample area shown in Figure 2.1 in order to test the minimum feature sizes achievable during mask fabrication by chemical etching. Upon inspection of the fabricated data metal masks under an optical microscope, it was found that shadowing due to thermal evaporation was about 10 µm, as shown in Figure 2.3 (a) and (b), and the minimum sized transistor pattern achievable was 40 µm, as shown in Figure 2.3 (c) and (d). Thus, assuming the same etching conditions and shadowing effect for a single metal layer, if future shadow masks designed with 40 µm channel lengths, actual devices with approximately 30 µm channel lengths can be fabricated using shadow mask patterning.

The organic layer and gate insulator masks were patterned by myself in the University of Toronto at the Institute for Optical Sciences by laser micromachining using a pulsed Nd:YAG laser. As the starting material, stainless steel sheets of dimensions 137.8 mm by 97.52 mm with a thickness of 0.127 mm purchased from the company Microphoto Inc. were used. For masks that do not involve complicated patterns are not required in bulk and do not require strict alignment between masks, the major advantage of laser micro-machining versus professional fabrication by
photolithography and chemical etching is cost. During mask fabrication, care must be taken to set a consistent origin point to minimize misalignment of the starting shadow masks. More information on the laser micro-machining process can be found in Appendix A.

2.4 TFT Structure:

TFTs on glass substrates can be made in one of the four configurations shown in Figure 2.4. The advantages and disadvantages of each configuration will be highlighted in this section.

2.4.1 Bottom Gate Top Contact

The bottom gate top contact TFT structure as shown in Figure 2.4 (a) is commonly used for fabricating organic TFTs [8,9]. Since the gate insulator is deposited before the organic layer, it can be deposited from a wide range of methods including plasma-enhanced chemical vapor deposition (PECVD) and radio frequency (RF) magnetron sputtering. Another advantage of this structure is low contact resistance, due to the large effective area for injecting charge into the semiconductor channel. This area is indicated by red arrows in Figure 2.4 (a) and corresponds to the gate/drain and gate source overlap areas. The additional resistance encountered for the charge to travel down towards the semiconductor-gate insulator interface is termed the access resistance.
This access resistance is generally small in the case of organic TFTs, since the organic layer is generally a thin film. One of the disadvantages of this structure is that ultimately, photolithographic patterning of the source and drain contacts is not possible since the solvents used will damage the organic layer [11].

### 2.4.2 Top Gate Top Contact

The top gate top contact TFT structure as shown in Figure 2.4 (b) is rarely used for fabricating TFTs. The structure is mainly used in crude research experiments for verifying metal-oxide-semiconductor field effect transistor (MOSFET) characteristics from existing semiconductor materials that make up the substrate or are already deposited on a substrate [12,13]. Due to the very small effective area for charge injection into the channel, the contact resistance of this TFT configuration is expected to be very large. In the case of organic TFTs in this configuration, since the organic layer would have to be deposited first before other processing steps, the gate insulator would not be compatible with deposition methods such as sputtering, due to the damage to the organic material caused by energetic ions during deposition. Photolithographic patterning of the source and drain contacts is also not possible. One advantage of this method is that if a suitable gate insulator material can be applied, the gate insulator and gate electrode act as an encapsulation layer that would protect the organic material from moisture or oxygen degradation.

### 2.4.3 Bottom Gate Bottom Contact

The bottom gate bottom contact TFT structure as shown in Figure 2.4 (c) is commonly used for fabricating organic TFTs [14,11]. This method is the most practical, since the semiconductor layer is deposited last. A wide range of semiconductor materials such as various organic molecules and oxide semiconductors can be used, since they are not limited by any of the prior processing steps. Photolithographic patterning of gate and data metal possible. Since the gate insulator is deposited before the organic layer, it can be deposited from a wide range of methods including plasma-enhanced chemical vapor deposition (PECVD) and RF magnetron sputtering. One major disadvantage of this structure is the contact resistance of this
TFT configuration can be very large. This is due to the very small effective area for charge injection into the channel. This area is indicated by red arrows in Figure 2.4 (c) and corresponds to the thickness of the source and drain contacts. If the source and drain contacts are etched, the damage to the edges caused by the etching process will further increase the contact resistance.

2.4.4 Top Gate Bottom Contact

One advantage of this method is that if a suitable gate insulator material can be applied, the gate insulator and gate electrode act as an encapsulation layer that would protect the organic material from moisture or oxygen degradation. Another advantage of this structure is low contact resistance, due to the large effective area for injecting charge into the semiconductor channel. This area is indicated by red arrows in Figure 2.4 (d) and corresponds to the gate/drain and gate source overlap areas. The additional access resistance, as discussed in section 2.4.1, is again expected to be small in the case of organic TFTs, since the organic layer is generally a thin film. Photolithographic patterning of gate and data metal possible. A major disadvantage is that the gate insulator would not be compatible with deposition methods such as sputtering. Conventional thin-film processing techniques cause irreversible damage to the surfaces of van der Waals bonded compounds [5].

2.5 Organic Semiconductor Material Selection

To date, numerous semiconductor materials have been extensively studied for use as the organic material for OTFT devices [9]. For the purposes of the research discussed in this work, two organic molecules, buckminster fullerene (C_{60}) and copper phthalocyanine (CuPc) were chosen as possible candidates for OTFT fabrication. These two materials were selected because they are promising organic molecules available in high chemical purity in the Lu Group. They are currently being used extensively for OLED fabrication and thus do not present a problem of cross-contamination in the organic deposition chamber of the OLED cluster tools. Figure 2.5 shows the chemical structure of CuPc.
CuPc

C_{60} is a promising n-type organic semiconductor material. As is the case with many other n-type organic semiconductors, C_{60} is not air stable and its conductivity decreases rapidly upon exposure to air [16]. Field effect mobilities as high as 0.5 cm²/Vs have been reported for C_{60} OTFT devices [17], which is one of the highest mobilities reported for n-type devices.

CuPc is a promising p-type organic semiconductor material. The field effect mobility of single crystal CuPc devices has been reported to be as high as 1 cm²/Vs [12]. Another desirable property of CuPc is that it has been reported to be air stable [1], and thus encapsulation is not required. Au source and drain contacts are typically used in CuPc OTFT devices [1].

2.6 Initial OTFT Experiments

This section will discuss the device fabrication procedure and experimental results of initial OTFT experiments conducting using the fabricated OTFT shadow masks discussed in this chapter. The OTFT devices discussed in this section have Al₂O₃ as the gate insulator material. Results from OTFT devices using lithium fluoride and parylene as the gate insulator material are presented in Appendix B.
2.6.1 OTFT Device Fabrication

OTFT devices were fabricated in the bottom gate top contact configuration and the bottom gate bottom contact configuration. Al₂O₃ was used as the gate insulator layer, Au was used as the source and drain contact metal, CuPc was used as the organic semiconductor material and Cr was used as the gate metal contact.

The starting Corning 1737 glass substrates were cleaned in the same manner as described in section 3.1.2. The base pressures for the metal and organic chambers were ~10⁻⁸ Torr. 100 nm of Cr was deposited through a patterned gate metal shadow mask by RF magnetron sputtering at a power of 110 W. Pre-sputtering as performed for about 3 minutes before the sample was loaded in order to minimize contamination in the deposited Cr material. The pressure during sputtering was 1.5 x 10⁻² Torr. Shadowing effects were observed, where Cr atoms sputtered at an angle coat an area of about 1 mm outside of the defined shadow-mask area as can be seen in Figure 2.7 (a), which shows a picture of an OTFT device in the bottom gate bottom contact configuration.

The 220 nm thick aluminum oxide gate insulator films were deposited by RF magnetron sputtering (13.56 MHz) from a 99.99% ceramic Al₂O₃ target of 2 inches diameter in 99.999% Ar gas. The chamber pressure during deposition was 1 mTorr, the substrate to target distance was approximately 15 cm, and the net applied RF power was 200 W. A 100 nm thick layer of CuPc was deposited as the organic semiconductor material. This CuPc layer was deposited in the organic chamber at a temperature of 400 °C and the growth rate corresponding to these temperatures was between 0.3 Å/s and 0.9 Å/s. The CuPc layer thickness and deposition parameters were chosen based on considerations regarding the initial growth, nucleation and resulting morphology of CuPc layers [18] and agree with the optimum thickness reported to maximize the field effect mobility in CuPc OTFTs [19]. The pressure during deposition was 3.1 x 10⁻⁸ Torr. Au source and drain deposition was performed by thermal evaporation. The pressure during deposition was 2.7 x 10⁻⁷ Torr and the Au layer thickness was 80 nm.

The fabricated OTFT devices were measured at room temperature in air using an HP4155B semiconductor parameter analyzer.
2.6.2 Experimental Results

This section will present and discuss the initial experimental results for OTFT devices fabricated.

![Figure 2.6](image1.png)

(a)

Figure 2.6 Plot of current for CuPc OTFT: (a) W/L = 500µm/500µm, (b) W/L = 500µm/400µm

Figure 2.6 shows a plot of the OTFT current versus a sweep of the gate voltage of the OTFT device for two different OTFT devices in the bottom gate bottom contact.
configuration. In the plot in Figure 2.6 (a), the gate leakage current is observed to be the lowest out of all OTFT devices tested, however, any MOSFET characteristics are still masked by the dominant gate to source and gate to drain leakage current. The plot in Figure 2.6 (b) corresponds to that of a typical device tested, where dielectric breakdown has likely occurred and large current spikes are observed. MOSFET characteristics are not observed. Figure 2.7 (b) shows an optical micrograph of the Au source contact on an OTFT device in the bottom gate top contact configuration. Areas of localized dielectric breakdown of the Au film are confirmed along the edge of the source contact. The breakdown mechanism will be discussed in detail in section 4.3.2.

![Image of OTFT device with localized dielectric breakdown](image)

(a) (b)

Figure 2.7 Picture of (a) fabricated CuPc OTFT device and (b) optical micrograph showing localized dielectric breakdown at the Au source contact

In summary, dominant gate leakage currents and large current spikes are observed for all of the OTFT devices tested in both the bottom gate top contact and bottom gate bottom contact configurations and MOSFET characteristics were not observed. Based on these initial OTFT experiments, it has been confirmed that the major problem to be addressed is large leakage current and low breakdown voltages of the gate insulator.
2.7 Chapter Summary

In this chapter, the advantages and disadvantages of various starting substrates and patterning methods have been presented and evaluated. It was decided based on practical considerations that OTFT devices would be fabricated on glass substrates and that shadow mask patterning would be implemented due to its compatibility with the OLED cluster tools and to minimize contamination.

OTFT shadow masks were designed using AutoCAD and patterned. Using the newly patterned shadow masks, OTFT devices were fabricated using CuPc as the organic semiconductor layer and RF magnetron sputtered aluminum oxide as the gate insulator material. Based on these initial OTFT experiments, it has been confirmed that the major problem to be addressed is large leakage current and low breakdown voltages of the gate insulator. The focus of the project will be to find a materials combination and recipe that is compatible with a low temperature process and can support high breakdown voltages and low leakage currents as discussed in section 1.2.
References


3 \textbf{Al}_2\text{O}_3 \text{ GATE INSULATOR CHARACTERIZATION}

For application as an OTFT gate insulator, it is necessary to have a thin film dielectric that has low leakage current, a high dielectric constant and high breakdown strength. \textit{Al}_2\text{O}_3 is a high-\textit{k} dielectric material of high interest, since it is abundant, low cost, chemically stable, and has excellent physical properties. In the case of TFTs for flat panel display applications, it is desirable to have a low temperature process that is compatible with large area, low cost plastic or glass substrates. RF magnetron sputtering is a low temperature process compatible with large area flexible substrates and \textit{Al}_2\text{O}_3 films with excellent leakage and breakdown characteristics have been reported using this method [1]. This chapter will focus on the characterization of RF magnetron sputtered aluminum oxide (\textit{Al}_2\text{O}_3) as the gate insulator for OTFTs. The figures of merit considered are thickness uniformity, surface roughness, leakage current and breakdown voltage.

3.1 \textbf{Experiments}

All experiments were performed in the OLED Cluster Tools in the Lu Group as shown in Figure 1.9. The following subsections will detail the metal-insulator-metal device test structure and the fabrication and measurement procedures.

3.1.1 \textbf{Metal Insulator Metal Capacitor Devices}

In order to characterize the electrical properties of the \textit{Al}_2\text{O}_3 films, metal-insulator-metal (MIM) capacitor devices were fabricated and tested. In the case of the bottom gate bottom contact OTFT structure as discussed in section 2.4.3, the parasitic source-gate and drain-gate capacitance, where leakage current and dielectric breakdown typically occurs can be modeled as MIM capacitor devices. A schematic top and cross-sectional view of the MIM test samples has been included in Figure 3.1. Twenty MIM test devices exist on each sample. The common top electrode line was orthogonal to the bottom electrode lines. MIM devices of dimensions 1 mm × 2 mm are located at the intersection of two electrode lines with an \textit{Al}_2\text{O}_3 layer between them. The top electrode
is common for all capacitors to ensure that each of the MIM devices is accessible for testing at all times. In the event that the bottom electrode were common and the MIM devices at the edges of the sample were to fail, an open circuit could exist in the bottom electrode on both sides. In this case, the test devices in the middle of the sample cannot be tested, as the overlying oxide layer would prevent direct contact to those bottom electrodes.

![Figure 3.1 Schematic (a) cross-section and (b) top view of MIM test devices](image)

For the devices discussed in this chapter, Al was used as the material for the top and bottom electrodes. Al was chosen as the electrodes for initial testing since it has good adhesion to glass, high conductivity and is less prone to significant oxidation due to the formation of a self-passivating native oxide layer when exposed to air.
3.1.2 Fabrication and Measurement Procedure

MIM capacitor devices were fabricated on Corning 1737 glass substrates. The substrates were cleaned in an ultrasonic bath with acetone for 10 minutes, followed by rinsing in methanol and then deionized water. Baking on a hot plate was performed at 200 °C for 30 minutes in order to remove excess moisture from the glass sample. UV ozone exposure was performed for 15 minutes as the final cleaning step, prior to loading in vacuum inside a Kurt J. Lesker Cluster Tool. For the bottom and top electrodes, 100 nm of Al was thermally evaporated through patterned shadow masks. The aluminum oxide films of 220 nm thickness were deposited by RF magnetron sputtering (13.56 MHz) from a 99.99 % ceramic Al₂O₃ target of 2 inch diameter in 99.999 % Ar gas. The chemical purity of the aluminum oxide film was confirmed by X-ray photoelectron spectroscopy (XPS) analysis and the results are presented in Appendix C. The chamber pressure during deposition was 1 mTorr, the substrate to target distance was approximately 15 cm, and the applied RF power was 200 W. The base pressure for metal deposition and sputtering were ~10⁻⁸ Torr. These parameters were optimized to maximize the deposition rate given the fixed substrate to target distance in the sputtering system.

The fabricated MIM capacitors were measured at room temperature in air using an HP4155B semiconductor parameter analyzer for leakage current measurements and an HP4280 capacitance meter for capacitance measurements. Capacitor measurements were performed at 1 MHz at zero voltage bias. To prevent crosstalk between devices during leakage current measurements, the common top electrode was always grounded and negative and positive voltages were applied to each individual bottom electrode.
3.2 Results and Discussion

This section will discuss the results obtained from characterizing the fabricated MIM test devices.

3.2.1 Surface Roughness

Figure 3.2 shows an atomic force microscopy (AFM) image of a 220 nm thick RF magnetron sputtered Al$_2$O$_3$ film deposited on a Corning 1737 glass substrate [2].

![AFM image of Al$_2$O$_3$ film](image)

Figure 3.2 shows an atomic force microscopy (AFM) image of a 220 nm thick RF magnetron sputtered Al$_2$O$_3$ film deposited on a Corning 1737 glass substrate. The presence of pinholes or grains was not observed and the RMS surface roughness of the Al$_2$O$_3$ film was found to be 0.2 nm, which is similar to the roughness of the underlying glass substrate. SEM was also used in an attempt to characterize the morphology of the film, however, features were not observed due to charging effects of the insulator material. Details of the SEM analysis are included for reference in Appendix C.3.
3.2.2 Thickness Uniformity

This section will first describe the method used to determine the dielectric constant of the RF magnetron sputtered aluminum oxide film. Subsequently, the thickness uniformity of the aluminum oxide film will be estimated based on the extracted values of the dielectric constant as a function of the spatial position of the MIM device on a sample.

\[
\varepsilon_r = \frac{C \times d}{A \times \varepsilon_0}
\]  

(3.1)

The dielectric constant \( \varepsilon_r \) of the sputtered \( \text{Al}_2\text{O}_3 \) film was extracted using equation 3.1. From equation 3.1, the capacitance value \( C \) was measured for each MIM device in a sample and the area of the MIM capacitors, \( A \), was confirmed using an optical microscope and scale. The physical constant \( \varepsilon_0 \) represents the permittivity of free space and the value \( 8.85 \times 10^{-14} \) F/cm was used. The final thickness of the aluminum oxide layer was determined from a calibrated quartz crystal thickness monitor during oxide deposition. The tooling factor of the quartz crystal thickness monitor for \( \text{Al}_2\text{O}_3 \) was calibrated using a profilometer and the step profile used for calibration is shown in Appendix C.2.

![Figure 3.3 Plot of dielectric constant of \( \text{Al}_2\text{O}_3 \) vs. spatial position](image)
Figure 3.3 shows a plot of the measured dielectric constant value versus the spatial position of each MIM capacitor as indicated in the picture of the actual device for two different samples. From these results, the dielectric constant was determined to be 8.0±0.2, which is similar to reported results from sputtered Al₂O₃ films, which range from 7 to 10 [3].

Since the dielectric constant of a material is a material property intrinsic to that particular material, it is expected to be constant for each capacitor device. From equation 3.1, the physical constant $\varepsilon_0$ is also constant and the capacitance value $C$ is measured. Thus, any variation observed in the dielectric constant as a function of spatial position can be interpreted as resulting from either variations in the thickness of the oxide layer $d$, or variations in the capacitor area $A$. During aluminum oxide deposition, the sample holder is continuously rotated in order to improve the resulting thickness uniformity of the film. If thickness non-uniformity present, radial non-uniformity should be observed. The data from Figure 3.3 indicates that the worst-case non-uniformity in terms of thickness from one MIM device to the next cannot be more than 5%. The actual non-uniformity in thickness is likely much lower than this number since radial non-uniformity is not observed, while the same trend in non-uniformity can be observed in two separate samples. This observation is consistent with the possibility that area differences exist from one MIM device to the next, due to either variations in the shadow mask pattern used, or varying degrees of shadowing from one MIM device to the next, due to the shadow mask being not perfectly flat and in flush with each MIM device.

### 3.2.3 MIM Capacitors with Al Electrodes

The fabricated MIM capacitor devices, as discussed in section 3.1, were tested by applying a potential difference between the top and bottom electrodes starting from 0 V ramping up to 100 V by 1 volt increments. Figure 3.4 shows a normalized plot of the leakage current density versus the applied electric field to each capacitor device. Of the twenty MIM devices, in the sample, only two devices failed due to dielectric breakdown [4], resulting in a short circuit between the top and bottom Al electrodes. The
remaining 18 devices still functioned as capacitors after testing. The results demonstrate that RF magnetron sputtered aluminum oxide is an excellent candidate for the gate insulator material for OTFT devices based on the consistently high breakdown fields observed. The upper limit, in terms of the voltage applied for testing OTFTs, is generally 100 V [5,6,7] due to the limitations of common semiconductor parameter analyzers. It is also impractical to apply higher voltages during testing.

![Figure 3.4 Plot of leakage current for Al/Al₂O₃/Al capacitor structure](image)

It was found from initial experiments that using an insulator layer of 135 nm thickness resulted in significantly lower breakdown fields as shown in Appendix B.3. A simple way to minimize the leakage current through an insulator is to use a thick gate insulator layer. However, this is not practical in the case of field effect transistors (FETs), since the current drive capability of an FET device is inversely proportional to the thickness of the gate insulator layer. To illustrate this point, the drain current of an OTFT, in the saturation and linear regimes, can be approximated by the following equations [8]:
From equation 3.2, \( I_{DSat} \) represents the drain to source current in the saturation regime. From equation 3.3, \( I_{Dlin} \) represents the drain to source current in the linear regime. In both equation, \( \mu \) represents the field effect mobility of the majority carrier, \( V_{th} \) represents the threshold voltage, \( V_D \) represents the drain to source voltage, \( V_{GS} \) represents the applied gate to source voltage, and \( W \) and \( L \) represent the gate width and length respectively. The capacitance of the gate insulator layer, \( C_{ox} \) in equations 3.2 and 3.3 is given by:

\[
C_{ox} = \frac{\varepsilon_{ox} \varepsilon_0 A}{d} \tag{3.4}
\]

From equation 3.4, \( \varepsilon_{ox} \) represents dielectric constant of the gate insulator material, \( \varepsilon_0 \) represents the permittivity of free space, \( A \) represents the capacitance area, and \( d \) represents the thickness of the insulator layer.

By comparing the equations for the drain to source current to equation 3.4, it is apparent that the drain current of an OTFT is inversely proportional to the thickness of the gate insulator. In summary, based on the considerations of breakdown field and current driving capability, it was determined that 220 nm would be the appropriate aluminum oxide thickness to continue future experiments for MIM capacitors and ultimately OTFTs.

### 3.2.4 Effects of Annealing

To investigate the effects of annealing on the electrical characteristics of the aluminum oxide film, MIM samples were prepared as described in section 3.1.2, with the exception that samples were removed from vacuum and annealed in an \( N_2 \) ambient
for 3 hours prior to the deposition of the top Al electrode. Annealing was performed prior to the deposition of the top electrode in order to minimize Al diffusion into the oxide during the annealing process. In order to ensure a fair comparison between devices, a custom sample holder was designed and constructed to allow for the fabrication of a MIM sample with the same structure as shown in Figure 3.2, but with four 1 inch by 1 inch substrates instead of one 2 inch by 2 inch substrate. After the initial bottom electrode deposition, followed by the aluminum oxide deposition, the four samples were removed from vacuum and placed inside a glove box. One sample was left as the reference sample, where no annealing was performed and the remaining samples were annealed in an oven at temperatures of 300 °C, 400 °C and 500 °C for 3 hours in an N\textsubscript{2} ambient. It has been reported that annealing in an N\textsubscript{2} ambient for metal-aluminum oxide-silicon structures reduces the surface charge density of RF magnetron sputtered Al\textsubscript{2}O\textsubscript{3} films [9]. The maximum annealing temperature was kept at 500 °C to ensure that the temperature of the glass substrate did not exceed 666 °C, the strain point of Corning 1737 glass. After the annealing process has been completed, the four samples were loaded back into the cluster tools and the final top Al electrode was deposited. Testing was performed in the same manner discussed in section 3.1.2.

![Plot of leakage current density for different annealing conditions](image)

Figure 3.5 Plot of leakage current density for different annealing conditions
Figure 3.5 shows a plot of the leakage current density versus the applied electric field to each capacitor device fabricated with different annealing conditions. It is observed that MIM devices measured from the unannealed sample consistently have lower leakage current and higher breakdown strength compared with MIM devices from annealed samples. Possible causes of the poor performance observed for annealed devices could be due to contamination in the oven during annealing, contamination during transport or diffusion of the Al from the bottom electrode into the oxide layer during annealing. Based on these results, since annealing was observed to have a detrimental effect on the electrical performance of the oxide, future devices were fabricated and characterized without annealing.
3.3 Chapter Summary

MIM capacitor devices were fabricated and the electrical characteristics of RF magnetron sputtered Al₂O₃ films were studied. MIM capacitor devices with Al top and bottom electrodes and a 220 nm thick Al₂O₃ insulator layer were found to have breakdown fields that consistently exceeded 4.5 MV/cm and seem promising for application as the gate insulator of OTFTs, where such high voltage operation is generally necessary in order to overcome the low field effect mobilities of organic materials.

The maximum thickness variation of the Al₂O₃ films between two MIM capacitor devices in the same sample was found to be 5%. The actual non-uniformity in thickness should actually be less since the 5% variation also accounts for the effects of capacitor area variations.

The surface roughness of a 220 nm RF magnetron sputtered Al₂O₃ films was found to be very flat with a RMS roughness of 0.2 nm that is comparable to the underlying glass substrate. The extracted dielectric constant of the Al₂O₃ film was found to be 8.0±0.2, which is consistent with reported results from sputtered Al₂O₃ films.

MIM devices annealed in an N₂ ambient for 3 hours at temperatures between 300–500 °C were found to exhibit higher leakage currents and lower breakdown voltages compared to unannealed samples.
References

4 EFFECTS OF CONTACTS ON Al₂O₃ MIM DEVICES

Although many studies have reported on the optimization of MIM capacitors with high-\(k\) dielectrics [1,2], very little study has been reported on the effect of the electrode material on the device performance [3] and more specifically, parameters such as leakage current and breakdown strength, which has previously been attributed to the work function of the metal [4]. Traditionally, the choice of electrode material in MIM devices for various applications has generally been based on factors such as adhesion, process compatibility, conductivity, and work function compatibility. In this section, the impact of different electrode materials on the leakage current and breakdown strength of RF magnetron sputtered Al₂O₃ thin films is reported and a method to improve the breakdown and leakage characteristics by applying an Al diffusion barrier is presented.

4.1 Requirements for OTFT contacts

For selecting OTFT contact materials, the general requirements for a good contact are excellent adhesion to the substrate, scratch resistance and high conductivity. Based on this criteria, Cr and Al were chosen as candidates for the bottom or gate contact metal.

For the source and drain contacts, in addition to the requirements mentioned above, it is necessary to select proper materials based on their work function in order to minimize the contact resistance at the metal semiconductor junction as detailed in section 1.1.3. Higher work function materials such as ITO, Au, Cu and Ni are used for efficient hole injection [5-7]. Materials with lower work functions such as Al and Ag are used for efficient electron injection [8,9].
4.2 Experiments

The following subsections will detail the metal-insulator-metal device test structure, and the fabrication and measurement procedures.

4.2.1 Metal Insulator Metal Capacitor Devices

In order to characterize the effects of the contact material on the electrical properties of the Al₂O₃ films, metal-insulator-metal (MIM) capacitor devices were fabricated and tested. A schematic top and cross-sectional view of the MIM test samples has been included in Figure 3.2. The details of this design are discussed in section 3.1.1.

4.2.2 Fabrication and Measurement Procedure

MIM capacitor devices were fabricated on Corning 1737 glass substrates. The substrates were cleaned in an ultrasonic bath with acetone for 10 minutes, followed by rinsing in methanol and then deionized water. Baking on a hot plate was performed at 200 °C for 30 minutes in order to remove excess moisture from the glass sample. UV ozone exposure was performed for 15 minutes as the final cleaning step, prior to loading in vacuum inside a Kurt J. Lesker Cluster Tool. All aluminum oxide films of 220 nm thickness, were deposited by RF magnetron sputtering (13.56 MHz) from a 99.99 % ceramic Al₂O₃ target of 2 inch diameter in 99.999 % Ar gas. The chamber pressure during deposition was 1 mTorr, the substrate to target distance was approximately 15 cm, and the applied RF power was 200 W. The base pressure for metal deposition and sputtering were ~10⁻⁸ Torr. More details on the fabrication procedure are discussed in section 3.1.2.

For MIM devices prepared to study the effects of the bottom electrode as discussed in section 4.3.1, the 100 nm common Al top electrode was thermally evaporated through a patterned shadow mask. The Al and Cr bottom electrodes were deposited by thermal evaporation and RF magnetron sputtering respectively, through a patterned shadow mask. The thickness of all bottom electrodes was kept constant at
100 nm. In order to ensure a fair comparison between devices, a four 1 inch by 1 inch substrates were used, as discussed in section 3.2.4. After the initial bottom electrode deposition, UV ozone treatment for 1 hour in air was performed to partially oxidize the bottom electrodes for two substrates, one with Al and one with Cr in an attempt to improve the electrical characteristics of the MIM device.

For MIM devices prepared to study the effects of the top electrode as discussed in section 4.3.2, the 100 nm Al bottom electrode was thermally evaporated through a patterned shadow mask. Cu, Ni, Ag, Au and Al top electrodes of 100 nm thickness were thermally evaporated through a patterned shadow mask. All devices were fabricated on a 2 inch by 2 inch substrate.

MIM devices were fabricated to study the effects of a diffusion barrier between top electrode and insulator as discussed in section 4.3.4. For these devices, the 100 nm Al bottom electrode was thermally evaporated through a patterned shadow mask. The 100 nm Al diffusion barrier was evaporated through a patterned shadow mask, corresponding to the top electrode pattern, on the aluminum oxide film prior to deposition of the top electrodes. As the final fabrication step, Cu, Ag, and Au top electrodes of 50 nm thickness were thermally evaporated through a patterned shadow mask that was approximately 0.5 mm smaller than the top electrode mask on either side of the electrode line in order to avoid the unwanted effects of shadowing to interfere with the test of the diffusion barrier. The exact reduction in the width of the top electrode lines was confirmed with an optical microscope and scale and this effect was taken into account during the calculation of device area for the normalized leakage current values shown in Figure 4.7. All devices were fabricated on a 2 inch by 2 inch substrate.

All MIM capacitors were measured at room temperature in air using an HP4155B semiconductor parameter analyzer for leakage current measurements and an HP4280 capacitance meter for capacitance measurements. Capacitor measurements were performed at 1 MHz at zero voltage bias. To prevent crosstalk between devices during leakage current measurements, the common top electrode was always grounded and negative and positive voltages were applied to each individual bottom electrode.
4.3 Results and Discussion

This section will discuss the results obtained from characterizing the fabricated MIM test devices.

4.3.1 Effects of Bottom Contact Material

In order to determine a suitable gate metal contact material, MIM devices with Al and Cr bottom electrodes were tested.

![Figure 4.1 Plot of leakage current for Cr and Al bottom electrodes](image)

Figure 4.1 shows a normalized plot of the leakage current density versus the applied electric field to MIM devices with Cr and Al bottom electrodes. From the plot of current density vs. applied electric field, it was found that devices with Al bottom electrodes had higher breakdown voltages and lower leakage current compared to devices with Cr bottom electrodes. It is observed that MIM devices with Al bottom electrodes consistently exhibit higher breakdown voltages and lower leakage currents. On two samples, UV ozone treatment was performed on the bottom contact metal for one hour in order to partially oxidize the surface of the metal prior to oxide deposition.
This UV Ozone treatment was found to have no significant effect on the leakage current and breakdown characteristics of the devices.

One possible reason for the observed increase in leakage current for MIM devices with Cr bottom electrodes is due to the increased capacitor area due to increased shadowing from the sputtered Cr bottom electrode. Instead of having a 1 mm width in the bottom electrode like the thermally evaporated Al electrodes, sputtered Cr electrodes have a width of approximately between 1.5 mm – 1.7 mm when observed under an optical microscope. In addition, it was observed that the bottom Cr electrodes were not totally electrically isolated from each other, due to shadowing effects. Thus, for each set of Cr bottom electrodes, after testing the first device, the subsequent devices were already shorted to the top electrode via the breakdown path of the first device tested. Since the separation distance between the bottom electrodes is 1 mm, this indicates that the shadowing of the Cr electrodes extends upwards of 0.5 mm on each side, even though the very thin layer cannot be easily discerned optically. Due to the relatively poor electrical performance of Cr bottom electrodes and an undefined electrode area due to the effects of shadowing it was decided that Al is the best bottom electrode material to be used for future studies of MIM capacitors devices and for the gate insulator for OTFT devices.

### 4.3.2 Effects of Top Contact Material

For the purposes of a comparative study on the effect of different top metal electrodes, all MIM devices have a 100 nm thick Al bottom electrode and a 220 nm thick Al₂O₃ insulator. Al was chosen as the bottom electrode material for testing since it was found to exhibit excellent leakage current and breakdown characteristics when used as a contact on aluminum oxide.

In order to test the compatibility of potential source and drain contact metals selected based on their work function, MIM capacitors with Al bottom electrodes and various top electrode materials were fabricated and tested. Few studies have reported the effects of different contact metal on the leakage and breakdown characteristics of MIM devices. In this work, it was observed that the top metal contact material has a
significant effect on the leakage and breakdown characteristics of the capacitor devices tested.

Figure 4.2 shows a plot of the typical leakage and breakdown behavior of MIM capacitor devices with different top metal electrodes. Devices with Al top electrodes consistently exhibited low leakage currents and high breakdown strength. Devices with Ag top electrodes were found to consistently exhibit the highest levels of leakage current and lowest breakdown strength. Cu top electrode devices are observed to have higher breakdown voltages than Ag top electrode devices. Ni top electrode devices are observed to have slightly higher breakdown voltages than Cu top electrode devices. All MIM devices tested with Al, Ag, Ni and Cu top electrodes ultimately failed due to dielectric breakdown [10] resulting in a permanent short circuit between the metal electrodes.

Devices with Au top electrodes were found to consistently exhibit what Klein [11] describes as a self-healing breakdown mechanism, which is when a hole is formed in the oxide film and metal, during localized dielectric breakdown, thus reducing the effective area of the MIM devices. Figure 4.3 (a) shows optical micrographs of images
taken before and after testing. The spots observed after testing correspond to areas where localized breakdown has occurred. Scanning laser confocal microscope studies confirmed the presence of a crater-shaped defect extending from the Au electrode into the oxide, as seen in the cross-sectional profile in Figure 4.3 (b). The red line in Figure 4.3 (b) indicates where the cross-sectional profile was taken. The observations of localized breakdown for Au top contacts is consistent with the localized breakdown observed in the Au source contact of a fabricated Al₂O₃ OTFT device shown in Figure 2.7 (b).

![Image](image_url)

Figure 4.3  (a) Optical microscope images of Au MIM devices before and after breakdown and (b) scanning laser confocal microscope profile of crater shaped defect in Au MIM devices

In Figure 4.2, this localized self-healing breakdown or apparent current spikes, is consistently observed for devices with Au top electrodes. As current densities increased for the Au devices, an open circuit would exist near the end of testing as indicated in Figure 4.2. This open circuit occurs due to the loss of an electrical contact between the tungsten probe and the gold layer. This behaviour was commonly observed at applied fields greater than 3.5 MV/cm. When the tungsten probe is adjusted and a electrical contact is re-established between the gold electrode, all Au top electrode MIM device tested were confirmed to still function as a capacitors. All Au devices functioned as capacitors after varying degrees of localized breakdown had occurred, with a measured capacitance decrease corresponding with the reduced top electrode area as shown in
Chapter 4 – Effects of Contacts on Al₂O₃ MIM Devices

Development of Al₂O₃ Gate Dielectrics for Organic Thin Film Transistors

Figure 4.3 (a). Short circuiting of electrodes was not observed for any of the Au devices tested.

4.3.3 Effects of Polarity

In order to gain more insight into the mechanism behind the strong dependence of the breakdown field on the electrode material, MIM capacitor devices with Al top electrodes and Al bottom electrodes were fabricated and tested by applying positive and negative voltages to the bottom electrode. The fabrication and testing procedure is described in section 3.1.2.

![Graph showing leakage current versus applied electric field](image)

**Figure 4.4** Plot of leakage current for different polarities of applied fields

From the plot of the current density versus applied electric field shown in Figure 4.4, the polarity of the applied voltage was found to have no significant impact on the leakage and breakdown characteristics of the devices tested. This result can be expected since the device is symmetrical in terms of structure. The only difference between the top and bottom electrode interface is the deposition sequence. The interface between the bottom Al electrode and the oxide consists of an existing aluminum layer that has an RF magnetron sputtered Al₂O₃ layer deposited on top of it. The interface between the
top Al electrode and the oxide consists of an existing RF magnetron sputtered Al$_2$O$_3$ layer with a thermally evaporated Al layer deposited on top of it. One can expect the two interfaces to have possibly differences in terms of trapped charge, roughness, coverage and dangling bonds. These properties seem to have minimal effect on the leakage current and breakdown voltage characteristics in this case.

To study the effects of polarity on non-symmetrical devices, MIM devices with an Ag bottom electrode and an Al top electrode and MIM devices with an Al bottom electrode and an Ag top electrode were fabricated and tested. The electrode thickness was kept constant at 100 nm and the Al$_2$O$_3$ thickness was constant at 220 nm.

![Figure 4.5](image.png)

Figure 4.5 Plot of leakage current for different polarities of applied fields for Ag/Al$_2$O$_3$/Al devices with both Ag as the bottom electrode and top electrode

From the plot of the current density versus applied electric field shown in Figure 4.5, it is observed that negatively biased Ag electrodes had higher breakdown voltages than positively biased Ag electrodes. For two devices, tested, breakdown was not
observed after 100 V of applied bias in the case of the negatively biased Ag electrode tests.

From Figure 4.5, it is also observed that devices with positively biased silver bottom electrodes had higher breakdown voltages than devices with positively biased top electrodes. The difference again between the top and bottom electrode interface is the deposition sequence. The interface between the bottom Ag electrode and the oxide consists of an existing Ag layer that has an RF magnetron sputtered Al₂O₃ layer deposited on top. The interface between the top Ag electrode and the oxide consists of an existing RF magnetron sputtered Al₂O₃ layer with a thermally evaporated Ag layer deposited on top, and this type of interface is observed to result in slightly lower breakdown voltages. One possible explanation is if the Al₂O₃ layer is rough, the thermally evaporated Ag on top could more readily fill in crevices, resulting in concentrated electric field distributions at those areas, ultimately resulting in dielectric breakdown at lower applied electric fields.

### 4.3.4 Electric Field Enhanced Cation Diffusion

In general, Fowler-Nordheim tunneling or Frenkel-Poole emission are responsible for leakage current through ultra-thin insulator materials. Since 220 nm is a relatively thick film, tunneling current is not expected to be significant. Previous studies on the effect of the top contact material on the leakage properties of MIM capacitors discussed the cause of leakage current in terms of the reactivity of the electrode material [12], and the work function of the electrode material [4].

<table>
<thead>
<tr>
<th>Top electrode material</th>
<th>Al</th>
<th>Ni</th>
<th>Cu</th>
<th>Ag</th>
<th>Au</th>
</tr>
</thead>
<tbody>
<tr>
<td>Typical breakdown field (MV/cm)</td>
<td>&gt; 4.5</td>
<td>1.6</td>
<td>1.0</td>
<td>0.25</td>
<td>-</td>
</tr>
<tr>
<td>Work function (eV)</td>
<td>4.20</td>
<td>5.22</td>
<td>5.10</td>
<td>4.64</td>
<td>5.47</td>
</tr>
</tbody>
</table>
Comparing the breakdown voltage to the work function [13] of the respective top metal electrodes shown in Table 4.1, no correlation is observed from the experimental results. In addition, since Al₂O₃ has high chemical stability, Ag, Cu, Ni, and Au electrode materials should not react with the Al₂O₃ film at the interface.

It is possible that the observed leakage behavior for Ag, Cu, Ni and Al MIM capacitors is based on a two-step process. First, the metal atoms at the anode-Al₂O₃ interface become ionized when a positive voltage is applied. Subsequently, the cations migrate through the oxide due to an electric field driven cation diffusion process, similar to what has been observed in studies involving the electrochemical cation doping of mixed alkali glass [14] and other ceramic materials [15,16]. Although there exists a large amount of theoretical work on defects and diffusion in alumina, there is currently no universally accepted theory on the diffusion mechanism [17]. Handy [18] has reported that crystalline Al₂O₃ is known to have a cation deficient spinel structure, where an average of two vacant cation sites are randomly distributed per unit cell, which favors the diffusion of cations. Handy further proposes that amorphous Al₂O₃ has a similar but disordered anion structure with possibly a greater number of unoccupied cation sites, which help facilitate cation diffusion.

In Figure 4.6, (a) the ionization energy of different metals and (b) their diffusion coefficients measured at 1473 K, accounting for diffusion tail effects, are plotted as a function of typically observed breakdown voltages for MIM devices [19]. Diffusion tail effects are relevant to MIM devices because a diffusion tail can act as a conductive path in the oxide and trigger dielectric breakdown. Data for Au was not included in Figure 4.6 because the breakdown field of Au top electrode MIM devices is not well-defined. In the case of the Ni, Ag, Al and Cu top electrode MIM devices, the breakdown fields were quantified in terms of a leakage current threshold value. Since Au top electrode MIM devices exhibit localized self-healing breakdown, it would be an invalid comparison to quantify the breakdown field in the same manner. Data for Cu was not included in Figure 4.6 (b) since, to the best of the author’s knowledge, the diffusion coefficient for Cu in aluminum oxide accounting for deep penetration tails on diffusion profiles has not been reported in literature. Ag and Cu are known to be fast diffusing elements in crystalline Al₂O₃, while Ni is classified as an intermediate diffusing cation and finally the constituent atom Al is very slow in diffusing [17]. A trend is observed
such that the magnitude of the breakdown field is inversely proportional to the diffusion coefficient of a particular metal in $\text{Al}_2\text{O}_3$. The ionization energies for the most common cations for each element also exhibit a trend when plotted against typical breakdown voltages. The monovalent cations $\text{Ag}^+$ and $\text{Cu}^+$ require the least energy to become ionized from its ground state and are observed to have the lowest breakdown voltages.

![Figure 4.6 Plot of (a) ionization energy and (b) logarithmic diffusion coefficient at 1473 K of various cations and metals respectively vs. typical breakdown field of MIM capacitors with corresponding top electrode metals [19].](image)

The possibility of cation diffusion is further strengthened with observations that the breakdown field of $\text{Ag}-\text{Al}_2\text{O}_3-\text{Al}$ MIM devices with positively biased Al electrodes is significantly higher than that of devices with positively biased Ag electrodes as discussed in section 4.3.3. Results from section 4.3.3, that show the effects of polarity having no significant effect on $\text{Al}-\text{Al}_2\text{O}_3-\text{Al}$ MIM devices are also consistent with the possibility of cation diffusion.
4.3.5 Effects of a Diffusion Barrier

For applications involving MIM structures, it is often desirable to select top electrode materials based on their properties such as high conductivity in the case of Cu for interconnects for microelectronic circuits or high work functions such as Au, in the case of organic TFT source and drain contacts to allow for efficient charge injection. In order to use these top contact metals, while minimizing the leakage current and maximizing the breakdown strength of Al₂O₃ MIM devices, we have fabricated and tested such devices with an Al diffusion barrier. The fabrication procedure is described in section 4.2.2.

![Figure 4.7](image-url)  
Figure 4.7 Plot of leakage current for different top contacts with an Al barrier layer

Figure 4.7 shows a plot of the typical leakage and breakdown behavior of MIM devices with different top metal electrodes of 50 nm thickness, on top of a 100 nm Al top electrode layer, as a function of electric field intensity. The 100 nm Al layer behaves as an effective diffusion barrier and the leakage current of Cu, Ag and Au top
electrodes is much reduced and the breakdown voltage is significantly enhanced. Au devices showed no signs of self-healing breakdown. The minimum improvements in the breakdown field observed for devices with Cu and Ag top electrodes are 1.5 MV/cm and 1.75 MV/cm, respectively. It is interesting that although the leakage and breakdown characteristics have been significantly improved with the addition of the relatively thick Al diffusion barrier, Ag devices had the lowest breakdown voltages followed by Cu, and Au, the same trend observed without the additional Al layer. The cause could be due to grain boundary diffusion of Ag and Cu top electrodes through the polycrystalline Al layer resulting in the same general trend observed in Figure 4.2. The diffusion constants of Au, Cu and Ag in Al at 923 K are $1.56 \times 10^{-8}$, $3.92 \times 10^{-8}$ and $4.14 \times 10^{-8}$ cm$^2$/s respectively [20]. Au has the tendency to form intermetallic compounds with Al even at room temperature [21], thus it is possible that this reaction prevents Au atoms from further diffusing through the Al barrier layer, resulting in breakdown results that are consistently comparable to Al only top metal electrodes in MIM devices.
4.4 Chapter Summary

In summary, the leakage current and breakdown strength of Al₂O₃ MIM capacitors has been observed to have a strong dependence on the electrode material. In the case of bottom electrode contacts, thermally evaporated Al contacts were found to exhibit higher breakdown voltages compared to sputtered Cr bottom contacts. In addition, thermally evaporated Al electrodes have a well-defined pattern compared to sputtered Cr, which exhibits significant shadowing effects.

To investigate the effects of the top electrode material on the electrical characteristics of Al₂O₃ thin films, MIM devices with Al, Ni, Cu, Au and Ag top electrodes were fabricated with Al bottom electrodes. Due to the self-healing nature of the localized breakdown observed in Au MIM devices, the breakdown field was not well defined. It was found that MIM devices with Al, Ni, Cu and Ag top electrodes failed due to dielectric breakdown and that the breakdown field was clearly material dependant. Al top electrode MIM devices consistently exhibited the highest breakdown fields, followed by Ni, Cu and Ag MIM devices. The electrical characteristics were found to relate well to material properties, of the contacting metals, such as ionization potential and diffusion coefficient. Based on these observed trends and results from tests on MIM devices with different polarities, it is proposed that the mechanism for such behavior could be based on the electric field enhanced diffusion of metal cations through the insulator layer.

For Al₂O₃ capacitors, the application of a thin Al layer, acting as a diffusion barrier, effectively suppresses the leakage current and increases the breakdown strength of MIM devices with Au, Ag and Cu top metal contacts. This result is promising for OTFT fabrication, since OTFT devices can be potentially fabricated using Au, Ag or Cu source and drain contact metals for efficient charge injection, in the bottom gate bottom contact configuration, while maintaining high breakdown fields using an Al₂O₃ gate insulator.
References


5 CONCLUSIONS

OTFTs were designed and fabricated in an UHV environment on glass substrates using shadow masks for device patterning. OTFT devices were fabricated using CuPc as the organic semiconductor layer and RF magnetron sputtered aluminum oxide as the gate insulator material. Based on these initial experiments results, improvements were found to be necessary in order to reduce the leakage current and increase the breakdown voltages of the gate insulator.

MIM capacitor devices were fabricated and the electrical characteristics of RF magnetron sputtered Al$_2$O$_3$ films were studied. MIM capacitor devices with Al top and bottom electrodes and a 220 nm thick Al$_2$O$_3$ insulator layer were found to have breakdown fields that consistently exceeded 4.5 MV/cm. The maximum thickness variation of the Al$_2$O$_3$ films between two MIM capacitor devices in the same sample was found to be less than 5%. The surface roughness of a 220 nm RF magnetron sputtered Al$_2$O$_3$ films was found to be very flat with a RMS roughness of 0.2 nm that is comparable to the underlying glass substrate. The extracted dielectric constant of the Al$_2$O$_3$ film was found to be 8.0±0.2, which is consistent with reported results from sputtered Al$_2$O$_3$ films. MIM devices annealed in an N$_2$ ambient for 3 hours at temperatures between 300°C and 500°C were found to exhibit higher leakage currents and lower breakdown voltages compared to unannealed samples.

The leakage current and breakdown strength of Al$_2$O$_3$ MIM capacitors has been observed to have a strong dependence on the electrode material. Thermally evaporated Al bottom contacts were found to exhibit higher breakdown voltages compared to RF magnetron sputtered Cr bottom contacts. It was found that MIM devices with Al, Ni, Cu and Ag top electrodes and Al bottom electrodes failed due to dielectric breakdown. Al top electrode MIM devices consistently exhibited the highest breakdown fields, followed by Ni, Cu and Ag MIM devices. Due to the self-healing nature of the localized breakdown observed in Au MIM devices, the breakdown field was not well defined. Based on these observed trends and results from tests on MIM devices with different polarities, it is proposed that the mechanism for such behavior could be based on the electric field enhanced diffusion of metal cations through the insulator layer. For
Al₂O₃ capacitors, the application of a thin Al layer, acting as a diffusion barrier, effectively suppresses the leakage current and increases the breakdown strength of MIM devices with Au, Ag and Cu top metal contacts. This result is promising for OTFT fabrication, since OTFT devices can be potentially fabricated using Au, Ag or Cu source and drain contact metals for efficient charge injection, in the bottom gate bottom contact configuration, while maintaining high breakdown fields using an Al₂O₃ gate insulator.

For future work, OTFT devices can be fabricated using Al₂O₃ as the gate insulator and Al as the gate, and source and drain contact metals to achieve high breakdown voltages. Since Al has a low work function, n-type organic semiconductor materials such as C₆₀ can be used as the active later in OTFT devices, in order to achieve efficient charge injection. Due to the extreme sensitivity of C₆₀ to air and moisture, an efficient encapsulation method would be required. p-type OTFTs can also be fabricated with an using an Al₂O₃ gate insulator and an Al diffusion barrier so that higher work function source and drain metals can be used. Secondary ion mass spectroscopy (SIMS) can be used to check for material diffusion into insulator for different top metals to confirm the electric field enhanced cation diffusion phenomena. RF magnetron sputtered insulating films of promising materials such as Ta₂O₅ and HfO₂ can be studied as possible candidates for the OTFT gate insulator material.
A. LASER MICROMACHINING

This section is intended to provide the reader with guidelines and helpful hints in the event that it is necessary to perform custom laser micromachining of shadow masks using the pulsed Nd:YAG laser at the Institute for Optical Sciences (IOS) at the University of Toronto.

A.1 Guide to Laser Micromachining

This section will begin by provide some background information on the laser micromachining process and proceed to provide an overview of the laser micromachining process at IOS at the University of Toronto.

A.1.1 Background Information on Laser Micromachining

The material included in this background section was taken from reference [1]. Since laser micromachining is a thermal process, the effectiveness depends on thermal and optical properties of materials, rather than mechanical properties. One advantage is, since laser machining is a non-contact process, the energy transfer between the laser and the material occurs through irradiation. Thus, no cutting forces generated by the laser and mechanically induced material damage, wear to the cutting blade and machine vibration is minimized.

The two types of laser cutting exist for processing metals are reactive gas cutting and laser fusion cutting. For reactive cutting, an oxygen gas jet is used and material removal is achieved through high-temperature oxidation reactions. For laser fusion cutting, the laser beam serves as a high-temperature heat source to propagate chemical reactions.

The three major factors for laser cutting are the removal rate, the dimensional accuracy and the surface quality of the material.
A.1.2 Overview of Laser Micromachining Process at IOS

The specifications of the Nd:YAG laser at IOS is as follows: laser power is ~3 W, rep rate ~5000 Hz and the wavelength is 1064 nm. The dimensional accuracy of the laser at IOS is approximately 20 µm. The removal rate is dependant on the both the power and current setting of the laser in additional to the speed at which the laser is moving during cutting. Depending on the particular material, these parameters can be optimized based on the exact conditions at the time of the experiment, such as focusing of the beam. The power of the laser should be set by the individual responsible for maintaining the Nd:YAG laser at IOS and for safety reasons and this limit should not be exceeded.

The following is a list of information from the author’s experience with laser micromachining at IOS:

- For cutting rectangles, it was found that smaller rectangles generally required more repetitions to cut than larger rectangles with the number of repetitions in order to cut the rectangle ranging from 10 times to 100 times.
- It was found that reactive cutting, using a stream of oxygen gas, for stainless steel masks of thickness 0.127 mm is more effective than fusion cutting without the oxygen gas stream. Fusion cutting takes significantly longer and the heat generated can warp the shape of the mask, especially for small feature sizes.
- Residue remaining from reactive cutting can be easily removed by physical polishing.
- Cutting is not even on the different sides of a rectangle. For example, 10 repetitions, may be sufficient to cut three sides of a rectangle, however, the remaining side may require another 5 repetitions before it is cut.
- The simplest way to specify a pattern to cut is to manually write the G-code file, such as those shown in section A.2, and to directly load them into the Unidex 600 MMI Controller interface program to direct the movement of the stage.

The following section contains G-code examples for tracing squares that are centered and off-centered. Comments are provided for each command.
A.2 G-Code Examples

Note: All G-code examples assume that the laser is aligned exactly at the center of the mask prior to execution of the code.

_G-code example for tracing a rectangle that is centered:_

```gcode
G71        ; Metric Units
(PSOT,0,0,1) ; Shutter off
G92 X0.0 Y0.0 ; Set Reference Position/sample should be centered
G90        ; Absolute Position
F200.0     ; Set feed rate is 200 mm/s
G1 X-0.4 Y1.2 ; On a corner of the square
F50        ; Set feed rate is 50 mm/s
(PSOT,0,0,0) ; Shutter on
;RPT 5      ; 5 Repititions
G1 X0.4 Y1.2 ; Tracing Rectangle
G1 X0.4 Y-1.2
G1 X-0.4 Y-1.2
G1 X-0.4 Y-1.2
;ENDRPT

(PSOT,0,0,1) ; Shutter off
F200.0     ; Set feed rate is 200 mm/s
G1 X0.0 Y0.0 ; Back to Origin
M2         ; End of Program
```

_G-code example for tracing rectangle that is off-centered:_

```gcode
G71        ; Metric Units setting
```
(PSOT,0,0,1) ; Shutter off
G92 X0.0 Y0.0 ; Set Reference Position/sample should be centered
G90 ; Absolute Position setting
F200.0 ; Set feed rate is 200 mm/s
G1 X-0.4 Y1.2 ; On a corner of the square
F50 ; Set feed rate is 50 mm/s
(PSOT,0,0,0) ; Shutter on

;RPT 5 ; 5 Repititions
G1 X0.4 Y1.2 ; Tracing Rectangle
G1 X0.4 Y-1.2
G1 X-0.4 Y-1.2
G1 X-0.4 Y-1.2
;ENDRPT

(PSOT,0,0,1) ; Shutter off
F200.0 ; Set feed rate is 200 mm/s
G1 X0.0 Y0.0 ; Back to Origin
M2 ; End of Program

Disclaimer:

This guide is not intended to act as a replacement for the U600 User’s Guide, or the G code manual, which provides extensive detailed information on operational procedures and commands. This guide is not a substitute for specific training or experience. The author assumes no liability for any individual's use of or reliance upon any material contained or referenced herein.

References:

B. EXPERIMENTAL RESULTS

This section contains experimental results form OTFT and MIM capacitor devices from initial experiments.

B.1 Lithium Fluoride OTFT Devices

Prior to the OTFT mask design process discussed in Chapter 2, OTFT devices were first fabricated using existing shadow masks, as shown in Figure B.1. A 250 nm thick layer of lithium fluoride (LiF) was deposited on top of the CuPc layer to serve as the gate dielectric material. Since the substrate was kept at room temperature during deposition, the resulting LiF layer should be amorphous [1]. A 100 nm layer of copper phthalocyanine (CuPc) was used as the active layer and a bottom contact top gated structure was implemented. The thickness of the Au contacts was 50 nm. One sample was fabricated which contains 9 transistor devices. The channel width of all devices was constant at 1 cm (10000 µm), while the channel lengths have sizes of 2 mm (2000 µm), 1 mm (1000 µm) or 0.5 mm (500 µm).

![Schematic of OTFT device with LiF as the gate insulator layer](image)

Figure B.1 Schematic (a) cross sectional view and (b) top view of fabricated OTFT device with LiF as the gate insulator layer
The purpose of this initial experiment is to become familiarized with the Cluster Tools, used for device fabrication in addition to developing a measurement procedure and verifying the functionality of the measuring equipment. LiF was chosen as the material to begin the initial OTFT experiments since it is commonly used in OLED fabrication and its deposition and patterning procedure is compatible with the cluster tool process. The experimental results showed that the gate leakage dominates source to drain current in all devices tested. In these devices, even if semiconductor characteristics were present, they are masked by the gate leakage current. Figure B.2 shows an example of the gate to source leakage current dominating over the drain to source current. A direct short circuit was observed between the gate and source contacts of two of the nine devices tested. In the case those devices, pinholes were likely present in the LiF film.

![Current versus Gate Voltage Sweep](image)

**Figure B.2** Plot of current versus gate voltage sweep of LiF OTFT device

Based on the experimental results from this section, it is apparent that LiF is not a promising candidate for use as the gate insulator for OTFT fabrication due to the large leakage currents observed. From observations from devices where the gate electrode
was directly shorted to the source electrode, it is probable that pinholes are also likely in the film.

**B.2 Parylene OTFT Devices**

Organic TFT devices were fabricated using the material Parylene C as the gate insulator and tested. The gate insulator was deposited at a thickness of 2 µm by a physical vapor deposition process at the Bahen clean room (BA7145). The ideal thickness would be between 0.2 µm to 0.4 µm, however, the current sample was done along with a batch of samples from another lab and the purpose is mainly to test the compatibility of Parylene C with the current OTFT fabrication process employed.

![Schematic](image)

Figure B.3 Schematic (a) cross sectional view and (b) top view of fabricated OTFT device with parylene C as the gate insulator layer material

A 100 nm thick copper phthalocyanine (CuPc) was used as the active layer and a bottom contact bottom gated structure was implemented as shown in Figure B.3 (a). RF magnetron sputtering was used to deposit the first 150 nm thick Cr gate metal layer. Au source and drain contacts of 80 nm thickness were deposited by thermal evaporation. One sample was fabricated which contains 11 transistor devices. The channel width of
all devices was constant at 1 cm (10000 µm), while the channel lengths have sizes of 2 mm (2000 µm), 1 mm (1000 µm) or 0.5 mm (500 µm).

The Parylene C deposition was performed by lab technician Yimin Zhou of ECTI. The Parylene C dimer in powder form was purchased from Specialty Coating Systems. This powder was loaded into an oven and heated to 150 °C and changed to a vapor state. This vapor passes through a pyrolysis furnace where it is heated to 650 °C and changed to its monomer form. The sample to be coated is kept at room temperature in the subsequent coating chamber. Excess process gas is collected in a cold trap. The resulting parylene layer is pin-hole free, and will conformally coat over edges, points and internal areas. The last feature mentioned poses a problem for device fabrication using a shadow mask since the space between the shadow mask and the sample is also coated. Referring to the top view of the device is shown in Figure B.3 (b), although the thickness of the parylene C layer indicated in blue was greatest at the area indicated, due to the physical vapor deposition process, a thin layer of Parylene was coated on other parts of the sample that were covered by the shadow mask. Thus, in order to contact the Cr gate metal, the thin layer of Parylene on the Cr surface was physically scratched off before the tungsten probe was applied to contact the electrode. In order for no shadowing to occur, the mask would have to contact the substrate and be airtight, which was not possible. This is the main reason why Parylene C was found to be incompatible with our current process. The second reason is due to transportation from the cleanroom in the Bahen Center to the OLED Cluster Tool in the Pratt building would likely contribute to contamination of the device at the organic-insulator interface, which is undesirable since that is the most important interface in the OTFT device.

Referring to Figure B.4, which shows a plot of the current versus a gate voltage sweep of a parylene OTFT device, no apparent MOSFET characteristics were observed. After gradually increasing the gate voltage sweep and not observing any semiconductor characteristics in the organic material, the gate voltages were swept in both the positive and negative directions incrementally until 40 V. The drain current is pretty much constant with respect to the applied gate voltage. The source current is comprised of the sum of the drain current and the gate current. The gate leakage current is low, which can be expected due the relatively thick insulator layer used.
Due to the thick gate insulator material for this particular sample, the lack of MOSFET characteristics is likely due to the insufficient strength of the electric field at the insulator-semiconductor interface in supporting charge accumulation and modulate the channel conductivity.

After this parylene OTFT experiment, it was decided that subsequent experiments should focus on the use of RF magnetron sputtered materials as the gate insulator material, due to its compatibility with device fabrication using shadow mask patterning and the OLED cluster tool in the Lu Group, thus minimizing the effects of unwanted contamination.

### B.3 Aluminum Oxide MIM Capacitor Devices

MIM Capacitor devices with Al top and bottom electrodes were fabricated and tested in the same manner as discussed in section 3.1, with the only difference being that the thickness of the insulator was 135 nm instead of 220 nm.
The fabricated MIM capacitor devices were tested by applying a potential difference between the top and bottom electrodes starting from 0 V ramping up to 40 V by 1 volt increments. Figure B.5 shows a normalized plot of the leakage current density versus the applied electric field to each capacitor device. After testing up to 40 V, all 20 capacitor devices in the sample had failed due to dielectric breakdown. Compared to Figure 3.4, it is apparent that MIM devices with a 220 nm thick oxide exhibit much higher normalized breakdown fields compared to MIM devices with a 135 nm thick RF magnetron sputtered Al₂O₃ layer. For OTFT testing, it is desirable to apply upwards of 100 V, while maximizing the capacitance density due to the inherent low mobility of organic materials. This is especially the case during the initial development phase before optimized processing conditions have been found in order to maximize the field effect mobility of the particular organic material. Thus based on these initial experiments on Al₂O₃ MIM capacitor devices, it was decided that future experiments focus on 220 nm thick Al₂O₃ layers in order to consistently achieve higher breakdown fields.
References:

C. MATERIALS CHARACTERIZATION

The RF magnetron sputtered aluminum oxide films were characterized by various methods including X-ray photoelectron spectroscopy measurements, profilometer measurements, and scanning electron microscopy measurements. The results from these studies are presented in this section.

C.1 X-Ray Photoelectron Spectroscopy Results

X-ray photoelectron spectroscopy (XPS) was performed on the aluminum oxide films in order to confirm the chemical purity of the film. The results are shown in Figure C.1, which shows the XPS spectrum of the surface of an RF magnetron sputtered film of aluminum oxide. The spectrum shows the presence of only the following elements, Al, C and O. The presence the C element is due to exposure to air of the sample.

![Figure C.1 Plot of the XPS spectrum from the surface of an RF magnetron sputtered aluminum oxide film](image-url)
C.2 Profilometer Measurement Results

The tooling factor is a parameter used to adjust for the difference in material deposited on the quartz sensor versus the substrate. With an original tooling factor of the thickness monitor set at 100%, a 300 nm film of Al₂O₃, as indicated on the quartz crystal thickness monitor, was deposited by RF magnetron sputtering on a silicon wafer. The actual measured thickness of this film, from a Tencor alpha-step profilometer, was determined to be 135 nm. Figure C.2 shows the results for the Tencor Alpha-step profilometer calibration measurement for the Al₂O₃ film.

![Tencor Alpha-step profilometer calibration measurement for Al₂O₃](image)

The actual tooling factor was adjusted according to the following formula C.1:

$$Tooling_{ACTUAL} = Tooling_{APPROXIMATION} \times \frac{Thickness_{ACTUAL}}{Thickness_{QCM}}$$  \hspace{1cm} (C.1)

From equation C.1, the approximated tooling factor used was 100 %, the thickness on the quartz crystal monitor was indicated to be 300 nm and the actual measured thickness was 135 nm. Based on these parameters, the actual tooling factor was calculated to be 45 %. Thus for future depositions, the tooling factor of the
thickness monitor was adjusted to 45% to properly calibrate the thickness reading for the Al₂O₃ material. Using the new calibration parameters, the extracted dielectric constant over two successive samples, as discussed in section 3.2.2, was found to agree well with published results.

C.3 Scanning Electron Microscopy Results

![SEM images of Al₂O₃ film](image1)

![SEM images of Al₂O₃ film](image2)

Figure C.3 SEM images of Al₂O₃ film
Scanning electron microscope (SEM) images of the aluminum oxide film were taken with a Hitachi S5200 SEM microscope. Focusing was performed on artifacts located on the sample. For the images taken are of 220 nm sputtered aluminum oxide film on a silicon substrate. Due to charging effects, the morphology of the film could not be distinguished from the SEM images. The aluminum oxide film was subsequently coated with a layer of carbon in an attempt to improve the resolution of the images by reducing the effects of charging, however, the focused images on the films remained featureless at high magnifications. In an attempt to reduce the charging effects of the insulating film, the acceleration voltage was varied between 15 kV to 1 kV, however, the effects of charging were still apparent.