A PMOS TRANSISTOR FOR A LOW POWER 1 V CMOS PROCESS

by

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A Thesis submitted in conformity with the requirements for the degree of Master of Applied Science in the Department of Electrical and Computer Engineering
University of Toronto

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ABSTRACT

Due to the growth of the battery powered electronics consumer market, the use of integrated circuits in low power applications has become the focus of intense work in the last few years. Developing a technology capable of operating at a low supply voltage is the most straightforward way to accommodate low power applications. A major hurdle in realizing a low voltage, sub-micron CMOS technology is the requirement of dual gate doping, n+ for an n-channel device and p+ for a p-channel device. Tailoring the PMOS transistor to a low voltage CMOS technology is the focus of this thesis. The PMOSFET requires special attention because of the process difficulties arising in fabricating a p-channel device with a p+ poly gate. High frequency and quasi-static C-V tests on p+ poly gates fabricated at various conditions were used to establish the fabrication conditions of a p-type gate on 200 Å gate oxide without boron penetration into the channel or polydepletion of the gate. Surface channel PMOS devices compatible with 1 V applications were subsequently fabricated with a minimum $L_{eff}$ of 2.2 μm, a $V_{to}$ of -370 mV, an $S$ of 83 mV/dec and a low off-state leakage current of 2.5 pA/μm. This work can easily be extended to submicron devices.
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CHAPTER 1

INTRODUCTION

1.1. The Emergence of Low Power Technology

Since the establishment of CMOS as the mainstream technology for digital system design, optimization of chip area, circuit speed, and functionality have been the pre-eminent drivers behind the improvement of technology. During this time, the power dissipation metric has been little more than an afterthought in all but the most power frugal (μW range) of designs such as wristwatches, biomedical devices, and neural computers. However, these trends have undergone a profound change in the last three years, with electronic system power-efficiency beginning to gain considerable attention from the industry. This emergence of low-power electronics into the mainstream has been prompted by a variety of factors, the main ones being:

1. The growth of battery powered, portable consumer electronics is the key driver for low-power technology development [1, 2]. Portable systems require that even power efficient CMOS must be adapted to adequately support complex systems without being a significant drain on battery life.

2. As transistors are scaled down to increase speed, hot-carrier effects, gate oxide integrity, and device breakdown all require a reduction in operating voltage if adequate reliability is to be maintained for deep submicron dimensions [3].

3. The reduction of heat dissipation, which not only improves the reliability of the system but, also opens the door for higher levels of integration; allowing system-on-a-chip realizations and eliminating the need for expensive packaging solutions.
The most straightforward and effective method of increasing the energy efficiency of a circuit is via a reduction of the supply voltage [4]. CMOS logic power dissipation can be mainly attributed to:

1. The dynamic power, $P_d$ dissipated in switching a load capacitance $C_L$

$$P_d = \alpha C_L V_{DD}^2 f$$

where $f$ is the clock-frequency, $\alpha$ is the activity ratio (the number of times the node switches within each clock cycle) and $V_{DD}$ is the supply voltage.

2. The static power, $P_s$ dissipated when a CMOS gate is in the standby mode (i.e. no changing signals are present at the inputs)

$$P_s = I_{off} V_{DD}$$

where $I_{off}$ is the off-state leakage current that flows from supply to ground.

The dynamic power dissipation generally consumes the largest share of a system's power budget. Since $P_d$ is proportional to the square of the supply, a down-scaling of $V_{DD}$ becomes a very effective way of reducing the active power drain. $P_s$ is critical in precision applications and portable instruments with long down-times such as lap-top PCs and cellular telephones and is best minimized by reducing the subthreshold leakage current as well as the supply voltage.

The disadvantages of reducing the supply voltage are most critical for analog circuit design. In analog applications, an adequate signal-to-noise ratio must be maintained. This, and the need to maintain precision, become very difficult goals to meet at low supply voltages. Possible solutions include biasing the devices in the weak inversion region, avoiding cascode configurations and maintaining rail-to-rail operation.

Figure 1.1 [5] illustrates the predicted reduction in the CMOS supply voltage standard as the gate length is scaled down over the next ten years. This trend is expected because of the demand for increasingly complex integrated systems operating at low power budgets.
Figure 1.1: CMOS scaling trends for the next 10 years (a) shows the scaling of the supply voltage range for low power applications while (b) shows the expected scaling trend of the minimum gate length.

Circuit approaches to accommodate sub-2 V applications without changes to the technology have been attempted [6-9]. However, as supplies are scaled into the 1 V regime, the need for low voltage CMOS technology becomes imperative.

1.2. Low-Voltage CMOS Transistors

1.2.1. Threshold Voltage and Leakage Current

Correctly scaling the device threshold voltage, \( V_{th} \), with the supply is the key step in the design of a low voltage process. \( V_{th} \) is of significant importance in defining the performance of a MOS device by virtue of its influence on logic levels, noise-margins, and speed. However, it takes on added weight in a low power process which requires an optimized energy-delay product. The energy, \( E \), required to charge a load capacitance \( C_L \) in a CMOS gate is

\[
E = \frac{1}{2} C_L V_{DD}^2
\]

(1.3)
and the delay $t_d$ (assuming long-channel transistors) for the same gate is given by

$$t_d = \frac{Q}{I} = \frac{C_L V_{DD}}{\mu C_{ox} (W/L) (V_{DD} - V_{th})^2}$$

(1.4)

where $\mu$ is the carrier mobility, $C_{ox}$ the gate capacitance and $W$ and $L$ the gate width and length, respectively. It follows that, by differentiating the product of Eqs. (1.3) and (1.4) with respect to $V_{DD}$, the minimum energy-delay product $(E_{td})_{\text{min}}$ is achieved when $V_{DD} = 3V_{th}$. Thus, for a generic 1 V supply, a suitable choice for the threshold voltage is approximately $\pm 300$ mV considering power dissipation and speed.

Reducing $V_{th}$ to improve energy-delay is compromised by an increase in the subthreshold leakage current as shown in Figure 1.2. The subthreshold leakage current, $I_D$ is the drain current that flows between the source and drain when the gate-source voltage $V_{GS}$ is below the threshold voltage and is given by

$$I_D = I_o \frac{W}{L} e^{\frac{q(V_{GS} - V_{th})}{kT}} (1 - e^{-\frac{qV_{DS}}{kT}}) = I_S e^{\frac{q(V_{GS} - V_{th})}{kT}}$$

(1.5)

where $I_o$ is the characteristic current, $I_S$ is the subthreshold current at $V_{GS} = V_{th}$, and $\kappa$ is given by

$$\kappa = \left(1 + \frac{C_{\text{dep}}}{C_{ox}}\right)^{-1}$$

(1.6)

where $C_{ox}$ and $C_{\text{dep}}$ are the gate oxide and depletion capacitances, respectively.

The rate at which the subthreshold current decreases with reducing $V_{GS}$ is specified by the inverse subthreshold slope, $S$ defined as

$$S = \frac{1}{\frac{\partial}{\partial V_{GS}}} \log(I_D)$$

(1.7)
The minimum theoretical value for $S$ is 60 mV/decade at 300 K.

The subthreshold leakage current at zero gate voltage (off-state leakage current), $I_{off}$ is sensitive to $S$ and $V_{to}$ as illustrated in Figure 1.2 where a comparison of the $I_D$-$V_{GS}$ transfer characteristics of two MOS devices with different threshold voltages is made. This diagram illustrates the ensuing increase in the off-state leakage current with a decrease in threshold voltage. By defining the threshold voltage $V_{to}$ in the weak inversion region\(^1\), the following expression for the off-state leakage current can be generated to illustrate the effect of threshold voltage and inverse subthreshold slope on $I_{off}$

$$I_{off} = I_s 10^{\frac{-V_{to}}{S}}$$  \hspace{1cm} (1.9)

where it is seen that the off-state leakage current is exponentially dependent on $V_{to}$ and $S$ from $V_{to}$ to $V'_{to}$.

**Figure 1.2:** Comparison of the effect $V_{to}$ scaling has on device leakage current.

---

\(^1\) Unless otherwise stated, for the remainder of this thesis, $V_{to}$ is defined by extrapolation of the linear $I_D$-$V_{GS}$ curve.
In order to minimize $I_{off}$ in a low-voltage technology $S$ must be reduced as much as possible.

### 1.2.2. Low-Voltage PMOS Transistors

The keystone in implementing a low-power CMOS process is the proper design of the PMOS transistor. The p-channel device merits special attention because its fabrication requires a $p^+$-doped polysilicon gate (as opposed to the ubiquitous $n^+$ doped gate). The need for the p-type gate can be explained by examining the equation for the threshold voltage defined as

$$V_{th} = \phi_{MS} - 2\phi_F - \frac{Q_f}{C_{ox}} + \frac{Q_B}{C_{ox}} + \frac{qD_i}{C_{ox}}$$

(1.10)

where $\phi_{MS}$ is the gate-semiconductor work function, $\phi_F$ is the Fermi potential, $\phi_S$ is the channel potential underneath the gate oxide, $Q_f$ is the fixed oxide charge, $Q_B$ is the semiconductor bulk charge, $D_i$ is the dose of the channel threshold adjust implant, and $C_{ox}$ is the gate-oxide capacitance. As shown in Figure 1.3, $\phi_{MS}$ is dependent on the type of material used to make the gate.

**Figure 1.3:** Gate-semiconductor work function difference versus $n$-type Si substrate doping for aluminum, gold, $n^+\_s$, and $p^+$-polysilicon gates. (From [10])
Using the $\phi_{MS}$ values given in Figure 1.3 and referring to Eq. 1.10, it can be shown that a PMOS device with a $p^+$ poly gate requires an n-type threshold adjust implant to attain a -300 mV threshold voltage, while a PMOS transistor controlled by an $n^+$ poly gate needs a counter-doping p-type threshold adjust implant into its n-well in order to achieve the same threshold voltage. The fact that a $p^+$ poly gate eliminates the use of p-type threshold adjusts in the channel becomes crucial as devices are scaled. P-type threshold adjust implants move the conduction channel of the PMOS device away from the surface of the transistor and into the bulk. A "buried channel" device of this sort, as shown in Figure 1.4, benefits from an improved mobility (since there is no surface scattering of the mobile charge carriers), but suffers from a much degraded inverse subthreshold slope, $S$ making it unsuitable for low-power applications [11]. Also, due to its increased subthreshold conduction, a buried channel device suffers from poor short-channel characteristics which makes it impractical as the technology is scaled deep into the submicron region [12].

![Diagram](image)

**Figure 1.4:** PMOS buried transistor (a) Doping profile in the channel region (b) Cross section of the device.
1. P+poly gates give rise to two substantial fabrication problems as geometries are scaled and the gate-oxide thickness is reduced.

1. Device performance can be degraded by the penetration of boron used to dope the p+ poly gate through the thin gate oxide and into the channel. This is due to the high diffusivity coefficient of boron through silicon-dioxide [11]. This impurity migration into the channel is a problem not only as oxide thickness is reduced, but also as source/drain junctions become shallower and require BF2 as a boron source. Since boron diffusion through the oxide is enhanced by the presence of fluorine [13] a revision to the standard practice of simultaneous junction/gate doping may be necessary.

2. Reducing the amount of boron introduced into the gate to curb its rapid diffusion results in a non-degenerately doped gate which no longer acts as an equipotential surface. A gate of this type can be depleted of charge near the surface of the gate oxide (due to the charge in the channel) thus increasing the effective oxide thickness and decreasing the ability of the gate to control the channel. This phenomenon is referred to as the polydepletion effect [14].

The above problems require material, doping, and thermal budget compromises in the fabrication process in order to realize a functional PMOS transistor. In addition to these issues, the device must be designed as a complement to the NMOS transistor and must take into consideration all the fabrication requirements of a suitable low-power n-channel device.

1.3. Thesis Objectives and Outline

Although studies into implementing p+ poly gates for low voltage MOS applications have been, and continue to be, well documented in the literature, very little work has been done in developing a technology suitable for 1 V applications. Furthermore, reports focusing on the process requirements and development of 1 V CMOS compatible technologies are, to the author's knowledge, rare and cursory in their discussions of the key fabrication issues.

In this light, the objectives of this thesis are to resolve and experimentally verify the technological issues involved in the fabrication of a PMOS transistor compatible with a baseline low power, low voltage CMOS process. Specific objectives include:
1. P⁺ poly gate fabrication

2. Substrate engineering to avoid short channel effects and to attain \( V_{tp} = -300 \text{ mV} \) and \( S < 85 \text{ mV/decade} \) with accompanying low off-state leakage current

The aim of the experimental work is to generate long-channel (>1 \( \mu \text{m} \)) transistors for use in standard circuit architectures designed for 1 V operation. In addition, it is also the goal of this project to outline the technological issues and directions required to successfully scale the devices into the submicron regime.

Chapter 2, discusses the low-voltage process and device simulation along with scaling issues. Chapter 3, discusses the fabrication procedure and measured performance of the PMOS transistors. A conclusion to the thesis is drawn in Chapter 4 along with suggestions for future work.
References


CHAPTER 2

PMOS PROCESS AND DEVICE SIMULATION

2.1. Introduction

In this chapter, the process and device simulations involved in the design of the low voltage PMOS transistor are presented. The PMOS process is designed to be compatible with a low voltage, twin-well CMOS process presently under investigation at the University of Toronto. Therefore, the thermal budget requirements of the CMOS process were included in the design of the PMOS fabrication sequence. Process simulations were performed using 1D (one-dimensional) TSUPREM-3\(^1\) and 2D (two-dimensional) TSUPREM-4\(^2\) simulators as a means of approximating the necessary fabrication conditions at various stages of the process. These simulators numerically estimate the diffusion, segregation, and implantation of dopant impurities as well as the growth rate and deposition of oxide and nitride on several different semiconductor materials [1].

The device characteristics of the PMOS transistor were investigated using the 2D device simulator, MEDICI\(^3\). This simulator takes as input device cross-sections with arbitrary doping profiles and solves for the terminal voltages and currents. MEDICI is also used to show the impact of scaling the low voltage PMOSFET into the deep submicron regime.

---

1. TSUPREM-3 is a trademark of Technology Modeling Associates, Inc. (TMA)
2. TSUPREM-4 is a trademark of Technology Modeling Associates, Inc. (TMA)
3. MEDICI is a trademark of Technology Modeling Associates, Inc. (TMA)
2.2. Process Design and Simulations

2.2.1. Process Specifications

The cross-section of the low voltage PMOSFET is shown in Figure 2.1. The p-channel transistor is designed to be fit within an n-well in order to make it more naturally portable to a CMOS technology. An 8-9 Ω-cm (~1.7×10^{15} cm^{-3}) p-type <100> orientation wafer was chosen as the substrate. The low background doping leaves room for fabricating the low doped n-well (~1.0×10^{16} cm^{-3}) needed to realize a -300 mV threshold voltage. The low substrate doping also allows for the individual optimization of an NMOS transistor, should the PMOS process be expanded into a CMOS technology. The depth of the well is designed for 2 μm in order to safely avoid vertical punchthrough below 3 V. The gate oxide thickness, dictated by its reproducibility from run-to-run, was chosen to be 200 Å. The thickness of the p^+ polysilicon gate layer was selected to be 0.3 μm, out of consideration for the surface topology and poly wire resistance. The gate must be fabricated without any boron penetration or polydepletion effect problems. The source/drain junction depth was chosen to be 0.3 μm as a compromise between minimizing short-channel effects and junction sheet resistance. Lightly doped drains (LDD) were not included in the design of the device because the 1 V supply voltage is too low to give rise to significant fields in the channel. Aluminum is used for metallization. Titanium-tungsten (TiW) alloy is sputtered before the aluminum in order to act as a blocker against the spiking of aluminum through the shallow source and drain junctions. The device parameters are summarized in Table 2.1.

Table 2.1: Low Voltage PMOS Device Parameters

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
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<td>Threshold Voltage</td>
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<td>-300</td>
<td>mV</td>
</tr>
<tr>
<td>Oxide thickness</td>
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<td>Å</td>
</tr>
<tr>
<td>(P^+ poly) Gate thickness</td>
<td>t_{G}</td>
<td>3000</td>
<td>Å</td>
</tr>
<tr>
<td>Source/drain junction depth</td>
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<td>Å</td>
</tr>
<tr>
<td>n-well surface concentration</td>
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<td>cm^{-3}</td>
</tr>
<tr>
<td>n-well depth</td>
<td>x_{well}</td>
<td>2</td>
<td>μm</td>
</tr>
</tbody>
</table>
2.2.2. \( P^+ \) Poly Gate Fabrication Options

The following summarizes the procedural options available for the fabrication of the \( P^+ \) polysilicon gate. The goal of each option is to provide a process within which degenerately doped \( p^- \) type poly gates can be formed without any penetration of dopant through the gate oxide.

1. Chemical vapor deposition (CVD) can be used at temperatures below 600 °C to fabricate an amorphous silicon gate (as opposed to the polycrystalline structure normally associated with the gate material) \[2\]. Amorphous silicon does not have the columnar microstructure, pinholes and small grain size of polycrystalline silicon and thus tends to retard the diffusion and channeling of dopants introduced into it via implantation \[3\]. This is a significant advantage because the absence of columnar structures in amorphous silicon slows the penetration of implanted boron dopants in the gate. As a result, a higher temperature anneal can be applied to the gate to adequately activate most of the boron dopants without causing penetration through the gate oxide. Annealing the amorphous silicon structure above 600 °C will recrystallize it into a polycrystalline structure \[4\].
2. Employing a nitrogen-doped-poly-buffer layer between the p⁺ poly gate and the gate oxide has been shown to be effective in stopping boron penetration into the channel [5]. This process requires the deposition of a very thin (~50 Å) nitrogen doped poly layer (nitrogen concentration \(~1\times10^{21} \text{ cm}^{-3}\) followed by in-situ boron-doped deposition of the rest of the poly gate. The nitrogen-doped-poly acts to stop the diffusion of boron before the dopant reaches the gate oxide. The advantage of this approach is that boron penetration is dependent on the ability of the nitrogen-doped buffer to stop the diffusion of dopants into the channel. This allows the gate oxide thickness to be downscaled without fear of boron penetration and without the need for altering the gate doping and fabrication conditions. Aside from the processing difficulties of reproducibly depositing a very thin nitrogen-doped layer, a drawback to this approach is the uncertainty in the efficiency of boron diffusion into the nitrogen-doped layer which can cause variations in the gate work-function and lead to problems with accurate \(V_{to}\) prediction.

3. An increasingly popular method of preventing boron penetration involves the incorporation of nitrogen into the gate oxide to act as a diffusion retarding shield. Such nitride doped oxide layers involve a standard oxidation of silicon in \(\text{O}_2\) ambient followed by a rapid thermal nitridation (RTN) in a \(\text{NO}\) [6], \(\text{N}_2\text{O}\) [7] or \(\text{NH}_3\) [8] ambient. Nitridation changes the standard gate oxide to an oxynitride, \(\text{SiO}_x\text{N}_y\) with mole fractions \(x\) and \(y\) dependent on the RTN temperature and nitrogen concentration [9]. Although nitridation of the gate oxide improves tolerance to hot-carrier injection and reliability, it increases the oxide fixed charge density, degrades mobility, suffers from difficult control and reproducibility and requires a high thermal budget unless special process steps are taken [8, 10, 11].

4. Another alternative involves growing a thin oxide atop undoped polysilicon (i.e. a polyoxide) before implantation of \(\text{BF}_2\) (a source of boron) into the gate. \(\text{BF}_2\) implants have a small projected range and do not penetrate deep into the poly, however fluorine segregation at the gate-SiO₂ interface (after an activation anneal) acts to enhance the diffusion of boron through the gate oxide [12]. Experimental results show that the thin polyoxide acts to getter the fluorine at the top of the poly gate, reducing the segregation of fluorine impurities at the poly-SiO₂ interface and suppressing the penetration of boron through the gate oxide [13]. By allowing \(\text{BF}_2\) to be used as a dopant for the gate
this option has the potential for simultaneously doping the gate and forming shallow (<0.3 μm) source/drain junctions with a single implant.

In this work, the first option was used to fabricate the poly gate, because it offers the simplest fabrication requirements and shows applicability to gate oxide thicknesses as low as 150 Å [3, 14]. The critical parameters in the gate's fabrication include the dose used for boron implantation [9] and the temperatures used for annealing [7, 9]. Since rapid thermal annealing (RTA) is effective in reducing boron ion penetration through the gate [15], this approach was used to activate the boron implant.

2.2.3. Process Flow

Cross-sectional diagrams of the various stages of the fabrication sequence are shown in Figure 2.2. A total of 6 masks were used for the process.

A phosphorus implant through screen oxide as shown in Figure 2.2(a), is used to introduce the n-well dopants into the starting substrate. The dopant impurities are then subjected to a drive-in anneal to form a blanket n-well throughout the entire wafer. Standard LOCOS (LOCal Oxidation of Silicon) isolation technology is used to generate a thick field oxide that defines the active region of the device as shown in Figures 2.2(b) and (c) using mask #1 (the active region mask).

A sacrificial oxide is grown and immediately etched for the purpose of oxidizing-out any damage at the silicon surface. The gate oxide is then grown and a phosphorus $V_{to}$-adjust (threshold adjust) is implanted through it as shown in Figure 2.2(d).

The gate is fabricated by low pressure chemical vapor deposition (LPCVD) of amorphous silicon. As already mentioned, amorphous silicon acts to inhibit the penetration of boron into the channel by virtue of its non-columnar microstructure. The gate deposition is followed by a low-energy boron implant into the polysilicon as shown in Figure 2.2(e). A thick layer of silicon-nitride is deposited on top of the gate to protect it from the source/drain B$_2$F$_2$ implants to follow. The structure is then exposed to a rapid thermal anneal (RTA) which takes into account the step required to form a poly-poly capacitor in an experimental CMOS process.
Photoresist is patterned atop the nitride-poly stack using mask #2 (the gate delineation mask). The nitride-polysilicon stack is then dry etched using reactive ion etching (RIE) to form the gate fingers, as shown in Figure 2.2(f). RIE is used to obtain anisotropic etching of the gate stack.

The source/drain junctions are implanted using BF$_2$ through a photoresist pattern defined using mask #3 as shown in Figure 2.2(g). The thick silicon-nitride atop the gate acts to keep any BF$_2$ from entering the gate.

Well contact regions are implanted with phosphorus through a photoresist pattern defined using mask #4 as shown in Figure 2.2(h). All the nitride is then removed with a selective wet etch solution. A thick LPCVD isolation oxide layer is deposited as shown in Figure 2.2(i) through which contacts will be made to the gate and junction regions.

A high temperature RTA is applied to simultaneously active all dopants in the p$^+$ gate, source/drain junctions, threshold adjust, and well contact, and to densify the isolation oxide. A high temperature RTA was used in order to adequately activate the gate and source/drain dopants and remove implantation-induced crystallographic defects without allowing the dopants sufficient time to diffuse throughout the device [16]. This high temperature, short-time anneal is intended to strike a balance between avoiding the polydepletion effect in the gate and preventing boron penetration into the channel.

Mask #5 is used to define the openings in the oxide for metal contacts to the source, drain, gate, and substrate as shown in Figure 2.2(j).

After sputtering titanium-tungsten and aluminum the metal is patterned using mask #6 to form the final structure as shown in Figure 2.2(k).
Phosphorus Implant (n-well doping)

Mask #1 (FOX)

Mask #2 (PPOLY)

Mask #3 (PJUNC) BF₂ Implant
p⁺ source/drain junctions

Boron Implant (doping the gate)

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2.2.4. Process Simulations

After finalizing the process flow, TSUPREM-3 was used to establish the initial process conditions required to fabricate the n-well, threshold adjust, and source/drain junctions. This includes all implantation, diffusion, oxidation, annealing, and material deposition steps from the n-well implant to the SWS oxide densification anneal. Since the process simulator does not accurately model the implantation and diffusion of boron in amorphous and polycrystalline silicon, experimental results for the dopant distribution in the gate were used¹.

A summary of the low-voltage PMOS process steps is included in Table 2.2. A more detailed process summary is given in Appendix A. The process conditions described in the table

¹ A summary of the experimental work carried out on the gate is included in Chapter 3.
up to and including the final 1100°C RTA were derived using TSUPREM-3 process simulations.

Table 2.2: Low Voltage PMOS Process Summary

<table>
<thead>
<tr>
<th>STEP</th>
<th>PROCESS</th>
<th>CROSS-SECTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Starting material</td>
<td>4” &lt;100&gt; p-type boron doped wafers, ρ=8-9 Ω-cm (1.7×10^{15} cm^{-3})</td>
<td></td>
</tr>
<tr>
<td>Screen oxide growth</td>
<td>Dry oxidation, 950°C, 63 min., thickness=300 Å</td>
<td></td>
</tr>
<tr>
<td>Introducing the n-well dopants</td>
<td>Ion implantation, phosphorus, E=150 keV, Q_i=8×10^{11} cm^{-2}</td>
<td>Figure 2.2 (a)</td>
</tr>
<tr>
<td>Well dopant drive-in</td>
<td>Furnace anneal, dry oxidation 1100°C, 10 min., wet oxidation 1100°C, 5 min., 1100°C, 6 hrs., N₂ ambient</td>
<td></td>
</tr>
<tr>
<td>Stress-relief oxide growth</td>
<td>Dry oxidation, 950°C, 96 min., thickness=400 Å</td>
<td></td>
</tr>
<tr>
<td>Deposition of nitride as part of LOCOS</td>
<td>LPCVD nitride deposition, thickness=1200 Å</td>
<td></td>
</tr>
<tr>
<td>Patterning the nitride (left over active regions)</td>
<td>Photolithography (mask #1), Nitride RIE etch, Oxide wet etch</td>
<td>Figure 2.2 (b)</td>
</tr>
<tr>
<td>Field oxide growth</td>
<td>Dry oxidation, 950°C, 10 min Wet oxidation, 950°C, 250 min Dry oxidation, 950°C, 10 min, thickness=7100 Å</td>
<td></td>
</tr>
<tr>
<td>Opening up active regions</td>
<td>Nitride wet etch, Oxide wet etch</td>
<td>Figure 2.2 (c)</td>
</tr>
<tr>
<td>Sacrificial oxide (to clean active region surface)</td>
<td>Wet oxidation, 900°C, 25 min, thickness=500 Å, Oxide wet etch</td>
<td></td>
</tr>
<tr>
<td>12.5 min. 1000°C gate oxidation, 98% O₂, 2% HCl</td>
<td>Dry oxidation, 900°C, 55 min, 90% O₂, 10% HCl, thickness=200 Å</td>
<td></td>
</tr>
<tr>
<td>Threshold voltage adjustment</td>
<td>Ion implantation, phosphorus, E=50 keV, Q_i=1×10^{11} cm^{-2}</td>
<td>Figure 2.2 (d)</td>
</tr>
<tr>
<td>Deposition of α-poly gate</td>
<td>LPCVD amorphous silicon deposition, thickness=3000 Å</td>
<td></td>
</tr>
<tr>
<td>STEP</td>
<td>PROCESS</td>
<td>CROSS-SECTION</td>
</tr>
<tr>
<td>-------------------------------------------</td>
<td>-------------------------------------------------------------------------</td>
<td>---------------</td>
</tr>
<tr>
<td>Setting the work function of the gate</td>
<td>Ion implantation, E=25 keV, Q=5.0×10^{15} cm^{-2}</td>
<td>Figure 2.2 (e)</td>
</tr>
<tr>
<td>Deposition of nitride blocker</td>
<td>LPCVD nitride deposition, thickness=1800 Å</td>
<td></td>
</tr>
<tr>
<td>Nitride densification/CMOS capacitor, oxide densification</td>
<td>Rapid Thermal Anneal (RTA), 900°C, 1 min, N₂ ambient</td>
<td></td>
</tr>
<tr>
<td>Formation of the gate structure</td>
<td>Photolithography (mask #2), Reactive Ion Etch (RIE) of nitride and polysilicon layers</td>
<td>Figure 2.2 (f)</td>
</tr>
<tr>
<td>Gate re-oxidation</td>
<td>RTA, 900°C, 1 min in O₂ ambient</td>
<td></td>
</tr>
<tr>
<td>Screen nitride layer deposition</td>
<td>LPCVD nitride deposition, thickness=200 Å</td>
<td></td>
</tr>
<tr>
<td>Formation of p⁺ source/drain junctions</td>
<td>Photolithography (mask #3) Ion implantation, BF₂, E=40 keV, Q=1.0×10^{16} cm^{-2}</td>
<td>Figure 2.2 (g)</td>
</tr>
<tr>
<td>Formation of n⁺ well contacts</td>
<td>Photolithography (mask #4) Ion implantation, phosphorus, E=70 keV, Q=5.0×10^{15} cm^{-2}</td>
<td>Figure 2.2 (h)</td>
</tr>
<tr>
<td>Removal of nitride blocker</td>
<td>Nitride wet etch</td>
<td></td>
</tr>
<tr>
<td>Isolation oxide deposition</td>
<td>LPCVD oxide deposition, thickness=7000 Å</td>
<td>Figure 2.2 (i)</td>
</tr>
<tr>
<td>Formation of contact windows to source, drain, gate, and substrate</td>
<td>Photolithography (mask #5), oxide wet etch</td>
<td>Figure 2.2 (j)</td>
</tr>
<tr>
<td>Titanium-Tungsten spiking barrier formation</td>
<td>Sputtering of TiW layer, thickness=1000 Å</td>
<td></td>
</tr>
<tr>
<td>Metallization</td>
<td>Sputtering of Al layer, thickness=9000 Å</td>
<td></td>
</tr>
<tr>
<td>Metal patterning</td>
<td>Photolithography (mask #6), Aluminum and TiW wet etch</td>
<td>Figure 2.2 (k)</td>
</tr>
<tr>
<td>Aluminum sintering</td>
<td>Furnace anneal in forming gas, 450°C, 25 min</td>
<td></td>
</tr>
</tbody>
</table>
The TSUPREM-3 process simulations were first carried out on the n-well and threshold adjust. The simulated well and channel profile were then used (as the background concentration) for the source/drain and n+ well contact junction simulations. The low voltage PMOS transistor does not require extensive 2D process simulation because it does not include an LDD. Figure 2.3 summarizes the simulation results on the various regions of the device.

Figure 2.3: 1D simulated vertical doping profiles in (a) the channel and well, (b) source/drain.

The doping profile of the channel region is shown in Figure 2.3(a). The concentration of the n-well at the surface is $1 \times 10^{16}$ cm$^{-3}$ and the depth is 2.4 μm. The phosphorus threshold voltage adjust implant raises the channel surface concentration to $2.7 \times 10^{16}$ cm$^{-3}$.
The doping profile of the source/drain region is shown in Figure 2.3(b). The junction depth is 0.28 μm and the surface concentration is $2.2 \times 10^{20}$ cm$^{-3}$. The junction sheet resistance is 32 Ω/□. The flat concentration profile near the surface indicates that the p-type dopants have reached their solid-solubility limit. The sharp taper of the source/drain profile from high to low concentration is desirable because it lowers the spreading resistance of the junctions.

### 2.3. Long Channel Device Simulations

A sample of the PMOS transistor cross-section investigated by MEDICI and used to extract the current-voltage and small-signal characteristics is shown in Figure 2.4. Devices of varying channel lengths (1 to 10 μm, drawn) were simulated. All the vertical (i.e., vs. y-axis) doping profiles were determined using TSUPREM-3 while the lateral (i.e., vs. x-axis) extension of the source/drain regions was determined with TSUPREM-4 and analytically modeled in MEDICI. The device simulation was an iterative process with the fabrication conditions altered and the device electrically re-tested until the $V_{to}$ specifications were met and $S$ reduced as far as possible.

![Figure 2.4: 2D MEDICI simulation structure.](image)

The minimum feature size obtainable with the University of Toronto fabrication facilities utilized in this work is 3 μm (see Appendix B). For drawn gate lengths of 3 μm, the PMOS device considered in this work has an effective channel length, $L_{eff}$ of 2.6 μm. To confirm analytically that the 3 μm gate resolution exhibits long channel behavior, the following expression is employed [17]
where $L_{min}$ is the minimum effective channel length required to avoid short-channel effects, $x_j$ is the source/drain junction depth, $t_{ox}$ is the gate oxide thickness, $l_s$ and $l_d$ are the depletion region widths at the source and drain respectively and (const) is $8.8 \ \mu$m$^{-1/3}$. Eq. 2.1 indicates that an effective channel length, $L_{eff} > 1.1 \ \mu$m is necessary to avoid short-channel effects considering a channel doping of $2 \times 10^{16} \ \text{cm}^{-3}$ an $x_j$ of 0.3 \ \mu$m and a $t_{ox}$ of 200 \ \AA. This result indicates that the PMOS device examined in this work maintains long-channel behavior at a gate resolution of 3 \ \mu m.

\[
L_{min} = (\text{const}) \left[ x_j t_{ox} (l_s + l_d)^2 \right]^{1/3}
\] (2.1)

2.3.1. I-V Characteristics and Threshold Voltage

The simulated $I_D$-$V_{GS}$ transfer characteristics for a 3 \ \mu m device with an effective gate length of $L_{eff} = 2.6 \ \mu$m are shown in Figures 2.5 (a) and (b). $V_{DS}$ is maintained at -50 mV following standard threshold voltage measuring procedure [18]. The $V_{to}$ is defined as the value of $V_{GS}$ intercepted by a line extrapolated from the point of maximum slope on the linear $I_D$-$V_{GS}$ curve. This technique was used to extract a threshold voltage of -312 mV, satisfying the $V_{to}$ specification\(^1\). In this definition of the threshold voltage, $V_{to}$ acts as the $V_{GS}$-axis intercept of a line describing the relationship between drain current and gate voltage of a MOS device under strong inversion operating in the linear region (i.e. $V_{GS} > V_{DS} + V_{to}$). This interpretation of $V_{to}$ finds direct use in SPICE current modelling equations above threshold and is easily extracted from experimental measurements [19]. The simulated inverse subthreshold slope $S$ extracted by measuring the inverse slope of log($I_D$)-$V_{GS}$ in the weak inversion regime, is 76 mV/dec. The device leakage current with 0 V applied at the gate and -1 V applied between drain and source is 1.4 pA/\mu m.

---

\(^1\) An alternative definition of the threshold voltage is the gate voltage required to cause a predetermined value of drain current to flow [18, 19, 20]. A drain current of 10 nA/(W/L) is commonly chosen for defining the $V_{to}$ of low voltage devices. Using this method the $V_{to}$ is extracted to be -248 mV.
Figure 2.5: Simulated (a) transfer and (b) subthreshold characteristics for the $L_{\text{eff}} = 2.6 \ \mu m$ PMOS transistor.

MEDICI simulations of $V_{t0}$ and $S$ as functions of the channel length are shown in Figure 2.6. The results indicate that the device begins to exhibit short channel effects at drawn gate lengths around 2 $\mu m$ ($L_{\text{eff}} = 1.6 \ \mu m$) after which $V_{t0}$ and $S$ rapidly roll-off.

Figure 2.6: Device roll-off characteristics for (a) threshold voltage and (b) inverse subthreshold slope

The most direct way of extending long channel device behavior into the 1 $\mu m$ regime is by reducing the oxide thickness. This comes at the expense of having to re-evaluate the fabrication
thermal budget and its impact on boron penetration from the gate into the channel.

### 2.3.2. Small-Signal Parameters

The small-signal transconductance and output conductance parameters were extracted from the simulated current-voltage characteristics. The simulated transconductance versus drain voltage results are shown in Figure 2.7 for devices with effective gate lengths of 1.6 μm and 2.6 μm. The transconductance values at $V_{GS} = V_{DS} = -1$ V for the 1.6 μm and 2.6 μm devices are 8.9 mS/mm and 6.1 mS/mm, respectively. The maximum current in deep saturation at $V_{GS} = -1$ V is 3.6 μA/μm for the 1.6 μm device and 2.3 μA/μm for the 2.6 μm device. The intrinsic device voltage gain $g_m/g_{ds}$ at $V_{DS} = -1$ V and $V_{GS} = -1$ V is 30 and 33 for the 1.6 μm and 2.6 μm devices, respectively.

![Figure 2.7: Simulated transconductance characteristics for 2 μm and 3 μm drawn gate length devices.](image)

### 2.4. Device Scaling

A 1 V supply environment leaves room for device scaling into the sub-micron regime without rise to serious concerns for reliability. Keeping this in mind, a reduction of the drawn gate length to 0.35 μm and a down scaling of the oxide thickness to 60 Å represent realistic low power technology goals for the industry to meet before the end of the century [5, 21-23].

The process described at the beginning of this chapter can be adopted to accommodate a
0.35 µm technology. The most critical feature of a scaled device from a processing point of view is the thickness of the gate oxide. Avoiding boron penetration through dielectrics becomes exceedingly difficult since boron diffusion through SiO2 becomes exponentially dependent on oxide thicknesses below 80 Å [24]. Thus, not only does boron penetration play a major role, but so does gate oxide thickness control. Further, to avoid short-channel effects source/drain junctions must be made more shallow and a punchthrough stopper region included under the channel [25].

The deep submicron device simulation structure is the same as the one calculated for the long channel case with the obvious changes to the gate length and doping profiles. Nitride cap layers in the p⁺ poly gate are assumed to eliminate boron penetration through the gate oxide. The source/drain junctions are 80 nm deep to limit short channel effects, a realizable depth for current experimental technologies as shown in [26], with a sharp taper and no LDD to reduce junction resistance parasitics. The effective channel length is 0.25 µm.

2.4.1. I-V Characteristics and Threshold Voltage

The simulated linear region $I_D-S-V_G$ characteristics for the sub-micron device are shown in Figures 2.8 (a) and (b).

![Figure 2.8: Simulated (a) transfer and (b) subthreshold characteristics for the sub-micron transistor.](image)
The values of $V_{to}$ and $S$ extracted from Figure 2.8 are -308 mV and 64 mV/dec respectively. The device leakage current with 0 V applied at the gate and -1 V applied between drain and source is 20 pA/μm a value limited by the punchthrough stopper.

Figure 2.9, shows the portability of the technology to higher voltages with $I_{DS-V_{DS}}$ characteristics running up to -4 V. Above this voltage the 60 Å gate oxide is assumed to break down. From Figure 2.9 it can be seen that the device begins to show significant short channel effects above -2 V and punchthrough above -3 V.

![Figure 2.9: Deep sub-micron p-channel performance at higher gate and drain voltages.](image)

### 2.4.2. Small Signal Parameters and High Frequency Performance

The small-signal transconductance and output conductance parameters were extracted from the simulated current-voltage characteristics. An AC analysis was also carried out on the devices by sweeping a small-signal input across frequencies ranging from 10 MHz to 30 GHz under various biasing conditions. Y-parameters were obtained from these simulations and, in turn, used to extract the simulated S-parameters from which the values of $f_T$ (unity gain cutoff

1. A threshold voltage of -206 mV is measured at a drain current of 10 nA/μm.
frequency) and \( f_{\text{MAX}} \) (maximum frequency of oscillation) were calculated. For the purpose of maximizing the \( f_{\text{MAX}} \), simulations were carried out assuming interdigitated devices with six gate fingers and the use of polycides to lower the gate sheet resistance to 7 \( \Omega/\mu\) [27]. The width per gate finger is 5 \( \mu\)m (30 \( \mu\)m total width).

The simulated transconductance versus gate voltage results are shown in Figure 2.10. The transconductance at \( V_{\text{DS}} = -1 \) V and \( V_{\text{GS}} = -1 \) V is 93 mS/mm. The intrinsic device voltage gain \( g_m/g_{\text{DS}} \) at \( V_{\text{DS}} = -1 \) V and \( V_{\text{GS}} = -1 \) V is 3. Figure 2.11 compares the device gain parameter, beta to other high performance bulk CMOS technologies reported in the literature.

**Figure 2.10:** Simulated transconductance characteristics for 0.35 \( \mu\)m (\( L_{\text{eff}} \)=0.25 \( \mu\)m) PMOS transistor

**Figure 2.11:** Comparison of PMOS gain parameter, beta between this study and other work reported in the literature.
The simulated dependence of $f_T$ and $f_{MAX}$ on gate voltage is plotted in Figure 2.12. The simulated $f_T$ of 10 GHz and $f_{MAX}$ of 38 GHz make this transistor superior to BiCMOS-class bipolar devices of current vintage [27] and indicate that this device is fast enough to find use in RF applications even at a 1 V supply.

![Image of Figure 2.12](image_url)

**Figure 2.12:** Simulated $f_T$ and $f_{MAX}$ dependence on the gate bias for $0.35 \mu m$ ($L_{eff} = 0.25 \mu m$) devices with 6 gate fingers and a total width of 30 $\mu m$.

### 2.5. Conclusions

This chapter presented the device fabrication and performance issues and simulation results. Specifically, the low voltage PMOS process flow was defined and verified with 1D and 2D process simulations and its performance under low voltages examined with 2D device simulations. Process simulations showed that a low voltage PMOS transistor could be fabricated within a low voltage CMOS process. Device simulations showed that a -300 mV long channel transistor with sub-80 mV/dec subthreshold swing and low leakage current is possible.

The performance of deep submicron p-channel transistors was studied using 2D device simulations. It was shown that besides achieving the requisite $V_{to}$ and $S$ specifications these devices are suitable for high performance 1 V applications.
References


CHAPTER 3

PMOS FABRICATION AND CHARACTERIZATION

3.1. Introduction

This chapter presents the experimental work done to verify the process and device simulation results presented in Chapter 2. The experimental work was carried out in two parts:

1. MOS capacitors were fabricated and characterized. This was done for the purpose of finding p⁺ gate implant and anneal conditions suitable for achieving an equipotential gate structure (i.e. avoid the polydepletion effect) without allowing boron to penetrate through a 200 Å gate oxide into the channel.

2. Using the gate fabrication conditions determined from the MOS capacitor studies, PMOS transistors were fabricated and characterized in order to verify their suitability for 1 V applications.

This chapter includes the process characterization results of both the MOS capacitor and PMOS device fabrication runs. Also presented are the results of electrical I-V and C-V measurements on the transistor and capacitor. These measurements were used to study boron penetration and extract device parameters such as mobility, $V_{to}$, inverse subthreshold slope, device leakage current, $g_m$, and $g_{ds}$. The experimental results presented are for typical devices obtained from two different batches of wafers.

3.2. Experimental Low Voltage PMOS Process Development

Most of the work presented in this chapter is based on experimental results. Due to the advanced nature of this process (i.e. p⁺ poly gate incorporation, use of a deep and low doped well,
shallow source drain junctions and the requirement of a low threshold voltage) the default simulator models were unable to predict with adequate accuracy the fabrication conditions required to meet device specifications. A proper calibration of the simulator would require extensive experimental testing under specific control conditions and would have to account for second and probably third order effects. Thus, process simulators were used only to establish trends in the process conditions and as starting points for the experimental work used to refine the fabrication steps.

There are four important technology issues involved in the fabrication of the low voltage PMOS device. Each is dealt with individually in the following sub-sections. The first is the fabrication of a p+ poly gate without boron penetration or polydepletion. The second is the realization of a low doped n-well with a flat concentration profile and a 2 μm depth which is sufficient to prevent vertical punchthrough below 3 V. The third is the formation of the threshold adjust region needed to attain a -300 mV threshold voltage. The fourth is the fabrication of shallow 0.3 μm p' source/drain junctions to minimize short-channel effects.

3.2.1. P+ Poly Gate Fabrication

Using the MOS capacitor structure represented in Figure 3.1.(a), high frequency capacitance-voltage (HF C-V) measurements were carried out to evaluate whether boron penetration from the p+ poly gate through the gate oxide occurred. Boron penetration is assessed by noting positive shifts in the flat-band voltage, $V_{fb}$ (from expected $V_{fb}$ values) extracted from HF C-V curves as illustrated in Figure 3.1(b). A rise in $V_{fb}$ is expected if the boron acceptor dopants penetrating through the oxide form a sheet of positive charge in the channel near the gate oxide/substrate interface. Taking boron penetration into account, the flatband voltage can be expressed as [1].

$$V_{fb} = \phi_{MS} - \frac{q(N_B - N_F)}{C_{ox}}$$

(3.1)

where $\phi_{MS}$ is the gate-to-substrate contact potential, $N_F$ is the fixed oxide charge density, $C_{ox}$ is the capacitance of the gate oxide, and $N_B$ is the effective density of boron in the channel.

The polydepletion effect in the gate is identified by using QS (quasi-static) C-V measurements to monitor the inversion capacitance $C_{inv}$. As illustrated in Figure 3.1(c), QS C-V measurements with steadily decreasing $C_{inv}/C_{ox}$ ratios in the inversion region (as the voltage is
decreased) indicate that the poly gate is depleted.

![Diagram of MOS capacitor structure](image)

**Figure 3.1:** Illustrations of (a) the MOS capacitor test structure, (b) high frequency C-V tests to determine boron penetration, and (c) quasi-static C-V tests to assess the polydepletion effect.

MOS capacitor structures were fabricated on 3-4 Ω-cm (~ 1.5×10¹⁵ cm⁻³) n-type (phosphorus doped) wafers. A low doped substrate was chosen in order to make it easier to identify a small amount of boron penetration into the channel. Capacitors with different gate oxide thicknesses of 200, 400, 600, and 700 Å were fabricated for the purpose of establishing a $V_{fb}$ reference. The p⁺ poly gates were formed by implanting a boron of dose 5×10¹⁵ cm⁻² at an energy of 25 keV into 0.3 μm of amorphous silicon. The gate dopants were activated and annealed using a rapid thermal anneal of 1100°C for 20 s. A test sample was also annealed at 1100°C for 40 s in order to test for boron penetration at longer anneal times. The gate was patterned using reactive ion etching (RIE). The capacitor area was 222 μm × 222 μm.

In order to establish whether any boron diffused through the gate oxide, it is important to identify a $V_{fb}$ reference above which boron penetration is assumed to have occurred. To establish this reference, fabricated MOS capacitor structures with gate oxide thicknesses larger than 200 Å were used. Boron penetration is not expected to occur at these gate insulator thicknesses. Since $V_{fb}$ varies linearly with gate oxide thickness due to the effect of $qN_F/C_{ox}$ (see Eq. (3.1)) the measured flat-band voltages for the thick gate oxides can be extrapolated to a lower oxide thickness. Thus, a reference $V_{fb}$ related to the gate fabrication conditions, but independent of boron penetration, can be determined for an oxide thickness of 200 Å.

The measured flatband voltages as a function of gate oxide thickness under different annealing conditions are illustrated in Figure 3.2(a). The straight line shown in the figure repre-
resents the reference $V_{fb}$ at the corresponding oxide thickness.

The experimental results indicate that an amorphous silicon gate atop 200 Å gate oxide subjected to a boron implant of $5 \times 10^{15}$ cm$^{-2}$ at 25 keV and a 1100°C, 20 s anneal does not exhibit penetration. As a contrast, the capacitor sample annealed at 1100°C for 40 s has a $V_{fb}$ 384-442 mV higher than expected. This difference corresponds to approximately a $4.2 \times 10^{11}$ cm$^{-2}$ density of boron penetration under the oxide. The high-frequency C-V measurements for the two different gate samples annealed for 20 and 40 s are compared in Figure 3.2(b). The shift expected between samples with and without boron penetration is clearly illustrated in this figure.

![Figure 3.2](image)

**Figure 3.2:** (a) Extracted $V_{fb}$ results of MOS capacitors from HF C-V measurements shown vs. gate oxide thickness. (b) Comparison of C-V profiles with and without penetration.

In order to evaluate the extent of the polydepletion effect on the fabricated poly gates, quasi-static C-V measurements were carried out on a 200 Å gate oxide capacitor. In Figure 3.3, the measured quasi-static and high frequency results are shown for the p$^+$ poly gate implanted with a boron dose of $5 \times 10^{15}$ cm$^{-2}$ at 25 keV and annealed at 1100°C for 20 s.
Figure 3.3: *QS C-V data shown along side HF C-V measurements indicates a C/C\textsubscript{ox} near unity which is a sign that the gate structure does not suffer from the polydepletion effect.*

The quasi-static capacitance measured in deep inversion is within 1-2% of the oxide capacitance in the accumulation region. Also, since $C_{\text{inv}}$ does not decrease further in the inversion region it is safe to assume that the gate does not exhibit any polydepletion phenomena.

Figure 3.4 shows the poly gate doping profile obtained using spreading resistance analysis (SRA). The measured sheet resistance of the poly gate was 50 $\Omega$\textpercm.

*Figure 3.4: The measured boron concentration profile in the gate.*
In addition to the $5 \times 10^{15}$ cm$^{-2}$, 25 keV boron implant discussed above, MOS capacitor devices were formed with boron implanted at $1 \times 10^{16}$ cm$^{-2}$, 25 keV and $5 \times 10^{15}$ cm$^{-2}$, 20 keV. Neither one of these two gate fabrication conditions resulted in boron penetration or polydepletion. The final gate fabrication condition settled on consisted of the $5 \times 10^{15}$ cm$^{-2}$, 25 keV boron implant and a 1100°C, 20 s. activation anneal.

3.2.2. Well Fabrication

Various phosphorus implant and anneal conditions were tested in order to achieve an n-well with a surface concentration of $1 \times 10^{16}$ cm$^{-3}$ and a depth of 2 µm. These objectives were met for a well implant dose of $1.6 \times 10^{12}$ cm$^{-2}$ at 80 keV (through 300 Å of screen oxide) followed by a 13 hour 1100 °C anneal. Figure 3.5 shows the final well profile obtained using spreading resistance analysis (SRA).

![Graph showing net active concentration profile](image)

**Figure 3.5:** The measured (using SRA) net active concentration profile in the well implanted using phosphorus at $1.6 \times 10^{12}$ cm$^{-2}$, 80 keV and annealed at 1100 °C for 13 hours.

3.2.3. Threshold Adjust

The channel profile necessary to attain a -300 mV threshold voltage was determined using MEDICI simulations. Experimental implant tests were then carried out in an effort to achieve an expected profile close to that specified in the device simulations. The implant condition settled on
used a $7 \times 10^{11}$ cm$^{-2}$ phosphorus dose at an energy of 40 keV followed by an activation anneal at $1100^\circ$C for 20 s. The peak measured concentration in the channel after this implant was $3 \times 10^{16}$ cm$^{-3}$ and it had a depth of roughly 0.1 μm. The measured channel profile (using SRA) is shown in Figure 3.6. MEDICI simulations using the doping shown in Figure 3.6 as input, predict a threshold voltage of -324 mV.

![Graph](image)

**Figure 3.6:** The measured (using SRA) net active concentration profile in the channel region of the device.

### 3.2.4. Source/Drain Fabrication.

The p$^+$ source/drain junctions tests were carried out with the objective of realizing shallow 0.3 μm depths. In order to achieve this depth, a BF$_2$ dose of $1 \times 10^{16}$ cm$^{-2}$ was implanted into the silicon at various energies through a 200 Å layer screen of silicon-nitride. The source/drain implant energy was finalized at 80 keV and resulted in a junction 0.29 μm deep when subjected to the $1100^\circ$C, 20 s gate anneal. The peak boron concentration was $6 \times 10^{19}$ cm$^{-3}$ and the sheet resistance was 131 Ω/□. The resulting junction profile (obtained from SRA) is shown in Figure 3.7.
3.3. Fabrication of Low Voltage PMOS Transistors

A detailed description of the PMOS fabrication process is given in Appendix A with a discussion of each step of the process. The test chip was laid out using 3 µm minimum line widths and 3 µm alignment tolerance. The device layout specifications are discussed in Appendix B. The test chip used to fabricate the devices is 2650 µm x 4000 µm and is shown in Figure 3.8.

Figure 3.7: The measured (using SRA) boron active concentration profile in the source/drain junction.

Figure 3.8: Test Chip Layout
The process test inserts implemented in the chip include MOS capacitors for process and device characterization. TLM (transfer length method) transmission line patterns for sheet resistivity measurements of poly gate and diffusion regions, and Kelvin cross structures for extraction of the contact resistance. The transistors included in the test chip are:

(a.) 30 μm wide (single gate) Si p-MOSFET's with gate lengths of 2 μm, 3 μm, 5 μm, 10 μm and 20 μm respectively, separate well contacts and input/output pads of 110×110 μm for DC measurements.
(b.) 180 μm wide (single gate) Si p-MOSFET's with gate lengths of 2 μm, 3 μm, 5 μm, 10 μm and 20 μm respectively, separate well contacts and input/output pads of 110×110 μm for DC measurements.
(c.) 180 μm wide interdigitated (6 gate fingers) Si p-MOSFET's with gate lengths of 2 μm, 3 μm, 5 μm, 10 μm and 20 μm respectively, separate well contacts and input/output pads of 110×110 μm for DC measurements.
(d.) 300 μm wide interdigitated (6 gate fingers) Si p-MOSFET's with gate lengths of 2 μm, 3 μm, 5 μm, 10 μm and 20 μm respectively, well contacts strapped to the source and input/output pads of 50×50 μm compatible with signal-ground probes for S parameter probing.
(e.) Two 4×4 transistor arrays; one with transistors of dimension 3×110 μm and the other with transistors of dimension 3×30 μm to measure mismatch of device characteristics.
(f.) One long and wide transistor (FATFET) 100×100 μm Si p-MOSFET, with 110×110 μm input and output pads, intended for C-V profiling and effective channel length extraction.

A micrograph of an implemented device with a gate length of 3 μm and gate width of 180 μm is shown in Figure 3.9.
3.4. PMOS Device Characterization

In order to confirm the suitability of the fabricated PMOS device to 1 V applications the dc and low frequency characteristics of both long ($L_{\text{eff}} = 20 \ \mu\text{m}$) and short ($L_{\text{eff}} = 2.2 \ \mu\text{m}$) channel transistors were measured. Due to process variations, the gate oxide thickness of the fabricated p-channel devices was 230 Å, a 15% increase over the expected thickness of 200 Å. As with the process simulator, the device simulator models need to be calibrated to properly predict device behavior. This is especially crucial when dealing with the low voltage characteristics of transistors intended for low power applications. Since the device simulator was not calibrated in this work, its predictions were only useful in showing general trends and roughly estimating the performance of the device. The device characteristics presented in the following sections are based on experimental results.

3.4.1. C-V Characteristics and Mobility Profiling

Measuring the carrier mobility is an important means of confirming the performance leverage of a technology. In the case of the low voltage PMOS transistor the hole mobility is
expected to suffer due to the surface conduction nature of the device. An accurate method discussed by Voinigescu [2] was used in measuring the effective carrier mobility versus gate voltage. Using this technique, the measured gate-source capacitance $C_{GS}$ and the linear region transconductance $g_m$ are used to obtain the effective hole mobility $\mu_{peff}$ as a function of gate to source voltage from the expression

$$\mu_{peff}(V_{GS}) = \frac{g_m L_{eff}^2}{2V_{DS}C_{GS}}$$

(3.2)

where $L_{eff}$ is the effective device channel length. The C-V characteristics of a long channel ($L_{eff} = 20 \mu m$) p-channel transistor are shown in Figure 3.10. The $C_{GS}$ curve obtained is that expected for a MOS device operating in the linear region, with the capacitance curve quickly reaching a plateau once the channel is strongly inverted.

![Figure 3.10: The measured $C_{GS}$ of a fabricated long channel p-MOSFET in the linear region](image)

The linear region transconductance measurement is shown in Figure 3.11. The curve rises sharply as the channel is formed, saturates, and starts to decrease as the mobility degrades due to the increasing surface field at higher $V_{GS}$. 
Figure 3.11: The transconductance characteristics of the long channel p-MOSFET in the linear region.

The effective hole mobility vs. \((V_{GS} - V_{to})\) in the linear region, as extracted using Eq. 3.2 is shown in Figure 3.12 below. The peak mobility is 150 cm\(^2\)/Vs and occurs at \(V_{GS} = -0.7\) V. This value is typical of the room temperature hole mobility observed in surface channel Si p-MOSFET's [3].

Figure 3.12: The hole mobility versus gate voltage as measured on the FATFET, in the linear region.
3.4.2. I-V Characteristics

As described in the previous chapter, the threshold voltage is defined as the \( V_{GS} \)-axis intercept of the line tangent to the inflection point of the \( I_D-V_{GS} \) curve in the triode region of operation. Typical current-voltage characteristics in the linear region of device operation are shown in Figure 3.13. The effective gate length of these MOSFET’s is 2.2 µm. The effective gate length was determined using the transresistance method [4]. The average threshold voltage, inverse subthreshold slope and leakage current measured for each device length is listed in Table 3.1. For the purpose of comparison, threshold voltage values defined by a constant current level of 10 nA/(W/L) are also included in Table 3.1. The variability of each parameter across the wafer is also included in the column. The average threshold voltages measured remained consistent between the two batches of wafers tested. The measured threshold voltage of -370 mV is suitable for 1 V supply applications.

![Figure 3.13: Measured results of the linear region transfer characteristics of the low voltage PMOS device.](image-url)
Table 3.1: Threshold Voltage Summary

<table>
<thead>
<tr>
<th>Effective Length (μm)</th>
<th>Extrapolated ( V_{to} ) (mV)</th>
<th>Constant Current ( V_{to} ) (10 nA/(W/L)) (mV)</th>
<th>Inverse Subthreshold Slope (mV/dec)</th>
<th>Leakage Current (V( _{GS}=0 ) V, V( _{DS}=-1 ) V (pA/μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.2</td>
<td>-368.9±12%</td>
<td>-301.9±12%</td>
<td>83.7±1%</td>
<td>2.5±10%</td>
</tr>
<tr>
<td>4.7</td>
<td>-388.8±9%</td>
<td>-306.1±12%</td>
<td>83.8±1%</td>
<td>1.1±10%</td>
</tr>
<tr>
<td>10</td>
<td>-400.3±7%</td>
<td>-304.5±13%</td>
<td>82.9±1%</td>
<td>0.5±10%</td>
</tr>
<tr>
<td>20</td>
<td>-399.2±5%</td>
<td>-295.4±15%</td>
<td>83.0±1%</td>
<td>0.4±10%</td>
</tr>
</tbody>
</table>

The measured subthreshold slope and off-state leakage current of roughly 80 mV/dec and 2.5 pA/μm are in close agreement with much of the reported work on low voltage PMOS devices [3], [5-10]. As expected, the reported value of \( S \) is an improvement over those inherent to buried channel devices where the inverse subthreshold slope can range from 95 to 140 mV/dec [3, 11, 12].

The \( I_{D-V_{DS}} \) output characteristics of the devices over a 1 V range are shown in Figure 3.14. The saturation current, \( I_{DSAT} \) is 1.6 μA/μm at V\( _{GS} = V_{DS} = -1 \) V for the measured PMOS devices with \( L_{eff} = 2.2 \) μm.

![Figure 3.14: Measured drain current characteristics of low voltage PMOS devices.](image-url)
3.4.3. Transconductance and Output Conductance

Figures 3.15 (a) and (b) show the experimental device transconductance and output conductance characteristics ($L_{\text{eff}} = 2.2 \ \mu\text{m}$), respectively. The $g_m$ at $V_{\text{GS}} = V_{\text{DS}} = -1 \ \text{V}$ is $4.5 \ \text{mS/mm}$ and a peak $g_m$ of $6.3 \ \text{mS/mm}$ is reached at $V_{\text{GS}} = -1.4 \ \text{V}$. The output resistance at the saturation current is $53 \ \text{k}\Omega$ for the $180/2.2 \ \mu\text{m}$ device. The small signal intrinsic voltage gain $g_m/g_{ds}$ in deep saturation is 44.

![Figure 3.15: Measurement of the (a) transconductance and (b) output conductance of the low voltage PMOS device.](image)

3.4.4. Breakdown Characteristics

The device breakdown characteristics are included to show the p-channel transistor's ability to withstand high voltage stress. The channel punchthrough characteristics with the gate grounded and the drain-source voltage swept are shown in Figure 3.16 (a). The punchthrough voltage is approximately $-17 \ \text{V}$ for the $2.2 \ \mu\text{m}$ device. Another important breakdown characteristic for the low-voltage PMOS device is the voltage between drain and bulk at which vertical punchthrough occurs through the n-well between the drain and the p-type substrate. The vertical punchthrough characteristics are shown in Figure 3.16 (b). From the figure, it is seen that the vertical punchthrough occurs at approximately $-7.5 \ \text{V}$.
3.5. Conclusions

A CMOS compatible, low-voltage, PMOS process was developed and implemented. P+ poly gates were successfully fabricated without boron diffusion into the channel or the polydepletion effect. Deep, low-concentration n-wells with a flat profile were implemented along with suitable threshold voltage adjust implants and shallow source/drain junctions. Device measurements demonstrate a -370 mV threshold voltage (based on the extrapolation technique of measuring threshold voltage) an 83 mV/dec inverse subthreshold slope and a very low leakage current in agreement with other surface channel PMOS devices, indicating the compatibility of the fabricated transistors with 1 V, low power applications.

Figure 3.16: (a) Channel punchthrough and (b) vertical punchthrough characteristics of fabricated p-channel devices.
References


CHAPTER 4

CONCLUSIONS

The focus of this thesis has been the development and fabrication of a CMOS compatible p-channel MOSFET suitable for 1 V supply applications. The necessary characteristics for this device are a low threshold voltage of approximately -300 mV and a low leakage current <100 pA/\mu m, in the off-state. These two requirements are simultaneously satisfied with the use of a p-type polysilicon gate whose positive workfunction requires an n-type threshold voltage adjust to set the $V_{to}$ to -300 mV. To attain accurate threshold voltages, control current leakage, and maintain device repeatability the penetration of boron dopants from the p$^+$ poly gate must be prevented. To maintain drive and suppress short channel effects the p$^+$ poly gates must be doped heavily enough to avoid the polydepletion effect.

Due to process model inaccuracy in predicting the implantation and diffusion of boron into amorphous silicon and silicon-dioxide, MOS capacitor studies were first carried out. These tests were used to determine the process conditions needed in order to fabricate a p$^+$ poly gate without boron penetration or polydepletion. Once the gate fabrication conditions were established the low voltage PMOS transistor process was completed and low voltage PMOS devices were implemented in the University of Toronto fabrication facilities.

The -370 mV threshold voltage attained for these devices is close to the target value and still compatible with 1 V supply albeit at reduced current driving capability. In order to more closely approach a $V_{to}$ of -300 mV the device oxide growth and threshold voltage adjust implant conditions would require further optimization. The 83 mV/dec inverse subthreshold slope attained is in close agreement with the value reported in other PMOS transistor work and the low off-state leakage current of 2.5 pA/\mu m is very attractive for digital low power applications. The measured peak hole mobility of 150 cm$^2$/Vs is in good agreement with the value expected of surface channel PMOS devices and a positive indicator of process quality.

Aside from further optimizing the individual process steps of the current design, more work is necessary in adapting the process to a micron/submicron technology. This would require
a reduction in the gate insulator thickness and a re-assessment of the gate fabrication conditions needed to avoid boron penetration and polydepletion of the gate. Integrating the p-channel transistor with an n-channel MOSFET to form a low-voltage CMOS technology with two flavors of poly gates would allow for accurate assessments to be made of circuit performance, packing density, and leakage. The inaccuracy of process and device simulation software proved itself to be a major impediment throughout the course of this thesis. A worthwhile effort would be to focus on systematically calibrating various implant, diffusion, and segregation models for BF₂, boron, and phosphorus in silicon and polysilicon. A closer agreement between simulated and “real-world” results would significantly lighten the amount of experimental work required to successfully fabricate a device in future.
APPENDIX A

LOW VOLTAGE PMOS FABRICATION PROCESS DESCRIPTION

A detailed description of the low voltage PMOS transistor fabrication process is given below. This description is intended to serve as a reference for future work on the low voltage device. Steps such as photolithography, photoresist removal, cleaning and wet etch are conventional processing steps. For convenience they are given below in the description of the fabrication process flow. All of the steps described are optimized to achieve the appropriate specifications for the PMOS device. The wafers used in the fabrication process are p-type (boron doped) with resistivity 8-9 Ω-cm, 4” diameter and orientation <100>.

All photolithography process steps described below use MICROPOSIT 1350J photoresist. Photoresist spinning is done at 6000 rpm for 40 seconds for both HMDS and photoresist. Both pre-bake and post-bake are done at 90°C for 30 minutes. Photoresist development is done in a solution containing 1 part DI water and 1 part MICROPOSIT MF-312 developer for 45 seconds. Photoresist is removed using acetone. When removing photoresist after high dose/high energy implantation the photoresist asher machine is required.

All wafer cleaning processes use the three-step cleaning method described in the UTICL Data Sheet. The solutions used in each of the three cleaning steps are as follows (ratio given by volume): Removal of heavy organic contaminants - H₂SO₄ (Sulfuric Acid):H₂O₂ (Hydrogen Peroxide¹) = 1:1, Removal of light organic contaminants - DI wafer:H₂O₂:NH₄OH (Ammonium Hydroxide²) = 5:1:1, Removal of inorganic (atomic and ionic) contaminants - DI water:H₂O₂:HCl (Hydrochloric Acid³) = 6:1:1. The thin oxide grown after each cleaning step is removed by dipping the wafers in 5% HF (Hydrofluoric Acid, diluted 9:1 from 48% HF) for 5 seconds.

¹. Hydrogen peroxide: 30% unstabilized
². Ammonium Hydroxide: 28%
³. Hydrochloric Acid: 37%

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The process of oxide wet etch is done in buffered oxide etch solution with etch rate of 550 Å/min for thermally grown oxide.

All ion implantation steps were performed by the Implant Center, San Jose, CA.

**Fabrication Process Flow:**

1. **Clean the wafers.**

2. **Grow n-well implant screen oxide (dry oxidation process).**
   The target oxide thickness is ~ 300 Å. Dry oxidation is done at T=950°C, TIME=63 min.

3. **Implant phosphorus (energy E=80 keV, dose QI=1.6×10^{12} cm^{-2}).**
   Blanket n-well implant. The cross-section during this step is shown in Figure A.1 (a).

4. **Etch the oxide.**
   Remove the screen oxide.

5. **Clean the wafers.**

6. **Drive in the n-well.**
   Grow oxide on the surface to prevent dopant out-diffusion in two steps 1. Dry oxidation at T=1100°C, TIME=10 min. 2. Wet oxidation at T=1100°C, TIME=5 min. the target thickness is ~ 1700 Å. Follow with drive-in anneal at T=1100°C, TIME=13 hrs. in N_{2} ambient.

7. **Etch the oxide.**
   Etch the oxide grown during n-well drive-in.

8. **Clean the wafers.**

9. **Grow stress relief oxide.**
   Oxide designed to relieve stress on nitride during FOX growth. The target thickness is ~ 400 Å. Dry oxidation is done at T=950°C, TIME=96 min.

10. **Deposit LPCVD nitride.**
    The target thickness is ~1200 Å. This nitride is intended to protect the active region from oxidation during field oxide growth.

11. **Pattern the LPCVD nitride with photolithography process (mask #1, FOX).**
    Patterning of the device active area.

12. **De-scum process (Reactive Ion Etching (RIE) with oxygen).**
    All the RIE processes in this fabrication flow are performed in a SEMI GROUP 1000 TP/CC RIE System. This step is used to clean the edges of the photoresist to give a better line and clear away
any stray photoresist that may be in the open areas where the resist should have been removed.

**De-scum recipe:** 100% O$_2$ flow (flow rate 100 sccm), throttle pressure=120 mTr, power=50%, time=15 seconds.

**13. RIE of the LPCVD nitride.**
In this step the nitride is etched where the field oxide is to be grown.

**RIE nitride etch recipe:** 50% CHF$_3$ (freon-23) - 50% C$_2$F$_6$ (freon-116), throttle pressure=120 mTr, power=65%. The etch rate of the nitride is approximately 900 - 1000 Å/min. The cross-section after this step is shown in Figure A.1 (b).

**14. Clean the wafers.**

**15. Grow field oxide (wet oxidation).**
The target thickness is ~6500 Å. It is done in three steps consisting of a dry oxidation T=950°C, TIME=10 min. followed by a wet oxidation, T=950°C, TIME=250 min., and finished with another dry oxidation, T=950°C, TIME=10 min. The two dry oxidations are intended to grow a better quality oxide at the surface of the silicon and a more dense oxide (to better resist etching) at the surface of the field oxide.

**16. Wet-etch LPCVD nitride.**
The nitride over the active regions is etched using a selective nitride wet etching solution that does not etch the field oxide.

**17. Wet-etch stress relief oxide.**
The stress relief oxide that remains over the active regions is removed. The cross-section after this step is shown in Figure A.1 (c).

**18. Clean the wafers.**

**19. Grow sacrificial oxide (wet oxidation).**
The sacrificial wet oxide is grown with a target thickness ~600 Å at T=900°C, TIME=25 min. This is done for the purpose of oxidizing-out any damage that the surface silicon may have incurred during processing. Further, this step removes any potential nitride polymer left over at the edges of the field oxide following the nitride RIE.

**20. Etch the sacrificial oxide.**

**21. Clean the wafers.**

**22. Grow gate oxide (dry oxidation).**
The gate oxide is grown at T=900°C, TIME=55 minutes in 90% O$_2$ and 10% HCl ambient. The O$_2$ and HCl gas mixture is allowed to flow in the furnace for 15 minutes before putting in the wafers in order to stabilize the gas flow. Following this procedure will result in grow oxide films with thicknesses close to the process simulations.
23. Implant phosphorus (energy $E = 40$ keV, dose $Q_I = 7.0 \times 10^{11}$ cm$^{-2}$).
Blanket threshold voltage adjustment. The cross-section during this step is shown in Figure A.1 (d).

24. Clean the wafers.

25. Deposit LPCVD amorphous silicon (gate).
The target thickness is 3000 Å. The amorphous silicon is intended to prevent the deep penetration of boron gate dopants close to the gate-oxide interface. The gate converted to a polycrystalline silicon after deposition of nitride (which is done at 800°C).

26. Implant boron (energy $E = 25$ keV, dose $Q_I = 5.0 \times 10^{15}$ cm$^{-2}$).
This ion implantation is used to dope the p$^+$ poly gate. The cross-section during this step is shown in Figure A.1 (e).

27. Clean the wafers.

28. Deposit LPCVD nitride.
The target thickness is 1800 Å. The nitride is intended to block the BF$_2$ source/drain implant dopants from entering the gate.

29. Remove the nitride and polysilicon layers from the back of the wafers.
This step is required in order to prepare the wafers for RTA (Rapid Thermal Anneal). All the RTA processes are done with the Heatpulse$^\text{TM}$ 410 rapid thermal processor. The monitoring of the temperature (above 800°C) is done with a pyrometer whose readings are dependent on wafer backside emissivity. The pyrometer is set to detect the emissivity of bare silicon on the back of the wafer. Since, during an LPCVD process, material is deposited on both the front and back of the wafer, care must be taken that all deposited materials are removed from the back before RTA.

A coat of photoresist must be spread on top of the wafer in order to protect the nitride when etching the back, but since photoresist on bare nitride is stripped by the nitride etch solution, the nitride on the back is removed using RIE which can only remove material on one side of a wafer at a time. The polysilicon on the back is removed with a wet polysilicon etch which does not etch nitride.

30. Clean the wafers.

31. RTA.
The wafers are annealed at 850°C for 1 min. This is done to simulate the poly-poly capacitor oxide densification of an experimental process under research at the University of Toronto. This RTA also helps to densify the nitride blocker.

32. Pattern the nitride-poly gate stack with photolithography process (mask #2 GATE).
This photolithography step patterns the nitride-poly gate stack.
33. RIE of undesired areas of LPCVD nitride.
In this step, a nitride blocker pattern is formed using reactive ion etch (RIE) and the reactive ion etch stopped after all unpatterned nitride is etched.

34. RIE of undesired areas of LPCVD polysilicon.
The polysilicon gate is formed in this step.

**RIE polysilicon etch recipe:** A specified poly etching recipe was followed. It consisted of 75% Cl2 flow (Cl2 flow rate of 64.5 sccm is used), throttle pressure=45 mTr, power=45%. The photoresist used to pattern the gate is not removed after nitride etch. This is done in order to keep the poly etch from removing any nitride. The etch rate of p-type polysilicon measured in this study was approximately 1000 - 1100 Å/min.

35. Remove the photoresist.

36. Etch the undesired areas of the gate oxide
Any remaining gate oxide that was underneath the etched areas of poly is removed using reactive ion etch. The cross-section after this step is shown in Figure A.1 (f).

**RIE oxide etch recipe:** 50% CHF3 (freon-23) - 50% C2F6 (freon-116) flow (CHF3 flow rate of 25 sccm and C2F6 flow rate of 12 sccm are used), throttle pressure=95 mTr, power=60%. The 50% flow for both gases is specified in the process program. The actual nominal values for the flow rates given above are calculated using the gas correction factors from the gas flow conversion chart in the manual for this equipment. The etch rate of the LPCVD oxide is approximately 1000 Å/min.

37. Clean the wafers.

38. Re-oxidizing RTA.
This step is used to fix any damage between the poly gate and the gate oxide around the periphery of the gate structure. Since reactive ion etching may cause oxide damage at the edges of the gate, an RTA at T=900°C, TIME=1 min. in O2 ambient is used to grow more oxide around any potential damage in that area.

39. Clean the wafers

40. Deposit thin LPCVD nitride
The target thickness is ~ 200 Å. This oxide is used as a screen layer during the subsequent source/drain and n-well contact implantations.

41. Pattern windows for BF2 implantation with photolithography process (mask #3, PJUNC).
This photolithography process is used to open windows in the photoresist through which the p+ source/drain junctions are implanted.

42. Implant BF2 (energy E = 80 keV, dose Qf = 1.0×10^16 cm^-2).
This implant is intended to form the source/drain junctions. The cross section during this step is shown in Figure A.1 (g).

43. Remove photoresist.

44. Clean the wafers.

45. Pattern windows for phosphorus implantation with photolithography process (mask #4, NJUNC).
This photolithography process is used to open windows in the photoresist through which the n⁺ n-well contact junctions are implanted.

46. Implant phosphorus (energy E = 70 keV, dose Q₁ = 5.0×10¹⁵ cm⁻²).
This implant is intended to form the n⁺ n-well contact junctions. The cross-section during this step is shown in Figure A.1 (h).

47. Remove photoresist.

48. Etch the LPCVD nitride.
The nitride blocker and the implant screen nitride are removed in selective nitride wet etch solution.

49. Clean the wafers.

50. Deposit LPCVD oxide
The target oxide thickness is ~ 6000 Å. This oxide is the isolation layer between the devices and the metal layer. The cross section during this step is shown in Figure A.1 (i).

51. Etch oxide off the back of the wafer
The LPCVD oxide is etched off the back of the wafer before the densification RTA.

52. Clean the wafers.

53. RTA.
In order to activate and re-distribute the dopants in the gate, threshold adjust, source/drain and well contacts an RTA of T = 1100°C, TIME = 20 seconds in N₂ ambient is applied. The anneal has the secondary role of densifying the oxide used for SWS formation.

54. Pattern the contact windows before metal deposition with photolithography process (mask #5, CON).
This photolithography process defines the metal contact opening windows.

55. Etch oxide to define contact windows.
The cross-section after this step is shown in Figure A.1 (j).

56. Remove the photoresist

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57. Clean the wafers.

58. Sputter TiW.
TiW is used as a barrier material which prevents the spiking of Al into and through the p⁺ source/drain junctions. The target thickness is ~ 1000 Å.

59. Sputter Al.
Al is used to form the metallization interconnects and contacts. The target thickness is ~ 8000 Å.

60. Pattern the aluminum with photolithography process (mask #6, MET).

61. Etch the aluminum.
The etch solution used in this step is H₃PO₄ (Phosphoric Acid):HNO₃ (Nitric Acid):CH₃COOH (Acetic Acid):DI Water = 25:1:5:1.67 (by volume). The temperature of the solution is sustained at 45°C during the process.

62. Remove the photoresist

63. Etch the TiW.
Al acts as the mast in the etching of the TiW. The etchant used is HNO₃ (Nitric Acid). The temperature of the solution is sustained at 45°C during the process.

64. Anneal the wafers.
Metal sintering is done in this step at T=450°C, TIME=20 min. The cross-section after this step is shown in Figure A.1 (k).

[Diagram of Phosphorus Implant (n-well doping)]
Appendix A. Low Voltage PMOS Fabrication Process Description

Mask #1 (FOX)

- silicon-nitride
- stress relief oxide

(b)

Field oxide

(c)

Phosphorus Implant (threshold voltage adjustment)

(d)
Boron Implant
(doping the gate)

amorphous silicon
gate

Boron Implant (doping the gate)

nitride blocker

gate oxide

nitride blocker

gate oxide

Mask #2 (PPOLY)

Mask #3 (PJUNC) BF₂ Implant (p⁺ source/drain junctions)

screen nitride

gate oxide

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Mask #4 (NJUNC) Phosphorus Implant (n⁺ well contact)

screen nitride

n-well

p-substrate

(h)

LPCVD oxide

n⁺ p⁺ p⁺

n-well

p-substrate

(i)
Figure A.1: Cross-sectional diagrams of the low-voltage PMOS process.
APPENDIX B

DEVICE LAYOUT SPECIFICATIONS

The minimum photolithography resolution for the experimental fabrication process is 3 μm. The mask layers used in layout design are summarized in Table B.1.

Table B.1: Mask Layers for the Chip Design

<table>
<thead>
<tr>
<th>Mask #</th>
<th>Layer Name</th>
<th>Description</th>
<th>Alignment with respect to mask #</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>FOX</td>
<td>Device active area</td>
<td>-</td>
</tr>
<tr>
<td>2</td>
<td>PPOLY</td>
<td>p⁺ poly gate delineation</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>PJUNC</td>
<td>p⁺ doped source/drain</td>
<td>1</td>
</tr>
<tr>
<td>4</td>
<td>NJUNC</td>
<td>n⁺ doped contact to substrate</td>
<td>1</td>
</tr>
<tr>
<td>5</td>
<td>CON</td>
<td>Metal to diffusion or poly contacts</td>
<td>2</td>
</tr>
<tr>
<td>6</td>
<td>MET</td>
<td>Metal interconnects</td>
<td>5</td>
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</tbody>
</table>

The layout design rules are based on the minimum feature size (3 μm) and mask alignment tolerance (3 μm) which are imposed by the Karl Suss MJB3 mask aligner. The layout design rules for the low voltage PMOS devices are illustrated in Figure B.1 and summarized in Table B.2.
Figure B.1: Layout design rules for a low voltage PMOS transistor.

Table B.2: Layout Design Rules for Low Voltage PMOS Transistor

<table>
<thead>
<tr>
<th>Layer</th>
<th>Rule #</th>
<th>Description</th>
<th>Dimensions (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>FOX</td>
<td>1.1</td>
<td>Minimum width of device active areas</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>1.2</td>
<td>Minimum length of device active areas</td>
<td>23</td>
</tr>
<tr>
<td></td>
<td>1.3</td>
<td>Minimum dimensions of the openings for n⁺ implantation for contacts to the substrate</td>
<td>40x40</td>
</tr>
<tr>
<td>PPOLY</td>
<td>2.1</td>
<td>Minimum length</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>2.2</td>
<td>Minimum PPOLY overlap of FOX</td>
<td>4</td>
</tr>
<tr>
<td>PJUNC</td>
<td>3.1</td>
<td>PJUNC must cover the device active areas</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>3.2</td>
<td>PJUNC minimum overlap of FOX</td>
<td>4</td>
</tr>
</tbody>
</table>
Table B.2: Layout Design Rules for Low Voltage PMOS Transistor

<table>
<thead>
<tr>
<th>Layer</th>
<th>Rule #</th>
<th>Description</th>
<th>Dimensions (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NJUNC</td>
<td>4.1</td>
<td>NJUNC must cover the openings for n⁺ implantation for contacts to the substrate</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>4.2</td>
<td>NJUNC minimum overlap of FOX</td>
<td>4</td>
</tr>
<tr>
<td>CON</td>
<td>5.1</td>
<td>CON must be over a conducting layer (PPOLY, PJUNC, NJUNC)</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>5.2</td>
<td>Minimum CON dimensions</td>
<td>4x4</td>
</tr>
<tr>
<td></td>
<td>5.3</td>
<td>Minimum PPOLY overlap of CON</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>5.4</td>
<td>Minimum PPOLY clearance of CON</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>5.5</td>
<td>Minimum FOX clearance of CON</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>5.6</td>
<td>Minimum GATE CON clearance to FOX</td>
<td>7</td>
</tr>
<tr>
<td>MET1</td>
<td>6.1</td>
<td>Minimum Width</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>6.2</td>
<td>Minimum Spacing</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>6.3</td>
<td>MET1 overlap of CON</td>
<td>3</td>
</tr>
</tbody>
</table>