Emitter-Up Heterojunction Bipolar Transistor 
Compatible Laser

by

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A thesis submitted in conformity with the requirements 
for the degree of Master of Applied Science 
Graduate Department of Electrical and Computer Engineering 
University of Toronto

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Abstract

A novel integration technique, one which utilizes a common epitaxial layer structure to achieve dual functional devices, is investigated. In particular, this work focuses on the possibilities of integrating a single quantum well laser and a npn-heterojunction bipolar transistor (HBT) in this fashion. Due to the inherent structural and operational differences between the laser and HBT, compatibility issues are presented and discussed with the aid of a numerical model. An emitter-up HBT compatible laser, that retains many prominent HBT features, is proposed. Numerical simulations show that the laser performance (i.e. ~20 mA threshold and 44% efficiency) are comparable to typical lasers. The proposed laser was fabricated along with all of the necessary post-growth processing. The first experimental trial resulted in lasers with lasing threshold characteristics at ~30 mA.
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Chapter 1

Laser-Transistor Integration

1.1 Introduction

Optoelectronic integrated circuits (OEICs), which is the compilation of photonic devices and electronic devices, is seen as a vital building block or foundation for next generation's technologies. The ability to combine optical and electronic devices on a common semi-insulating substrate opens up the potential for greater functionality at lower costs. This is regarded as the significant advantage over its hybrid counterparts wherein discrete devices are interconnected via external means (i.e. wire bonds).

Electronics underwent long ago an evolution of great success from individual discrete devices to integrated circuits. New applications and functionalities enjoyed by
today's society would not be possible were it not for the considerable efforts which went into understanding and perfecting the integration process. This is the evolution which is now slowly beginning to take place in optoelectronic devices.

Already, in the field of optical telecommunications the advantages of integrated receivers, which are comprised of integrated transistors and photodetectors, have successfully been demonstrated [1]. However, attempts at integrating a laser with its driving transistor, the components which form the transmitter of a fiber optic communication network, have been far from successful. Proposed integrated transmitters which do have respectable performance attributes have had to go through undesirable, highly complex fabrication processes, while those devices which are relatively simple to fabricate have unattractive performance characteristics. The inherent advantages of these integrated devices have yet to outshine their hybrid competitors.

1.2 Laser-Transistor Integration Techniques

While the idea of integrating a laser and a transistor has drawn research attention from the scientific community and industry for at least the past decade, nearly all the different attempts fall into two simple, brute force approaches: selective area growth/regrowth; and vertical integration.

1.2.1 Selective Area Growth/Regrowth

The concept of this technique is implicit in its name; desired devices are grown or regrown only in desired locations. Many proposed integrated laser-transistor devices adopted this technique [2-6] in which the substrate is masked leaving openings where one type of device
is grown. Then a second mask would cover the first device while exposing the area on the substrate where the second type of device would be grown. This description is for selective area growth. In selective area regrowth, the layers for the first type of device is grown on the complete wafer followed by a dry or wet etch to define the device structure. The material layers for the second type of device is then grown in masked areas.

One advantage of selective area growth/regrowth is the inherent opportunity to optimize the layer structures of each type of device independently since they are grown during different growth runs and the integration is purely mechanical. A general pictorial of the resultant integration of a single quantum well (QW) laser and a heterojunction bipolar transistor (HBT) using selective area growth/regrowth is shown in Fig. 1-1.

![QW Laser Diagram](image)

Fig. 1-1. Integrated QW laser-HBT via selective area growth/regrowth.

The biggest drawback with this technique, which is regarded as a brute force approach to integration, lies in the demands in a sequence of stringent processing steps. The technological processing complexities reduce the yield, the reliability, and ultimately
increase the cost of fabricating an integrated device.

Another major disadvantage is the thermal cycling effects which occur in growing the second type of device. The high temperatures necessary to grow the second type of devices may affect and alter the layer composition and layer doping of the already grown device.

1.2.2 Vertical Integration

The second major approach at integrating a laser and a HBT is vertical integration [7-11]. Again, as the name suggests, this method involves the growth of one type of device on top of the other type of device. A diagram depicting a vertically integrated QW laser and HBT is shown in Fig. 1-2.

![Diagram of vertically integrated QW laser and HBT](image)

**Fig. 1-2.** Integrated QW laser-HBT via vertical integration.

In this case, the laser is grown first followed by an thick isolating layer. The transistor is then grown stacked on top of the isolating layer. A distributed capacitance results due to the accumulation of charges on either side of the isolating layer [12]. This is
detrimental for the speed performance of the transistor and the laser. Also, vertical integration produces an integrated device which is not planar in nature. It is known that planar integration produces highly reliable, high yielding devices.

1.3 Motivation: Common Layer Bipolar-Laser-Transistor-Structure

It can be generalized that those integrated devices which do have respectable performance attributes have so far required highly complex fabrication processes while those devices which are relatively simple to fabricate have unattractive performance characteristics. All these integration attempts are rooted in the incompatibility of the internal structures of the lasing device and the transistor, and the fact that existing approaches all attempt to bring these structures mechanically together as they are. Therefore, a simple to fabricate monolithically integrated laser-transistor, with minimum compromises to individual device performances, can be expected to significantly advance the development of OEICs and realize its full potentials.

One approach to the laser-transistor integration could be to devise a structure which can provide both laser and transistor functions. Only a single epitaxial growth would be required since a common material layer structure is used and it is planar by definition. Thus, the fabrication process is greatly simplified leading to increasing reliability, repeatability, and yield. Also, the demands in packaging are reduced when compared to hybrid solutions lending itself to the potential of providing lower cost solutions. This new class of device, by making use of a common contact (i.e. n-contact of laser is also used as the collector contact of transistor) as shown in Figure 1-3, also eliminates some or all of the
wire interconnects between the two components, which are commonly present in other integration techniques, between the laser and the transistor. This significant reduction of parasitics associated with wire bonds greatly increases the intrinsic speed limit of the integrated device.

The idea of fabricating a monolithically integrated laser-transistor on the same epitaxial layer attracted more than just our attention. Two independent proposals appeared at Photonics West'97 [13, 14]. Although the device performances obtained in their work did not compare to the state-of-the-art integrated laser-HBT devices fabricated by other integration techniques, the experimental results did show that the idea was feasible and could be used as a stepping stone to further improvements. However, the ultimate device performances achievable using this idea of a common epitaxial layer structure are still unknown. The underlying device physics of the new structures in either of the operational modes remains unclear. The unique device operation is the main motivation behind the work presented in this thesis.
The common layer structure strategy necessarily imposes more constrains in the design, and the experimental conditions required to achieve optimal performances in both laser and transistor functions are more stringent than that for the individual functions. This work explores this new integration approach first from a theoretical angle, which is believed to be the first on this subject, instead of the commonly used empirical trial-and-error approach presently taken by the other groups. By understanding the underlying internal physical mechanisms responsible for the operation of this type of integrated device, one can begin to realize its individual and integrated device performance possibilities. Informed by the theoretical analysis, a new structural design that minimizes the compromises to the individual laser and transistor performances will be proposed and experimentally explored.

1.4 Organization of Thesis

The objective of this thesis is to understand the device operations of existing integrated laser-transistor devices and to explore possible improvements and/or new device concepts. Then, as a demonstration of the utility of the obtained insights and understanding, a new structural design will be presented.

In Chapter 2, typical structural characteristics for a single QW laser and a npn-HBT will be presented. Following the usual design rules for the laser and HBT, one can argue that the devices cannot be and should not be achieved using a common layer structure. In this section, we will discuss the compatibility issues involved if these two devices were to be integrated using a common epitaxial layer structure. Also, a detailed analysis of an issue which is only apparent when designing a layer configuration which can be used as both a
laser and a transistor is presented with the aid of numerical simulations. More specifically, the placement of the p-contact when transforming a npn-HBT layer configuration into a laser configuration will be discussed.

To investigate further the compatibility issues presented in the previous chapter, Chapter 3 will present analysis on issues such as the effect of inserting a quantum well on HBT performance, the effect of inserting a displaced p-n junction layer on the HBT, and the effect of having a heavily doped base layer in the active region of the laser. These issues will be studied on a proposed layer structure. The novelty of our proposed structure is the improved compatibility with the HBT accomplished by retaining many of the high speed characteristics of the transistor. Results from numerical simulations for both the laser and transistor are analyzed and discussed.

Chapter 4 describes the processing steps involved in the fabrication of the emitter-up HBT compatible laser presented in the previous chapter. A detailed processing procedure followed will be presented along with the difficulties and problems encountered in our fabrication. Results from experimental testing of the laser will be discussed and analyzed.

Finally, Chapter 5 will summarize the findings and the significant contributions of this thesis. Also, ideas for future work in this direction will be presented.
Chapter 2

HBT Compatible Laser Design Issues

The design of a quantum well laser and a heterojunction bipolar transistor follow different criteria due to their inherent differences in desired device functionalities. The design of transistor mainly concerns itself with carrier dynamics and minimizing charge storage, whereas for the laser the optical aspects are equally as important as the maximizing of carrier confinement. Thus, structural differences in the design of a laser and a transistor are required. Material compositions, layer thicknesses, and doping profiles are just a few of the design parameters which could be altered to make a device perform their desired tasks.

In this chapter, a general description of the layer configurations for typical QW lasers and HBTs are presented. Then, with the intent to design a common layer
configuration to provide both lasing and transistor action, compatibility issues will be discussed. Many of these compatibility issues such as the necessary level of doping in the base region of the HBT and its effect on the laser, the effect of placing a QW in the HBT, and the layer thicknesses required to provide optical confinement for the laser but also affordable by high speed transistors will be investigated. However, these issues are not exclusively unique to the design of an integrated laser-transistor using a common epitaxial layer as they have, in some form or another, been studied as issues when designing individual devices. These compatibility issues will be dealt in depth in Chapter 3 using a specific layer design. This chapter will focus on the different options available, in particular the placement of the p-contact, in transforming a HBT layer structure into a laser structure. This issue is unique to this particular integration approach.

2.1 Typical Structures

The methodology used in the design of a typical laser structure is very different than the one used when designing a typical HBT. The following discussion will give general design rules for a typical single QW laser and a npn-HBT.

2.1.1 Single QW Laser

There are many variations in designing a laser such as the use of graded layers, delta-dopings, and multiple strain compensated quantum wells just to name a few. However, only a basic description of a typical laser will be given here emphasizing the attributes commonly present in most lasers.

A single QW laser structure is sketched in Fig. 2-1(a) indicating the typical layer
Fig. 2-1. Typical single QW laser (a) layer structure and (b) material bandgap characteristics. Higher doping concentrations represented by darker shadings.

dimensions, the placement of the quantum well with respect to the p-n junction, and the doping concentrations. As shown, the quantum well is usually placed in the center of the device with layers consisting of progressively increasing bandgap materials extending from either side as shown in Fig. 2-1(b). In other words, the quantum well is comprised of the lowest bandgap material, the immediate layers surrounding the quantum well (the barrier) is of higher bandgap material, and then thick cladding layers of the highest bandgap material are used. Contact layers, which are usually low bandgap material to allow for the formation of ohmic contacts, form the outer layers.

As a result of the layer configuration, the electrons and holes injected in from their respective contacts will meet and accumulate at the quantum well where they recombine by the stimulated process. Ideally, the optical mode is peaked in the quantum well since
higher refractive indexes are associated with lower bandgaps. However, a more important consideration is the percentage of the optical mode that overlaps with the gain region. The cladding layers are made sufficiently thick (> 1 μm) to ensure that the optical mode tail is ideally zero at the metal contacts due to the highly absorbing nature of metal.

The doping concentration profiles start with heavily doped contact layers to ensure good ohmic contacts, reducing to typical values in the $10^{17}$ cm$^{-3}$ range for the cladding layers, and finally to undoped quantum well and barrier layers. This doping profile is opposite to the optical mode profile in that where the optical mode is strongest, the doping is the weakest. This reduces the amount of free carrier absorption and is another reason why the cladding layers are intentionally made thick.

2.1.2 npn-HBT

For a high speed npn-HBT, the device dimensions are generally small when compared to those of a laser. A typical npn-HBT device structure is shown in Fig. 2-2(a) with the accompanying material bandgap characteristics shown in Fig. 2-2(b).

The base layer is usually the most heavily doped layer in the transistor. Concentrations of p-type doping are usually greater than $10^{19}$ cm$^{-3}$ to reduce the base resistance. A reduced base resistance increases the maximum oscillation frequency, $f_{\text{max}}$. The definition of $f_{\text{max}}$ and other figures of merit to judge the performance of a transistor are given in Appendix 2. The base layer is also the thinnest layer in the device to reduce the electron transit time from the emitter-base junction to the base-collector junction, thus increasing the cutoff frequency $f_T$. 
Fig. 2-2. Typical npn-HBT (a) layer structure and (b) material bandgap characteristics. Higher doping concentrations represented by darker shadings.

The emitter layer is moderately n-doped with a larger bandgap material than that used for the base layer. A valence band offset is created at the base-emitter junction to discourage the flow of holes from the base to the emitter thus increasing the emitter injection efficiency and the current gain of the transistor. The emitter region is still capped off with a heavily doped lower bandgap material to enable the formation of ohmic contacts.

The collector layer is usually the thickest of the three regions ranging from less than a half of a micron to almost 1 μm and it is the lightest doped layer in the $5 \times 10^{16} \text{ cm}^{-3}$ range. The material used for the collector can either be of low bandgap material like the base layer or a higher bandgap material similar to the one used for the emitter layers as shown in Fig. 2-2(b) by the dashed lines. With a heterojunction at the emitter-base and at the base-
collector interface, a double heterojunction bipolar transistor (DHBT) is created. One example where a double heterojunction formation is employed is in the design of a symmetric transistor. A symmetric transistor is one in which the common layer structure can be configured either emitter-up or collector-up. For either a single heterojunction or a double heterojunction transistor, the collector layer still requires a low bandgap contact layer.

### 2.2 Compatibility Issues

As seen in the previous sections, the design of a typical single QW laser and a typical npn-HBT are very different. However, they do have some intrinsic features in common: they are both bipolar devices and operate in quasi neutral regime. Thus, it seems reasonable to ask if alterations to the laser and/or HBT layer structures could possibly create a compatible layer configuration. Exploring this possibility is the motivation of this work. A study of compatibility issues and the feasibility of creating a dual functional device from a common layer structure has not existed in the literature other than the two isolated empirical trials cited before [13, 14].

Typically for a high speed HBT a single heterojunction is used at the emitter-base junction. A double heterojunction is necessary in the formation of a laser to provide both electronic confinement for both types of carriers and optical confinement. Fortunately, when the additional heterojunction is placed at the collector-base junction of the transistor, reported experimental devices have shown that transistor performance does not degrade due to this additional barrier. In fact, it has been shown that the DHBT configuration improves the turn-on voltage [15, 16].
Intuitively, the placement of the quantum well should be in the base region, and it is expected to influence the performance of the HBT significantly. On one hand, the quantum well could trap minority carriers (i.e. electrons), but on the other hand, the quantum well could reduce the base resistance. After considering the other constraints from the laser and the HBT, in particular the placement of the heavily p-doped base layer with respect to the p-n junction of the laser structure, there are three locations in the HBT where the quantum well could be placed: at the emitter-base junction; at the collector-base junction; and deep within the collector region. The effect of placing a quantum well at the collector-base junction will be investigated in Section 3.2.1.

Other compatibility issues include the use of thin layers for higher speed HBTs, versus the thick cladding layers needed in lasers to provide good optical confinement. This will be addressed in Chapter 3 with reference to our layer structure design.

2.3 P-Contact Placement Study

Generally speaking, the common layer strategy imposes more constraints on the design of the integrated device, and the experimental conditions required to achieve optimal performances in both laser and transistor functions are more stringent than if they were designed individually. Issues that may have been deemed trivial when designing the laser and transistor separately, must now be re-examined to determine their impacts on a HBT compatible laser. One example is the placement of the laser contacts. In this section, a study of the effects of contact location on laser performance is conducted in an attempt to understand the underlying mechanisms contributing to the disparities found in literature.
2.3.1 Impacts by Inspection

Although a similar strategy was employed for the growth of the devices where the laser was created through the modification of the as-grown HBT layer structure, the experimental results for the structure reported in [13] and in [14] are dramatically different. The threshold current reported in [14] was 19 mA with a differential efficiency of 0.20 mW/ mA, while a threshold current of greater than 300 mA with a differential efficiency of 0.05 mW/mA was reported in [13]. Clearly, the discrepancies in the laser characteristics extend beyond the fact that the structure reported in [14] was constructed of eight strain compensated InGaAsP quantum wells while the structure reported in [13] had only one InGaAs quantum well. The quantum wells were placed in similar locations (i.e. in the collector) with respect to the HBT layer structure. One difference was the configuration of the p-contact for the laser, but it is not obvious at all that this is the reason since both use thick cladding layers to confine the optical mode, and both employ heterobarriers above and below the active quantum wells confining the carriers as in a conventional double heterojunction laser.

2.3.2 Impacts, Assessments, and Underlying Physics

Using a self-consistent finite-element model, FELES (Finite-Element-Light-Emitter-Simulator) [17], the internal operation of one representative HBT compatible laser reported in [13] is examined. More details for the FELES model are found in Appendix 1.

To form a laser, a single step epitaxial growth process with the layers grown to suit a HBT device can be used. To transform the transistor structure into a laser, normal mesa etching and contact formation are necessary steps. Depending on where the p-contact is
placed, additional steps may be necessary before metallization. Three possibilities of forming a laser device from the grown HBT layer structure are investigated as shown in Fig. 2-3. One obvious case, which can easily be transformed into a laser given the presence of a highly doped p-type base layer, is to place the p-contact directly on the base layer (BASE case), similar to what was done to the structure reported in [13].

![Diagrams showing three possibilities for forming a laser device](image_url)

Fig. 2-3. Investigated p-contact placement possibilities (a) EMITTER case, (b) BASE case, and (c) BASE-IMP case.

A variation to this idea proposed in [13] would be to ion implant the quantum well and collector regions below the p-contacted base layer (BASE-IMP case). Intuitively, this would create a funnelling effect of carriers towards the center of the device providing for an improved material gain overlap with the fundamental optical mode. In modeling, we have chosen to idealize the proton implantation and subsequent annealing (used to retrieve the base conductivity) by: reducing the carrier mobilities in the implanted regions to minimum values; assuming the implantation was uniform with no modifications in carrier lifetimes;
and leaving the base layer underneath the contacts unaffected. Also, the refractive indices of the different material layers are assumed unchanged. These approximations (or idealizations) may be over simplifications, however, it was found that modifications to them do not affect qualitatively the findings reported hereafter as they will become clear later.

The third case studied was used in the structure reported in [14] where a doping type-conversion process is employed to convert the n-doped emitter layers to p-type facilitating the formation of the p-contact on top of the ‘emitter’ ridge as in a typical laser (EMITTER case).

The material compositions and layer dimensions are shown in Fig. 2-4 with the
type converted from n-type to p-type. However, to isolate the effect of the contact placement on laser performance, the emitter layers have been assumed to be p-type. The fundamental optical mode shape is identical for all three cases. A cavity length of 600 μm with cleaved facets and a ridge width of 2 μm were used in the modeling.

2.3.3 Simulation Results for p-Contact Placement Cases

Results from the modeling show that there is a substantial difference in laser performance depending on the method used in converting a HBT material layer structure into a laser. From the single facet output light power versus injection current shown in Fig. 2-5, the threshold current is many times greater if the p-contact is placed on the base layer of the HBT (BASE case) as opposed to when the HBT emitter layers are converted to p-type and placed atop the emitter ridge (EMITTER case). Also the differential efficiency of the BASE case laser is lower with roll-off starting at approximately twice the threshold current.

![Fig. 2-5](image-url)
A larger threshold current for the BASE case is understandable upon a close inspection of the configuration and locations of the contacts. A direct transverse current path running on either side of the laser from the n-contact to the p-contacts exists as shown in Fig. 2-6. Unfortunately, the optical mode is peaked in the center of the ridge and thus

Fig. 2-6. Transverse electron current density for (a) EMITTER case and (b) BASE case. The shaded area outlines the device structure.
results in a poor optical mode-gain overlap. Worse yet, it was found that this current, of holes and electrons, could travel from contact to contact directly without radiatively (or even nonradiatively) recombining. From Fig. 2-7, which quantifies the current components

![Figure 2-7](image)

Fig. 2-7. Current components for (a) EMITTER case and (b) BASE case. The contribution of electron current for the emitter layer contact case is insignificant.

of both carrier types as well as the total current at the p-contact, it is observed that the majority of the current is from the flow of electrons into the contact. The EMITTER case resembles a typical laser whereby the current at the p-contact is almost only due to the flow of holes with a near zero contribution from the electrons. This strongly suggests the lack of effective electron confinement. The current components at the n-contact were also investigated for both cases and was found to have only electron current components suggesting that the hole confinement for both cases are adequate.

For the BASE case, since the majority of the current or leakage current passes on either side of the laser, one would suspect a greater accumulation of carriers away from the middle of the device. The distribution of electrons along the quantum well is shown in Fig.
2-8. As the bias is increased, the concentration of electrons away from the center of the device grows much faster for the BASE case than the EMITTER case. A similar trend is seen in the distribution of holes. With a large concentration of electrons and holes in the BASE case, the material gain away from the center of the laser is large. However, due to the rapidly decaying nature of the fundamental optical mode, the carriers on the side cannot contribute greatly to lasing. Thus, the carriers recombine nonradiatively, dramatically reducing the differential efficiency.

To remedy the problem of the high leakage currents intuitively expected, the authors of [7], placed the p-contacts on the base layer, proposed to implant protons underneath the contact regions (BASE-IMP case). This would increase the resistivity on the sides of the laser and force the holes to travel laterally then transversely (vice versa for electrons) down the middle of the device. However, from the results presented above we know that in the unimplanted BASE case it is the electron confinement that is not effective.

Fig. 2-8. Lateral electron density profile, for increasing bias, along the quantum well for (a) EMITTER case and (b) BASE case.
An electron distribution profile along the QW, shown in Fig. 2-9, demonstrates the effectiveness of implantation. At low currents, the implantation does help to confine the electrons to the center of the QW. A similar situation occurs for the holes, thus greatly reducing the threshold current via an improved material gain overlap with the optical mode. However, as currents increase beyond the threshold (e.g. 155 mA), the BASE-IMP case starts to resemble the situation observed with the BASE case as there is an increased accumulation of electrons and holes away from the center of the laser suggesting that the electron confinement is again the source of the problem. A plot of the percentage of injected current at the p-contact comprised of electron leakage current is shown in Fig. 2-10 indeed showing the electron leakage still accounts for over 50% and more at higher biases. A reduction of leakage current for the BASE-IMP case demonstrates the effectiveness of the implantation. However, one can also conclude that the electron confinement, in particular the graded GaAs-Al$_{0.3}$Ga$_{0.7}$As layer between the p-contact and
Fig. 2-10. Percentage of electron leakage current of the total injected current for (a) BASE case and (b) BASE-IMP case.

the QW which was inserted by the authors of [13] for this very purpose, is not effective enough. The authors did note that this additional graded layer would hinder the performance of the HBT; and thus replacing the graded layer with a larger barrier layer is not an option.

Unlike the positive effect implantation had on reducing the threshold current, the differential efficiency suffered. With an implantation, the mobility of carriers are dramatically reduced resulting in a 'trap' like region for carriers. Not only is there accumulation of electrons, holes are also trapped due to the tendency toward charge neutrality. A transverse cross-section through the implanted region (cross-section I as depicted in Fig. 2-4) is shown in Fig. 2-11 depicting the distribution of holes. A higher hole concentration is observed for the BASE-IMP case with the disparities becoming greater for higher currents. The difficulty of carriers escaping this region once they have entered due
to their low mobilities makes them perfect candidates to recombine via a variety of nonradiative processes. Fig. 2-12 examines what proportion nonradiative recombination accounts for the total injected current. Not surprisingly, the nonradiative recombination

![Graph](graph1.png)

**Fig. 2-11.** Transverse hole density profile, for increasing injection current, along cross-section I for (a) BASE case and (b) BASE-IMP case.

![Graph](graph2.png)

**Fig. 2-12.** Total current (solid line) and recombination current in the implanted layers (dashed line) for (a) BASE case and (b) BASE-IMP case.
current of the BASE-IMP laser accounts for a greater portion of the total current than in the BASE case. This can explain the observed lower differential efficiency for the BASE-IMP laser. The superlinear behaviour of the nonradiative recombination current, in particular the nonlinear dependence of spontaneous and Auger recombination current on carrier concentration, is the dominant factor which is governing the rapid roll-off of differential efficiency observed for both the BASE and BASE-IMP cases. Roll-off occurs earlier for the BASE-IMP case due to the greater rate of accumulation of carriers at a lower injection current as observed previously in Fig. 2-11.

Although intuition may lead us to believe that the performance of the laser would be improved with the assistance of implantation, from our physical modeling of the EMITTER, BASE, and BASE-IMP lasers, this expectation is more of wishful thinking. The threshold current did improve from the BASE to BASE-IMP case. However, an even lower threshold was observed for the EMITTER case. As a consequence of the presence of leakage current in the BASE-IMP laser, for a given current injection, the concentration of electrons and holes in the quantum well is reduced thus resulting in a lower material gain. Therefore, a higher threshold current for the BASE-IMP laser than in the EMITTER is not unexpected. The large disparities of differential efficiency between the BASE-IMP and EMITTER laser has been discussed already when comparisons to the BASE laser were made.

As evident from the reported results of a 300 mA threshold [13], the implantation process and subsequent annealing to restore the conductivity of the p-contact layer is difficult to optimize. The authors attribute their observed high threshold current to leakage current caused by their unoptimized processing of the laser structure. However, from our
understanding of the mechanisms governing this device operations, it is clear that even with an idealized post-processing procedure assumed in our modeling, the performance of the laser is intrinsically inferior to the emitter case and even the unprocessed base case in terms of differential efficiency.

2.3.4 Summary of Findings for p-Contact Placement Study

The seemingly trivial issue of contact placement for a typical laser has been shown to have a large effect on the laser performance for an HBT compatible laser. Although by placing the p-contact directly on the p-type base layer simplifies the fabrication process, it is shown that the laser performance is much poorer when compared to a laser with the exact same structure but with the p-contact placed on the emitter. A proposal in the literature to improve the laser which has the p-contact directly placed on the p-type base layer by implementing a current funneling implantation was examined. We find that not only is it difficult to realize due to the complex effects of implantation and subsequent annealing, it is intrinsically unable to improve any other aspect of the laser performance other than the threshold.

2.4 Conclusion

From the simulation of practical structures, with an example discussed in Chapter 3, and from reported experimental results, the idea of designing a layer structure which affords the possibility of being dual functional has been shown to be feasible. The proposed device in [14] shows good performance (i.e. 19 mA threshold and 0.20 mW/mA differential efficiency) when compared to a typical laser that has its layers optimized to perform just as
a laser. Even with the proposed device in [13], merely moving the p-contact from the base layer to the emitter layer would reduce the threshold from 140 mA to 30 mA with a differential efficiency of 0.35 mW/mA. The performances are not yet at par with today’s lasers of conventional structure, however, one must bear in mind that the proposed structures have not benefited from years of countless design iterations that the conventional lasers have had.
Chapter 3

Emitter-Up HBT Compatible Laser

In this chapter, the design of an emitter-up HBT compatible laser will be undertaken. Using numerical simulations to aid in the design for both lasing and transistor action, a layer configuration is proposed. Compatibility issues such as the insertion of additional layers to accommodate the necessity of having a particular layer in either the laser or HBT (i.e. insertion of quantum well for the laser) or deviations from the typical laser or HBT structures will be investigated. The experimental implementation of the proposed design will be presented in Chapter 4.

3.1 Design

By considering the design and compatibility issues presented in the previous chapter, an
attempt to design a single quantum well laser and npn-HBT from a common epitaxial layer is undertaken. Through the understanding of the mechanisms responsible for the performance of each type of device, a layer configuration shown in Fig. 3-1 was determined.

![Layer configuration diagram](image)

<table>
<thead>
<tr>
<th>Layer Type</th>
<th>Thickness</th>
<th>Doping</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaAs</td>
<td>100 nm</td>
<td>p-7e18</td>
</tr>
<tr>
<td>Al$<em>{0.3}$Ga$</em>{0.7}$As</td>
<td>200 nm</td>
<td>p-4e17</td>
</tr>
<tr>
<td>GaAs</td>
<td>70 nm</td>
<td>p-5e18</td>
</tr>
<tr>
<td>In$<em>{0.2}$Ga$</em>{0.8}$As</td>
<td>70 nm</td>
<td>n-5e16</td>
</tr>
<tr>
<td>GaAs</td>
<td>500 nm</td>
<td>n-5e16</td>
</tr>
<tr>
<td>Al$<em>{0.3}$Ga$</em>{0.7}$As</td>
<td>100 nm</td>
<td>n-7e18</td>
</tr>
<tr>
<td>Al$<em>{0.4}$Ga$</em>{0.6}$As</td>
<td>1.5 µm</td>
<td></td>
</tr>
</tbody>
</table>

Fig. 3-1. Layer configuration for an emitter-up HBT compatible laser. Dopings written in italics are assumed values after type conversion.

by numerical simulations to possess good laser and transistor characteristics. The layers shown in Fig. 3-1 is the structure for the laser. The transistor structure has the exact same layer configuration except for the doping type of the top two layers. In the case of the laser, these two layers have already assumed to have been type converted from the as-grown n-type to a p-doping. While acknowledging that type conversion is not trivial at all, we have chosen for this study to focus on intrinsic device operations rather than the attributes or technical issues of generic processing steps that are commonly performed. In keeping with this philosophy, for our first trial implementation, a wafer would be grown with the proper
HBT layers but with the top two layers grown as it would have been had a type conversion process been performed. The main reasoning behind starting with a HBT structure instead of a laser lies in the critical dependence on precise doping profiles, not easily achievable by type conversion processes, on the operation of the transistor. Also, n-type to p-type conversion processes can compensate for higher concentrations of background dopants.

One of the unique features of our design, which makes it more compatible with the HBT than in the reported structures, is the preservation of short layer thicknesses, in particular the emitter layer, for higher speed transistor operation. The use of a very thin ridge with dimensions comparable to typical emitter layer thicknesses for high speed HBTs has been demonstrated to give rise to good lasing characteristics [18]. The ridge thickness for our design is only 300 nm.

The laser reported in [18] was grown on an n-type substrate with an arbitrarily thick lower cladding. Thus, the task of creating a good ohmic contact and providing optical confinement in the vertical direction is made simpler. Since the emitter-up HBT compatible laser is to be grown on semi-insulating material, the luxury of having a thick lower cladding layer that is to be shared with a high speed transistor is unavailable. Assuming a collector layer thickness of 500 nm, the distance from the low bandgap GaAs n-contact layer to the lower bandgap active region is not large enough to prevent the optical mode to be easily attracted away from the active region into the low bandgap GaAs n-contact layer underneath. One solution is to make the collector layer from a higher bandgap material, however, this will create a larger conduction band barrier for electrons trying to leave the base thus reducing the cutoff frequency. Another solution is to insert an electrically passive thick higher bandgap Al_{x}Ga_{1-x}As 'optical cladding layer' between the
n-contact layer and the GaAs substrate. As the concentration of Al is increased, the optical mode becomes better confined to the active region as shown in Fig. 3-2. A 40% Al concentration is chosen due to device processing considerations. \( \text{Al}_x\text{Ga}_{1-x}\text{As} \) material oxidizes, with the oxidization rate increasing with increasing Al concentrations. However, a bigger concern is that after oxidization takes place at an exposed interface, the oxidization process would propagate along the Al based material layer into unexposed regions. At

![Graphs showing electric field profiles](image)

Fig. 3-2. Optical mode profiles corresponding to an optical cladding layer, \( \text{Al}_x\text{Ga}_{1-x}\text{As} \) with (a) \( x=20\% \), (b) \( x=30\% \), (c) \( x=40\% \), and (d) \( x=50\% \). The relative transverse refractive index profile is shown by dotted lines as a reference.
concentrations of approximately 40% and less, oxidization will still occur, however, the oxidization process will self-terminate near the exposed interface instead of propagating along the layer [19]. The inability of hydrofluoric acid (HF) to etch Al based materials with less than 40% Al at room temperature is another reason for choosing to use \( \text{Al}_{0.4}\text{Ga}_{0.6}\text{As} \). HF is commonly used to etch \( \text{SiO}_2 \).

The optical mode profile obtained using a two-dimensional mode calculation, shown in Fig. 3-3, is consistent with the relevant results from a one-dimensional mode solver used to generate the profiles shown in Fig. 3-2. The optical mode is asymmetric and does indeed extend into inserted \( \text{Al}_{0.4}\text{Ga}_{0.6}\text{As} \) optical cladding layer. However, the optical mode still peaks in the quantum well.

Using a ridge width of 2 \( \mu \text{m} \), a cavity length of 600 \( \mu \text{m} \), and facet reflectivities of

\[
\begin{align*}
\text{Al}_y\text{Ga}_{1-y}\text{As} & \quad \text{In}_x\text{Ga}_{1-x}\text{As} \\
0 & \quad 0 \quad x \quad y
\end{align*}
\]

**Fig. 3-3.** Two-dimensional optical mode profile with the material composition in the transverse direction shown for reference.
30% at cleaved facets, the optical light power versus injection curve for the laser is computed using our proven CAD tool, FELES, and is plotted in Fig. 3-4. The threshold current is observed to be around 20 mA with a slope efficiency of 44%, both comparable to the results of a conventional laser of similar cavity dimensions as computed by the CAD tool and experimentally confirmed.

![Graph of output light power versus injection current for the emitter-up HBT compatible laser.](image)

**Fig. 3-4.** Output light power versus injection current for the emitter-up HBT compatible laser.

The HBT layer structure, shown in Fig. 3-5, is identical to the laser except for the doping of the emitter layers. Using a base and a collector contact width of 2 μm, an emitter contact width of 1 μm, and keeping the collector-emitter bias at 2.0 V while ramping the base-emitter bias from 0 V to 1.7 V, the current gain (β) as a function of the collector current density, \( J_c \), is shown in Fig. 3-6(a). The cutoff frequency (\( f_T \)) dependence on \( J_c \) is shown in Fig. 3-6(b). The current gain remains relatively flat from low to medium biases with a rapid drop-off at higher biases. The cause for this drastic deterioration can be attributed to the roll off of the emitter injection efficiency.
Fig. 3-5. Layer configuration for an emitter-up HBT. Layers with dopings written in italics undergo type conversion to transform the structure into a laser.

Fig. 3-6. HBT merits (a) current gain, and (b) cutoff frequency as a function of collector current density.
3.2 Design Issues

The proposed layer configuration, given in Fig. 3-1, includes features that are not present in a typical single QW laser or typical npn-HBT. The formation of a displaced base-collector p-n junction, the inclusion of a quantum well in the HBT, and the presence of a highly p-doped layer adjacent to the quantum well of the laser will be addressed individually in the following sections.

3.2.1 Displaced Base-Collector p-n Junction

The insertion of an additional layer between the base/quantum well layer and the collector layer creates a situation where the heterojunction is not at the same location as the p-n junction. In other words, the p-n junction at the base-collector interface is displaced with respect to the base-collector heterojunction. The use of a displaced base-collector p-n

![Diagram](image)

Fig. 3-7. Band diagram for transistor (a) without the n-GaAs layer, and (b) with the n-GaAs layer.
junction has been shown to improve the performance of the transistor [20], however, the main motivation for the insertion of a 0.07 μm GaAs layer between the quantum well and the Al_{0.3}Ga_{0.7}As collector layer in the proposed structure is not to achieve potentially better transistor performance, but to complement the 0.07 μm GaAs base layer on the other side of the quantum well as shown in Fig. 3-7. With GaAs layers on both sides of the quantum well aids in centering the peak of the optical mode over the quantum well region as shown in Fig. 3-8 A laser structure designed without the additional GaAs layer would force the optical mode peak away from the quantum well and into the base layer as seen in Fig. 3-8(b). Inevitably, this would increase the threshold current due to the reduced gain-optical mode overlap, and reduce the efficiency due to increased free carrier absorption from the heavily doped base layer. From Fig. 3-8(c) and Fig. 3-8(d), the optical confinement of the mode in the quantum well region is significantly improved by reducing the amplitude of the secondary peak situated over the GaAs collector contact layer.

Using the structure given in Fig. 3-5, the effect of the displaced p-n junction at the base-collector interface on the transistor is studied. Shown in Fig. 3-9(a) and Fig. 3-9(b) are the simulated results for $\beta$ and $f_T$, respectively. The transistor with the displaced p-n junction layer is represented by the dotted lines, while the transistor with the heterojunction at the p-n junction is represented by the solid lines.

The addition of the GaAs displaced junction layer appears to have no effect on $\beta$ as the two curves overlap each other. This is contrary to the results in [20] where there was a dramatic improvement in $\beta$. The mechanism claimed to be responsible for the improvement in [20] was the change in electric field at the base-collector junction which
Fig. 3-8. Optical mode profiles corresponding to (a) a laser with the displaced p-n junction layer, and (b) a laser without the displaced p-n junction layer. Figures (c) and (d) show the entire mode for case (a) and (b), respectively. The relative transverse refractive index profile is shown in dotted lines as a reference.

made it feasible for electrons to be swept out of the base region, thus reducing the electron concentration available for recombination. For the proposed structure, the transverse electric field is shown in Fig. 3-10. The two transistors have similar profiles at low and medium biases. At higher biases, significant differences in the transverse electric field does occur. However, at higher biases the recombinations at the emitter-base junction, in
Fig. 3-9. HBT merits (a) current gain, and (b) cutoff frequency as a function of collector current density for a HBT with (dotted line) and without (solid line) the displaced p-n junction layer.

Fig. 3-10. Transverse electric field for a HBT with (dotted line) and without (solid line) the displaced p-n junction layer. The transverse bandgap profile is shown for reference.
particular the emitter injection efficiency, play a dominate role in determining the current gain. The current gain is identical because the emitter-base junction remained unchanged for both cases.

One interesting observation at higher biases is the shift of the electric field peak away from the quantum well region to into the collector layer for the transistor without the displaced p-n junction layer. A shift is not observed for the transistor with the additional GaAs layer as the position of the transverse electric field peak remained in the quantum well region. The electric field in the quantum well region is weaker for the transistor without the additional GaAs layer, therefore, a greater accumulation and trapping of electrons in the quantum well can occur. This accounts for the smaller $f_T$ at high biases for the transistor without the displaced p-n junction.

### 3.2.2 Quantum Well HBT

Intuitively, the insertion of a quantum well in a HBT is thought to have detrimental effects. The reasoning behind this assertion is that a quantum well would act as a trap for charges to effectively slow down the electron as it traveled from the emitter to the collector and also to enhance the recombination probability with a hole. Therefore, one would expect either a lowering of the current gain, a reduction of $f_T$, or possibly both. On the other hand, one can speculate that once the quantum well gets filled after an initial charging period, the carriers would just flow over the quantum well seamlessly without additional delays. Indeed, recently HBTs have been experimentally demonstrated with quantum wells intentionally inserted. The purpose of adding a quantum well was not to design a HBT compatible laser, but to use the quantum well as an etch stop layer [21] or to enhance the
current gain of the transistor [22, 23]. Taking the layer configuration depicted in Fig. 3-5, an investigation on the effect the quantum well has the proposed transistor design's current gain and $f_T$ is performed.

Comparing a transistor with a quantum well in the base with two that are identical everywhere except the absence of a quantum well, the current gain and the cutoff frequency are shown in Fig. 3-11. The difference in the two transistors without quantum wells is the thickness of the base layer. One transistor has a 0.07 μm base (dashed line), while the other has a 0.08 μm base (solid line). This is compared to the transistor with a 0.07 μm base and a 0.01 μm quantum well (dotted line).

![Graphs showing current gain and cutoff frequency](image)

Fig. 3-11. HBT merits (a) current gain, and (b) cutoff frequency as a function of collector current density for HBTs with varying base compositions.
The results are not so surprising. The transistor with the shortest base offers better current gain and cutoff frequency. What may be unexpected is the performance of the transistor with the quantum well. The current gain in the quantum well transistor outperformed the transistor of the same total base length (i.e. 0.08 \micron) referred to as the 'longer base' transistor. However, this is not the case for $f_T$ where the longer base transistor had a similar performance to the shorter base transistor and they were both substantially better than the quantum well transistor.

One obvious observation from the results is the confirmation that the shorter the base, the larger the $\beta$ and the higher the $f_T$. A simple explanation for the improved $\beta$ is the improved base transport factor. For a uniformly doped base, the shorter the distance the electron has to travel from the emitter-base to the base-collector junction, the fewer chances the electron has to recombine with a hole and not reach the collector. This argument holds for low to medium biases, however, for higher biases the current gain values for all three transistors converge. This suggests that another mechanism is determining the current gain. The emitter injection efficiency is thought to be the mechanism influencing $\beta$ at high biases. With increasing bias, the valence band barrier at the emitter-base heterojunction is reduced allowing for more holes to enter the emitter region as shown in Fig. 3-12.

The differences observed at high bias for $f_T$ can be explained by Fig. 3-13 where the transverse electron density distribution is shown for the longer base transistor (solid line) and the quantum well transistor (dotted line). The distribution of electrons are similar from low to medium biases, however, at high biases accumulation of electrons in the quantum well occurs. Therefore, electrons traveling across the base from the emitter to the
Fig. 3-12. Hole density in the transverse direction for the longer base HBT. The transverse bandgap profile is shown for reference.

Fig. 3-13. Electron density in the transverse direction for the longer base HBT (solid line) and for the quantum well HBT (dotted line). The transverse bandgap profile for the quantum well HBT is shown for reference.
collector will effectively be captured, then attempt to escape from the quantum well. This
capture and escape process reduces the charging time across the base thus reducing the $f_T$
since the cutoff frequency is inversely proportional to the total charging and transit time
from emitter contact to the collector contact.

3.2.3 Base Doping

The idea of having a highly doped layer near or in the active region of a laser is
contradictory to conventional laser design rules. The highly doped layer will significantly
contribute to the non-radiative recombination and free carrier absorption and will
undoubtedly lead to an increase in the threshold current and a decrease of efficiency for the
laser. The question is how significant they are in a particular situation or structure relative
to the other factors. When designing a HBT compatible laser having a heavily doped base
region close to or in the active region may be unavoidable. In fact, in the design outlined
in Fig. 3-1, the base layer is adjacent to the quantum well. Therefore, it is necessary to
investigate the effect of base doping on the laser and HBT performance.

Using the layer parameters given in Fig. 3-1, we altered only the base dopings. P-
doping values of $10^{18}$ cm$^{-3}$ (dashed line), $5 \times 10^{18}$ cm$^{-3}$ (dotted line), and $10^{19}$ cm$^{-3}$ (solid
line) are used in the numerical simulations. The laser performance for the three different
base dopings are given in Fig. 3-14. As expected, the laser with the lowest base doping
performed the best with a threshold of 11 mA and an efficiency of 52%. Next the $5 \times 10^{18}$
cm$^{-3}$ doping, the doping level chosen in the proposed structure, gave a 20 mA threshold and
a 44% efficiency. The threshold continues to increase to 30 mA while the efficiency
Fig. 3-14. Output light power versus injection current for lasers with varying base dopings.

Fig. 3-15. HBT merits (a) current gain, and (b) cutoff frequency as a function of collector current density for HBTs with varying base dopings.
continues to decrease to 36% when the base doping increases to \(10^{19}\) cm\(^{-3}\). The main reason behind this trend is the increase of free carrier absorption in the base region.

The transistor performance is shown in Fig. 3-15. As observed, reducing the base doping improves the performance of the transistor in terms of \(\beta\) and \(f_T\). Intuitively, the reason for this improvement is the reduction of recombination in the base region. In particular, the base transport factor for the current gain becomes closer to unity. However, the decrease of the base doping does have a negative effect on \(f_{max}\) due to the increase of base resistance.

3.3 Conclusion

In this chapter, a layer configuration was proposed to achieve both laser action and transistor action. Although a common epitaxial layer structure is used, few compromises to either the laser or HBT were made. Additions or modifications to the layer structures to enhance the performance of one of the devices but which potentially alter the performance of the other device dramatically were studied. In particular, detailed analysis the effects the formation of a displaced p-n junction on the HBT, the insertion of a quantum well on the HBT, and the heavily doped base in the active region on the laser were performed.
Chapter 4

Experimentation and Results

Following the numerical simulations and analysis on the proposed design of an emitter-up HBT compatible laser presented in Chapter 3, the experimentation phase of the exploration will be discussed in this chapter. The laser is fabricated first instead of the HBT due to the more demanding processing requirements for the HBT fabrication and the limited access we have to the fabrication facility. Moreover, the HBT technology has been perfected, and its behaviour is well understood. The efforts in designing the common layer structure are centered around retaining HBT performance and structure as evident from the term ‘HBT compatible’ laser structure.

This work concentrations on the demonstration of the merits of designing a emitter-
up HBT compatible laser and thus a laser structure was grown bypassing the necessity of type converting the n-type emitter layer of the HBT to p-type for the laser. The process of type converting n-type to p-type layers is well known and has been successfully demonstrated by [14] and others. Thus, a replication of the type conversion process will not be duplicated during our first experimental trial. When final demonstration of the fully integrated laser-transistor device is desired, the layers would be grown according to the HBT layer configuration and thus type conversion would be necessary to form the laser.

4.1 Design Modifications

The layer configuration adopted for the design of the emitter-up HBT compatible laser is given in Fig. 3-1. However, design modifications were done either out of necessity to adhere to growth issues or to reduce the complexity of the post-growth processing. The changes made will only have a minimum effect, if any, to the operation or the performance of the laser and transistor.

One of the changes involved the insertion of a 5 nm GaAs layer at 150 nm intervals in the Al$_{0.4}$Ga$_{0.6}$As optical cladding layer. Thus, a total of 9 additional GaAs layers, or termed smoothing layers, were grown in the 1.5 μm optical cladding layer. The purpose of the smoothing layers is actually to ‘smooth’ the growth of the quantum wells and ensure they grow uniformly without additional strain. If not for the insertion of smoothing layers when growing thick Al based cladding layers, stress and defects during the growth of Al based materials would propagate onto the surface thus making good growth on top of such surfaces difficult. This technique is commonly used and the merits have been documented through experimental trials [24]. Smoothing layers were also inserted in the 0.5 μm
collector layer but at every 125 nm. The consequences of effectively having quantum wells in the collector of the HBT should not disturb the performance of the transistor since the collector is deeply reversed biased thus preventing many electrons from being trapped in the wells as they travel from the base to the collector contact.

One modification which may affect the performance of the laser is the reduction of the quantum well thickness from 10 nm to 6 nm. This was done due to ensure that the grown strained quantum wells would maintain their strain. With the quantum well thickness almost halved, the optical mode overlap with the gain region will be only a 6 nm region. Thus, the modal gain will be reduced resulting in a higher threshold current.

One other change in layer dimensions is to limit the amount of p-type diffusion from the heavily p-doped base layer into the undoped quantum well. This is accomplished by partitioning the base layer of 0.07 μm into a 0.01 μm undoped layer and keeping the remaining 0.06 μm of material unchanged. The undoped layer is placed between the heavily doped base layer and the quantum well.

Modifications to the doping levels were also made. The p-doping in the p-contact layer was increased from $7 \times 10^{18}$ cm$^{-3}$ to $2 \times 10^{19}$ cm$^{-3}$ to ensure the formation of low resistance ohmic contacts. Such a high p-doping concentration can be achieved by using zinc as the acceptor. The n-contact layer would not be able to reach the $7 \times 10^{18}$ cm$^{-3}$ levels as specified due to the low percentage of acceptors that will activate. As an example, a request of a $5 \times 10^{16}$ cm$^{-3}$ n-doping for the collector layers would require an donor concentration of $1 \times 10^{18}$ cm$^{-3}$.

With the modifications discussed above, the layers were grown using a MBE
growth method on a 3 inch wafer. The grown layer structure is shown in Fig. 4-1.

Alterations to the device structure, defined in post-growth processing, were also made. A strongly confined laser structure was processed instead of the weakly confined structure presented in Fig. 3-1. The motivation behind this change was to minimize the number of dry etches required. The dry etching process, as will be explained in Section 4.3.3, is a difficult procedure to achieve good results with. Each dry etch would require a number of calibration runs. Since the etching process is highly dependent on the layer structures used, the calibration should be performed on pieces of the wafer which the etching would be done on to properly characterize the dry etch. Unfortunately, there was only one wafer to fabricate working devices and to calibrate other processing steps. Thus, a one dry etch laser structure was chosen instead of the two etches required for the structure presented in Fig. 3-1. This proved to be a wise decision as even one dry etch was difficult

![Diagram of modified layer configuration for an emitter-up HBT compatible laser. Modifications are written in italics.](image-url)
to get the desired etch depths as will be described in Section 4.3.3.

4.2 Process Flow

There were a number of different approaches, in terms of sequence of processing flow, available for the processing of this laser. An important consideration in any fabrication process is the ease of aligning each mask layer onto a previous layer. For example, if the ridge of a laser is first defined, the deposition of metal just contacting the top of the ridge would be difficult due to the finite resolution of the machines involved in the photolithography process. The best case scenario would be the exact alignment of the contact metal onto the ridge. However, the most common scenario, one which should be assumed when designing the tolerances for the masks, would be the misalignment of the contact to the ridge resulting in metal hanging over one side of the ridge as shown in Fig. 4-2. This can potentially cause the laser to fail electrically. Of course, for this particular

![Diagram](image)

Fig. 4-2. Consequences of misalignment for metal deposition (a) equal to the ridge width and (b) less than the ridge width. The darker arrows indicate a larger portion of current flowing in that direction.
example, one could intentionally deposit metal covering only a portion of the ridge width leaving enough tolerances on either side. However even this modification does not alleviate the difficulties of alignment and may create potentially new concerns of nonuniform current injection into the laser if the contacts are not perfectly aligned to the center of the ridge. A self-aligned process for the p-contact and the ridge, where the definition of one of the two will inherently define the other, would be desirable. For the proposed structure, a self-aligned process can be achieved by defining the p-contact first. The contact would act as a mask when defining the ridge thus ensuring perfect alignment between the two.

The definition of the p-contact followed by the laser ridge are the first two out of five major processing steps for the laser. The fabrication state of the laser after each processing step is depicted in Fig. 4-3. Two figures are used to depict each step with one showing the laser ridge with its supporting structures that lie between each laser, and the other showing an expanded view of the ridge itself. The supporting structures, which are 200 µm in width located in between the laser ridges, consist of unetched material, and are important to ensure the structural rigidity of the laser ridge. One could image the wafer without the supporting structures as being a wafer almost completely etched with only 2, 3, or 4 µm laser ridges appearing every 500 µm. This makes the handling of the wafer extremely difficult during processing especially trying to prevent the wafer from flipping over where the ridges can easily be damaged.

The dry etch to define the ridge extends approximately 150 µm from both sides of the ridge. The rest of the material between lasers is left to provide the structural support. The dry etch exposes the GaAs n-contact layer where, as shown in step 3 of Fig. 4-3, the n-
Step 1: p-contact metallization

Step 2: ridge definition

Step 3: n-contact metallization
Step 4: SiO$_2$ for p-contact contact

Step 5: p-contact contact metallization

Fig. 4-3. The process flow is divided into 5 steps. Features surrounding the laser ridge and an expanded view of the ridge are shown for each step. The n-contact for the laser is formed. The n-contact formation is not a self-aligned process, therefore, to account for alignment limitations, a spacing of 1 $\mu$m was left between the ridge and the n-contact. Since the GaAs n-contact layer is heavily doped, the additional distance between the n-contact to the laser ridge should not contribute to the total resistance of the laser. The width of contacts should be made greater than 50 $\mu$m as the foot-stamp created by a wire bond is approximately 50 $\mu$m. A 100 $\mu$m n-contact width was formed to allow for external probes, in addition to wire bonds, to be used.
The p-contact width unfortunately is defined as the width of the laser ridge, thus it is too narrow to easily contact the metal. The purpose of the SiO₂ deposition, performed in step 4, is to provide a surface whereby additional p-contact metal can be deposited to make the p-contact on the ridge accessible. A thick SiO₂ layer is deposited on the side of the ridge without the n-contact metal. A small overlap of the SiO₂ layer with the existing p-metal on top of the ridge is done to account for the alignment difficulties and to ensure the SiO₂ is deposited up to the ridge to prevent the p-contact contact, formed in step 5, to unintentionally come in contact with the GaAs n-contact layer instantly creating a direct path from contact-to-contact bypassing the ridge.

Finally, in step 5 the p-contact contact metal is evaporated on top of the existing p-contact metal and extending approximately 100 μm onto the SiO₂. The p-contact contact metal is intentionally not extended to cover the entire exposed portion of existing p-contact metal on the ridge but stops 0.1 μm from the edge of the ridge.

4.3 Implementation of Processing Plan

With the processing flow for the fabrication of the emitter-up HBT compatible laser outlined in the previous section, this portion of the chapter will give an account to the implementation of that processing plan. A detailed step-by-step processing plan can be found in Appendix 3.

4.3.1 Photolithography

Photolithography involves the transferring of a pattern onto the semiconductor material
through the use of an intermediate layer of photoresist. The photoresist layer acts as a mask as it defines the areas on the wafer where further processing is to be done.

With a desired laser structure in mind, it is necessary to transfer the laser structure onto the photoresist by using a photomask. Each photomask defines a location of the wafer where a particular type of processing is to be done. For example, the n-contact metallization and p-contact metallization would need different photomasks since the placement of the two contacts are in different locations. For the processing flow depicted in Fig. 4-3, 5 different masks were required. A computer aided design program called Integrated Circuit Editor (ICED32) was used to define each photomask and assist in the layout of the laser structure. The alignment of each mask onto each other is done through the use of alignment marks. Space on each mask must of left to accommodate the alignment marks. The alignment marks used for this mask set are shown in Fig. 4-4.

Fig. 4-4. Alignment marks used to align each mask.

The transfer of the layouts of each layer onto a photomask is done through a pattern generator. The pattern generator accepts a computer file defining a specific photomask
layer and transfers the pattern onto a photomask. The photomask used is a glass plate having one side coated with a thin photoresist layer on top of a thin chromium layer. After, the pattern generator exposes the photoresist plate to UV light at the locations specified in the layout, the plate is immersed into a developer. The developer only removes the photoresist where it had been exposed to UV light. The exposed chromium is stripped off by using a chromium etch. Finally, the remaining photoresist is removed using a solvent. The result of this photomask making process is a glass plate with transparent (i.e. no chromium) and opaque (i.e. chromium still present) openings at desired locations.

Before any photolithography step, a standard wafer preparation is always done to promote the adhesion of the photoresist onto the surface of the wafer. This is achieved by placing the wafer into an oven where a flow of hexamethyldisilizane (HDMS) vapour is injected. The HDMS vapour reacts with the surface of the wafer making it hydrophobic. After the preparation of a wafer has been done, the wafer can be stored for many months without the need of a repeated HDMS process before photolithography is done.

The photoresist material is spun onto the wafer at speeds of 3000-4000 RPM for times anywhere between 30-60 seconds. The thickness of the photoresist is a function of the viscosity of the photoresist material, the speed and duration of the spinning. For our wafer, a 40 second spin at 3500 RPM resulted in a photoresist layer thickness of approximately 750 nm. It is important for the photoresist to be spun on with repeatable thicknesses as will be discussed.

The wafer is now prepared to have the pattern on the photomask transferred onto the photoresist. This is done by a 10X photolithographic system where the photomask is
exposed to UV light. Only the transparent areas of the photomask will permit UV to impinge onto the photoresist. The 10X notation represents the magnitude of the pattern reduction from the photomask onto the photoresist. Therefore, this particular photolithographic system reduces the feature sizes 10 times when transferring the patterns from the photomask to the photoresist. Depending on the thickness of the photoresist, the type of photoresist, and the material layers underneath the photoresist, the UV exposure time necessary to properly define the openings in the photoresist will vary. A ‘focus-exposure’ test, which exposes the photoresist for an array of different exposure times, is usually performed when starting a new processing flow. The optimum time can be found after developing the photoresist and checking the distances of known photomask patterns. If the photoresist is under-exposed, the resultant photoresist pattern will have its features under-defined (i.e. shorter than desired distances) and vice versa if over-exposed. The optimum exposure time found our wafer conditions was 2.1 seconds.

After the wafer has been patterned, the photoresist in the exposed regions will be removed when the wafer is immersed into a photoresist developer. The wafer now is ready for further processing in those exposed areas where photoresist is absent. After the desired processing is done for this step, the photoresist is removed from the entire wafer through the use of a solvent. The wafer is now prepared to undergo another photolithography process cycle using another mask.

The process from photomask making to patterning on the photoresist is repeated, in our case, five times; one for each of the processing steps described in the process flow shown in Fig. 4-3. From Sections 4.3.2 to 4.3.6, each of the processing steps will be elaborated on.
4.3.2 P-Contact Metallization (Step 1)

For metallization, the photolithography process described in the previous section is performed with modifications. Instead of opening areas where the metal is desired, the areas where the metal is unwanted are opened. Therefore, a reversal of the photomask is necessary thus lending to the name of this process, image reversal. The advantages to metallization image reversal has over the standard photolithography non-image reversal process is in the eventual lift-off of the metal in the undesired locations. The processing steps in a standard image reversal process is outlined in Fig. 4-5.

Fig. 4-5. Image reversal process: (a) masking of photoresist layer, (b) after exposure to ammonia to reverse photoresist layer's response to developer, (c) metallization and lift-off, and (d) resultant p-contact.

After the photoresist has been exposed to the UV light of the 10X photolithographic system, the wafer is then placed into an oven where it is subject to an ammonia gas. The
ammonia gas reacts with exposed photoresist causing it to be almost insoluble to the
standard developers used to develop photoresist. This process also makes the exposed
photoresist areas immune to further UV exposures. Exposing the entire wafer to UV light
will cause the previously unexposed photoresist to become soluble to photoresist
developers. The resulting photoresist mask would have an opening where metal is desired.

After the evaporation of metal, which will cover the entire wafer surface, a lift-off
process is done. The wafer is submersed into acetone which acts as a solvent for photoresist
even if the photoresist has been subjected to the ammonia image reversal process. Therefore, any metal which has photoresist between it and the semiconductor material will be removed or 'lifted off'. The image reversal process provides a photoresist profile as shown in Fig. 4-5(c). The cliff like profile prevents the metal on the photoresist to connect with the metal on the semiconductor thus making lift-off possible. For lift-off to be successful, the photoresist thickness must be greater than the thickness of the evaporated metal.

This image reversal procedure was performed successfully for the evaporation of
the p-contact metal (step 1). The p-contact metal recipe used was 200 Å of Pd, 300 Å of
Pt, 1200 Å of Au, and finally 400 Å of Pd. Since the p-contact is used as a mask for the
dry etching step described in the proceeding section, the final layer should consist of Pd
instead of Au to reduce the amount of sputtering during dry etching. The p-contact was
then annealed at 440°C for 90 seconds to promote alloying of the metals [25].
4.3.3 Ridge Definition (Step 2)

Using the p-contact metal as a mask to achieve a self-aligned ridge, etching of the ridge down to the n-contact layer was done in this step. To leave the supporting shoulders which lie between each laser unetched, SiO₂ was used as a mask. A 200 nm thick SiO₂ was deposited using a plasma enhanced chemical vapour deposition (PECVD) machine. Silicon dioxide is formed by the PECVD by reacting silane (SiH₄) with nitrous oxide (N₂O). Next the standard photolithography process was followed as described in Section 4.3.1. A HDMS wafer preparation was done followed by the spinning of photoresist. The photoresist was patterned with a 300 μm opening centered on the laser ridge. The exposed photoresist was subsequently removed by a developer uncovering the SiO₂ to be etched. This step along with the subsequent steps are depicted in Fig. 4-6.

The SiO₂ is dry etched using a reactive ion etching (RIE) technique that involves the chemical reaction of CHF₃ with SiO₂. With the particular recipe programmed into the RIE, the etch had a 2:1 selectively with photoresist. Therefore, one must confirm that there is enough photoresist covering the unetched SiO₂ to prevent the SiO₂ from etching. In our processing, there was 500 nm of photoresist remaining after the photolithography process and only 200 nm of SiO₂ to etch. The dry etch is an anisotropic etch thus produces the desired vertical SiO₂ walls. After the SiO₂ is etched in the opened areas, the photoresist was removed.

For our proposed structure, the next step is to dry etch the semiconductor material down to the 100 nm GaAs n-contact layer. The technique used to etch the GaAs based layers is an electron cyclotron resonance (ECR) etching technique which can be thought of
as an advanced RIE technique. The gases involved were chlorine based gases namely BCl₃, Cl₂, but also a small portion of Ar. The Cl₂ and BCl₃ are responsible for the etching of GaAs based materials while the Ar is used to constantly clean the surface during the etching process. The etch rate is dependent on many variables including the temperature, the proportion of each gas used, and the setup variables for the ECR machine.

Typically, the first etch is done for a much longer time than necessary to characterize the etching rate. This particular ECR machine had an interferometric setup to monitor the etch. Using the fringe patterns of the output intensity, one could calculate the
corresponding the etch depth as the etch was proceeding [26]. Unfortunately, the wafer to be etched had patterns of SiO$_2$ and metal on it already, thus the resulting fringe pattern was a superposition of many signals as shown in Fig. 4-7. It was decided that the interferometric

![Image](image_url)

2.9 $\mu$m for a 3 minute etch

Fig. 4-7. Fringe patterns from laser interferometer of the ECR.

setup could not be used to our advantage. A scanning electron microscope image (SEM) of the etch is shown in Fig. 4-8. An one second delineation etch consisting of H$_2$O$_2$:NH$_4$OH at a ratio of 25:1 is done on the sample before SEM images are taken to

![Image](image_url)

2.9 $\mu$m

GaAs smoothing layers

Fig. 4-8. SEM image of the 3 minute etch. Smoothing layers can be seen as white lines.
make different material layers distinct. For example, the presence of the GaAs smoothing layers is seen by the bright lines. The SEM image clearly shows that the etch went past the GaAs n-contact layer into the thick optical cladding layer. The calculated etch rate was approximately 900 nm per minute.

The next two etch attempts, performed again on small pieces broken off the original wafer, provided puzzling results. With etch rates differing by 10 seconds, which would definitely result in differing etch depths, the etch stopped at identical locations. The etch stopped at the GaAs n-contact layer and Al$_{0.4}$Ga$_{0.6}$As optical cladding layer interface as shown in Fig. 4-9. Therefore, both etches of differing times were 100 nm too deep, the

![Image](image.png)

Fig. 4-9. Similar etch termination depths for two different etch times. SEM image shows that the etch stopped at the Al$_{0.4}$Ga$_{0.7}$As optical cladding layer.

thickness of the GaAs n-contact layer. Answers to this apparent disparity were found when a ridge shown in Fig. 4-10 was observed. Severe amounts of undercutting, in the order of 200 nm per second, in the GaAs layers led us to believe that even if the etch had stopped in
Fig. 4-10. SEM image showing severe undercutting due to the delineation etch.

Fig. 4-11. SEM image of etch with photoresist spun on before delineation etch.
the GaAs n-contact layer, the mechanism responsible for the undercutting would easily remove the 100 nm GaAs layer. After some investigation, it was concluded that the quick delineation etch was responsible for the removal of GaAs material. To alleviate this problem, a thick layer of photoresist was spun on before the delineation etch.

Proper etch characterization could now be done as shown in Fig. 4-11. The dark region covering the semiconductor material is the photoresist material. In this particular etch attempt, the GaAs n-contact layer has not yet been etched as some \( \text{Al}_{0.3}\text{Ga}_{0.7}\text{As} \) collector layer is still present. A few more etchings were performed and checked using the SEM to confirm whether or not the etch entered the GaAs n-contact layer.

4.3.4 N-Contact Metallization (Step 3)

The n-contact metallization was done using an image reversal photolithography process followed by a lift-off of the unwanted metal. The location of the n-contact metal, as mentioned before, started 1 \( \mu \text{m} \) from the ridge and extended approximately 100 \( \mu \text{m} \) away. The gap between the ridge and the metal was intentionally left to minimize the possibilities of a short with the p-contact metal due to the inaccuracies of alignment.

The n-contact recipe used consisted of 750 Å of Pd, 1350 Å of Ge, 300 Å of Ti, and finally 500 Å of Pd. The annealing conditions were 415°C for 15 seconds. Since the annealing temperature is lower than the annealing temperature for the p-contact, the p-contact must be formed and annealed before the evaporation of the n-contact. SEM images, not shown here, confirmed the placement of the n-contact.
4.3.5 SiO₂ for P-Contact Contact (Step 4)

The fact that the width of the p-contact was designed to equal the ridge width of the laser for it to be self-aligned provides the necessity of this step. The existing p-contact metal is too narrow for easy external probing of the laser. Therefore, the addition or extension of the p-contact metal to allow for wire bonding or probing is necessary. Since both sides of the ridge are etched down to the n-contact layer, an isolating layer such as SiO₂ must be deposited before p-contact metal can be evaporated on top of it.

An deposition of approximately 0.5 μm of SiO₂ was performed on the entire wafer. Standard photolithography steps were taken to selectively etch away the SiO₂ in the undesired locations. The etch left SiO₂ from the support structure to just overlapping the existing p-contact metal. This was done to ensure that the p-contact metal would not unintentionally be left contacting the n-contact layer.

4.3.6 P-Contact Contact Metallization (Step 5)

The final step in the processing of this laser is the evaporation of a p-contact contact metal onto the newly deposited SiO₂ described in the previous section. This p-contact contact would extend the already existing p-contact on the ridge approximately 100 μm to enable direct probing.

The standard image reversal and lift-off processes were done. The recipe for the p-contact contact metal used was 200 Å of Ti followed by 500 Å of Au. The Ti metal layer would provide adhesion to the existing p-contact metal. No additional annealing was performed.
4.4 Device Characterization

After all of the processing steps were completed, the laser structures were first observed using an alpha-stepper and a SEM to check all of the layer thicknesses, to measure the resultant ridge widths, and to view the quality of the laser ridges.

A lateral profile of the laser structure showing the relative heights of each section is obtained from an alpha-stepper as shown in Fig. 4-12(a). Due to the large diameter tip used for the alpha-stepper, features in the order of the ridge width can not be resolved. This is the reason behind the almost 20 \( \mu\)m ridge width observed. The p-contact contact is on the left side of the ridge while the n-contact is on the right side of the ridge. A 50 \( \mu\)m distance from the end of each metal to the supporting structures is as intended. The p-contact contact is at a higher elevation then the n-contact due to the additional SiO\(_2\) isolating layer deposited. A top view of the laser structure is shown in Fig. 4-12(b).

After looking at many laser ridges using the SEM, a typical SEM image showing a 2 \( \mu\)m laser ridge is shown in Fig. 4-13. The quality of the laser ridge is undesirable as the ridge walls are not vertical with undercuts sporadically located along the wall. The p-contact contact and the SiO\(_2\) cannot be easily detected. One of the major concerns brought up in the SEM image is the possibility that the n-contact is not formed on the GaAs n-contact layer but rather on the Al\(_{0.3}\)Ga\(_{0.7}\)As collector layer. The bright rectangular shape object on the right side of the ridge is the n-contact metals. It seems as though there is a thin, roughly 50 nm Al\(_{0.3}\)Ga\(_{0.7}\)As layer between the metal and the GaAs layer. If this is the case, the n-contact resistance would be extremely large because the formation of the n-contact is now on wider bandgap material, but more importantly on very lightly doped
Fig. 4-12. (a) Relative thicknesses in the lateral direction obtained from an alpha-stepper, and (b) top view of the laser structure.
material (i.e. n-doped $5\text{e}16$).

The wafer was cleaved into bars to test the laser characteristics. Cavities lengths of approximately 1.5 mm were chosen in hopes to reduce the per unit length losses facet reflectivities contribution to the total per unit length losses. External probes were used to contact the laser. A output light power versus injection current for a 3 $\mu$m laser is shown in Fig. 4-14. Unfortunately, this laser failed at injection currents approaching 50 mA and no further tests could be performed. It is difficult to say whether or not the observed 8 mA threshold current represents the onset of lasing or just spontaneous emission. Spontaneous emission accounts for the total light output captured by the photodetector for current injections below lasing threshold. Above threshold, the contribution of stimulated emission to the total output light dwarfs the contributions made from spontaneous emission. The threshold current is marked by an usually abrupt change in slope efficiency from low to high. This change in efficiencies is not clearly seen in Fig. 4-14 suggesting
threshold may not have been reached. However, an exclusive statement that the light observed is only from spontaneous emission may be incorrect because of the minute amount of light captured by the photodetector. The quantity of light measurable was near the threshold of the photodetector. Therefore, if a change of slope efficiencies was present at the 8 mA, the amount of spontaneously emitting light before threshold would be comparable to the noise of the photodetector and thus undetectable.

Many more devices were tested with varying results. One common reoccurrence was the observation of emission at a wavelength corresponding to a deep red colour. The material layers Al$_{0.3}$Ga$_{0.7}$As or Al$_{0.4}$Ga$_{0.6}$As would produce emissions in the 650 nm wavelength range corresponding to the deep red colour. The emitted light is not observed consistently from the same location of the laser. Some lasers emit a line of the deep red coloured light along the ridge of the laser while others emit from what could be considered point sources in random locations along the ridge. These lasers which do emit ~650 nm
light have thresholds, or more correctly termed the onset of output light whether it is spontaneous or stimulated is unknown, at higher current conditions (i.e. > 50 mA). This may suggest that for these devices alternate 'leakage' paths exists with carrier accumulation and recombination occurring in the higher band Al based material layers.

One possible leakage path may have been formed if the additional SiO₂ layer was not deposited up to the edge of the ridge. This would result in a gap of exposed GaAs n-contact layer between itself and the ridge. With the subsequent evaporation of p-contact contact metal, some of the metal may in fact contact the GaAs n-contact layer. Thus, a direct current path would exist across the GaAs n-contact layer bypassing the ridge.

One device which did demonstrate a clearly identifiable change in slope efficiency is plotted in Fig.4-15. One interpretation of the results would have the spontaneous emission account for the light before the abrupt change in slope efficiencies at 33 mA and a stimulated emission dominated light emission after the 33 mA. An assertion that it is
indeed the spontaneous emission that is being observed below threshold can be made with some confidence after observing the spectrum. The spectrum, shown in Fig. 4-16, is gathered at a below threshold injection current level of 23 mA. The linewidth of the

Fig. 4-16. Spectrum for a 2 μm ridge laser taken at current level of 23 mA.

spectrum is approximately 50 nm centered at 960 nm. Unfortunately, the device failed after 35 mA and a spectrum above the threshold point could not be taken. The laser tested was a 2 μm ridge width device with a cavity length of 1.5 mm.

One interesting observation in Fig. 4-15 is the presence of a threshold for the spontaneous emission. Normally, spontaneous emission is present at any level of current injection. This suggests that another current path or more likely the contacts are acting as a diode prevent current injection into the semiconductor material. Without the presence of this additional current blockage (i.e. threshold approximately 13 mA), the lasing threshold would be shifted down to approximately 20 mA. This corresponds exactly with the simulated lasing threshold.
4.5 Fabrication Process Improvements

In the fabrication of the emitter-up HBT compatible laser, one critical processing step is the definition of the ridge using a dry etching technique. Many key structural features are highly dependent on the success of this dry etch. The verticality of the ridge walls is defined by the dry etch recipe used. More important, as experienced first hand in this work, is the formation of the n-contact. For the formation of the n-contact to be successful, all the semiconductor material layers from the n-contact layer to the top layer must be etched off. This step is necessary for our proposed structure, but will also apply to any structure grown on semi-insulating material. Using our proposed structure as an example, 950 nm of material would be etched in order to reach the n-contact layer. Depending on the gases used, the temperature setting, etc. the rate of etching will vary. At a typical rate of ~800 nm per minute for GaAs dry etching translates to approximately 70 seconds of etching for 950 nm. The etch must be controlled to stop within the n-contact layer which for our case is 100 nm thick. At the etching rate of ~800 nm per minute, there is only a 7 second window to stop the etch in the correct layer.

The complications associated with a dry etching processing step can be avoided by using an etch stop layer. The etch stop layer is usually a very thin layer grown just above the layer in which the dry etch is to stop. With the etch stop layer, one could either use a dry etch or a wet etch. The defining characteristic of the etch stop layer is the fact that for a given etching technique, the etch would not be able to etch through the etch stop layer. Therefore, the need for precise control of the etch is eliminated.

Depending on the placement of the etch stop with respect to the layer structure, this
additional layer may or may not affect the operation of the device. When a second experimental trial is proposed, consideration should be given to include an etch stop layer above the n-contact layer.

4.6 Conclusion

The first experimental trial of fabricating an emitter-up HBT compatible laser was less successful than desired. Tests have showed that many of the lasers were unable to reach threshold under room temperature conditions before electrically failing. The one laser device which did show evidence of lasing and had a threshold of ~30 mA, close to that modeled, also electrically failed before a spectrum above threshold could be taken.

SEM images of the lasers indeed confirm that the processed lasers are not of good quality with many undesirable features. These nonuniformities could be suggested as the cause for the unpredictable laser characteristics from one device to another. Due to the limited amount of semiconductor material, many characterization tests along the processing flow could not be performed.

The limited success of this first experimental trail does not imply that the design, nor the concept of dual functional devices from a common epitaxial layer structure is not feasible. Instead, the failure can be placed on the unfamiliarity of processing techniques necessary to fabricate this device. Experimental trails of new processes and/or new devices are often difficult to master because of the lack of precedents.

There are many more, perhaps thousands, of samples that have yet to be measured and tested and will be after they are cleaved and wire bonded. More lasing samples are
expected to be found with the results analyzed and modeled to guide us in the design of layer structures and processing steps for ensuing trials.
Chapter 5

Conclusion

5.1 Summary of Work

The major thrust of this work was the exploration and investigation of a novel laser-transistor integration strategy. Instead of the brute force approaches adapted by most integration attempts such as selective area growth/regrowth and vertical integration, the approach presented in this work provides a more elegant solution in which a common layer structure is used to achieve dual or multi-functionalities.

In the literature, experimental devices providing both lasing and transistor action utilizing the common layer structure strategy have been reported. These experimental demonstrations have been purely empirical in nature. Addition constraints are imposed on
the design of the common layer structure to support two functionalities. In this work, compatibility issues between a laser structure and a HBT structure were investigated. With the aid of a numerical model, FELES, traditional views and thinking that a QW laser structure would be incompatible with a npn-HBT structure has been shown to be incorrect. Although the structures are inherently different, in this work we have shown that major differences such as the insertion of a quantum well into a HBT structure and the presence of a heavily doped region adjacent to the quantum well for the laser do not have negative impacts on the performance of the laser or transistor. In fact, with the insertion of an additional displaced p-n junction layer to provide better optical mode confinement for the laser the cutoff frequency performance for the HBT improved.

With the discovery that a structurally compatible laser-HBT device could be designed without compromising either device performance, an emitter-up HBT compatible laser was proposed. Unlike the reported structures found in the literature [13,14], our design retains many of the features that constitute a high speed HBT and yet still possess good laser characteristics. From numerical simulations, a single QW laser lased at a current threshold of 20 mA with a slope efficiency of 44%. The npn-HBT transistor had current gains near 1000 and cutoff frequencies in the 50 GHz range depending on the bias. Growth of our proposed design was carried out followed by the necessary post-growth processing. Some difficulties in the dry etching processing step was experienced and it is believed that the uncertainty in the accuracy of the etch, and subsequent n-contact metallization, as the primary reason behind the poor performance of the lasers. Most lasers did not lase at room temperature and electrically failed at moderate current levels. However, there were a few lasers which had characteristics that suggested that they were lasing. A typical sign of
lasing threshold is the abrupt change in slope efficiency. One laser clearly showed an abrupt change in slope efficiency at a current level of 33 mA and with the elimination of the apparent diode like characteristics at either the contacts or through another current path, the threshold current would be brought down to 20 mA. This corresponds to our simulated results.

5.2 Future Work

The work presented in this thesis can be viewed as the first step in the investigation of integrating devices using a common epitaxial layer structure. We have successfully demonstrated through numerical simulations that an integrated laser-HBT device using the same layer configuration does not hinder the performance of the individual devices. Although the first experimental trial did not reflect the simulated performances, the concept is still promising. More work in the fabrication and processing of the laser device, and in the future the transistor device along with an integrated laser-transistor device, is needed to validate the idea of creating a dual functionality device from a single layer configuration.

The concept of using a common epitaxial layer structure to create more than one device functionality has just begun to be explored. The number of different devices which could be integrated together using a common layer structure strategy could very well approach the number of permutations one could make with any given set of devices. In other words, many combinations are possible. Already in the literature there exists experimental demonstrations of a vertical cavity surface emitting laser (VCSEL) integrated with a field effect transistor (FET) [29], a VCSEL integrated with a HBT [30, 31], and a lateral current injection (LCI) laser integrated with a FET [32-33]. However, all of these
attempts use a common epitaxial layer structure, but also employ an empirical approach. Therefore, there exists an opportunity to explore different integrated devices from a theoretical point of view. Each of the devices have characteristics uniquely theirs. Thus depending on which combination of devices are integrated together, the optimum layer configurations will differ. The ultimate device performance of each combination, which could be a direction for further explorations, will also differ.
Appendix 1

FELES

The simulation tool, FELES, is a two-dimensional model which self-consistently solves Poisson’s equation, the electron and hole continuity equations, the wave equation, and the photon rate equation [17]. Included in the model is Shockley-Read-Hall, spontaneous, and stimulated recombination. In addition to including mirror losses, bulk losses and free carrier absorption were accounted for in all regions. The values used for free carrier absorption in GaAs is $\alpha_{electron} = 3 \times 10^{18} \text{ cm}^{-2} \times n$ and $\alpha_{hole} = 7 \times 10^{18} \text{ cm}^{-2} \times p$.

The dependence of material gain on carrier density in the quantum well was calculated using an improved formalism described in [27]. The gain function used for 10 nm In$_{0.2}$Ga$_{0.8}$As quantum well is $g = 1411.43 \ln \left( \frac{n_{tr}}{1.449 \times 10^{18}} \right)$.

The model used has shown good agreement with all reported experimental results for the devices in [13, 14]. More importantly, the model is used to uncover the underlying physical mechanisms responsible for their device performance and it is this improved understanding that can help the future development of improved methodologies for the device design and optimization.
Appendix 2

Transistor Figures of Merit

The merits of a HBT are usually given in terms of its current gain and its frequency response. The common-emitter current gain, $\beta$, is defined as,

$$\beta = \frac{\partial J_c}{\partial J_b}$$

where $J_c$ and $J_b$ are the current densities in the collector and base respectively. Another definition of current gain is the common-base current gain, $\alpha$, given by,

$$\alpha = \frac{\partial J_c}{\partial J_e}$$

where $J_e$ is the current density in the emitter. A simple relationship exists between the two current gain definitions,

$$\beta = \frac{\alpha}{1 - \alpha}$$

To get a physical sense of what the current gains represent, an expansion of $\alpha$ breaks the current gain into three factors [28]:

- emitter injection efficiency $\gamma = \left( \frac{J_{ne}}{J_{ne} + J_{pe}} \right)$
- base transport factor $\alpha_T = \left( \frac{J_{nc}}{J_{ne}} \right)$
- recombination factor $\delta = \left( \frac{J_{ne} + J_{pe}}{J_{ne} + J_{pe} + J_R} \right)$
where \( J_{ne}, J_{pe}, J_{nc} \) and \( J_R \) are the current densities due to electrons in emitter, holes in emitter, electrons in collector, and recombination in the space charged region, respectively. Ideally, \( \alpha=1 \) meaning that all electrons injected from the emitter would end up in the collector. For \( \alpha \) close to 1 translates to a high \( \beta \).

As the frequency of the input signal is increased, there occurs a point when the signal is changing faster than the time required for an electron to travel from the emitter to the collector. When this happens, the transistor response becomes increasingly out of phase with the input signal, and thus the amplitude of the current gain decreases. The frequency at which the magnitude of \( \beta \) is equal to unity is known as the cutoff frequency, \( f_T \) and is defined as,

\[
f_T = \frac{1}{2\pi \tau_{ec}}
\]

where \( \tau_{ec} \) is the emitter to collector transit time for an electron. This total transit time can be expressed as a sum of transit times through the individual regions,

\[
\tau_{ec} = \tau_e + \tau_b + \tau_c
\]

where \( \tau_e, \tau_b, \) and \( \tau_c \) are the transit times through the emitter, base, and collector regions, respectively.

The maximum oscillation frequency, \( f_{max} \), is calculated by,

\[
f_{max} = \sqrt{\frac{f_T}{8\pi R_b C_{bc}}}
\]

where \( R_b \) is the base series resistance, and \( C_{bc} \) is the base-collector capacitance.
Appendix 3

Processing of Integrated Device: Plan

**Standard Positive Lithography:**

1) vapour prime wafer with YES oven (HMDS process)
2) while spinning, spray on acetone followed by isopropanol making sure acetone does not dry to remove any photoresist residue
3) OCG 897-7i, 3500 rpm, 40 sec to get a thickness of 0.764 μm, n=1.614
4) solvent bake 1 min at 90 °C
5) expose in 10X stepper with focus 251 and exposure time 2.1 sec
6) post-exposure bake 1 min at 115 °C
7) develop OCG OPD (4)262 for 1 min
8) hard bake 1 min at 115 °C
9) O₂ descum using PT72 for 0.25 min

**Standard Image Reversal Lithography:**

1) vapour prime wafer with YES oven (HMDS process)
2) while spinning, spray on acetone followed by isopropanol making sure acetone does not dry to remove any photoresist residue
3) OCG 897-7i, 3500 rpm, 40 sec to get a thickness of 0.764 μm, n=1.614
4) solvent bake 1 min at 90 °C
5) expose in 10X stepper with focus 251 and exposure time 2.1 sec
6) image reversal process in YES oven
7) flood exposure for 60 sec
8) develop OCG OPD (4)262 for 1 min
9) O₂ descum 0.5 min to clean PR in exposed areas

P-Contact Metallization:

1) standard image reversal lithography with mask L5 named ridge05.dat (p-contact metallization)
2) oxide etch HCl:H₂O 1:1, 30 sec to prepare surface for immediate metallization, followed by DI-H₂O, and N₂ blow dry
3) evaporation of p-metal 200 Å Pd / 300 Å Pt / 1200 Å Au / 400 Å Pd
4) lift-off unwanted metal by soaking in acetone and blowing acetone with plunger. Then place in isopropanol, followed by DI-H₂O, and N₂ blow dry
5) RTA at 440 °C for 90 sec

Ridge Definition:

1) NH₄OH:H₂O = 1:10 for 15 sec, DI-H₂O, N₂ blow dry to clean surface
2) deposit entire surface with 200 nm of SiO₂
3) standard positive lithography with mask L1 named ridge01.dat (ridge definition)
4) NH₄OH:H₂O = 1:10 for 15 sec, DI-H₂O, N₂ blow dry to clean surface
5) RIE etch of SiO₂ using process 2 on the PT72; claimed etch rate is 325 Å per minute and a selectivity of 2:1 with photoresist
6) Some oxide may form on top of GaAs material, therefore use a 15 sec oxide etch NH₄OH:H₂O = 1:10
7) ECR etch ridge
8) water to remove HCl from the Cl₂ based ECR etch, DI-H₂O, N₂ blow dry
9) remove SiO₂ using PT72

N-Contact Metallization:

1) standard image reversal lithography with mask L2 named ridge02.dat (n-
contact metallization)

2) oxide etch HCl:H2O 1:1, 30 sec DI-H2O, N2 blow dry to prepare surface for immediate metallization

3) evaporate n-contact 750 Å Pd / 1350 Å Ge / 300 Å Ti / 500 Å Pd

4) lift-off unwanted metal by soaking in acetone and blowing acetone with plunger. Then in isopropanol, followed by DI-H2O, and N2 blow dry

5) RTA at 415 °C for 15 sec

SiO2 for P-Contact:

1) NH4OH:H2O = 1:10 for 15 sec, DI-H2O, N2 blow dry to clean surface

2) deposit SiO2 0.5 μm on entire surface

3) standard positive lithography with mask L3 named ridge03.dat (SiO2 deposition for p-contact contact overlay)

4) NH4OH:H2O = 1:10 for 15 sec, DI-H2O, N2 blow dry to clean surface

5) RIE etch of unwanted SiO2

6) remove PR with 30 minute acetone followed by isopropanol, DI-H2O, and N2 blow dry

P-Contact Contact:

1) standard image reversal lithography with mask L4 named ridge04.dat (p-contact contact)

2) oxide etch HCl:H2O 1:1, 30 sec DI-H2O, N2 blow dry to prepare surface for immediate metallization

3) evaporate p-contact contact 200 Å Ti / 500 Å Au

4) lift-off unwanted metal by soaking in acetone and blowing acetone with plunger. Then isopropanol, followed by DI-H2O, and N2 blow dry
References


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