EFFICIENT LINE-CONNECTED VOLTAGE-CONDITIONER WITH MINIMUM DISTURBANCE TRANSFER TO STAND-ALONE MODE

by

Armen Baronijan

A thesis submitted in conformity with the requirements for the degree of Doctor of Philosophy
Department of Electrical Engineering
University of Toronto

©Copyright by Armen Baronijan 1998
The author has granted a non-exclusive licence allowing the National Library of Canada to reproduce, loan, distribute or sell copies of this thesis in microform, paper or electronic formats.

The author retains ownership of the copyright in this thesis. Neither the thesis nor substantial extracts from it may be printed or otherwise reproduced without the author’s permission.

L’auteur a accordé une licence non exclusive permettant à la Bibliothèque nationale du Canada de reproduire, prêter, distribuer ou vendre des copies de cette thèse sous la forme de microfiche/film, de reproduction sur papier ou sur format électronique.

L’auteur conserve la propriété du droit d’auteur qui protège cette thèse. Ni la thèse ni des extraits substantiels de celle-ci ne doivent être imprimés ou autrement reproduits sans son autorisation.
Efficient Line-Connected Voltage-Conditioner with Minimum Disturbance Transfer to Stand-Alone-Mode

Armen J. Baronijan
Department of Electrical and Computer Engineering
University of Toronto, Toronto, Canada

Abstract

This thesis deals with a novel efficient line-connected voltage-conditioning system (VCS) with minimum disturbance transfer to stand-alone mode. The proposed VCS is used for conditioning a terminal voltage of the critical load on the equipment level. It offers advantages over a conventional rectifier-inverter system in terms of efficiency/harmonic generation and over existing line-connected systems in terms of transfer time/dynamic response. To the authors best knowledge, the concept of a solid-state breaker realized with the controlled turn-on/turn-off switch has been introduced for the first time in this thesis. By using the proposed power converter topology, controller structure independent of the load parameters and line-disturbance detection method, the system conforms to the different susceptibility requirements of the critical equipment.

A detailed power circuit and controller description of the proposed current-source-inverter voltage-conditioning system (CSI-VCS) are given. A steady-state analysis of the proposed system is performed including the higher order harmonics. A system controller is designed in order to achieve the two objectives that follow. The first objective is to provide the fast transfer from the line-connected mode to the stand-alone mode in the case of line disturbance. The second objective is to obtain the fast
transient response under load disturbance and to provide, in the steady-state, the output voltage of low total harmonic distortion. Proposed is one algorithm for synchronization to the line voltage fully implemented in software. A novel line-voltage disturbance detection scheme is developed and implemented in software. A 1kVA DSP-controlled laboratory prototype is built to verify the theoretically obtained results. A systematic design procedure and design example are presented and validated using a computer simulation.
Acknowledgments

I wish to express my sincere gratitude and appreciation to my supervisor, Professor S.B. Dewan, for his valuable guidance, encouragement and financial support throughout the preparation of this thesis.

I would like to thank the Professors and friends in Power Group for many useful discussions. Though they are too numerous to list by name, the author is grateful to each of them. I am particularly indebted to Prof. Dawson, Prof. Iravani, Prof. Bonert, Dr. Pande, Dr. Karshenas, Dr. Tripathy, Dr. Krebs and Dr. Namjoshi.

I wish to express my gratitude to my parents Josip and Miroslava for their encouragement and support over all those years of education that culminated into this thesis.

Special appreciation goes to my wife Sofia for her help, understanding and support during my graduate studies and during the preparation of this thesis. I sincerely appreciate her help with editing and drawing the figures.
Dedication

This thesis is dedicated to the memory of my father Josip.
Contents

1 Introduction .................................................. 1
   1.1 Available Solutions and Literature Review ................. 4
   1.2 Problem Definition and Thesis Objectives .................. 5
   1.3 Proposed Solution and Achieved Performance ............... 8
       1.3.1 The Choice of the Inverter Type for the Proposed VCS .... 9
       1.3.2 Achieved Performance .................................. 11
   1.4 Thesis Outline ............................................. 12

2 Description and Operation Modes of a CSI Voltage Conditioning System ....................................... 15
   2.1 Description of the Proposed CSI-VCS ...................... 19
       2.1.1 Power Circuit Description ............................ 19
       2.1.2 System Controller Description ....................... 22
   2.2 Modes of Operation and Typical Waveforms of the CSI-VCS .... 27
2.2.1 CSI-VCS in Line-Connected Mode .................................. 29

2.2.2 Transfer from Line-Connected to Stand-Alone Mode ......... 29

2.2.3 CSI-VCS in Stand-Alone Mode .................................... 35

2.2.4 Transfer from Stand-Alone to Line-Connected Mode ....... 38

2.3 Experimental Setup of the CSI-VCS ............................... 41

2.3.1 Power Circuit Experimental Setup ............................... 41

2.3.2 System Controller Experimental Setup .......................... 43

3 Steady-State Analysis of a CSI Voltage Conditioning System ..... 48

3.1 Steady-State Analysis of the CSI-VCS in Line-Connected Mode ... 51

3.2 Steady-State Analysis of the CSI-VCS in Stand-Alone Mode ..... 56

4 Design of a CSI-VCS Controller ..................................... 76

4.1 Description of the CSI-VCS Controller ............................ 78

4.2 CSI-DC-Chopper Unit Controller Design ......................... 82

4.2.1 CSI Controller Design ........................................ 85

4.2.2 DC-Chopper Controller Design ................................ 97

4.3 Static-Switch Controller Design ................................ 106

5 Design Procedure and Design Example ................................ 113

5.1 Design of the Output Filter and the DC-link Current Reference ... 116

vi
5.2 DC-link Inductor Design ........................................... 120
5.3 Design of the AC-link Inductor ................................. 121
5.4 Design of the Static-Transfer-Switch Snubber Circuit ..... 124
5.5 Design Procedure .................................................. 125
5.6 Design Example ..................................................... 128
  5.6.1 Design Specifications of a 10kVA CSI-VCS .............. 129
  5.6.2 Design of a 10kVA CSI-VCS ............................... 130
  5.6.3 Simulation Results for a 10kVA CSI-VCS ............... 132

6 Conclusions .......................................................... 143

A System Parameters of a CSI-VCS .............................. 147
  A.1 System Specifications ........................................... 147
    A.1.1 Rated Values ............................................... 147
    A.1.2 Base Values ............................................... 148
  A.2 System Parameters ............................................. 149
    A.2.1 Components in the Power Circuit ....................... 149
    A.2.2 Parameters of the Voltage Sources .................... 150
    A.2.3 Parameters Related to System Implementation .......... 150
    A.2.4 Controller Parameters .................................... 150
B  Output Voltage Reference Synchronization 151

C  Line Disturbance Detection Method 160

D  Digital Implementation of PWM for DC-chopper and CSI 176

Bibliography 189
List of Principal Symbols

**Currents**

\[ iload \] - Load current
\[ i_C \] - Output filter capacitor current
\[ i_{inv} \] - Current source inverter output current
\[ i_s \] - Line current
\[ i_d \] - DC-link current
\[ I_{d,ref} \] - DC-link current reference

**Voltages**

\[ v \] - Output voltage
\[ v_s \] - Line voltage
\[ v_{inv} \] - Current source inverter input voltage
\[ v_{cho} \] - DC-chopper output voltage
\[ v_{ref} \] - Output voltage reference
\[ V_d \] - DC-chopper input voltage

**Circuit Components**

\[ S_s \] - Solid-state breaker switch
\[ S_d \] - DC-chopper switch
\[ S_1, \ldots, S_4 \] - Current source inverter switches
\[ D_d \] - DC-chopper diode
\[ D_1, \ldots, D_4 \] - Solid state breaker diodes
\[ D_s \] - Solid state breaker snubber diode
Circuit Impedances

\( C \) - Output filter capacitance
\( L_d \) - DC-link inductance
\( R_d \) - DC-link resistance
\( L_{ac} \) - AC-link inductance
\( R_{ac} \) - AC-link resistance
\( R_s \) - Solid-state breaker snubber resistance
\( C_s \) - Solid-state breaker snubber capacitance
\( L_e \) - AC-source internal inductance
\( R_e \) - AC-source internal resistance

Frequencies

\( f \) - Fundamental frequency
\( w \) - Fundamental angular frequency
\( f_s \) - Switching frequency of the inverter and DC-chopper

Control Signals

\( c_{CSI} \) - Current source inverter control signal
\( c_{cho} \) - DC-chopper control signal

Transfer Functions

\( P_{CSI} \) - CSI transfer function
\( K_{CSI} \) - CSI controller transfer function
\( S_{CSI} \) - CSI sensitivity function
\( T_{CSI} \) - CSI complementary sensitivity function
$P_{cho}$ - DC-chopper transfer function
$K_{cho}$ - DC-chopper controller TF in the feedback path
$F_{cho}$ - DC-chopper controller TF in the forward path
$T_{cho}$ - DC-chopper complementary sensitivity function
$R_{cho}$ - Input disturbance sensitivity function

**Switching Functions**

$SW_{CSI}$ - CSI switching function
$SW_{cho}$ - DC-chopper switching function

**Miscellaneous**

$m_a$ - Amplitude modulation index
$m_f$ - Frequency modulation index
$T_c$ - Switching period
Chapter 1

Introduction

Voltage conditioners are commonly used in industry in order to improve the power quality delivered to the sensitive equipment which cannot withstand power disturbances. The power quality requirement is usually expressed in the form of the susceptibility curve which gives the permissible supply voltage variation for a given time duration. In general, the susceptibility curve should be defined for a specific load. A guideline for design of the operational range for sensitive equipment is given by the CBEMA curve[3], shown in Figure 1.1.

In order to satisfy the susceptibility requirements of the sensitive equipment, two different types of voltage conditioning systems (VCSs) are used. These are: stand-alone type and line-connected type.

The stand-alone VCS[41, 42, 43, 45] is realized as a serial rectifier-inverter type. The disadvantage of this type of VCS is the low efficiency due to the power loss in the converter stage.

The line-connected VCS[4, 5, 6, 7] is used to provide higher energy efficiency than the stand-alone type. There are two problems related to the practical realization of
Figure 1.1: An envelope of voltage tolerances that is representative of
the present design goal of a cross section of the electronic
equipment manufacturing industry[3].

to the existent line-connected VCSs. First, they can not clear the short-circuit on the
line side. Second, after detecting that the line-disturbance has reached the threshold
limit, the system has to wait for the line-current to drop to zero before it switches to
the stand-alone mode. This makes the system unable to conform to the susceptibility
requirements specified by the CBEMA curve. Both of the problems are related to
the static-switch configuration which is realized as an anti-parallel connection of two
thyristors.

In order to overcome these drawbacks, in this thesis, a novel line-connected VCS
is proposed. The aforementioned problems of existing line-connected VCSs are solved
by using a controlled turn-on-turn-off switch(IGBT) as the circuit-breaker, which to
the author's best knowledge has not been reported in the literature.

Under normal operating conditions, the proposed system operates in the line-connected mode. If the line voltage disturbance threshold limit is reached, the static-switch instantly cuts-off the line. This, in turn, provides the minimum disturbance transfer to the stand-alone mode which conforms to the susceptibility requirements specified by the CBEMA curve. By doing so, the efficient operation is provided without any penalty in the performance during the transfer. In addition, the proposed system operating in line-connected mode can conform to even more stringent susceptibility requirements during the transfer than the ones given by the CBEMA curve.

In the case of reaching the line voltage disturbance threshold limit, the proposed system switches to the stand-alone mode. In stand-alone mode, the necessary load disturbance rejection is provided and the tight output voltage tolerances are satisfied.

Based on these characteristics, the proposed topology, unlike the existing voltage conditioning equipment, provides efficient operation and the performance which satisfies the requirements specified by the CBEMA curve.

The issues discussed so far are elaborated in the following sections of this chapter. The existing VCSs and literature review are given in Section 1.1. The problems associated with the realization of line-connected VCSs which provide minimum disturbance transfer to stand-alone mode are identified and thesis objectives are stated in Section 1.2. The proposed solution and achieved performance are discussed in Section 1.3. Finally, in Section 1.4, the thesis outline is given.
1.1 Available Solutions and Literature Review

In the early stage of static-voltage-conditioning-equipment development the following three basic concepts were under consideration: the continuity of energy supply, the quality of the voltage wave and the rate of availability (reliability) [41]. The proposed configuration that best satisfied the three aforementioned concepts is shown in Figure 1.2 in the form of a block diagram. In the case of a conventional stand-alone connection type of voltage conditioning equipment [11, 21, 35, 40, 36, 37, 41, 42, 43, 45, 55, 57, 58, 59, 64], the rectifier supplies power to the inverter while charging the battery. AC power of fixed frequency and fixed amplitude is supplied to the load by the inverter. This traditional configuration is discussed in numerous papers [41, 42, 43, 45]. The drawback of this configuration is the low efficiency which results because of losses in the power converter stage.

![Block Diagram](image)

**Figure 1.2:** A simplified block diagram of a conventional stand-alone connection type of voltage conditioning equipment.

In the late 1970's a line-connected inverter system named TRIPORT [4, 5, 6, 7] was introduced for the first time by Bell Laboratories to provide higher energy efficiency than the traditional serial rectifier-inverter VCS. The line-connected inverter system [8, 9, 10] is shown in Figure 1.3 in the form of a block diagram. It has two modes of operation. In the line-connected mode, under normal operating conditions, power obtained from the AC line is delivered directly to the load. In the case of an AC
input power failure, the line connected inverter system switches to the stand-alone mode, the static-switch after line-current zero-crossing cuts-off the utility line and the inverter takes over the load.

![Block Diagram](image.png)

Figure 1.3: A simplified block diagram of line-connected type of voltage conditioning equipment.

The existing line-connected VCSs can not satisfy the susceptibility requirements specified by the CBEMA curve. This is due to the fact that after detecting a disturbance on the line, the VCS has to wait for the line current to decrease to zero in order to transfer to the stand-alone mode. Furthermore, the existing VCSs can not clear the short circuit on the line side.

### 1.2 Problem Definition and Thesis Objectives

In order to build a line-connected VCS with minimum disturbance transfer to the stand-alone mode, the system functions have to be identified. Based on these functions, the thesis objectives are defined.

The basic algorithm for controlling a line-connected voltage conditioning system is shown in Figure 1.4, in the form of a flow-chart.
Figure 1.4: A basic algorithm for controlling the proposed line-connected voltage-conditioning system.

The sensing of the line and load voltages and currents is performed in the first place, so that the decision on the operation mode of the static-switch and the inverter can be made.

The function of the static-switch is to isolate an AC input source from feeding the load in the case of a line voltage disturbance. For controlling the on-off state of the static-switch, the threshold disturbance detection takes place in the second step of the control algorithm. The decision is based on the measurements of the load current (short-circuit detection on the line side) and AC-line voltage quality evaluation (line voltage disturbance detection algorithm).

Based on the on-off state of the static-switch, the two different modes of operation of the inverter VCS are distinguished, namely line-connected mode and stand-alone
In line-connected mode, the line voltage is not regulated by the inverter, and is used to power the load. The amplitude of the output voltage reference is set to the desired value and is synchronized to the input line voltage.

In stand-alone mode, AC power is supplied to the load only by the inverter. The output voltage reference of desired amplitude and frequency is generated and synchronized to the line voltage in the case of reaching the input voltage disturbance threshold limits. In the case of the mains outage, this reference is free-running and is synchronized to the line after the AC-line voltage recovery. Using the output voltage reference and output voltage measurement, the feedback control provides the fixed amplitude, fixed frequency AC power to the critical load under varying load conditions.

The main objective of this thesis is to provide the analysis, modeling, control strategy, design and implementation of a single-phase voltage-conditioning system which performs the aforementioned functions. To achieve this objective, the following research is conducted in this thesis:

1. The reliable detection method of the line disturbance threshold limits is developed in order to determine the optimum mode of operation of the system in real-time.

2. The static-transfer switch with a bidirectional current flow handling capability is proposed and the method for its instantaneous on-off control is developed.

3. The robust output voltage controller is designed to provide a fast transient response under varying load conditions in the stand-alone mode.

4. The method for the output voltage synchronization with the input AC-line is developed.
5. An organized analysis, design and evaluation approach for a single-phase voltage conditioning system, in stand-alone and line-connected modes is developed.

6. The steady-state characteristics of the proposed voltage conditioning system are investigated, in order to determine the configuration circuit component ratings.

7. The system model suitable for the analysis and design of the controller of a single-phase VCS is developed in continuous-time.

8. The time-domain computer simulation code for a single-phase voltage conditioning system is developed.

9. The systematic design procedure for a single-phase voltage conditioning system is proposed and a design example is presented.

10. The experimental verification is performed and the measured values are compared with the predicted simulation results of the proposed voltage conditioning system.

1.3 Proposed Solution and Achieved Performance

The proposed line-connected voltage-conditioning system is shown in Figure 1.5 in the form of a block diagram. The basic structure is the same as of the existing line-connected VCSs except for the static-switch topology. Instead of using the anti-parallel connection of two thyristors, the proposed static-switch is realized with the controlled turn-on/turn-off switch $S_s$ and four diodes $D_1, \ldots, D_4$, connected in the bridge configuration. The snubber circuit which consists of diode $D_s$, resistor $R_s$ and capacitor $C_s$ is used to limit the voltage across the switch $S_s$ during its turn-off. The proposed static-switch topology provides the means for instantaneous cut-off of the line.
The static-switch configuration shown in Figure 1.5 is providing the function of instantaneous cut-off of the line with the minimum number of switches. The alternate configuration for the static-switch which minimizes the on-state loss is the anti-parallel combination of IGBT switch with a diode in series.

1.3.1 The Choice of the Inverter Type for the Proposed VCS

The concept of voltage-conditioning and the feasibility of fast transfer proposed in this thesis are both valid apart from the type of the inverter which is used. It is apparent that either voltage-type or current-type inverter can be used in the proposed voltage-conditioning system. In this thesis the current-source inverter (CSI) is selected for the reason that is discussed next.

A simplified power circuit diagrams of the VCS's using current-type and voltage-type inverters are shown in Figure 1.6 and 1.7, respectively. Based on these power circuit diagrams, a simplified failure analysis has been performed, and the following has been concluded. In the case of a single-switch failure (short-circuit through one of the switching devices), a current source-type inverter is able to provide the continuity of energy supply by operating in the line-connected mode. This is due to the fact that in a current-type inverters the voltage across the output filter capacitor is not
influenced by the inverter input voltage. In the case of a single-switch failure, a voltage-type inverter has to have some means of actively disconnecting the inverter from the output in order to continue operating in line-connected mode. This is due to the fact that the output voltage of a voltage-type inverter is defined by the input voltage to the inverter. This would require an active switch at the output terminals of the VSI, further increasing the complexity of the system.

Figure 1.6: A simplified power circuit diagram of a VCS using a current-type inverter.

Based on this simplified failure analysis, the CSI is selected as the preferable inverter-type for the proposed VCS. This is in order to improve the availability and provide the continuity of energy supply. The choice of the optimal inverter type for
VCS is out of the scope of this thesis. Only the complete analysis of both VSI and CSI can show the complete set of advantages/disadvantages for each topology.

1.3.2 Achieved Performance

The achieved performance of the proposed CSI-VCS is discussed in this section with the help of Figure 1.8.

![Allows voltage supply amplitude variations versus time duration](image)

Figure 1.8: Allowable voltage supply amplitude variations versus time duration:

a) provided by the CSI-VCS operating in the line-connected mode,

b) provided by the CSI-VCS operating in the stand-alone mode and
c) specified by the CBEMA curve.

In line-connected mode and during the transfer to stand-alone mode, the proposed CSI-VCS satisfies susceptibility requirements specified by curve b) shown in Figure
1.8. It can be seen that these requirements are more stringent than those specified by the CBEMA curve shown in Figure 1.8 c). This means that the proposed system provides the efficient operation in line-connected mode under normal operating conditions and performs the transfer to stand-alone mode which complies with the susceptibility requirements that are more stringent than the ones specified by the CBEMA curve. This allows the CSI-VCS to operate in the line-connected mode and perform efficient operation as long as the line voltage is inside the specified permissible limits.

In stand-alone mode, necessary load disturbance rejection with the CSI-VCS is achieved within one sampling period. This is shown by curve a) in Figure 1.8. The small area around the origin represents the voltage variation versus time duration which the CSI-VCS tolerates under varying load conditions. The straight line of zero amplitude extended over the time interval (sampling period,∞) represents the zero steady-state error achieved after only one sampling period.

In summary, the CSI-VCS proposed in this thesis offers the advantages in terms of efficiency, transfer time and dynamic behavior over the existing voltage-conditioning systems.

1.4 Thesis Outline

This thesis consists of six chapters and five appendices. In this chapter, the motivation for this thesis is outlined, the problem is defined, the literature overview is given and the thesis objective and thesis outline are presented.

In Chapter 2, a description of the proposed single-phase, current-source-inverter (CSI) voltage-conditioning-system(VCS) is given. Both power circuit and controller diagrams are presented and the function of each part or block on the diagram is
described. The operation of the system in line-connected and stand-alone modes is described and characteristic voltage/current waveforms are presented. A transfer between line-connected mode and stand-alone mode is discussed. Furthermore, a 1kVA laboratory prototype used in this thesis to verify all the theoretical results is described.

In Chapter 3, a model of the proposed CSI-VCS in the time-domain is derived. In order to determine the power flow in the system and ratings of the system components, a steady-state analysis of the proposed CSI-VCS is performed. Based on Fourier analysis, the expressions for all voltage/current waveforms of the CSI-VCS power circuit are derived. In order to verify this analysis, the operation of a proposed single-phase CSI-VCS is simulated and the experiments on a 1kVA laboratory prototype are performed. The simulation results are verified by experiment.

In Chapter 4, a P-controller for the CSI and a PI-controller for the DC-chopper are designed. Both controller are designed in continuous time using the loopshaping technique. The simulation/experimental results, demonstrating the dynamic behavior of the system in stand-alone mode under load disturbances, are shown. The static-transfer-switch on/off controller is designed and simulation/experimental results during the transfer are presented.

In Chapter 5, a design procedure and design example of a single-phase CSI-VCS are presented. The system analysis presented in Chapters 2, 3 and 4 is used to design a CSI-VCS with a 10 kVA rating. The design procedure and design example are validated by the simulation package PECAN.

In Chapter 6, the conclusions and contributions of the thesis are summarized and future research work is suggested.

In Appendix A, the parameters of a 1kVA CSI-VCS used for the simulations/experiments are given. Design specifications for a 1kVA system are given and based on the design
procedure, the system parameters are calculated.

In Appendix B, an algorithm used in this thesis for creating the output voltage reference which is synchronized to the line voltage is proposed. The FIR-filter used for zero-crossing detection of the line-voltage is designed first. Next, the mechanism for generating the free-running output voltage reference in the case of a line-voltage outage is described. Finally, the synchronization procedure after the line-voltage recovery is proposed.

In Appendix C, a scheme for detecting the disturbances on the line is proposed. First, the output voltage relative error is defined. Next, using the integral error method, the quality of a line voltage is quantified. Finally, the line-voltage disturbances are simulated/created and the simulation/experimental results, demonstrating the performance of the detection algorithm, are shown.

In Appendix D, a digital implementation of the PWM scheme used for driving the DC-chopper and CSI switches is presented. The hierarchy of graphic design files and files itself, designed by MAX-PLUSII from Altera, are also presented.
Chapter 2

Description and Operation Modes of a CSI Voltage Conditioning System

In this thesis, a high-efficient VCS with fast transfer time used for improving the quality of the power delivered to sensitive electronic equipment has been proposed. The need for introducing this system has been stated in the thesis introduction. In order to provide the insight to the voltage conditioning system structure and to obtain a better understanding of the system performance, this chapter includes a description and operation of the proposed line-connected, single-phase voltage conditioning system realized with the current-source inverter (CSI). In addition, this chapter serves as the basis for the steady-state analysis and controller design of the system performed in the subsequent chapters. This system consists of a power circuit which converts electrical power from DC to AC side in the case of the line voltage/current disturbance and a controller which takes care of the way this transfer/conversion process is performed. The overall system structure is shown in Figure 2.1 in the form of the
The system consists of three main building blocks: AC and DC power sources, CSI voltage conditioning system and a load.

The AC-power-source is the main system power source which supplies the energy to the load under normal operating conditions and is provided by the utility. The DC-power source serves as the backup power source in the case of the AC-mains disturbance or failure.

The function of the CSI voltage conditioning system is to provide AC-voltage of fixed amplitude and frequency in the case of the main AC-power source disturbance or failure. It consists of the power circuit, voltage and current sensors and the system controller.

In Section 2.1, the power circuit and the controller diagram of the CSI voltage conditioning system are presented and the function of each part or block on the diagrams is defined in order to describe main operating functions of the system components.

The power circuit of the proposed power supply system consists of a one-quadrant chopper, a DC-link inductor, a full-bridge single-phase CSI, static-transfer-switch, AC-link inductor and an output filter. A detailed description of the performed function and configuration for each section of the power circuit is given.

The system controller performs the following functions: output voltage synchronization, line voltage disturbance detection, static-switch control, output voltage control and DC-link current control. In order to provide the output voltage reference waveform, a novel output voltage synchronization algorithm has been proposed. A novel line voltage disturbance detection algorithm is developed which is able to decide on the main mode of the system operation (stand-alone or line-connected). This decision is made based on the design specifications or susceptibility curve of the crit-
Figure 2.1: A simplified block diagram of a line-connected single-phase CSI voltage conditioning system with AC and DC power sources and the load.

The function of the voltage controller is to provide a fixed frequency, fixed amplitude output voltage waveform with low total harmonic distortion (THD) during steady-state operating conditions, and small overshoot/undershoot with fast response under load transient conditions. The DC-chopper current controller is providing a constant DC-link current to the CSI under
all operating conditions of the system. The block diagram, structure and function of each of the controllers are described in Section 2.1.2.

In Section 2.2, the basic operating principles of the proposed voltage conditioning system are described. The system is operating in line-connected mode under normal operating conditions. Under the line voltage disturbance or short circuit on the line side, the system controller initiates the transfer to stand-alone mode. This is in order to provide the controlled and reliable power flow to the critical load. So, the system operation in line-connected and stand-alone mode is described and typical waveforms are presented in this section. The transfer modes from line-connected to stand-alone mode in the case of the line voltage disturbance and return to the line after its recovery are discussed. The operation of the system is simulated using the simulation package for power electronic circuits (PECAN). The simulation and experimental results of the proposed voltage conditioning system, for all operating modes, are presented and compared in the case of a 1kVA laboratory prototype.

In section 2.3, an experimental 1kVA laboratory prototype used to verify the operation of the proposed CSI-VCS is described. The modular structure is used for the power circuit realization. The separate power units have been used in the experiment for DC-chopper, CSI and static-switch. All of the modules are built using IGBT's as main switches. The digital implementation of the system controller has been used for the reasons stated in the introduction of this thesis. The controller of the proposed voltage conditioning system is realized with the A/D boards [30], DSP-based controller-board UHP 40 [28], and the level shifter board, all developed at the University of Toronto. The control algorithm, implemented in software, is developed in C. In order to tune-up the controller parameters, set the reference values and monitor the internal values of the main controller processor TMS320C40, the fast serial communication "Hot-Link" interface [29] between the system controller and the host-PC is established and described in this section.
2.1 Description of the Proposed CSI-VCS

In this section the power circuit and system controller description are given and the function of each of the CSI-VCS building blocks is defined.

In Section 2.1.1, a simplified power circuit diagram of the proposed voltage conditioning system is shown and the configuration and function of the building blocks are presented.

In Section 2.1.2, the proposed control structure is identified and the main structure and function of different controller sections are defined.

2.1.1 Power Circuit Description

The proposed power circuit system consists of a one-quadrant DC-chopper, DC-link inductor, a single-phase CSI, static-switch, AC-link-reactor and output filter. A simplified power circuit diagram of the proposed voltage conditioning system with DC-voltage source, AC-mains connected and the load is shown in Figure 2.2.

A DC-chopper with square wave output voltage is a DC-voltage to current converter. It consists of the main switch $S_d$ and the diode $D_d$. By appropriate switching of the main switch $S_d$, the chopper provides a constant DC-link current $i_d$ in spite of all load disturbances or input voltage changes. It normally operates in two modes: the duty interval and the freewheeling interval, during a chopping cycle. During the duty interval the main switch $S_d$ is on and the chopper output voltage $v_{\text{cho}}$ is $V_d$. During the freewheeling interval the diode $D_d$ is conducting while the switch $S_d$ is off, and chopper output voltage $v_{\text{cho}}$, is zero. Providing unipolar square wave output voltage and constant DC-link current, it operates in the first quadrant of the I-V plane.
Figure 2.2: A simplified power circuit diagram of a line-connected single-phase CSI voltage conditioning system with the DC-voltage source and the load.

The function of the DC-link inductor $L_d$ is to exhibit high impedance current source characteristic required for the CSI. It also limits the ripple factor of the DC-link current waveform $i_d$ to a prescribed level. Since the output of the CSI is connected to the load through output filter $C$, the value $L_d$ is not affected by the nature of the load. So, the value for $L_d$ is affected only by the CSI and DC-chopper switching frequencies and a predefined ripple factor for the DC-link current.

The main function of the CSI is to convert the DC-link current $i_d$ into phase
AC-current $i_{\text{load}}$ through output filter capacitor $C$. It has inherent four quadrant capability. It is simple in construction, and is realized with the same self-commutated switching devices $S_1, \ldots, S_4$ as DC-chopper. Using the switching devices that can not support reverse voltage, a suitable diode must be connected in series.

The load filter $C$ provides low harmonic distortion of the output voltage waveform $v$, while drawing from the CSI minimal possible reactive power. The load is assumed to be linear with lagging power factor.

In order to isolate the AC-source feeding the short-circuit on the load side and to isolate the CSI feeding the short-circuit on the AC-line side, the static-transfer switch has been used. It consists of switch $S_s$ and four diodes $D_1, \ldots, D_4$ in the diode bridge configuration. In the line-connected mode the main switch $S_s$ is on and the diodes $D_1, \ldots, D_4$ provide the path for both positive and negative half-cycles of the line-current $i_s$. In the stand-alone mode of the system operation the main switch $S_s$ is off, disconnecting the AC-source from the load.

In the case of the system transfer from the line-connected to stand-alone mode, the snubber circuit which consists of diode $D_s$, resistor $R_s$ and capacitor $C_s$ is used to limit the overvoltage across the switch $S_s$ while the current through the switch turns off. Since the static-switch is designed to provide the means of instantaneous cut-off of the AC-line, the accumulated energy stored in the AC-link reactor $L_{ac}$ is transferred to the snubber capacitor $C_s$ through diode $D_s$ during the turn off of the switch $S_s$. The snubber capacitor $C_s$ stays charged as long as the CSI-VCS is operating in the stand-alone mode and it starts discharging through the resistor $R_s$ and switch $S_s$ as soon as the line-connected mode is resumed.

The function of the AC-link reactor $L_{ac}$ is to limit the rise of the current when the short-circuit on the line side occurs. It has to be large enough to limit the rise of the current under fault conditions on the line side and small enough, so that the
output voltage $v$ is within specified steady-state limits.

2.1.2 System Controller Description

The function of the CSI-VCS is to provide the fixed amplitude, fixed frequency output voltage waveform in the steady-state and small under/overshoot under line and load disturbances. Furthermore, in order to provide the efficient transfer of energy from the power source to the load, the energy provided for the load is obtained from the AC-source under normal operating conditions. Under line disturbances the function of the CSI-VCS is to condition the output voltage and compensate for these interruptions. This task of monitoring the states of the system, processing the data, making the decisions on the mode of the system operation and conditioning the load voltage is performed by the system controller. This is in order to provide uninterruptible power to the critical load in an efficient, reliable and controllable manner.

The proposed CSI-VCS controller block diagram is shown in Figure 2.3. The main blocks are the output voltage reference synchronization, line voltage disturbance detection, output voltage controller, static-switch controller, DC-chopper controller and PWM for CSI/DC-chopper. The function of each controller block is described in the following sections.

In order to provide the output voltage reference $v_{ref}$ which is synchronized to the line voltage $v_s$, the following procedure has been proposed in this thesis. First, the zero crossings of the line voltage have been detected. Second, the voltage reference look-up table has been created for the nominal frequency of 60Hz and is reinitialized periodically by each incoming zero crossing event. In addition, the mechanism for providing the free-running voltage reference in the case of the line voltage blackout is provided. Finally, the voltage reference look-up table for 61Hz has been created in order to compensate for the phase shift between the line voltage and output voltage.
Figure 2.3: A simplified block diagram of a line-connected single-phase CSI voltage conditioning system controller.

Reference in the case when line voltage has resumed after the outage. The reason for using the look-up table for 61Hz and other details of the algorithm performing the synchronization procedure are given in Appendix B of this thesis.

The line voltage disturbance detection has taken place in the control algorithm in order to determine the optimal mode of operation of the system at any given time. The algorithm structure used for line voltage disturbance detection is shown in the form of the block diagram in Figure 2.4. The line voltage $v_s$ has been sensed and compared with the output voltage reference $v_{ref}$ in order to define the relative error $\text{error}_{rel}$ of the line voltage. In order to evaluate the weight of the relative error of the line voltage, the susceptibility curve of the electronic equipment which the CSI-VCS
is conditioning has to be known in advance. To do so, the relative error $error_{rel}$ is calculated and weighted in such a way that the weighted error (relative error multiplied by its weight) integrated over time is reaching the disturbance threshold limit exactly after the time interval specified by the equipment susceptibility curve.

![Diagram](https://via.placeholder.com/150)

Figure 2.4: The basic structure of the line voltage disturbance detection block shown in Figure 2.3.

In order to provide the output voltage waveform of fixed amplitude/frequency with a good transient response, the robust controller with the feedforward structure has been used in this thesis. The problem of load disturbances is treated by incorporating a feedforward load current loop (measured value of the load current $i_{load}$) with fast acting output capacitor current feedforward (calculated value of the output filter current $i_{C,ff}$). This is used in addition to the standard feedback output voltage control structure shown in Figure 2.5. The proportional controller is used for the output voltage control-loop. The output voltage control block produces the control signal $c_{CSI}$ based on the difference between the reference output voltage waveform $v_{ref}$ and the actual output voltage waveform $v$. In order to drive the CSI, the control signal $c_{CSI}$ is fed to the SPWM modulator and the switching functions $SW_{S1}, \ldots, SW_{S4}$ for CSI switches $S_1, \ldots, S_4$ are generated. The proposed control strategy provides
excellent dynamic response in the advent of load disturbances.

![Diagram](image)

Figure 2.5: The basic structure of the output voltage controller block shown in Figure 2.3.

The function of the DC-chopper controller is to provide the constant DC-link current $i_d$ under all operating conditions of the system. It is realized with a lag-lead controller and an integrator in the feedback-path, as shown in Figure 2.6. The reference DC-link current $I_{d,ref}$ is compared with the measured DC-link current $i_d$ and the error signal is fed to the controller. The obtained control signal $c_{cho}$ at the output of the regulator is fed to the PWM modulator in order to produce switching function $SW_{S_d}$ for driving the DC-chopper switch $S_d$.

![Diagram](image)

Figure 2.6: The basic structure of the DC-chopper controller block shown in Figure 2.3.
The static-switch controller is an on/off controller of the main static-transfer switch \( S_2 \). The decision on the on/off state of the switch is based on the line-current/line-voltage disturbance threshold limits and status of the synchronization provided by the \texttt{sync\_flag} signal. This is shown in the form of the logic/block diagram in Figure 2.7. The transfer to stand-alone mode is initiated (signal \texttt{set} becomes high) by reaching either line voltage (signal \texttt{transfer} high) or line current threshold limits (signal \texttt{curr\_flag} high). This status of the output signal \( SWS_2 \) is held using the hold line. The return to the line, after the fault has been cleared, is performed after the \texttt{sync\_flag} is set and when both \texttt{transfer} and \texttt{curr\_flag} are reset (signal \texttt{reset} becomes low). This sets the \texttt{reset} signal, which in turn sets the gating signal \( SWS_2 \) for the static-switch \( S_2 \).

![Logic/block diagram](image)

Figure 2.7: The basic structure of the static-switch controller block shown in Figure 2.3.
2.2 Modes of Operation and Typical Waveforms of the CSI-VCS

The main operating features in different modes of system operation are defined in this section. Steady-state simulation and experimental results for each of the CSI-VCS operation modes are presented. In addition, the operation of the proposed system during the transition from one mode to another has been discussed and characteristic waveforms are presented. The power circuit parameters of the system used throughout this chapter for the simulation and experimental setup are shown in Figure 2.8.

Based on the line current and line voltage disturbance threshold limits and CSI-VCS specifications, two different modes of the system operation are distinguished:

- Line-connected mode, and
- Stand-alone mode.

Under normal operating conditions the CSI-VCS operates in the line-connected mode. In this way the power to the load is delivered from the AC-mains, providing efficient energy transfer. In the case of the disturbance on the line side, the proposed system switches to stand-alone mode. This is in order to condition the output voltage seen by the critical load. The system operates in stand-alone mode as long as the line voltage is out of specifications tolerable by the load. As soon as the line voltage recovers, the CSI-VCS switches again to the line-connected mode. The details of the system operation in line-connected and stand-alone mode, as well as the transitions from one to another mode are presented in the following paragraphs.
<table>
<thead>
<tr>
<th>Component</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>$D_1, \ldots, D_4$</td>
<td>R411-1240, IR</td>
</tr>
<tr>
<td>$S_1, \ldots, S_4$</td>
<td>CM400HA-12H, Powerex</td>
</tr>
<tr>
<td>$S_d, D_d$</td>
<td>PM50RSA120, Powerex</td>
</tr>
<tr>
<td>$S_s$</td>
<td>CM400HA-12H, Powerex</td>
</tr>
<tr>
<td>$V_s$</td>
<td>115V $\pm$ 20% -13%</td>
</tr>
<tr>
<td>$V$</td>
<td>115V $\pm$ 10% -6%</td>
</tr>
<tr>
<td>$S$</td>
<td>1kVA</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_d$</td>
<td>220V</td>
</tr>
<tr>
<td>$R_{d/L_d}$</td>
<td>0.1$\Omega$/10mH</td>
</tr>
<tr>
<td>$C$</td>
<td>100$\mu$F</td>
</tr>
<tr>
<td>$C_s$</td>
<td>3600$\mu$F</td>
</tr>
<tr>
<td>$R_s$</td>
<td>50$\Omega$</td>
</tr>
<tr>
<td>$R_{ac} + R_e$</td>
<td>0.2$\Omega$</td>
</tr>
<tr>
<td>$L_{ac} + L_e$</td>
<td>2mH</td>
</tr>
</tbody>
</table>

Figure 2.8: A power circuit schematic diagram of the line-connected single-phase CSI-VCS with the parameters used in the experiment.
2.2.1 CSI-VCS in Line-Connected Mode

Under normal operating conditions the proposed CSI-VCS operates in the line-connected mode. The overall system structure in this mode of operation is shown in Figure 2.8 with the static-transfer-switch $S_s$ in the on-state. The power to the load is delivered by the utility i.e. AC-mains in this case. The line current $i_s$ is flowing through the diode rectifier $D_1, \ldots, D_4$ and switch $S_s$. The snubber capacitor $C_s$ is discharged and snubber diode $D_s$ and resistor $R_s$ are not conducting. The line current $i_s$ is split into the load current $i_{load}$ and output filter capacitor current $i_C$.

The DC-chopper and CSI are inactive in this mode, which means that switches $S_1, \ldots, S_4$ and switch $S_d$ are off. The DC-link current $i_d$ and inverter output current $i_{inv}$ are zero.

The characteristic waveforms of the proposed CSI-VCS in this mode of operation are presented in Figure 2.9 (simulation results) and in Figure 2.10 (experimental results). The parameters of the system used for the simulation and experimental results are shown in Figure 2.8. As can be seen, the output voltage $v$ and load current $i_{load}$ are sinusoidal. The load current $i_{load}$ is 36deg lagging the output voltage $v$ since the load power factor is 0.8. The complete agreement between simulation and experimental results can be observed.

2.2.2 Transfer from Line-Connected to Stand-Alone Mode

In the case of the line voltage/current disturbance, the proposed CSI-VCS switches to stand-alone mode. This is in order to provide the output voltage of required quality on the load side.

Whenever the disturbance threshold limit on the line side is reached, the CSI-VCS controller sets the command for transfer of the system to stand-alone mode. This
Figure 2.9: Simulation Results: Characteristic output voltage $v$ and load current $i_{load}$ waveforms of the proposed CSI-VCS shown in Figure 2.8 and operating in line-connected mode.
Figure 2.10: **Experimental Results:** Characteristic output voltage $v$ and load current $i_{load}$ waveforms of the proposed CSI-VCS shown in Figure 2.8 and operating in line-connected mode.
command initiates two parallel processes: turning off the static-switch and turning on the CSI-VCS.

The process of turning off the static-switch begins with turning off the switch $S_s$. This initiates the transfer of the accumulated energy in the AC-link reactor $L_{ac}$ to the snubber capacitor $C_s$. The path for this transfer is provided through the snubber diode $D_s$ which conducts the line current $i_s$ during the commutation process. At the same time, this snubber circuit prevents the excessive overvoltage across the switch $S_s$ during its turn-off.

The process of turning on the CSI-VCS starts with setting the DC-link current reference $I_{d,ref}$. In response to this step command, the DC-chopper starts modulating the DC-voltage $V_d$ in order to build the DC-link current $i_d$ through the DC-link inductor $L_d$. Using the SPWM, the CSI starts delivering energy to the critical load. The line current $i_s$ starts decreasing to zero, while the CSI output current $i_{inv}$ starts delivering the required load current $i_{load}$ and output filter current $i_C$.

The characteristic waveforms of the CSI-VCS shown in Figure 2.8, during the transition, are presented in Figure 2.11(simulation results)/Figure 2.12(experimental results). In Figure 2.11 a) the overvoltage of 10% has been detected in the line voltage 81 milliseconds prior to the transfer. The resulting overvoltage in the output voltage waveform $v$ can be seen on the same Figure 2.11 b)(simulation results)/Figure 2.12 b)(experimental results). After detecting that the output voltage $v$ has been out of the specifications for critical amount of time, the system controller initiates the transfer signal. This is manifested by setting the DC-link current reference $I_{d,ref}$ and switching off the switch $S_s$ at $t = 58 ms$, shown in Figure 2.11 c)(simulation results)/Figure 2.12 c)(experimental results). In response to this command, the DC-link current $i_d$ starts building up(Figure 2.11 c)(simulation results)/Figure 2.12 c)(experimental results)) and energy accumulated in the AC-link inductor $L_{ac}$ starts transferring to the snubber capacitor $C_s$, then charging it. At the same time($t = 58 ms$), the CSI starts providing
Figure 2.11: **Simulation Results:** Characteristic voltage and current waveforms of the proposed CSI-VCS shown in Figure 2.8 in the case of transfer from line-connected to stand-alone mode. The transfer is initiated by the line overvoltage of 10% occurring 81 milliseconds prior to the transfer.
Figure 2.12: Experimental Results: Characteristic voltage and current waveforms of the proposed CSI-VCS shown in Figure 2.8 in the case of transfer from line-connected to stand-alone mode. The transfer is initiated by the line overvoltage of 10% occurring 81 milliseconds prior to the transfer.
output current $i_{inr}$ while the line current $i_s$ is decreasing to zero. After this transient, the output voltage $v$ starts almost instantaneously to track its reference $v_{ref}$ as seen in Figure 2.11 b)(simulation results)/Figure 2.12 b)(experimental results). After this transition, the system reaches the steady-state, operating in the stand-alone mode.

2.2.3 CSI-VCS in Stand-Alone Mode

The equivalent circuit of the CSI-VCS in stand-alone mode is shown in Figure 2.8 with the static-transfer-switch $S_s$ in the off-state. The function of the proposed system in this mode of operation is to provide the output voltage of specified amplitude and frequency under any load conditions. The output voltage reference $v_{ref}$ is generated in the controller and is free-running. The output voltage feedback control with the feedforward and the DC-chopper control are active in this mode. The power to the load is delivered by the CSI-VCS using the DC-power source. The steady-state simulation and experimental results of the system shown in Figure 2.8 and operating in stand-alone are presented in Figure 2.13(simulation results)/Figure 2.14(experimental results).

The simulated and experimental results show that the output voltage $v$ (Figure 2.13 a)/Figure 2.14 a)) and load current $i_{load}$ (Figure 2.13 b)/Figure 2.14 b)) are sinusoidal with low total harmonic distortion. The output filter capacitor $C$ absorbs most of the inverter output current harmonics(Figure 2.13 c)/Figure 2.14 c)), leaving only small amount of harmonic content in the load current $i_{load}$. The DC-link current $i_d$ is shown in Figure 2.13 d)/Figure 2.14 d) and is of low ripple content fluctuating around its reference value $I_{d,ref}$. The complete agreement between the simulation and experimental results can be observed.
Figure 2.13: Simulation Results: Characteristic voltage and current waveforms of the proposed CSI-VCS shown in Figure 2.8 and operating in stand-alone mode.
Figure 2.14: Experimental Results: Characteristic voltage and current waveforms of the proposed CSI-VCS shown in Figure 2.8 and operating in stand-alone mode.
2.2.4 Transfer from Stand-Alone to Line-Connected Mode

After a line voltage/current disturbance has disappeared, the proposed CSI-VCS switches back to the line-connected mode. This is in order to provide the more efficient power transfer of the required quality to the critical load.

In this mode of the system operation, the system controller resets the transfer command as soon as the line voltage/current are inside the permissible limits. With reference to Figure 2.8, the static-switch $S_s$ is turned on again at that instant and zero DC-link current reference $I_{d,ref}$ is generated. The snubber capacitor $C_s$ starts discharging through snubber resistor $R_s$ and switch $S_s$. The switch $S_s$ is handling at this time both this discharging current as well as the building up line current $i_s$. The diode bridge $D_1,\ldots, D_4$ starts conducting the line current $i_s$, enabling the power flow from the AC-mains to the load. The DC-chopper switch $S_d$ is turned off, forcing the DC-link current $i_d$ to freewheel through the diode $D_d$ and CSI switches. The inverter output current $i_{inv}$ starts decreasing to zero. Again, the line current $i_s$ is split into load current $i_{load}$ and output filter capacitor current $i_C$.

In order to illustrate the CSI-VCS performance in this transition mode, the characteristic voltage/current waveforms of the system shown in Figure 2.8 are presented in Figure 2.15(simulation results)/Figure 2.16(experimental results). The reset of the transfer signal is initiated at $t = 58ms$ by the system controller. This means that the recovery of the line has been detected and the conditions to go back to the line-connected mode are met. At that instant, zero DC-link current reference command is generated by the controller forcing the DC-link current $I_{d,ref}$ to zero(Figure 2.15 c)/Figure 2.16 c). At the same instant($t = 58ms$) the snubber capacitor $C_s$ starts discharging. Furthermore, the line current $i_s$ starts coming-in and compensating the load current $i_{load}$, while the inverter current $i_{inv}$ is decreasing to zero. Finally, the output voltage waveform $v$ during the transient is shown in Figure 2.15 b)/Figure 2.16
Figure 2.15: Simulation Results: Characteristic voltage and current waveforms of the proposed CSI-VCS shown in Figure 2.8 in the case of transfer from stand-alone to line-connected mode. This transfer is initiated by the line voltage recovery at $t = 58\, ms$. 
Figure 2.16: Experimental Results: Characteristic voltage and current waveforms of the proposed CSI-VCS shown in Figure 2.8 in the case of transfer from stand-alone to line-connected mode. This transfer is initiated by the line voltage recovery at $t = 58\,ms$. 
b). It can be seen that the output voltage $v$ is tracking the output voltage reference $v_{\text{ref}}$ during the transient with almost negligible over/undershoot.

2.3 Experimental Setup of the CSI-VCS

In this section, the system power circuit and the controller experimental setup on which the proposed control algorithm is implemented are presented.

In Section 2.3.1, a power circuit setup for experimental verification of the proposed CSI power supply system is presented. The modular structure which is used allows the separate structural and functional description for each of the modules used in the setup.

In Section 2.3.2, a digital implementation of the CSI-VCS controller has been introduced. Furthermore, a description of the A/D board AD_UHP40, main control DSP-based board UHP_40, level-shifter board and “Hot-Link”-board PC_UHP40 on which the system controller functions are implemented is given. The control functions implemented in the main-board processor TMS320C40 are identified. The PWM design for CSI and DC-chopper is presented in Appendix D and the gating logic for the static-transfer-switch implemented in the FPGA FLEX8000 from ALTERA is presented in Chapter 4.

2.3.1 Power Circuit Experimental Setup

The basic power circuit schematic diagram of the CSI-VCS used for the experimental setup in this thesis has already been shown in Figure 2.8. In the following sections the modules used in the real experimental setup of the CSI-VCS are described. The function of each of the building blocks is already explained in Section 2.1.1. of this
For the experimental setup, the motor-generator set is used which provides the DC-voltage $V_d$ of 220V and has a low inner impedance. The DC-voltage ripple is measured to be approximately 2V peak-to-peak.

The existing laboratory module is used for the DC-chopper. The DC-chopper module is implemented using a one leg of the intelligent power module: Intellimod Module PM50RSA120 Three Phase + Brake IGBT Inverter, 1200V, 50A from POWEREX. The gating board for the main switch $S_d$ is provided in the module itself. The signals needed to be provided by the user are logic +15V signals obtained from the Level-Shifter board.

The CSI used in the experimental setup is realized with four single IGBTMOD H-series CM400HA-12H 1200V, 400A modules from POWEREX and the power diodes SM14PCR050 1400V, 50A connected in series with the main switches.

The Static-Transfer-Switch is realized by using the single IGBTMOD H-series CM400HA-12H 1200V, 400A module from POWEREX and four R411-1240 1200V, 50A power diodes. In order to prevent the overvoltages across the IGBT module $S_s$ during the switching and allow for the instantaneous transfer, the snubber circuit has been connected consisting of: resistor $R_s=50\Omega$, electrolytic capacitor $C_s=3600\mu F$ and power diode IR40HF40 400V, 40/A(International Rectifier) for $D_s$.

The DC-link inductor $L_d$ used in the experiment is a 10mH, ferrite inductor. The value of the AC-link inductor $L_{ac}$ is 2mH. Both inductors have been taken off the shelf.
2.3.2 System Controller Experimental Setup

The proposed CSI-VCS controller is realized with the A/D boards[30], DSP-based general purpose controller board[28], level-shifter board and ATM-board[29]. The block diagram of the system controller is shown in Figure 2.17.

In order to obtain the digital values of the measured system voltages and currents the A/D board AD_UHP40[30] has been used in the CSI-VCS experimental setup. The DSP-based controller board used in the experimental setup is UHP40[28] and all the control functions are realized on this universal controller board. The gating logic and appropriate switching functions for the CSI, DC-chopper and Static-Switch obtained at the output of the controller board are processed through the level-shifter board in order to adjust the voltage levels of the gating logic signals for the IGBT gating boards. The ATM-board[29] serves as the interface between the host-PC and the controller board UHP40 in order to monitor the internal values of the main DSP-processor in real-time using the MONITOR program[31].

The detailed description and function of each of the controller setup components is given in the following paragraphs and the processing of the system signals is shown in the form of the block diagram in Figure 2.18.

A/D board AD_UHP40

The function of the A/D board AD_UHP40[30] is to convert the measured state variables of the proposed CSI-VCS(obtained from the sensors) from the analog to the digital domain. The A/D board is a four-channel board based on the MAX120 A/D 12-bit data resolution successive approximation converter from MAXIM, with a conversion time of 5μs at 20MHz. In the experimental setup, two of these boards are connected to ComPorts 1 and 2 of the DSP TMS320C40 on the UHP40 controller board. The measured signals from experimental setup power circuit connected to the
Figure 2.17: A simplified block diagram of the proposed CSI-VCS controller hardware realization with the A/D boards, UHP40 main controller board, level-shifter board and ATM-board.
Figure 2.18: A simplified block diagram of the proposed CSI-VCS signal processing performed in the controller shown in Figure 2.17.

A/D board 1 are: output voltage $v$ and AC-source voltage $v_s$. The signals connected to the A/D board 2 are: load current $i_{load}$, AC-source current $i_s$ and DC-link current $i_d$.

**Controller Board UHP40**

The measured values of the CSI-VCS state variables obtained from the A/D boards are processed on the UHP40 controller board. Based on the control algorithm, the
gating signals for driving the DC-chopper, CSI and Static-Transfer Switch are generated at the output of the UHP40.

The UHP40 board is a VME-Bus based general-purpose controller board developed at the University of Toronto[28]. The main processor on the board is a floating-point DSP TMS320C40 from Texas Instruments where the control algorithm for the proposed CSI-VCS is downloaded and executed. The proposed control algorithm is written in C, linked to the DSP-kernel object file and executed on an interrupt basis as explained in [31]. The control signal $c_{cho}$ for the DC-chopper and control signal $c_{CSI}$ for the CSI are calculated during the sampling interval in the TMS320C40 and these values are written to the input registers of the on-board FPGA FLEX8000 from ALTERA at each sampling instant. Based on the digital PWM design realized in the FPGA, the gating signals for driving the DC-chopper, CSI and Static-Switch are obtained from the bidirectional buffers connected to the output of the FPGA. In order to design the fast acting protection of the CSI module, the output of the overvoltage comparator is connected to the FPGA input and the freewheeling of the CSI switches is provided when the fault condition (overvoltage) is detected.

**Level Shifter Board**

In order to provide the gating logic signals for DC-chopper, CSI and Static-Switch power modules, the $+5V/TTL$ signals obtained at the output of the UHP40 board are processed through a level-shifter board in order to provide $+15V/CMOS$ signals needed to drive the gating boards for these modules. The board is bidirectional digital logic converter board based on the level-shifter IC MC14504 from MOTOROLA. The output signals which are processed are the gating pulses $SW_{S1}, \ldots, SW_{S4}$ for the CSI, gating pulse $SW_{S4}$ for DC-chopper and the gating pulse $SW_{S4}$ for Static-Switch.

**ATM Board PC-UHP40**

The function of the ATM board[29] is to provide the data communication between
the AT-Bus (at the host-PC side) and the ComPorts of the TMS320C40 (DSP side on the UHP40 board) in real-time. In order to meet the bandwidth of the DSP’s ComPorts of 192Mbits/s, the design of the ATM board is based on the ATM standards and realized with the CY7B923 HOTLink Transmitter and CY7B933 HOTLink Receiver from CYPRESS capable of transferring the data at these speeds. During the development of the control algorithm for the proposed system, this communication link has been used to tune up the controller parameters on-line and to observe the DSP internal variables and CSI-VCS process variables using the DSP-MONITOR graphical-user interface (GUI) program[31].
Chapter 3

Steady-State Analysis of a CSI Voltage Conditioning System

In Chapter 2 of this thesis, a description of the proposed CSI-VCS, shown in Figure 3.1, has been given and the operation of the system explained. In this chapter, a steady-state analysis of the same system is performed in order to obtain analytical expressions for all internal system variables. Furthermore, the operation of the proposed system has been performed on a 1kVA laboratory prototype and the obtained experimental results have been compared with the analytical solutions. This analysis serves for determining the voltage/current ratings of the system components i.e. for the system design, which is performed in chapter 5 of this thesis.

Based on the discussion on CSI-VCS operating modes, performed in Chapter 2 of this thesis, it has been concluded that the proposed system can operate in two different modes, namely: line-connected mode and stand-alone mode. Therefore, the steady-state analysis of the proposed system, performed in this chapter, is done separately for each mode of operation.
Figure 3.1: A simplified power circuit diagram of a line-connected single-phase CSI voltage conditioning system with the AC-mains, DC-voltage source and the load.

The steady-state analysis of the CSI-VCS in line-connected mode is performed in section 3.1. The phasor diagram is presented for nominal operating conditions of the system in this mode of operation. Based on this phasor diagram and time-domain equations, the analytical expressions for system voltages and currents are derived. In order to verify the performed analysis, these internal variables of the system are then plotted as functions of time and compared with the respective waveforms obtained experimentally.
In section 3.2, a steady-state analysis of the single-phase CSI-VCS in stand-alone mode has been performed. Using the Fourier analysis, the harmonic components of the internal system voltages and currents are determined. First, a sinusoidal-pulse-width modulation (SPWM) switching function $SW_{CSI}$ for the CSI is defined. Then, knowing the CSI switching function $SW_{CSI}$ and expression for the output voltage $v$, the CSI input voltage $v_{inv}$ is calculated. Since the average voltage across the DC-link inductor $L_d$ during each switching period has to be zero in the steady-state, the average DC-chopper output voltage $V_{cho,ave}$ has to be equal to the average CSI input voltage $V_{inv,ave}$. Based on this fact, the instantaneous DC-chopper voltage $v_{cho}$ has been defined and an appropriate switching function $SW_{cho}$ for the DC-chopper is calculated. After defining the DC-link model in such a way, the expressions for the DC-link current $i_d$, DC-chopper input current $i_{cho}$ and CSI output current $i_{inv}$ are obtained. Finally, knowing the load current $i_{load}$ and inverter output current $i_{inv}$, the output filter capacitor current $i_C$ and output voltage $v$ are calculated. This analysis is used for the power circuit design, ratings of the system components and determination of the power flow direction in the system. In order to verify this analysis, an experiment on a 1kVA laboratory prototype is performed. Finally, it is shown that all the current and voltage waveforms of the system, obtained analytically, almost coincide with the waveforms obtained from the experiment, verifying in such a way the performed steady-state analysis. In addition, the steady-state operation of the proposed system in the stand-alone mode is simulated using the C-code. The simulation results are presented on the same graphs with analytical solutions.

The results of the system analysis presented in this chapter have been obtained with the following assumptions in reference to Figure 3.1:

1. The line voltage $v_s$ is sinusoidal and harmonic-free.
2. The following switching elements are assumed to be ideal (zero resistance in on-state, infinite resistance in off-state, zero turn-on time and zero turn-off time):

50
$S_1, \ldots, S_4, S_d$ and $S_s$.

3. The following diodes are assumed to be ideal (zero voltage drop across it in on-state, infinite resistance in off-state and instantaneous cut-off during transition from forward to reverse bias): $D_1, \ldots, D_4$, $D_d$ and $D_s$.

4. The parameters of the AC-link reactor ($R_{ac}$ and $L_{ac}$), DC-link inductor ($R_d$ and $L_d$), output filter capacitor ($C$) and snubber ($R_s$ and $C_s$) are lumped and are defined in Appendix A.

5. The load is assumed to be linear with lumped parameters defined by the power rating of the system, the rated output voltage and the power factor, which are all given in Appendix A.

The additional assumptions related to the steady-state analysis of CSI-VCS operating in stand-alone mode are stated in Section 3.1.

3.1 Steady-State Analysis of the CSI-VCS in Line-Connected Mode

In this section, a steady-state analysis of the single-phase CSI voltage-conditioning system in line-connected mode has been performed. The analytical expressions for all internal voltages and currents of the proposed system are derived. In order to validate this analysis, a steady-state operation of the system has been performed on a laboratory prototype. The experimental results are compared with the results obtained analytically and complete agreement has been established.

The equivalent power circuit diagram of the CSI-VCS shown in Figure 3.1 and operating in line-connected mode is shown in Figure 3.2. In line-connected mode of system operation, the DC-chopper and CSI are inactive (in reference to Figure 3.1).
This means that the DC-link current $i_d$ and inverter output current $i_{inu}$ are zero. So, the power to the load is supplied only by the AC-source and the DC-chopper and CSI can be neglected in the following analysis.

![Static-Switch](image)

Figure 3.2: An equivalent power circuit diagram of a line-connected single-phase CSI-VGS shown in Figure 3.1 operating in line-connected mode.

Figure 3.3 shows the phasor diagram of the system shown in Figure 3.2, where the output voltage phasor $V$ is drawn as a reference phasor. The load current phasor $I_{load}$ is at lagging power factor angle $\phi$ and is resolved into an active component $I_{load,p}$ and a reactive component $I_{load,q}$. The phasor of the capacitor current $I_C$ is 90 deg leading. The line current phasor $I_s$, which is equal to the sum of the load current phasor $I_{load}$ and the capacitor current phasor $I_C$, is found by a graphical construction and is $\phi_s$ deg leading the reference output voltage phasor $V$. Using the Kirchhoff’s voltage law, the phasor of the AC-line voltage $V_s$ is found by graphical construction as the sum of the following phasors: output voltage $V$, resistive voltage drop $R_{ac}I_s$ and inductive voltage drop $X_{ac}I_s$. The AC-line voltage phasor $V_s$ is $\delta$ deg leading.

The time-domain equations of the proposed CSI-VCS in line-connected mode,
Figure 3.3: The phasor diagram of the CSI-VCS operating in the line-connected mode and shown in Figure 3.2.

shown in Figure 3.2, are obtained from first principles and are given by the following expressions:

\[ i_s = i_{\text{load}} + i_C, \]  \hspace{1cm} (3.1)

\[ v_s = R_{ac}i_s + L_{ac} \frac{di_s}{dt} + v \]  \hspace{1cm} (3.2)

and

\[ i_C = C \frac{dv}{dt}. \]  \hspace{1cm} (3.3)

The currents through the diode rectifier \( D_1, \ldots, D_4 \) are given by the following expressions:

\[ i_{D_1} = i_{D_2} = \begin{cases} 
0, & \text{if } i_s \leq 0 \\
i_s, & \text{if } i_s > 0
\end{cases} \]  \hspace{1cm} (3.4)

and

\[ i_{D_3} = i_{D_4} = \begin{cases} 
0, & \text{if } i_s \geq 0 \\
i_s, & \text{if } i_s < 0.
\end{cases} \]  \hspace{1cm} (3.5)
The current flowing through the static-transfer-switch $S_S$ is equal to the line current $i_s$:

$$i_{S_S} = i_s. \quad (3.6)$$

The following currents in the system shown in Figure 3.1 are equal to zero:

$$i_d = i_{inv} = i_{R_s} = i_{D_s} = 0. \quad (3.7)$$

Finally, the voltage $v_{C_S}$ across the snubber capacitor $C_S$ is equal to zero as well:

$$v_{C_S} = 0. \quad (3.8)$$

Based on the phasor diagram shown in Figure 3.3 and time-domain Eqs.(3.1)-(3.3), the rms values for voltages/currents in the proposed CSI-VCS, shown in Figure 3.2, are derived in the following paragraphs.

The rms values of the load current active component $I_{load,p}$ and load current reactive component $I_{load,q}$ are:

$$I_{load,p} = I_{load} \cos \phi \quad (3.9)$$

and

$$I_{load,q} = I_{load} \sin \phi. \quad (3.10)$$

Assuming that the output voltage $v$ is sinusoidal with the fundamental angular frequency $\omega$, the rms value of the output filter capacitor current $I_C$ can be derived from Eq.(3.3):

$$I_C = \omega CV, \quad (3.11)$$

where $V$ is the rms value of the output voltage $v$. The rms values of the line current active component $I_{s,p}$ and line current reactive component $I_{s,q}$ are obtained by using Eq.(3.1) as

$$I_{s,p} = I_{load,p} \quad (3.12)$$

54
\[ I_{s,q} = I_{load,q} + I_C. \] (3.13)

The rms value of the line current \( I_s \) and its phase angle \( \phi_s \) can be found by using Eqs.(3.12) and (3.13) in the following way:

\[ I_s = \sqrt{I_{s,p}^2 + I_{s,q}^2} \] (3.14)

and

\[ \phi_s = \arctan\left(\frac{I_{s,q}}{I_{s,p}}\right). \] (3.15)

Finally, the rms values of the line voltage active component \( V_{s,p} \) and line voltage reactive component \( V_{s,q} \) can be derived from the phasor diagram shown in Figure 3.3 as

\[ V_{s,p} = V + R_{ac} I_{s,p} + X_{ac} I_{s,p} \] (3.16)

and

\[ V_{s,q} = R_{ac} I_{s,q} + X_{ac} I_{s,q}. \] (3.17)

The rms value of the line voltage \( V_s \) and its phase angle \( \delta \) can be found by using Eqs.(3.16) and (3.17) in the following way:

\[ V_s = \sqrt{V_{s,p}^2 + V_{s,q}^2} \] (3.18)

and

\[ \delta = \arctan\left(\frac{V_{s,q}}{V_{s,p}}\right). \] (3.19)

Using the Eqs.(3.4)-(3.6), the rms values of the diode currents \( I_{D1}, \ldots, I_{D4} \) and the rms value of the static switch current \( I_{Ss} \) are calculated to be:

\[ I_{D1} = \ldots = I_{D4} = \frac{I_s}{\sqrt{2}} \] (3.20)

and

\[ I_{Ss} = I_s. \] (3.21)
The analytical solutions for the characteristic variables of the system shown in Figure 3.2, are plotted in Figure 3.4 and Figure 3.6 using the equations derived in this section. The system parameters are given in the Appendix A. In addition, the steady-state operation of the system, shown in Figure 3.2 is performed on the laboratory prototype using the same system parameters. The experimental results are shown in Figure 3.5 and Figure 3.7.

Assuming the sinusoidal output voltage \( v \) and using the Eq.(3.18) for the line voltage \( v_s \), it can be seen from Figure 3.4/Figure 3.5 that these waveforms obtained analytically are in close agreement with the same waveforms obtained experimentally. Furthermore, it can be seen that the line voltage \( v_s \) is leading 3 \( \text{deg} \) the output voltage \( v \) as predicted by Eq.(3.19).

The plotted analytical solutions for the load current \( i_{\text{load}} \), output filter capacitor current \( i_C \) and line current \( i_s \) are shown in Figure 3.6. The amplitude and the phase relationships between these currents given by Eqs.(3.9)-(3.15) and shown in the phasor diagram(Figure 3.3) are preserved on this plot. The same waveforms obtained from the experiment are plotted in Figure 3.7. Again, the agreement between the analytical solutions and experimental results is obvious, which verifies the steady-state analysis which is performed in this section.

3.2 Steady-State Analysis of the CSI-VCS in Stand-Alone Mode

In this section, the steady-state analysis of the CSI-VCS, operating in stand-alone mode has been performed. The equivalent power circuit diagram of the proposed system in this mode of operation is shown in Figure 3.8. In order to derive the analytical expressions for voltages and currents in the circuit, the Fourier harmonic
Figure 3.4: Analytical Solution: The steady-state waveforms of the line voltage $v_s$ and output voltage $v$ of the CSI-VCS shown in Figure 3.2, with the parameters given in Appendix A.
Figure 3.5: **Experimental Results:** The steady-state waveforms of the line voltage $v_s$ and output voltage $v$ of the CSI-VCS shown in Figure 3.2, with the parameters given in Appendix A.
Figure 3.6: **Analytical Solution:** The steady-state waveforms of the load current $i_{\text{load}}$ (dashed line), output filter capacitor current $i_C$ (dotted line) and line current $i_s$ (solid line) of the CSI-VCS shown in Figure 3.2, with the parameters given in Appendix A.
Figure 3.7: **Experimental Results:** The steady-state waveforms of the load current $i_{\text{load}}$ (dashed line), output filter capacitor current $i_C$ (dotted line) and line current $i_s$ (solid line) of the CSI-VCS shown in Figure 3.2, with the parameters given in Appendix A.
component analysis of the CSI input voltage $v_{inv}$ and DC-chopper output voltage $v_{cho}$ has been performed and equivalent DC-link model established. Based on this model, the analytical expressions for all the internal variables of the proposed system, operating in stand-alone mode, have been derived.

![Diagram of a line-connected single-phase CSI-VCS](image)

**Figure 3.8:** An equivalent power circuit diagram of a line-connected single-phase CSI-VCS shown in Figure 3.1 operating in stand-alone mode.

In stand-alone mode of operation of the proposed CSI-VCS a power to the load is delivered by the inverter. The AC-line has been disconnected from the rest of the system by turning-off the static-transfer-switch $S_*$, shown in Figure 3.1.

The system analysis presented in this section have been performed with the general assumptions stated in the introduction of this chapter and with the following additional assumptions in reference to Figure 3.8:

1. The output voltage $v$ is sinusoidal, harmonic-free, and is given by $v = \sqrt{2}V \sin \omega t$, where $V$ is the rms value and $\omega$ is the fundamental angular frequency.
2. The switching frequency of the DC-chopper is the same as the switching frequency of the CSI and is denoted as $f_c$.
3. The DC-component of the DC-link current is given and is denoted as $I_{d,0}$. This
is an initial condition necessary for the possible open-loop operation of the CSI.

4. The CSI is delivering rated current to an inductive load (PF=0.8) at 0.8 modulation index which represents the nominal operating condition for the system.

The time-domain equations for the CSI-VCS operating in stand-alone mode and shown in Figure 3.8 are:

\[ i_{inv} = i_{load} + i_C, \quad (3.22) \]

\[ v_{cho} = R_d i_d + L_d \frac{di_d}{dt} + v_{inv} \quad (3.23) \]

and

\[ i_C = C \frac{dv}{dt}. \quad (3.24) \]

The first step in the analysis is to find the CSI input voltage \( v_{inv} \), which is given as the product of CSI switching function \( SW_{CSI} \) and output voltage \( v \). The sinusoidal pulse-width modulated (SPWM) switching function \( SW_{CSI} \) of the CSI, obtained from the simulation is shown in Figure 3.9 (solid line), and the detailed view of that waveform is shown in Figure 3.10.

The Fourier series expansion of the SPWM switching function \( SW_{CSI} \) [24], for amplitude modulation index \( m_a = 0.8 \), gives

\[ SW_{CSI} = m_a \sin wt + 0.818 \sin (m_f wt) + \]
\[ 0.22 \sin ((m_f - 2)wt) + 0.22 \sin ((m_f + 2)wt) - \]
\[ 0.314 \sin ((2m_f - 1)wt) + 0.314 \sin ((2m_f + 1)wt) + \cdots, \quad (3.25) \]

where \( m_f \) is the frequency modulation index [24]. This waveform is plotted in Figure 3.9 with the dashed line. The same waveform \( SW_{CSI} \) has been obtained from the experiment and is plotted in Figure 3.11 and Figure 3.12. It can be seen that the CSI switching function \( SW_{CSI} \) plotted as a Fourier series obtained analytically, almost coincide with the switching function obtained from the simulation and from the
Figure 3.9: Simulation Results: The SPWM switching function $SW_{CSI}$ of the CSI shown in Figure 3.8. The waveform obtained from the simulation is shown in solid-line. The waveform obtained analytically by using Eq.(3.25) is shown in dashed-line.

Figure 3.10: Simulation Results: The detailed view of Figure 3.9: on the left for the time interval (0ms,0.6ms) and on the right for the time interval (3.4ms,4.0ms).
Figure 3.11: Experimental Results: The SPWM switching function $SW_{CSI}$ of the CSI shown in Figure 3.8.

Figure 3.12: Experimental Results: The detailed view of Figure 3.11: on the left for the time interval (0ms,0.6ms) and on the right for the time interval (3.4ms,4.0ms).
experiment. This justifies the time-domain simulation and the Fourier analysis of the CSI switching function $SW_{CSI}$, performed so far.

Based on this analysis, the expression for the CSI input voltage $v_{inv}$ is derived by simply multiplying the switching function $SW_{CSI}$ of the CSI and output voltage $v$:

$$v_{inv} = SW_{CSI} \cdot v.$$  \hspace{1cm} (3.26)

When Eq.(3.25) is substituted into Eq.(3.26), we obtain after some algebraic manipulation the Fourier series representation of the inverter input voltage:

$$v_{inv} = \frac{\sqrt{2}V}{2}[m_a - m_a \cos 2wt + 0.598 \cos ((m_f - 1)wt) - 0.598 \cos ((m_f + 1)wt) + 0.22 \cos ((m_f - 3)wt) - 0.22 \cos ((m_f + 3)wt) + 0.314 \cos (2m_f wt) - 0.314 \cos ((2m_f - 2)wt) + \cdots],$$  \hspace{1cm} (3.27)

The inverter input voltage waveform, obtained from the simulation, is plotted in Figure 3.13/3.14 with the dashed line. On the same plot, $v_{inv}$ has been plotted with the solid line as the Fourier series expansion given with Eq.(3.27). In addition, the same waveform of the CSI input voltage has been obtained from the experimental prototype of the proposed system and is shown in Figure 3.15/3.16. The parameters of the CSI-VCS used for the simulation and the experiment are given in Appendix A. Since the CSI input voltage waveforms shown in Figure 3.13/3.14 are almost identical to the same waveform obtained from the experiment, we can validate the time-domain simulation and verify Eq.(3.27).

The next step in the analysis is to obtain the expression for the DC-chopper output voltage $v_{cho}$. The fact that the average voltage across the inductor $L_d$ has to be equal to zero (in the steady-state) is used in the following discussion. In order to provide that condition for the voltage across the DC-link inductor $L_d$, the average DC-chopper output voltage $V_{cho,avg}$ during each switching interval has to be equal to the average CSI input voltage $V_{inv,avg}$ as shown in Figure 3.17. Assuming that the
Figure 3.13: Simulation Results: The steady-state waveforms of the CSI input voltage $v_{in}$ of the CSI-VCS shown in Figure 3.8, with the parameters given in Appendix A. Analytical solution is plotted with the solid line and the simulation result with the dashed line.

Figure 3.14: Simulation Results: The detailed view of Figure 3.13: on the left for the time interval (9ms,10ms) and on the right for the time interval (12ms,13ms).
Figure 3.15: Experimental Results: The steady-state waveforms of the CSI input voltage $v_{in}$ of the CSI-VCS shown in Figure 3.8, with the parameters given in Appendix A.

Figure 3.16: Experimental Results: The detailed view of Figure 3.15: on the left for the time interval (9ms,10ms) and on the right for the time interval (12ms,13ms).
switching frequencies of the CSI and DC-chopper are the same and equal to \( f_c \), this condition may be simplified by stating that the time integrals of \( v_{inv} \) and \( v_{cho} \) over the switching period \( T_c \) have to be the same. These integrals are denoted as \( \text{Area}_{CSI} \) and \( \text{Area}_{cho} \) respectively and are shown in Figure 3.17. The additional assumption which is made and is related to Figure 3.17 is that the carrier signals for both the CSI and DC-chopper are synchronized. The area \( \text{Area}_{CSI} \) is calculated to be:

\[
\text{Area}_{CSI} = \int_0^{t_0} \sqrt{2} V \sin wt \, dt - \int_{t_0}^{T_c} \sqrt{2} V \sin wt \, dt
\]

\[
= \frac{\sqrt{2} V}{w} [1 - 2 \cos wt_0 + \cos wt_c]. \tag{3.28}
\]

Equating the obtained \( \text{Area}_{CSI} \) with the \( \text{Area}_{cho} \), the expression for the DC-chopper on-period \( t_{on} \) can be derived as:

\[
t_{on} = \frac{\text{Area}_{CSI}}{V_d}, \tag{3.29}
\]

with the additional constraint that

\[
\text{if } v_{inv} < 0, \quad t_{on} = 0. \tag{3.30}
\]

Using Figure 3.17 and the facts stated so far, the DC-chopper on-periods \( t_{on} \) are calculated for each switching interval (for the entire fundamental cycle) from Eq. (3.29).
The \( t_{\text{on}} \) values of the DC-chopper output voltage \( v_{\text{cho}} \) are then numerically determined and using the same procedure as in [32], the following expression for the DC-chopper output voltage \( v_{\text{cho}} \) has been derived:

\[
v_{\text{cho}} = 70.14 + 79.25 \cos (2\omega t) + 75.5 \cos (m_f \omega t) + 38.3 \cos ((m_f - 2)\omega t) + 23.6 \cos ((m_f + 2)\omega t) - 21.0 \cos ((2m_f - 4)\omega t) + 16.34 \cos ((2m_f + 4)\omega t) + \cdots , \tag{3.31}
\]

The DC-chopper output voltage waveform \( v_{\text{cho}} \) obtained from the simulation and by using the Eq.(3.31) are plotted as a function of time in Figure 3.18 with the solid and dashed line respectively. The detailed views of these two waveforms are shown in Figure 3.19. The DC-chopper output voltage waveform \( v_{\text{cho}} \) obtained from the experiment is plotted in Figure 3.20/3.21. Simulation, analytical and experimental results shown in Figures 3.18-3.21 are obtained using the parameters of the system given in Appendix A. It can be seen that the simulated, analytical and experimental waveforms almost coincide. This verifies the proceeding steady-state-analysis and the time-domain simulation.

The DC-chopper switching function \( SW_{\text{cho}} \) is then given with:

\[
SW_{\text{cho}} = \frac{v_{\text{cho}}}{V_d},
\tag{3.32}
\]

and is of the same waveshape as the DC-chopper output voltage \( v_{\text{cho}} \), but scaled by the constant factor \( V_d \).

Using the derived analytical expressions for inverter input voltage \( v_{\text{inv}} \) (Eq.(3.27)) and DC-chopper output voltage \( v_{\text{cho}} \) (Eq.(3.31)), the equivalent DC-link model for the circuit shown in Figure 3.8 can be constructed. This model is shown in Figure 3.22. The voltage sources \( v_{\text{inv}} \) and \( v_{\text{cho}} \), shown in Figure 3.22, and expressed by Eqs.(3.27) and (3.31), are the equivalents of infinitely many series connected sinusoidal sources, each source having its own amplitude and frequency. To find the contribution of each source to the DC-link current \( i_d \), the principle of superposition has been used.
Figure 3.18: **Simulation Results:** The steady-state waveforms of the DC-chopper output voltage $v_{cho}$ of the CSI-VCS shown in Figure 3.8, with the parameters given in Appendix A. The analytical solution is plotted with dashed line and the simulation result with solid line.

Figure 3.19: **Simulation Results:** The detailed view of Figure 3.18: on the left for the time interval (11.5ms, 12ms) and on the right for the time interval (13.5ms, 14ms).
Figure 3.20: Experimental Results: The steady-state waveforms of the DC-chopper output voltage $v_{\text{cho}}$ of the CSI-VCS shown in Figure 3.8, with the parameters given in Appendix A.

Figure 3.21: Experimental Results: The detailed view of Figure 3.20: on the left for the time interval (11.5ms,12ms) and on the right for the time interval (13.5ms,14ms).
Figure 3.22: The equivalent DC-link model of the CSI-VCS shown in Figure 3.8.

For any one of the sinusoidal sources, the phasor domain expression for the DC-link current is

$$ I_d = \frac{V_{cho} - V_{inv}}{R_d + j\omega L_d}. \quad (3.33) $$

The proposed CSI-VCS shown in Figure 3.8 has been simulated using the system parameters given in Appendix A. The DC-link current waveform $i_d$ obtained from that simulation is plotted in Figure 3.23/Figure 3.24 with the solid-line. Using the same system parameters, the expression for the DC-link current has been derived using Eq.(3.33) and plotted in the same figures using the dashed line. The DC-link current waveform obtained from the experiment is shown in Figure 3.25/Figure 3.26. By comparing the DC-link current waveforms obtained from the simulation, analysis and experiment we can conclude that they almost coincide. This verifies the analysis performed so far and the time-domain simulation.

Using Eq.(3.33) for the DC-link current, the analytical expressions for the inverter current $i_{inv}$ and DC-chopper input current $i_{cho}$ can be expressed as follows:

$$ i_{inv} = SW_{CSI} \cdot i_d \quad (3.34) $$

and

$$ i_{cho} = SW_{cho} \cdot i_d \quad (3.35) $$

respectively.
Figure 3.23: Simulation Results: The steady-state waveforms of the DC-link current $i_d$ of the CSI-VCS shown in Figure 3.8, with the parameters given in Appendix A. The analytical solution is plotted with the dashed line and the simulation result is plotted with the solid line.

Figure 3.24: Simulation Results: The detailed view of Figure 3.23: on the left for the time interval (10ms, 10.6ms) and on the right for the time interval (20ms, 20.6ms).
Figure 3.25: **Experimental Results:** The steady-state waveforms of the DC-link current $i_d$ of the CSI-VCS shown in Figure 3.8, with the parameters given in Appendix A.

Figure 3.26: **Experimental Results:** The detailed view of Figure 3.25: on the left for the time interval (10ms,10.6ms) and on the right for the time interval (20ms,20.6ms).
The output filter capacitor current is equal to

\[ i_C = i_{\text{inv}} - i_{\text{load}} = SW_{CSI} \cdot i_d - i_{\text{load}}. \]  \hspace{1cm} (3.36)

Finally, using Eq.(3.36), the expression for the output voltage \( v \) is

\[ v = v(0^-) + \frac{1}{C} \int_0^t i_C \, dt. \]  \hspace{1cm} (3.37)

So, in this section, the analytical expressions for all internal variables of the system, shown in Figure 3.8, have been derived. Using the Eqs.(3.27), (3.31), (3.33), (3.34), (3.35), (3.36) and (3.37), all the voltages and currents labeled in Figure 3.8 can be determined. Finally, showing the close agreement between the simulation results, results obtained from the analytical expressions and the experiment, the steady-state analysis of the proposed CSI-VCS and the time-domain simulation have been verified.
Chapter 4

Design of a CSI-VCS Controller

The proposed efficient line-connected CSI-VCS for conditioning terminal voltage of the critical load has been described in Chapter 2 and the steady-state analysis of the same system has been performed in Chapter 3 of this thesis. In order to provide the load voltage of required quality in steady-state and specified transient behavior under line and load disturbances, the proposed CSI-VCS employs a system controller which is described in this chapter. The overall system controller structure and function of each block are described in the following sections of this chapter. Furthermore, a justification for using the proposed controller strategy is given.

In Section 4.1, the structure of the CSI-VCS controller is given and the main control objectives are stated. These are: an efficient power transfer from the line side to the load under normal operating conditions and safe/minimum-disturbance transfer to stand-alone mode in the case of the line disturbance. In addition, in stand-alone mode a control action is taken which enables the load voltage conditioning in the case of the load disturbance. In order to achieve all these requirements, an adequate system control structure is proposed in this section.

Under normal operating conditions of the system or during start-up, a critical
load is connected to the line through the static-switch. The internal voltage reference synchronized to the line voltage is generated internally in the controller, so that the transfer to stand-alone mode is possible in case of the line disturbance. At the same time, the controller monitors the line voltage constantly in order to determine the power quality of the line. In the case of excessive line voltage disturbance, the controller initiates the transfer to stand-alone mode. After the transfer has been completed, the power to the load is delivered by the CSI-DC-chopper section of the CSI-VCS. In stand-alone mode, the CSI-DC-chopper unit is providing the terminal voltage to the load of low THD and it is at the same time compensating for any load disturbances. As soon as the line-voltage-disturbance-detection controller block recognizes that the line has recovered, the system controller checks for the state of voltage reference synchronization and initiates the transfer request for going back to the line-connected mode. After the transfer to line-connected mode has been completed, the CSI-VCS re-enters the normal operating mode of system operation. In this way, the CSI-VCS controller provides the means of load voltage conditioning for any possible disturbance entering the system from the line or load side. Furthermore, in this section a description and function of each controller block are given.

The composite CSI-VCS controller functions are described in Section 4.2. These functions are incorporated in the controller in order to provide low THD in steady-state and good dynamic performance under load disturbances. A system mathematical model in this mode of operation is defined in order to study its dynamic behavior. The overall system is a two-input, two-output nonlinear system and is linearized around the equilibrium point. After the linearization, the CSI-VCS model is reduced to two single-input-single-output (SISO) subsystems which are decoupled. The separate controllers for the CSI and DC-Chopper are designed using the loopshaping technique. A P-controller for the CSI and a lag-lead controller with an integrator for the DC-chopper are designed. The simulation and experimental results are presented and advantages of using the proposed control method, independent of the load
parameters, are emphasized.

In Section 4.3, the controller functions which initiate and perform the transfer between stand-alone and line connected mode are described. The necessary conditions for initiating the transfer request are defined first. Second, the conditions for initiating the transfer execution are defined. In other words, a gating logic for turning-off and on the static-switch and its digital implementation are presented. Finally, the simulation and experimental results demonstrating the proposed control strategy are presented.

4.1 Description of the CSI-VCS Controller

In this section, the functions of the CSI-VCS controller are defined, controller structure presented and function of each controller block described. Furthermore, the reasons for using the proposed control strategy are given and basic assumptions used for the controller design are stated.

The main function of the CSI-VCS controller is to provide the output voltage to the critical load of required quality in an efficient way. The term 'required quality' implies the specified steady-state and transient performance of the system. The steady-state requirements are small steady-state error and low THD of the output voltage. The transient response requirements are fast response to reference input and good line and load disturbance rejection. All these requirements are achieved with the proposed converter topology and controller structure shown in Figure 4.1. The CSI-VCS controller takes care that the critical load is connected through the static switch to the line during normal operating conditions of the system. In the event of an excessive line voltage disturbance, the system controller initiates the operation of the system from the DC-source, since the line voltage no longer has the required quality. This is done by switching off the static-transfer-switch and delivering the main power
to the load using the CSI-DC-chopper part of the system. As soon as the line recovers from the disturbance, the controller transfers the load back to the AC-line and one full operating cycle is completed. In addition, the controller is taking care that the output voltage and line voltage are synchronized in the case of the transfer. This is achieved by the controller action of generating the internal output voltage reference which is synchronized to the line voltage at all times.

Figure 4.1: A simplified power circuit and controller diagram of a line-connected single-phase CSI voltage conditioning system with the AC-mains, DC-voltage source and the load.
In order to accomplish all the aforementioned functions, the controller structure shown in Figure 4.1 in the form of the block diagram is proposed in this thesis. The controller blocks are: synchronization, disturbance detection, static-switch controller, CSI controller, DC-chopper controller and PWM for the CSI and DC-chopper. A description of each controller block is given in the following paragraphs of this section.

A synchronization block performs the function of creating an internal voltage reference $v_{ref}$ which is in phase with the line voltage $v_s$ in order to enable the required conditions for smooth transfer between the line-connected and stand-alone mode. The reference voltage $v_{ref}$ is further used by the disturbance detection block and CSI controller block. In addition, the synchronization block sets the synchronization flag `sync_flag` in order to acknowledge to the static-switch controller block that the synchronization between line and load voltage is achieved. In this way the static-switch controller is allowed to initiate the transfer between the line-connected and stand-alone mode of systems operation. The details of the synchronization block design are given in Appendix B of this thesis.

The function of the disturbance detection block is to monitor the line voltage $v_s$ and to send a request `transfer` for transfer to the static-switch controller block. Based on the: 1) deviation of the line voltage $v_s$ from the voltage reference $v_{ref}$, 2) disturbance detection threshold limits set in the controller and 3) susceptibility curve of the critical load, this block initiates the transfer request. The request for transfer is based on the evaluation of the power quality of the line voltage and algorithm which decides on the optimal mode of CSI-VCS operation. The design of the disturbance detection controller block is performed in Appendix C of this thesis.

The static-transfer-switch controller block initiates the actual transfer to line-connected or stand-alone mode of CSI-VCS operation. This decision is based on the transfer request `transfer` coming from the line disturbance detection block, synchronization status flag `sync_flag` and line current threshold limit detection. There are
two cases when the static-switch controller block initiates the transfer: 1) short-circuit on the line side and 2) when a transfer request has been initiated from the disturbance detection block. In both of these cases, the static-switch controller checks for the state of the output voltage synchronization (status of sync_flag) and as soon as this flag is set, the transfer is initiated by sending the on/off gating signal to $S_x$. In addition, the step current command $I_{d,ref}$ for the DC-link controller block is generated at the output of the static-switch controller block. This command activates/deactivates the operation of the CSI-DC-chopper subsystem i.e. enables/disables the stand-alone mode of the CSI-VCS. The details of the static-switch controller design are given in Section 4.3 of this thesis.

The CSI-DC-chopper controller is a composite controller which consists of a DC-chopper controller and a CSI controller. The DC-chopper controller provides a constant DC-link current $i_d$ for proper operation of the CSI, while the CSI controller provides a sinusoidal output voltage $v$ of low distortion to the critical load. The DC-link current reference command $I_{d,ref}$ is generated in the static-switch controller block and the voltage reference for the CSI $v_{ref}$ is generated in the synchronization block. By processing the DC-link current error signal ($I_{d,ref} - i_{d,ref}$), a lag-lead controller with an integrator generates the control signal $c_{cho}$ which in turn through the feedback action forces the DC-chopper to regulate the DC-link current $i_d$. In the same way, by processing the output voltage error signal ($v_{ref} - v$), a P-controller generates a control signal $c_{CSI}$ which in turn through the feedback action forces the CSI to track the output voltage reference $v_{ref}$. The simulation and experimental results demonstrating the performance of the CSI and DC-chopper controllers are presented in Section 4.2 of this thesis.

The PWM blocks for the DC-chopper and CSI provide gating signals for IGBT's ($S_1, \ldots, S_4$ and $S_d$) based on the control signals $c_{CSI}$ and $c_{cho}$ obtained at the output of the CSI-DC-chopper unit controller. A digital implementation of the PWM for
the CSI and DC-chopper is realized in programmable logic device FLEX8000 from Altera. The design and the hierarchy of the graphic design files used to implement PWM for the CSI and the DC-chopper are given in Appendix D of this thesis.

4.2 CSI-DC-Chopper Unit Controller Design

In this section, a design of the composite CSI-DC-chopper controller is performed. A mathematical model of the CSI-DC-chopper subsystem is developed and linearized around the equilibrium point. After the linearization, the model reduces to two SISO decoupled subsystems so that the decentralized controllers for the CSI and DC-chopper can be designed. Furthermore, the justification for using the decentralized controller structure is given. The controller design is carried out by using the loop-shaping methods for sensitivity, complementary sensitivity and loop transfer functions of the system. By using this design method, the full understanding of the augmented system dynamic behavior is obtained and excellent performance is achieved.

In the case of the excessive line voltage disturbance, the system controller has to initiate the request for the transfer to stand-alone mode. At the same time, the system controller has to initiate the DC-link step current command $I_{d,ref}$. After the assertion of this command, the CSI has to modulate the DC-link current $i_d$ and provide the load with the sinusoidal load current $i_{load}$. That means that the composite CSI-DC-chopper controller has to regulate the DC-link current $i_d$ and to control the output voltage $v$. In order to design such a controller, the CSI-DC-chopper subsystem is modeled first.

An equivalent power circuit diagram of a line-connected single-phase CSI-VCS shown in Figure 4.1 operating in stand-alone mode is shown in Figure 4.2. From the first principles and relations obtained in Chapter 3 of this thesis, the basic circuit
relations related to this system are:

\[ v_{cho} = c_{cho} V_d = R_d i_d + L_d \frac{d i_d}{dt} + v_{inv}, \]  
(4.1)

\[ v_{inv} = c_{CSI} v \]  
(4.2)

and

\[ i_{inv} = c_{CSI} i_d = C \frac{dv}{dt} + i_{load}, \]  
(4.3)

where \( c_{cho} \) and \( c_{CSI} \) are control signals for the DC-chopper and CSI, respectively. In the Laplace i.e. frequency-domain, Eqs.(4.1), (4.2) and (4.3) can be written in the following form:

\[ c_{cho}(s) V_d = R_d I_d(s) + s L_d I_d(s) + c_{CSI}(s) v(s) \]  
(4.4)

and

\[ c_{CSI}(s) I_d(s) = s C V(s) + I_{load}(s). \]  
(4.5)

Based on Eqs.(4.4) and (4.5), the block diagram representation of the CSI-DC-chopper subsystem shown in Figure 4.2 is constructed and is shown in Figure 4.3. As can be seen from this block diagram, this system is a nonlinear, two-input-two-output
system. In order to design a system controller using linear control theory, this system is linearized using the standard linearization procedure given in [33]. The model is derived with the assumption that the inputs are perturbing the system in the vicinity of a nominal equilibrium point.

![Block diagram of a CSI-DC-chopper subsystem](image)

Figure 4.3: A block diagram of a CSI-DC-chopper subsystem shown in Figure 4.2. This block diagram represents the model of the proposed CSI-VCS operating in stand-alone mode.

The system model given by Eqs.(4.4) and (4.5) is rewritten in the state-space form as:

\[ \frac{di_d}{dt} = -\frac{R_d}{L_d}i_d - \frac{1}{L_d}c_{CSI}v + \frac{V_d}{L_d}c_{cho} \]  
\[ \frac{dv}{dt} = \frac{1}{C}c_{CSI}i_d - \frac{1}{C}i_{load}. \]  

(4.6)  
(4.7)

The equilibrium state vector \( x_e = [I_{d,e}^T \ V_e]^T \) corresponds to the nominal dc operating point of the system and is given by:

\[ x_e = [I_{d,ref}^T \ 0]^T. \]  

(4.8)

By substituting the state vector \( x_e \) into the system model ((4.6)-(4.7)), the input vector \( u_e = [c_{choe}^T \ c_{CSI,e}]^T \) at the equilibrium point is calculated as:

\[ u_e = \left[ \frac{R_d}{V_d}I_{d,ref}^T \ 0 \right]^T. \]  

(4.9)
The next step in the linearization process is to write the state equations for incremental variables, i.e. for deviations from the equilibrium. This yields the linear and time-invariant incremental model of the CSI-DC-chopper:

\[
\frac{d}{dt}(\Delta i_d) = -\frac{R_d}{L_d} \Delta i_d + \frac{V_d}{L_d} \Delta c_{cho}
\]  \hspace{1cm} (4.10)

\[
\frac{d}{dt}(\Delta v) = \frac{I_{ref}}{C} \Delta c_{CSI} - \frac{1}{C} \Delta i_{load}
\]  \hspace{1cm} (4.11)

Based on Eqs.(4.10) and (4.11), the block diagram of the linearized CSI-DC-chopper model is constructed and is shown in Figure 4.4. In order to simplify the notation, the incremental variables are replaced with the real variables. As can be seen from this block diagram, this system is a linear, decoupled, two-input-two-output model.

![Block Diagram of the Linearized CSI-DC-chopper Model](image)

Figure 4.4: A block diagram of the CSI-DC-chopper model obtained by linearization.

In the following subsections the SISO controller design for the CSI and DC-chopper is carried out respectively, using the decoupled linearized system shown in Figure 4.4.

4.2.1 CSI Controller Design

In this section, a controller for the CSI, independent of the load parameters, is designed in order to provide sinusoidal output voltage \( v \) with low THD in steady-state
and fast transient response during the disturbances or system parameter variations. First, the load current is used as the disturbance feedforward and the feedback loop using the proportional controller is designed. Second, a calculation delay (caused by the digital implementation of the controller) is inserted in the CSI feedback path and in order to meet the system stability requirements the controller gain is adjusted. Third, the output filter current feedforward is introduced in order to improve the CSI transient response. Finally, the simulation and experimental results are presented in order to demonstrate the excellent dynamic performance of the proposed controller.

The block diagram of the proposed CSI controller is shown in Figure 4.5. In order to design a controller with satisfactory sinusoidal reference tracking, the following has been done. First, the load current $i_{load}$ is measured and with the scaling factor $1/I_{d,ref}$ is fed-forwarded to the controller output $c_{CSI}$. This brings the fastest possible response due to the load disturbances. Second, a feedback control structure is proposed with the following design targets:

![Figure 4.5: A block diagram of the proposed controller structure for CSI shown in Figure 4.2.](image)

- Closed-loop stability (phase margin greater than 50 deg).
- Adequate command input response and
- Robustness with respect to plant parameter variations.
These performance design targets are translated into requirements on sensitivity and complementary-sensitivity closed-loop frequency response functions [33, 34, 54] which are introduced next. From Figure 4.5 we have:

\[ v = P_{CSI} K_{CSI} e_{CSI} = P_{CSI} K_{CSI} (v_{ref} - v), \]  

(4.12)

where

\[ P_{CSI} = \frac{I_{d,ref}}{sC} \]  

(4.13)

is the CSI transfer function, and \( K_{CSI} \) is the controller. Next, from Eq. (4.12) and Figure 4.5 for output voltage \( v \) and error signal \( e_{CSI} \) we obtain:

\[ v = \frac{P_{CSI} K_{CSI}}{1 + P_{CSI} K_{CSI}} v_{ref} = T_{CSI} v_{ref} \]  

(4.14)

and

\[ e_{CSI} = \frac{1}{1 + P_{CSI} K_{CSI}} v_{ref} = \frac{1}{1 + L_{CSI}} v_{ref} = S_{CSI} v_{ref}. \]  

(4.15)

The \( L_{CSI} = P_{CSI} K_{CSI} \) is the loop-gain, \( S_{CSI} \) is the CSI sensitivity function and \( T_{CSI} = 1 - S_{CSI} \) is the CSI complementary sensitivity function[33].

As can be seen from Eqs. (4.14) and (4.15), an adequate loopshaping ideally results in a complementary sensitivity function \( T_{CSI} \) that is close to 1 up to the bandwidth and transits smoothly to zero above this frequency [33]. This results in \( v = v_{ref} \) up to bandwidth, which is desirable. Similarly, it is desirable for sensitivity function \( S_{CSI} \) to be small up to bandwidth and approaches 1 above this frequency. This results in steady-state error \( e_{CSI} \) which approaches zero within the system bandwidth. In other words, the last two conditions result in a small steady-state error and satisfactory tracking which are the controller objectives stated in the introduction of this section. So, it is useful to think of closed-loop control of CSI in terms of \( T_{CSI} \) and \( S_{CSI} \). Given \( T_{CSI} \) and \( S_{CSI} \), the compensator \( K_{CSI} \) is derived as follows [33]:

\[ K_{CSI} = \frac{T_{CSI}}{S_{CSI} P_{CSI}}. \]  

(4.16)
This result implies that a design may be carried out by specifying $S_{CSI}$ or $T_{CSI}$. Eq.(4.16) then finds, uniquely, a controller that yields the desired $S_{CSI}$.

Using the parameters of the CSI-VCS given in Appendix A, a DC-chopper sensitivity function $S_{CSI}$ which is desirable is given with the following low-pass characteristic:

$$S_{CSI} = \frac{s}{s + 376800}$$  \hspace{1cm} (4.17)

and is shown in Figure 4.6. The crossover frequency of this filter is chosen to be 60kHz (376800 rad/s), which means that the steady-state error $e_{CSI}$ at 60Hz is less than 1% (attenuation at 60Hz is 40dB). This can be seen from Eq.(4.15) and Figure 4.6.

![Sensitivity and Complementary Sensitivity Function](image)

Figure 4.6: Low-pass characteristic of the CSI sensitivity function $S_{CSI}$(solid line) and complementary sensitivity function $T_{CSI}$(dashed line) given with Eqs.(4.17) and (4.18), respectively.
From Eq.(4.14), we have for complementary sensitivity function:

\[ T_{CSI} = 1 - S_{CSI} = \frac{376800}{s + 376800} \]  

(4.18)

and finally, from Eq.(4.16) for the controller \( K_{CSI} \):

\[ K_{CSI} = S_{CSI}P_{CSI} \frac{376800C}{I_{d,ref}} = 2.89. \]  

(4.19)

It can be seen from Eq.(4.19) that the obtained controller which satisfies the given specifications is a pure gain.

The next step in the CSI controller design is to analyze the influence of the calculation delay (caused by the controller digital implementation) on the system performance.

Using a first-order Padé approximation[33], the calculation delay block \( D \) is inserted in the CSI feedback path as shown in Figure 4.7. The Bode plot of the resulting CSI loop transfer function is shown in Figure 4.8.

![Figure 4.7](image)

Figure 4.7: A block diagram of the proposed controller structure for CSI shown in Figure 4.5 with the calculation delay block \( D \) included in the feedback path.

Figure 4.8 shows that the phase margin of the CSI loop with the calculation delay block \( D \) included is equal to -7 deg, causing the CSI feedback loop to be unstable. In
Figure 4.8: Bode plot of the CSI loop transfer function shown in Figure 4.7. The parameters of the system are given in Appendix A and $K_{CSI} = 2.89$. 
order to increase the phase margin and improve the stability, the CSI controller gain $K_{CSI}$ is reduced to 0.03. The Bode plot of the resulting CSI loop transfer function with $K_{CSI} = 0.03$ is shown in Figure 4.9.

Figure 4.9: Bode plot of the CSI loop transfer function shown in Figure 4.7. The parameters of the system are given in Appendix A and $K_{CSI} = 0.03$.

From Figure 4.9 it can be observed that the CSI loop transfer function has a phase margin of 62 deg, which is desirable.

In order to further improve the transient response of the CSI, it can be observed that the output filter reference feedforward $i_{C, ff}$, scaled by $1/I_{d, ref}$, can be used in addition to disturbance feedforward $i_{load, ff}$, as shown in Figure 4.10. This is explained in the following paragraphs.
If we assume that the reference output voltage $v_{\text{ref}}$ is given by:

$$v_{\text{ref}} = \sqrt{2}V_{\text{ref}} \sin wt,$$

then the output filter capacitor reference current is given by:

$$i_{C,\text{ref}} = C \frac{dv_{\text{ref}}}{dt} = \sqrt{2}wCV_{\text{ref}} \cos wt. \quad (4.21)$$

If we add the filter capacitor current reference $i_{C,\text{ref}}$ as the feedforward signal $i_{C,ff}$, as shown in Figure 4.10, the overall transfer function from reference input $v_{\text{ref}}$ to output $v$ reduces to 1. This holds as long as the load current measurement and model parameter($C$) are correct. In other words, adding the capacitor current reference $i_{C,\text{ref}}$ as the feedforward signal $i_{C,ff}$ to the CSI control signal $c_{\text{CSI}}$, the transient response is improved by eliminating all the dynamics of the system.

In order to demonstrate the performance of the proposed CSI-controller, the following simulation/experiment has been performed. The CSI-VCS has been operated in stand-alone mode under rated load conditions and system parameters defined in Appendix A. Figure 4.11(simulation results)/Figure 4.12(experimental results) shows the transient response of CSI-VCS for a sudden change of load i.e. from full load to
no load. As shown in Figure 4.11 (simulation results)/Figure 4.12 (experimental results), the transient interval from one state to the other is completed in one sampling interval with almost no overshoot/undershoot.

Figure 4.11: Simulation Results: Transient of the output voltage and load current for a sudden change from full-load to no-load. Simulation results for the controller shown in Figure 4.10 and parameters of the CSI-VCS given in Appendix A.
Figure 4.12: Experimental Results: Transient of the output voltage and load current for a sudden change from full-load to no-load. Experimental results for the controller shown in Figure 4.10 and parameters of the CSI-VCS given in Appendix A.
In addition, the CSI-VCS has been operated in stand-alone mode under no-load conditions and system parameters defined in Appendix A. Figure 4.13(simulation results)/Figure 4.14(experimental results) shows the transient response of CSI-VCS for the sudden change of load i.e. from no-load to full-load. As shown in Figure 4.13(simulation results)/Figure 4.14(experimental results), the transient interval from one state to the other is completed in one sampling interval with almost no overshoot/undershoot.

Figure 4.13: Simulation Results: Transient of the output voltage and load current for a sudden change from no-load to full-load. Simulation results for the controller shown in Figure 4.10 and parameters of the CSI-VCS given in Appendix A.
Figure 4.14: Experimental Results: Transient of the output voltage and load current for a sudden change from no-load to full-load. Experimental results for the controller shown in Figure 4.10 and parameters of the CSI-VCS given in Appendix A.
4.2.2 DC-Chopper Controller Design

In this subsection the DC-chopper controller is designed in order to regulate the DC-link current $i_d$ and maintain it at the constant level needed for the CSI to operate properly. A mathematical model of the DC-chopper is presented first and a feedback structure is proposed. The same loopshaping technique used for the design of the CSI-controller is used for the DC-chopper. Finally, simulation and experimental results are presented in order to demonstrate the dynamic performance of the augmented system.

A mathematical model of the DC-chopper is given by:

$$v_{cho} = c_{cho} V_d = R_d i_d + L_d \frac{di_d}{dt} \quad (4.22)$$

or in the Laplace(frequency) domain:

$$V_{cho}(s) = R_d I_d(s) + L_d s I_d(s). \quad (4.23)$$

In order to regulate the DC-link current in the DC-link a feedback controller structure for the DC-chopper shown in Figure 4.15 is proposed in this thesis.

Figure 4.15: A block diagram of the proposed controller structure for DC-chopper shown in Figure 4.2.

From Figure 4.15, we have:

$$i_d = P_{cho} v_{cho} = P_{cho} K_{cho} (I_d_{ref} - i_d), \quad (4.24)$$
where
\[ P_{cho} = \frac{V_d}{R_d + L_d s} \]  \hspace{1cm} (4.25)

is the DC-chopper transfer function and \( K_{cho} \) is the controller in the feedback path.

The objective is to design a compensator \( K_{cho} \) for the DC-chopper so as to satisfy the following constraints:

1. Track a step input with zero steady-state error.
2. The bandwidth of the closed-loop system should be less than 10 rad/s.
3. The phase margin should be larger than 50 deg.

In order to satisfy the first constraint, the controller must contain an integrator. The Bode plot of the DC-chopper loop transfer function with the integrator is shown in Figure 4.16.

In order to satisfy the second constraint, the gain of the DC-chopper loop transfer function is decreased to 0.001 and the resulting Bode plot shown in Figure 4.17.

Finally, in order to satisfy the third constraint, the medium frequency specifications are considered. This includes a design of a first-order compensator:
\[ \frac{1 + s/w_1}{1 + s/w_2}, \]  \hspace{1cm} (4.26)

where \( w_1 \) and \( w_2 \) are the break frequencies of the zero and pole, respectively, to achieve the phase margin specification. The key idea is to establish a slope of -1 around unity crossover, so as to increase the phase around unity crossover. Thus, a zero will change the slope from -2 to -1, and a pole will change it back to -2 for frequencies above the cut-off. This is achieved in the current design by using the zero \( w_1 = 1 \) and the pole \( w_2 = 0.1 \). The Bode plot of the DC-chopper loop transfer function with the controller \( K_{cho} = \frac{0.001(s+1)}{s(s+0.1)} \) is shown in Figure 4.18.
Figure 4.16: Bode plot of the DC-chopper loop transfer function shown in Figure 4.15. The parameters of the system are given in Appendix A and $K_{\text{cho}} = 1/s$. 

99
Figure 4.17: Bode plot of the DC-chopper loop transfer function shown in Figure 4.15. The parameters of the system are given in Appendix A and $K_{cho} = 0.001/s$. 

100
Figure 4.18: Bode plot of the DC-chopper loop transfer function shown in Figure 4.15. The parameters of the system are given in Appendix A and $K_{cho} = \frac{0.001(s+1)}{s(s+0.1)}$. 
It can be seen from Figure 4.18 that the achieved phase margin of the DC-chopper loop transfer function is 58 deg.

As a final step in the DC-chopper controller design, the influence of the calculation delay (caused by the controller digital implementation) on the system performance is analyzed.

Using a first-order Pade approximation[33], the calculation delay block \( D \) is inserted in the DC-chopper feedback path as shown in Figure 4.19. The Bode plot of the resulting DC-chopper loop transfer function is shown in Figure 4.20.

![Figure 4.19: Block diagram of the DC-chopper transfer function, calculation delay \( D \) and a controller \( K_{cho} \).](image)

Figure 4.19: Block diagram of the DC-chopper transfer function, calculation delay \( D \) and a controller \( K_{cho} \).

Figure 4.20 shows that the phase margin of the DC-chopper loop which includes the calculation delay block \( D \) has not been changed significantly. For this reason, the DC-chopper controller transfer function which is used in the current design is given by:

\[
K_{cho} = \frac{0.001(s + 1)}{s(s + 0.1)}.
\]  

(4.27)

A digital implementation of the controller given by Eq.(4.27) is performed using the bilinear(Tutsin) approximation[25].

The DC-chopper controller simulation and experimental results are presented in Figure 4.21 and Figure 4.22 respectively. The DC-link step current command \( I_{d,ref} \) is initiated at \( t = 10\text{ms} \) and the DC-link current \( i_d \) response is shown in Figure 102.
Figure 4.20: Bode plot of the DC-chopper loop transfer function shown in Figure 4.19. The parameters of the system are given in Appendix A and $K_{cho} = \frac{0.001(s+1)}{s(s+0.1)}$. 
4.21/Figure 4.22. It can be seen that the DC-chopper controller is providing fast response (rise time of 1ms) and excellent steady-state performance (low ripple of $i_d$).

Figure 4.21: Simulation Results: Transient of the DC-link current for a DC-link step current command. Simulation results for the controller shown in Figure 4.15 and parameters of the CSI-VCS given in Appendix A.
Figure 4.22: **Experimental Results:** Transient of the DC-link current for a DC-link step current command. Experimental results for the controller shown in Figure 4.15 and parameters of the CSI-VCS given in Appendix A.
4.3 Static-Switch Controller Design

In this section, a static-transfer-switch controller is designed in order to enable the reliable transfer between line-connected and stand-alone mode of CSI-VCS operation.

A digital logic implementation of the static-switch controller is shown in Figure 4.23. This implementation encompasses all the functions that the proposed static-switch controller performs. These functions are described in the following paragraphs of this section.

![Diagram of static-switch controller](image-url)

Figure 4.23: A digital logic implementation of the static-transfer-switch controller block shown in Figure 4.1.

In order to determine the conditions for transfer to one of the CSI-VCS modes (line-connected and stand-alone) the static-switch controller receives inputs from the synchronization block and line-disturbance detection block. These inputs are: `sync_flag` from the synchronization block, `transfer` signal from line disturbance detection block and line current `i_s`.

A transfer to stand-alone mode is initiated if the line-disturbance threshold limit is
reached (signal transfer high) or if the line current threshold limit is reached (signal curr_flag high). Setting the threshold limit for line disturbance detection is explained in Appendix B. Setting the threshold limit for line current is related to determining the short-circuit current and is beyond the scope of this thesis. If the transfer request has been initiated, the signal line Set is asserted if the output voltage reference is synchronized to the line voltage \( v \), (signal sync_flag high). This in turn provides the gating pulse to the static-switch \( S \), which transfers the CSI-VCS to stand-alone mode. This condition is held using the signal line Hold as long as the conditions to go back to line-connected mode are not met.

In order to demonstrate the transfer to stand-alone mode, the following experiment has been performed and the experimental results are presented in Figure 4.24/Figure 4.25. An overvoltage of 10% has been detected in the line voltage 81 milliseconds prior to the transfer. The resulting overvoltage in the output voltage waveform \( v \) can be seen on the same Figure 4.24 b)/Figure 4.25 b). After detecting that the output voltage \( v \) is outside of specified limits for a critical amount of time, the static-switch controller initiates the transfer signal transfer. This is accomplished by setting the DC-link current reference \( I_{d,ref} \) and switching off the switch \( S \) at \( t = 58ms \), shown in Figure 4.24 c)/Figure 4.25 c). In response to this command, the DC-link current \( i_d \) starts to build up (Figure 4.24 c)/Figure 4.25 c) and the energy stored in the AC-link inductor \( L_{ac} \) starts transferring to the snubber capacitor \( C_s \), charging it. At the same time \( t = 58ms \), the CSI starts providing output current \( i_{inv} \) while the line current \( i_s \) is decreasing to zero. After this transient, the output voltage \( v \) starts almost instantaneously to track its reference \( v_{ref} \) as seen in Figure 4.24 b)/Figure 4.25 b). After this transition, the system reaches the steady-state, operating in the stand-alone mode.

A transfer back to the line-connected mode is performed if the static-switch controller sets the signal Reset in reference to Figure 4.23. This is happening in the case
Figure 4.24: Simulation Results: Characteristic voltage and current waveforms of the proposed CSI-VCS shown in Figure 4.1 in the case of transfer from line-connected to stand-alone mode. The overvoltage of 10% on the line voltage occurred 81 milliseconds before the transfer. The parameters of the CSI-VCS are given in Appendix A.
Figure 4.25: **Experimental Results:** Characteristic voltage and current waveforms of the proposed CSI-VCS shown in Figure 4.1 in the case of transfer from line-connected to stand-alone mode. The overvoltage of 10% on the line voltage occurred 81 milliseconds before the transfer. The parameters of the CSI-VCS are given in Appendix A.
when the disturbance detection block detects the recovery of the line (transfer low) and the output voltage reference is synchronized to the line voltage (sync_flag high).

In order to illustrate the CSI-VCS performance in this transition mode, the characteristic voltage/current waveforms are presented in Figure 4.26 (simulation results)/Figure 4.27 (experimental results). The reset of the transfer signal is initiated at \( t = 59 ms \) by the system controller. This means that the recovery of the line has been detected and the conditions to go back to the line-connected mode are met. At that instant, the zero DC-link current reference command is generated by the controller forcing the DC-link current \( I_{d,ref} \) to zero (Figure 4.26 c)/Figure 4.27 c). At the same instant \( t = 59 ms \) the snubber capacitor \( C_s \) starts discharging. Furthermore, the line current \( i_s \) starts coming-in and compensating the load current \( i_{load} \), while the inverter current \( i_{inv} \) is decreasing to zero. Finally, the output voltage waveform \( v \) during the transient is shown in Figure 4.26 b)/Figure 4.27 b).

It can be seen that the output voltage \( v \) is tracking the output voltage reference \( v_{ref} \) during the transient with almost negligible over/undershoot.
Figure 4.26: Simulation Results: Characteristic voltage and current waveforms of the proposed CSI-VCS shown in Figure 4.1 in the case of transfer from stand-alone to line-connected mode. This transfer is initiated by the line voltage recovery at $t = 59ms$. The parameters of the CSI-VCS are given in Appendix A.
Figure 4.27: **Experimental Results**: Characteristic voltage and current waveforms of the proposed CSI-VCS shown in Figure 4.1 in the case of transfer from stand-alone to line-connected mode. This transfer is initiated by the line voltage recovery at $t = 59\text{ms}$. The parameters of the CSI-VCS are given in Appendix A.
Chapter 5

Design Procedure and Design Example

This chapter includes a design procedure and a design example for a line-connected, single-phase voltage conditioning system realized with a current-source inverter (CSI) shown in Figure 5.1. The procedure given in this chapter is used in order to design a CSI-VCS proposed in this thesis based on the given specifications and results obtained in Chapters 3 and 4. A design example is used to demonstrate the design procedure on a 10kVA system.

In Section 5.1, the output filter design is presented and the reference value for DC-link current $I_{d,ref}$ is determined. The output filter capacitor $C$ is designed to bypass unwanted CSI output current harmonics and to appear as a high impedance to the fundamental CSI output current. This is required in order to provide low THD of the output voltage waveform $v$. Furthermore, the minimum value for the DC-component of the DC-link current $I_{d,min}$ which is required for proper operation of the system up to rated operating conditions is determined. In order to lower the value of the output filter and DC-link current reference, a trial and error procedure proposed in
Figure 5.1: A simplified power circuit diagram of a line-connected single-phase CSI voltage conditioning system with the DC-voltage source and the load.

In this section, the design procedure for the DC-link inductor $L_d$ is developed and realized with a computer routine implemented in C.

In Section 5.2, the procedure for the design of the DC-link inductor $L_d$ is given. The design procedure is based on the DC-link model developed in Chapter 3 of this thesis. The DC-link inductor value is determined in order to provide constant DC-link current $i_d$ under all operating conditions of the system and to limit the ripple factor of the DC-link current to the specified level. The worst case design considerations are taken into account.
The value for the AC-link inductor $L_{ac}$ is defined in Section 5.3. The value of the AC-link inductor $L_{ac}$ is determined based on the steady-state analysis presented in Chapter 3 of this thesis. The design inputs are the specified short-circuit current level on the line side and the allowed steady-state output voltage error. Again, a trial and error procedure is proposed which yields the optimal design.

In order to design a snubber circuit for the static-transfer-switch, the analysis of the system during the transfer from line-connected to stand-alone mode (described in Chapter 4 of this thesis) has been performed in Section 5.4. The critical static-transfer-switch parameters such as capacitor value $C_s$ and the snubber resistor value $R_s$ are determined for the worst operating conditions.

Section 5.5. presents the procedure for the design of a single-phase CSI voltage conditioning system. The design procedure includes the power circuit component selection/ratings and the selection of the controller parameters. The system analysis established in Chapters 3, 4 and 5 is used to develop a step by step design procedure for the proposed CSI voltage conditioning system. The proposed design procedure has been used in this thesis to determine the parameters (given in Appendix A) of the 1kVA experimental setup.

Section 5.6. presents a design example for a 10kVA CSI voltage conditioning system. First, the design specifications are given and, based on the steps developed in the design procedure a 10kVA CSI-VCS is designed. This example is presented in order to show all the steps involved in the design procedure of the CSI-VCS. Finally, the simulation results are presented in order to validate the performed design procedure.
5.1 Design of the Output Filter and the DC-link Current Reference

This section gives the design procedure for the CSI output filter $C$ and for the DC-link current reference $I_{d,ref}$. The output filter $C$ is designed based on the design specification for the THD of the output voltage $v$. The DC-link current reference $I_{d,ref}$ is determined so that the CSI-VCS is able to provide the output filter current $i_C$ and the load current $i_{load}$ up to rated operating conditions.

The stand-alone mode is the critical mode of CSI-VCS operation for which the output filter $C$ and DC-link current reference $I_{d,ref}$ are designed for. Therefore, for the purposes of the design presented in this section, the equivalent circuit of the CSI-VCS operating in stand-alone mode is shown in Figure 5.2.

![Figure 5.2: An equivalent power circuit diagram of a line-connected single-phase CSI-VCS shown in Figure 5.1 operating in stand-alone mode.](image)

The first part of the design is to determine the minimum DC-value of the DC-link current $I_{d,min}$ that provides the required output filter current $i_C$ and load current $i_{load}$ up to rated operating conditions of the system. This current is then chosen to be the
DC-link reference current $I_{d,ref}$. The second part of the design is to determine the output filter capacitance $C$. The design is performed in such a way that the CSI-VCS operating with the DC-link current $i_d = I_{d,ref}$ has a total harmonic distortion (THD) of the output voltage $v$ which is within specified limits. To satisfy this design criteria, the following trial and error procedure is proposed in the following paragraphs.

From the following design specifications: $V$-desired rms value of the output voltage, $I_{load}$-rms value of the load current, $f$-fundamental output frequency and $f_s$-switching frequency, assume the following rms value for the output filter current $I_C$:

$$I_C = \frac{I_{load}}{k_{filter}} \quad (5.1)$$

where $k_{filter}$ is a constant. This $k_{filter}$ should be small enough to bypass unwanted CSI output current harmonics, and large enough to minimize the reactive power drawn from the CSI. The suggestion is to take $k_{filter} = 2$ for the initial guess[14].

The next step is to calculate the rms value for the CSI output current $I_{inv}$, for the assumed $I_C$ (Eq.5.1) and given $I_{load}$. From Chapter 3, we have for the CSI output current:

$$I_{inv} = \sqrt{I_C^2 + I_{load}^2} \quad (5.2)$$

The next step in the design is to determine the DC-link current $I_d$ which provides the required inverter current given with Eq.(5.2). In order to do so, the following reasoning has been used.

The modulation scheme used in the proposed CSI-VCS system is a pulse-width modulation (PWM) scheme. In order to provide sinusoidal output voltage and current, the used PWM technique for CSI is sinusoidal. So, in the steady-state, the modulation signal is a sinusoid, with an amplitude dependent on the DC-link current level and the load conditions. During the load variations, the amplitude and the phase of this modulation signal are changed, in order to modulate in the same way the CSI output
current $i_{in}$. So, the range of the amplitude variations of the modulation signal, has to be set properly in order for the system to be able to compensate for the load disturbances. The second concern with the proper selection of the modulation signal amplitude is the harmonic content in the output voltage. This issue is addressed in [24]. Reference [24] shows that a sinusoidal pulse-width modulation (SPWM), operating in the linear range (amplitude modulation index $M_a \leq 1$), and at high switching frequencies (frequency modulation index $M_f \geq 9$), has voltage harmonics as shown in Table 5.1[24].

Table 5.1: Generalized harmonic amplitudes of the output voltage waveform $v$ for a large $M_f (M_f \geq 9)$ and different modulation indices $M_a$.

<table>
<thead>
<tr>
<th>$h$</th>
<th>$M_a$</th>
<th>0.2</th>
<th>0.4</th>
<th>0.6</th>
<th>0.8</th>
<th>1.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fundamental</td>
<td>0.2</td>
<td>0.4</td>
<td>0.6</td>
<td>0.8</td>
<td>1.0</td>
<td></td>
</tr>
<tr>
<td>$M_f$</td>
<td>1.242</td>
<td>1.15</td>
<td>1.006</td>
<td>0.818</td>
<td>0.601</td>
<td></td>
</tr>
<tr>
<td>$M_f \pm 2$</td>
<td>0.016</td>
<td>0.061</td>
<td>0.131</td>
<td>0.220</td>
<td>0.318</td>
<td></td>
</tr>
<tr>
<td>$M_f \pm 4$</td>
<td></td>
<td>0.018</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$2M_f \pm 1$</td>
<td>0.190</td>
<td>0.326</td>
<td>0.370</td>
<td>0.314</td>
<td>0.181</td>
<td></td>
</tr>
<tr>
<td>$2M_f \pm 3$</td>
<td>0.024</td>
<td>0.071</td>
<td>0.139</td>
<td>0.212</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$2M_f \pm 5$</td>
<td></td>
<td>0.013</td>
<td>0.033</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$3M_f$</td>
<td>0.335</td>
<td>0.123</td>
<td>0.083</td>
<td>0.171</td>
<td>0.113</td>
<td></td>
</tr>
<tr>
<td>$3M_f \pm 2$</td>
<td>0.044</td>
<td>0.139</td>
<td>0.203</td>
<td>0.176</td>
<td>0.062</td>
<td></td>
</tr>
<tr>
<td>$3M_f \pm 4$</td>
<td>0.012</td>
<td>0.047</td>
<td>0.104</td>
<td>0.157</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$3M_f \pm 6$</td>
<td></td>
<td>0.016</td>
<td>0.044</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

So, for a SPWM, the amplitude of the fundamental-frequency component of the
CSI output current $I_{inv1}$ varies linearly with $M_a$ (provided that $M_a \leq 1$):

$$\sqrt{2} \cdot I_{inv1} = M_a \cdot I_d.$$  \hfill (5.3)

In order to provide the correct trade-off between low THD of the output voltage $v$ in steady state and safe margin during transients, the amplitude modulation index $M_{a,nom}$ for rated operating point of the system is chosen to be 0.8. With the amplitude modulation index selected in such a way, from Eq.(5.3), the minimum required value for DC-link current can be determined in the following way:

$$I_{d,min} = \frac{\sqrt{2}}{0.8} I_{inv1}.$$  \hfill (5.4)

The lowest value for the amplitude modulation index is at no load ($I_{load} = 0$). So, using the Eqs.(5.2)-(5.4) the amplitude modulation index at no load $M_{a,0}$ is given by:

$$M_{a,0} = \frac{\sqrt{2} \cdot I_C}{I_{d,min}}.$$  \hfill (5.5)

This gives the range for amplitude modulation index $M_a$ for all CSI-VCS operating points from no-load($M_{a,0}$) to full-load($M_{a,nom}$). In this way, for the worst harmonic conditions (no-load i.e. the lowest $M_a$), the lowest value for $C$ is determined in the following way.

For calculated $M_{a,0}$, the amplitude of the first significant harmonic $h$ present in the output voltage is determined from Table 5.1. The impedance of $C$ for the first significant harmonic $X_{ch}$ is:

$$X_{ch} = \frac{1}{M_f w C},$$  \hfill (5.6)

where

$$M_f = \frac{f_s}{f}$$  \hfill (5.7)

is the frequency modulation index.

The ripple voltage drop across the capacitor $C$ due to the harmonic $h$ is:

$$\Delta V_h = X_{ch} \cdot Amp_h \cdot I_{d,min},$$  \hfill (5.8)
where $Amp_h$ is the amplitude of the harmonic $h$ determined by interpolation from Table 5.1.

If $\Delta V_h$ is larger than specified, the constant $k_{filter}$ should be decreased and the procedure repeated. If $\Delta V_h$ is smaller than specified, the constant $k_{filter}$ should be increased and previous proposed procedure repeated. This is easily done by a simple computer routine.

**5.2 DC-link Inductor Design**

In this section the value for the DC-link inductor $L_d$ is determined in order to limit the DC-link current ripple under all operating conditions of the proposed CSI voltage conditioning system.

It is easy to conclude that the worst case condition i.e. the highest DC-link current ripple occurs during the zero crossings of the output voltage. For this reason, the design procedure for $L_d$ is performed in this section assuming that the CSI input voltage is zero.

So, with $v_{inv} = 0$, the chopper output voltage $v_{cho}$ is given with:

\[ v_{cho} = L_d \frac{di_d}{dt}, \]  

which implies that:

\[ di_d = \frac{1}{L_d} v_{cho} \, dt. \]  

If we integrate both sides of Eq.(5.10) for the time period $0 \leq \tau \leq t$:

\[ \int_{I_{d,-}}^{i_d} di_d = \frac{1}{L_d} V_d \int_0^t dt, \]  

where $I_{d,-}$ is the lower bound on the DC-link current, we get:

\[ i_d = I_{d,-} + \frac{1}{L_d} V_d t. \]
Substitution for \( i_d(t_{on}) = I_{d,+} \) in Eq.(5.12), gives for the ripple current \( \Delta I_d = I_{d,+} - I_{d,-} \):

\[
\Delta I_d = \frac{1}{L_d} V_d t_{on}. \tag{5.13}
\]

Since \( t_{on} = \frac{T_s}{2} \), the value for \( L_d \) is:

\[
L_d = \frac{1}{2\Delta I_d} V_d T_s, \tag{5.14}
\]

or:

\[
L_d = \frac{1}{2\Delta I_d f_s} V_d. \tag{5.15}
\]

So, the value for DC-link inductor is determined from Eq.(5.15). As a final check for determining the ripple content in the DC-link current, the procedure presented in Chapter 3 of this thesis should be used. If the calculated ripple in the DC-link is larger then specified, the value for the DC-link inductor should be increased. If the calculated ripple in the DC-link is smaller then specified, the value for the DC-link inductor should be decreased. This procedure should be repeated until the required ripple DC-link current content is obtained.

### 5.3 Design of the AC-link Inductor

This section defines the procedure for the design of the AC-link inductor \( L_{ac} \). The design goal is to determine \( L_{ac} \) in such a way that the output voltage steady-state error is inside the specified bounds under nominal operating conditions of the CSI-VCS.

The design procedure is based on the steady-state analysis of the CSI-VCS performed in Chapter 3 of this thesis and is done for the CSI-VCS operating in the line-connected mode. The power circuit diagram and the fundamental phasor diagram of the CSI-VCS in the line-connected mode are shown in Figure 5.3 and Figure 5.4, respectively. For the sake of simplicity, the resistance of the AC-line inductor \( R_{ac} \)
has been neglected in the following analysis. Based on this assumption, the following procedure has been used to define the value of AC-line inductor $L_{ac}$.

![Diagram of an equivalent power circuit diagram](image)

**Figure 5.3:** An equivalent power circuit diagram of a line-connected single-phase CSI-VCS shown in Figure 5.1 operating in line-connected mode.

Based on the specified load current $I_{load}$ and capacitor current $I_C$, the value for the line current $I_s$ can be determined as:

$$I_s = \sqrt{I_{s1,p}^2 + I_{s1,q}^2},$$

(5.16)

where:

$$I_{s1,p} = I_{load,p}$$

(5.17)

and

$$I_{s1,q} = I_C + I_{load,q}.$$  

(5.18)

Knowing the line current $I_s$, the active and reactive components of the line voltage can be determined from the phasor diagram shown in Figure 5.4 as:

$$V_{s1,p} = V_s \cdot \cos \delta = V - X_{ac} \cdot I_s \sin \phi_{ac}$$

(5.19)
Figure 5.4: The phasor diagram of the CSI-VCS operating in the line-connected mode and shown in Figure 5.3.

and

\[ V_{s1,q} = V_s \cdot \sin \delta = X_{ac} \cdot I_s \cos \phi_{ac}. \]  

(5.20)

Squaring and summing equations Eqs.(5.19) and (5.20), the following equation for the rms value of the line voltage \( V_s \) has been obtained:

\[ V_s^2 = V_{s1,p}^2 + V_{s1,q}^2 = V^2 - 2 \cdot V \cdot X_{ac} \cdot I_s \sin \phi_{ac} + X_{ac}^2 \cdot I_s^2, \]  

(5.21)

or

\[ I_s^2 \cdot X_{ac}^2 - 2 \cdot V \cdot X_{ac} \cdot I_s \sin \phi_{ac} + (V^2 - V_s^2) = 0. \]  

(5.22)

For the given values of rms value of the line voltage \( V_s \) and rms value of the output voltage \( V \), the value for \( X_{ac} \) can be determined from Eq.(5.22).
5.4 Design of the Static-Transfer-Switch Snubber Circuit

In this section, the selection and rating of the static-transfer-switch (STS) components $R_s$, $C_s$ and $S_s$ (shown in Figure 5.1) has been performed. The main function of the STS snubber is to limit the overvoltage across the main-switch $S_s$ during the transfer from line-connected to stand-alone mode. The second function of the STS snubber is to accumulate the stored energy trapped in the line inductor $L_{ac}$ during the transfer and dissipate it. In order to perform these functions, the snubber circuit configuration of Figure 5.1 is proposed in this thesis and is described in Chapter 2.

The capacitor $C_s$ is selected using the following reasoning. There are two ways by which the capacitor $C_s$ can be charged during the transfer from line-connected mode to stand-alone mode of CSI-VCS operation. The first way is through the conversion of electromagnetic energy accumulated in the AC-line reactor $L_{ac}$ to the electrostatic energy of capacitor $C_s$. If at this stage the voltage across $C_s$ is less than either the line voltage or the output voltage, the capacitor gets additional charge. The goal of the design is to select $C_s$ such that the voltage across it due to the first process is below the amplitude of the line voltage or output voltage.

From the principal of energy conservation, the accumulated energy in the AC-line reactor has to be equal to the energy accumulated in the capacitor after the transfer, or:

$$L_{ac} \hat{I}_s^2 = C_s U_{C_s,max}^2,$$

where $\hat{I}_s$ is the amplitude of the line current and $U_{C_s,max}$ is the maximum voltage across the $C_s$ after the first process has completed.

Since the maximum desired voltage across the capacitor $C_s$ is equal to either the amplitude of line voltage or output voltage (whichever is larger), we have from
In order to have some safety margin, the suggestion is to take a value of $C_s$ which is 20-30% higher than calculated from Eq.(5.24).

The next step in the design of the STS snubber is to select the resistor $R_s$. The function of the resistor $R_s$ is to limit the discharge current through the main STS $S_s$ during the transfer from stand-alone to the line-connected mode of CSI-VCS operation. The suggested value of the discharge current is selected to be 20% of the nominal current, so that the rating of the main switch $S_s$ is just slightly increased. So, the value for $R_s$ can be selected to be:

$$R_s = \frac{U_{C_s,\text{max}}}{1.2 \cdot \dot{I}_s}.$$  

(5.25)

From the previous discussion it is easy to derive rating for the STS main-switch $S_s$. The peak switch current is equal to:

$$I_{\text{swSS,peak}} = 1.2 \cdot \dot{I}_s.$$  

(5.26)

The forward blocking voltage capability $V_{FB,SS}$ for the STS main-switch $S_s$ and diodes $D_1, \ldots, D_4$ is equal to:

$$V_{FB,SS} = \sqrt{2} \cdot V.$$  

(5.27)

5.5 Design Procedure

In this section the design procedure for a CSI voltage conditioning system is developed. The proposed design procedure consists of the following steps:

1. Selection and rating of the output filter $C$. 

125
2. Selection of $I_{d,\text{ref}}$, the DC-link current reference value.

3. Selection of $V_d$, the system input DC voltage value.

4. Selection and rating of DC-link inductor $L_d$.

5. Selection and rating of AC-link reactor $L_{ac}$.

6. Selection and rating of the semiconductor switches for the DC-chopper and the CSI.

7. Selection of static-transfer-switch snubber components ($C_s$ and $R_s$).

8. Selection and rating of the semiconductor switch and diodes for static-transfer-switch.


10. Design of the DC-chopper controller.

These steps are further elaborated in the following paragraphs:

1) Selection and rating of the output filter $C$: The design information presented in Section 5.1. is used for this step.

2) Selection of $I_{d,\text{ref}}$, the DC-link current reference value: The design information presented in Section 5.1. is used for this step.

3) Selection of $V_d$, the system input DC-voltage value: It has been shown in Chapter 3 of this thesis that in steady-state the average DC-chopper output voltage $v_{cho,\text{ave}}$ is equal to the average CSI input voltage $v_{\text{inv,ave}}$ during each switching period. In order to be able to provide this voltage, the minimum average DC-chopper output voltage has to be equal to the sum of the output voltage amplitude $\hat{V}$ and the voltage drop across the CSI switches:

$$|v_{cho,\text{ave}}|_{\text{min}} = |v_{\text{inv}}|_{\text{max}} + 2\Delta V_F = \hat{V} + 2\Delta V_F,$$

(5.28)

where $\Delta V_F$ is the forward voltage drop across the CSI switch during the conduction.
So, in order to provide the voltage at the DC-chopper output terminals given by Eq.(5.28), the input DC-voltage $V_d$ has to be (under the assumption that the forward voltage drop across the switch in DC-chopper and CSI is the same):

$$V_d = |v_{cho,ave}|_{\text{min}} + \Delta V_F,$$  \hspace{1cm} (5.29)

or, by using Eq.(5.28):

$$V_d = \dot{V} + 3\Delta V_F.$$ \hspace{1cm} (5.30)

In the case when the available input voltage is lower than the required value obtained from the design procedure, the output transformer is needed in order to adjust the voltage level of the voltage conditioning system to the required load voltage.

4) Selection and rating of the DC-link inductor $L_d$: The design information presented in section 5.2. is used for the selection and rating of the DC-link inductor.

5) Selection and rating of the AC-link reactor $L_{ac}$: The information presented in Section 5.3. of this thesis is used to select the AC-link reactor $L_{ac}$.

6) Selection and rating of the semiconductor switches for the DC-chopper and the CSI: For the design of the switches and diodes for the DC-chopper and CSI, the peak switch and diode current are calculated. Another parameter of interest is forward voltage blocking capability ($V_{FB}$).

The peak switch and diode current for the DC-chopper are equal to the peak DC-link current:

$$I_{\text{sucho,peak}} = I_{d,\text{peak}} = I_{d,\text{ref}} + \frac{\Delta I_d}{2}.$$ \hspace{1cm} (5.31)

The peak switch current for the CSI is equal to the peak DC-link current:

$$I_{\text{suwCSI,peak}} = I_{d,\text{peak}} = I_{d,\text{ref}} + \frac{\Delta I_d}{2}.$$ \hspace{1cm} (5.32)
The voltage $V_{FB,cho}$ for the DC-chopper switch $S_d$ and diode $D_d$ is equal to the system input voltage, i.e.:

$$V_{FB,cho} = V_d.$$  \hfill (5.33)

The voltage $V_{FB,csi}$ for the CSI switches is equal to the maximum value of the output voltage, i.e.:

$$V_{FB,CSI} = \hat{V}.$$ \hfill (5.34)

7) Selection of static-transfer-switch snubber components $C_s$ and $R_s$: The information presented in Section 5.4 of this thesis is used to select the static-transfer-switch components $C_s$ and $R_s$.

8) Selection of semiconductor switches for the static-transfer-switch: The information presented in Section 5.4 of this thesis is used to select the STS main-switch $S_s$ and the diodes $D_1, \ldots, D_4$.

9) Design of the CSI controller: The information presented in Section 4.2.1 of this thesis is used to design a controller for the CSI.

10) Design of the DC-chopper controller: The information presented in Section 4.2.2 of this thesis is used to design a controller for the DC-chopper.

5.6 Design Example

In this section, an example how to design a 10kVA CSI-VCS is presented. First, the design specifications of the system are given. Next, the step by step design procedure proposed in Section 5.5. is used to determine all the parameters of a 10kVA CSI-VCS. Finally, the simulation results for the design example are presented and the achieved performance of the proposed system is discussed.
5.6.1 Design Specifications of a 10kVA CSI-VCS

The design specifications for a 10kVA system are given as follows:

- Volt-ampere rating of the system: VA=10kVA
- Switching frequency: $f_s=8kHz$
- RMS value of the line voltage: $V_s=230V$, +20%, -10%
- RMS value of the output voltage: $V=230V$, +10%, -5%
- Output voltage frequency: $f=60Hz$
- Load power factor: PF=0.8 lagging
- DC-link current ripple: $\Delta I_d = 10\%$
- Output voltage THD: THD$\leq 5\%$

In the following subsections, the parameters for a 10kVA CSI-VCS are calculated and presented in per-unit form. The base values for the used per-unit system are defined as follows:

- Base power: $S_b=10kVA$
- Base voltage: $V_b=230V$
- Base current: $I_b = \frac{S_b}{V_b} = 43.48A$
- Base impedance: $Z_b = \frac{V_b}{I_b} = 5.29\Omega$
- Base frequency: $f_b=60Hz$
- Base angular frequency: $\omega_b = 377rad/s$
- Base inductance: $L_b = \frac{Z_b}{\omega_b} = 0.014H$
- Base capacitance: $C_b = \frac{1}{\omega_b Z_b} = 501\mu F$
5.6.2 Design of a 10kVA CSI-VCS

1) and 2) Output filter and DC-link current reference design: The design procedure presented in section 5.1. is used in order to design the output filter $C$ and determine the reference value for the DC-link current $I_{d,ref}$. The steps presented in section 5.1. are employed to find the optimum value of the output filter and DC-link current reference to satisfy the given specifications. Using the design specifications and a computer routine it is found that these values satisfy the given system requirements:

$$C = 186\mu F = 0.37pu.$$ 
(5.35)

$$I_{d,ref} = 64A = 1.47pu.$$ 
(5.36)

Using the same computer routine, the following values for various variables of the CSI voltage conditioning system are obtained:

$$I_{inv} = 36.2A = 0.83pu.$$ 
(5.37)

$$I_C = 16A = 0.44pu.$$ 
(5.38)

$$M_{a,0} = 0.356.$$ 
(5.39)

$$\Delta I_d = 0.1I_{d,ref} = 6.4A = 0.15pu.$$ 
(5.40)

3) Selection of the system input DC-voltage level: The system input DC-voltage can be found by using the relation given by equation Eq.(5.30) in the design procedure.

$$V_d = \sqrt{2} \cdot 230V + 3 \cdot 2V \approx 330V.$$ 
(5.41)

4) DC-link inductor design: From the design procedure presented in section 5.2, the following optimum value for the DC-link inductor is determined in order to satisfy the given specifications for the allowed DC-link current ripple:

$$L_d = 3.22mH = 0.23pu.$$ 
(5.42)
The DC-link reactance is then:

$$X_d = 1.21 \Omega = 0.23pu.$$ \hspace{1cm} (5.43)

5) **AC-link reactor design:** From the design procedure presented in section 5.3, the following optimum value for the AC-link reactor is determined in order to limit the output voltage steady-state error to 3%:

$$L_{ac} = 1.635mH.$$ \hspace{1cm} (5.44)

The AC-link reactor impedance is then:

$$X_{ac} = 0.6164\Omega.$$ \hspace{1cm} (5.45)

Based on this value of AC-link reactor, the phase angle of the line current $I_s$ is calculated to be 16-deg lagging.

6) **Selection and rating of the semiconductor switches for the DC-chopper and the CSI:**

The peak switch and diode current for the DC-chopper is:

$$I_{sw,peak} = I_{d,peak} \approx 67.2A.$$ \hspace{1cm} (5.46)

The voltage $V_{FB,cho}$ for the DC-chopper switch and diode is:

$$V_{FB,cho} = 330V.$$. \hspace{1cm} (5.47)

The peak switch current for the CSI is:

$$I_{sw,peak} \approx 67.2A.$$ \hspace{1cm} (5.48)

The voltage $V_{FB,CSI}$ for the CSI switches is:

$$V_{FB,csi} \approx 330V.$$ \hspace{1cm} (5.49)
7) Selection of static-transfer-switch snubber components $C_s$ and $R_s$:

From Eq. (5.4), we have for $C_s$:

$$C_s = \frac{L_{ac} \hat{I}_s^2}{V} = \frac{1.635 mH \cdot 51.04^2 A}{324.3 V} = 1313 \mu F.$$  (5.50)

From Eq. (5.25), we have for $R_s$:

$$R_s = \frac{U_{C_s, max}}{1.2 \cdot \hat{I}_s} = 5.3 \Omega.$$  (5.51)

8) Selection and rating of the semiconductor switch for static-transfer-switch: The peak switch and diode current for the static-transfer-switch is:

$$I_{sw, peak} = 1.2 \hat{I}_s = 61.25 A.$$  (5.52)

The voltage $V_{FB, SS}$ for the static-transfer-switch $S_s$ and diodes $D_1, \cdots, D_4$ is:

$$V_{FB, SS} = \sqrt{2} \cdot V = \sqrt{2} \cdot 230 V = 324.3 V.$$  (5.53)

9) Design of the CSI controller: Using the parameters of the CSI-VCS given in Figure 5.5, from Eq. (4.17), the following gain $K_{CSI}$ is obtained for the CSI controller:

$$K_{CSI} = \frac{2C}{I_d T_s} = \frac{2 \cdot 186 \mu F}{64 \cdot 125 \mu s} = 0.0465.$$  (5.54)

10) Design of the DC-chopper controller: Using the same reasoning as in Section 4.2.2 of this thesis, the DC-chopper compensator $K_{cho}$ for the CSI-VCS shown in Figure 5.5 is derived as follows:

$$K_{cho} = \frac{0.2(s + 1000)}{s}.$$  (5.55)

5.6.3 Simulation Results for a 10kVA CSI-VCS

In order to validate the design procedure, a computer simulation is performed with the CSI-VCS parameters used in the design example, and the simulation results are
presented in this section. The circuit parameters obtained from the design procedure and used in the simulation are summarized in Figure 5.5.

In Figure 5.6, a steady-state simulation results of the CSI-VCS shown in Figure 5.5 and operating in line-connected mode are presented. In Figure 5.6a), the output voltage waveform $v$(solid line), line voltage $v_l$(dashed line) and output voltage reference $v_{ref}$(dotted line) are shown. It can be seen from this figure that the output voltage deviation from the reference value is small in the steady-state. In Figure 5.6b), the output filter capacitor current $i_C$(solid line), load current $i_{load}$(dashed line) and line current $i_s$(dotted line) are shown. From this figure, it can be seen, that the output filter current leads 90deg the output voltage and that the load current lags the output voltage by 36deg. Also, it can be seen that the line current lags the output voltage by 16deg as predicted in Section 5.6.2 of this thesis.

Figure 5.7 shows the steady-state simulation results of the CSI-VCS shown in Figure 5.5 and operating in stand-alone mode. In Figure 5.7a) the output voltage waveform $v$(solid line) and output voltage reference $v_{ref}$(dashed line) are shown. It can be seen from the simulation results that the output voltage is with low THD(3.7%) and that it perfectly tracks the output voltage reference. In Figure 5.7b), the DC-link current $i_d$(solid line) and DC-link current reference $i_{d,ref}$(dashed line) are shown. It can be seen that the ripple of the DC-link current completely complies with the design specifications(<10% ) and that the DC-link current perfectly tracks the DC-link current reference. This validates the controller design for CSI and DC-chopper.

In Figure 5.8a), the output voltage $v$ of the CSI-VCS(shown in Figure 5.5), operating in stand-alone mode, is shown in the steady-state. In Figure 5.8b), the harmonic content of the output voltage waveform $v$ is indicated. Also, it can be seen that the output voltage waveform has a low THD with the discrete spectrum as expected for the SPWM scheme which is used. The calculated THD of the output voltage...
Figure 5.5: A simplified power circuit diagram of a 10kVA line-connected single-phase CSI-VCS with the circuit parameters obtained from the design procedure.
Figure 5.6: The steady-state simulation results for the CSI-VCS shown in Figure 5.5 and operating in line-connected mode:

a) Output voltage waveform $v$ (solid line), line voltage $v_s$ (dashed line) and output voltage reference $v_{ref}$ (dotted line),

b) Output filter capacitor current $i_C$ (solid line), load current $i_{load}$ (dashed line) and line current $i_s$ (dotted line).
Figure 5.7: The steady-state simulation results for the CSI-VCS shown in Figure 5.5 and operating in stand-alone mode:

a) Output voltage waveform $v$(solid line) and output voltage reference $v_{ref}$(dashed line),

b) DC-link current $i_d$(solid line) and DC-link current reference $i_{d,ref}$(dashed line).
waveform is 3.7%, which satisfies the design specifications.

Figure 5.8: The steady-state simulation results for the CSI-VCS shown in Figure 5.5 and operating in stand-alone mode:  
a) Output voltage waveform \( v \),  
b) Amplitudes of the harmonics present in the output voltage.

Figures 5.9 and 5.10 show the simulation results for various variables of the CSI-VCS shown in Figure 5.5 and operating in the stand-alone mode. From Figure 5.9, it can be seen that the DC-chopper output voltage averaged over each switching instant coincides with the CSI input voltage averaged over the same period, as expected from the discussion presented in Section 3.2. From Figure 5.10 it can be seen that the output filter capacitor absorbs most of the inverter output current harmonics,
leaving only a small amount of harmonic content in the load current.

Figure 5.9: The steady-state simulation results for the CSI-VCS shown in Figure 5.5 and operating in stand-alone mode:

a) DC-chopper output voltage waveform $v_{cho}$,

b) CSI input voltage waveform $v_{inv}$. 
Figure 5.10: The steady-state simulation results for the CSI-VCS shown in Figure 5.5 and operating in stand-alone mode:

a) Output filter capacitor current $i_C$,

b) CSI output current $i_{inv}$. 
Figure 5.11 shows the simulation results for a sudden load change from full-load to no-load. The results show that the system is stable and has an instantaneous dynamic response with almost no over/undershoot. This shows the superior performance of the CSI and DC-chopper controller proposed in this thesis.

![Image of voltage and current graphs](image_url)

Figure 5.11: Transient of the output voltage $v$ and the load current $i_{\text{load}}$ for a sudden change from full-load to no-load. (Simulation results for the CSI-VCS shown in Figure 5.5 and operating in stand-alone mode).

Figure 5.12 shows the simulation results for a transfer from a line-connected to stand-alone mode of operation. The disturbance on the line side (undervoltage of 30%) occurred at $t = 0s$ and the disturbance detection algorithm initiated the transfer at $t = 0.02s$. The results show that the response time of the system is approximately 2
ms, since the perfect tracking of the output voltage reference in stand-alone mode is achieved by then.

Figure 5.12: Simulation results of the system shown in Figure 5.5 for the case of transfer from line-connected to stand-alone mode. The transfer occurred after the disturbance on the line has reached the threshold limit.

a) Output voltage waveform \( v \) (solid line) and output voltage reference \( v_{\text{ref}} \) (dashed line),

b) DC-link current \( i_d \) (solid line) and DC-link current reference \( i_{d,\text{ref}} \) (dashed line),

c) Voltage across the static-transfer-switch snubber capacitor \( C_s \).

Figure 5.13 shows the simulation results for a transfer from stand-alone to line-
connected mode of operation. At \( t = 0.02s \), the line voltage recovery is detected and the transfer back to the line is initiated at \( t = 0.021s \). The results show that the response time of the DC-link current to reach its reference value is approximately less than one millisecond. It can be also seen from the simulation that approximately one cycle is needed for the output voltage to settle down to its steady-state value. The oscillations present on the output voltage during the transfer are due to the resonance between the output filter capacitor \( C \) and the line reactor \( L_{ac} \).

![Graphical representation](image)

**Figure 5.13:** Simulation results of the system shown in Figure 5.5 for the case of transfer from stand-alone to line-connected mode. The transfer occurred after the line recovery was detected.

a) Output voltage waveform \( v \) (solid line) and output voltage reference \( v_{ref} \) (dashed line),

b) DC-link current \( i_d \) (solid line) and DC-link current reference \( i_{d,ref} \) (dashed line),

c) Voltage across the static-transfer-switch snubber capacitor \( C_s \).
Chapter 6

Conclusions

In this thesis, a novel efficient line-connected voltage-conditioner with minimum disturbance transfer to a stand-alone mode has been proposed. To the authors best knowledge, the concept of the solid-state breaker which is used in this thesis has not been reported in the literature so far. The proposed CSI-VCS offers the advantages in terms of efficiency, transfer time and dynamic behavior over the existing voltage-conditioning systems. The theoretical work presented in this thesis has been verified on an experimental 1kVA system which has been built. The main contributions and conclusions of this thesis are summarized as follows:

- A single-phase line-connected CSI-VCS with the capability of instantaneous transfer to stand-alone mode, which conditions the line voltage on the equipment level, has been proposed. By using the static-transfer-switch which performs the instantaneous transfer between on-line and off-line mode, the system overcomes the drawback of the existent VCS’s with extended transfer times. It is shown that the proposed system can conform to the susceptibility characteristics of different electronic equipment. The system can be widely used having in mind both increased interest in the power quality issue and more stringent
requirements for reliable power. The proposed system can conform to different power quality requirements with the changes being only in line voltage threshold limits. This improves the flexibility of the system.

- It has been shown that by using the off-line conditioning concept, the energy savings of up to 30% (measured on a 1kVA CSI-VCS prototype) are achieved. Using the line-connected mode and stand-alone mode, the efficient transfer of energy has been maintained with almost no penalty in the conditioning performance. In the case where the line voltage is within permissible limits, the CSI-VCS operates in line-connected mode. In the case of a line voltage disturbance or failure, the proposed system switches to the stand-alone mode and conditions the load voltage. This is achieved by using the proposed static-switch with instantaneous cut-off capability.

- The proposed system has excellent transient performance under load disturbances. This has been achieved using the loopshaping techniques in addition to feedforward in the controller design in stand-alone mode. The proposed control technique uses a simple controller design which is independent of the load parameters. Furthermore, with almost instantaneous transient response it perfectly tracks the output voltage reference.

- In order to detect a disturbance on the line side, a novel line-voltage-disturbance detection scheme has been proposed. The proposed method is well suited for real-time applications which are related to power quality issues. The method uses already existing digital filtering and integration techniques which are adapted for the disturbance detection algorithm. With software implementation proposed in this thesis the need for additional hardware has been eliminated.

- Steady-state analysis of the proposed CSI-VCS has been performed in order to determine the power circuit component ratings. The expressions for all system variables, including the harmonics, have been obtained. Fourier analysis has
been performed and the expressions for all system voltages/currents have been obtained.

- A systematic design procedure for the CSI-VCS has been proposed based on the steady-state analysis. In order to validate the design procedure, a 10kVA design example has been presented. The proposed design procedure has been followed step by step, and all the system parameters have been selected. Using the obtained parameters the system has been simulated. The agreement between the simulated and expected theoretical results has been achieved.

The suggestions for the future work include:

1. The optimal inverter-type for the proposed VCS has to be defined. The operation of the proposed VCS using the voltage-source inverter has to be studied. A systematic comparison procedure has to be defined and the advantages/disadvantages of using voltage-type and current-type inverters in the proposed VCS have to be investigated.

2. In order to further improve the efficiency of the proposed voltage-conditioner, the feasibility of employing other available devices for the solid-state breaker should be investigated. This includes emerging PIN-Schottky diodes for the static-transfer-switch diode bridge.

3. The implementation of the proposed system on a low-cost processor should be investigated in order to provide a more economical system solution. Software improvements such as optimal code are also possible.

4. In the case where large inrush currents are expected to be drawn by critical loads during their start-up, the proposed system can possibly provide a feasible solution. Such critical loads can be operated in line-connected mode during the start-up and transferred to the stand-alone mode in the case of a disturbance.
on the line. By using the proposed system in these applications, the rating of
the power converter stage operating only in stand-alone mode can be reduced.

5. A suggestion for future work is also to investigate a 3-phase CSI-VCS. The re-
search presented in this thesis is focused on a low-power single-phase CSI voltage
conditioning system. In order to employ the proposed converter configuration
for higher power levels, a three-phase CSI voltage conditioning system should
be investigated.

6. Finally, the application of the proposed VCS connected to the alternate sources
such as fuel-cells and wind-power plants should be investigated. These alternate
sources can not respond to sudden load changes. Therefore, the proposed CSI-
VCS can be possibly used in these applications in order to provide power balance
under all operating conditions.
Appendix A

System Parameters of a CSI-VCS

In this appendix, the CSI voltage conditioning system parameters used in Chapters 2, 3 and 4 of this thesis for the simulation and experiment are given. Furthermore, the base values for a per unit system are defined.

In this thesis, most of the numerical and simulation results are based on physical values of the parameters. The per unit system is mainly used for expressing the filter components \((L_d, C, L_{ac})\). The proposed CSI-VCS is shown in Figure A.1 and all the specifications and parameters given in this appendix are related to that Figure.

A.1 System Specifications

A.1.1 Rated Values

\[
\begin{align*}
S_{\text{rated}} &= 1000\text{VA} \quad \text{(Output Power)} \\
V_{\text{rated}} &= 115\text{V} \quad \text{(Output Voltage)} \\
f_{\text{rated}} &= 60\text{Hz} \quad \text{(Output Frequency)}
\end{align*}
\]
Figure A.1: A simplified power circuit diagram of a line-connected single-phase CSI voltage conditioning system with the AC-mains, DC-voltage source and the load.

\[ PF_{rated} = 0.8 \text{ lagging} \quad \text{(Load Power Factor)} \]

### A.1.2 Base Values

\[ S_b = S_{rated} = 1000\text{VA} \quad \text{(Base Power)} \]

\[ V_b = V_{rated} = 115\text{V} \quad \text{(Base Voltage)} \]
\[ f_b = f_{\text{rated}} = 60\text{Hz} \quad \text{(Base Frequency)} \]
\[ \omega_b = \omega_{\text{rated}} = 377\text{rad/s} \quad \text{(Base Angular Frequency)} \]
\[ I_b = \frac{V_b}{V_0} = 8.696\text{A} \quad \text{(Base Current)} \]
\[ Z_b = \frac{V_b}{I_b} = 13.22\Omega \quad \text{(Base Impedance)} \]
\[ L_b = \frac{V_b}{\omega_b} = 0.035\text{H} \quad \text{(Base Inductance)} \]
\[ C_b = \frac{1}{\omega_b Z_b} = 200\mu\text{F} \quad \text{(Base Capacitance)} \]

A.2 System Parameters

The switching frequency of the CSI is equal to the DC-chopper switching frequency and is chosen to be 8kHz. Based on the design procedure presented in chapter 5 of this thesis, the following parameters have been obtained for a 1kVA system.

A.2.1 Components in the Power Circuit

\[ R_d = 0.1\Omega \quad (0.0076 \text{ p.u.}) \]
\[ L_d = 10\text{mH} \quad (0.286 \text{ p.u.}) \]
\[ C = 100\mu\text{F} \quad (0.5 \text{ p.u.}) \]
\[ R_{ac} = 0.2\Omega \quad (0.038 \text{ p.u.}) \]
\[ L_{ac} = 1.7\text{mH} \quad (0.0486 \text{ p.u.}) \]
\[ R_s = 50\Omega \quad (3.78 \text{ p.u.}) \]
\[ C_s = 3600\mu\text{F} \quad (18.0 \text{ p.u.}) \]
A.2.2 Parameters of the Voltage Sources

\[ V_d = 220V \quad (1.913 \text{ p.u.}) \]
\[ E_e = 115V \quad (1.0 \text{ p.u.}) \]
\[ R_e = \text{n.a.} \quad (\text{n.a. p.u.}) \]
\[ L_e = \text{n.a.} \quad (\text{n.a. p.u.}) \]

A.2.3 Parameters Related to System Implementation

Sampling Frequency = 8kHz
Voltage Sensor Gain = 20V/V
Current Sensor Gain = 5A/V

A.2.4 Controller Parameters

\[ K_{cho} = \frac{0.001(s+1)}{s(s+0.1)} \]
\[ K_{CSI} = 0.03 \]
Appendix B

Output Voltage Reference Synchronization

In order for the CSI-VCS to perform the synchronization function described in Chapter 2, in this appendix, a novel scheme is proposed that can be used to phase-lock a voltage reference signal to the output voltage of an ac power supply. A synchronization scheme is used in order to provide the conditions for the safe transfer between the line-connected mode and stand-alone mode of the proposed system as described in Chapter 2 of this thesis.

Although there are many different synchronization schemes that can be found in the literature [69,70,71,72], all of them use the specific hardware to realize this function. In order not to use any additional glue logic for this function and to use the UHP40-platform[28](already used for the control function of the proposed CSI-VCS), the proposed algorithm has been fully implemented in software. The details of the design are given in the following paragraphs.

The proposed CSI-VCS is shown in Figure B.1. In order to provide the output
Figure B.1: A simplified power circuit diagram of a line-connected single-phase CSI voltage conditioning system with the AC-mains, DC-voltage source and the load.

voltage reference $v_{\text{ref}}$ which is synchronized to the line voltage $v_s$, the following procedure has been proposed in this thesis. First, zero crossings of the line voltage have been detected. Second, the voltage reference look-up table has been created for the nominal frequency of 60Hz and is reinitialized periodically by each incoming zero crossing event. In addition, the mechanism for providing the free-running voltage reference in the case of the line voltage blackout is provided. Finally, the voltage reference look-up table for 61Hz has been created in order to compensate for the
phase shift between the line voltage and output voltage reference in the case when line voltage has resumed after the outage. The phase shift occurs as a consequence of a finite response time of the predictive filter. The frequency of 61Hz is chosen since most of the equipment has ±1Hz tolerance in respect to the supply frequency (the 59 Hz would be a valid option as well). The details of the algorithm performing the synchronization procedure are given in the following paragraphs.

The digital filters described in [67, 68], and shown in the form of the block diagram in Figure B.2, have been used in order to reliably detect the zero crossings of the line voltage. A third-order median filter is used for notch suppression and a twelfth-order predictive FIR bandpass filter for overall delay compensation and noise suppression. The upsampling with interpolation has not been used as in [67, 68] since the obtained zero-crossing detection resolution was found to be satisfactory for the given application.

Figure B.2: A simplified block diagram showing the digital processing of the line voltage \( v_s \) for the purposes of synthesizing the synchronized output voltage reference \( v_{ref} \).

Based on the procedure described in [67, 68], and for the 60Hz line frequency, a sampling frequency of 8kHz and a prediction horizon of two-steps-ahead \( p = -2 \) the following transfer function has been obtained for the twelfth-order predictive FIR filter used in this thesis:

\[
H(z) = 0.225439 + 0.200691z^{-1} + 0.168833z^{-2} + 0.130994z^{-3} + 0.0885146z^{-4} + 0.0428996z^{-5}
\]
The amplitude and phase response of the predictor (B.1) are shown in Figure B.3. At the nominal frequency of $0.06\pi$, the amplitude response is equal to unity, and the phase delay is $-0.12\pi/0.06\pi = -2$ time units, corresponding to a forward phase shift of two sampling periods. One sampling period compensates for the delay introduced by the median filter and the other is provided to compensate for the calculation delay. The noise power gain, $\sum_{k=1}^{N}[h(k)]^2 = 0.25$.

The noise power gain is calculated as $\sum_{k=1}^{N}[h(k)]^2 = 0.25$. 

Figure B.3: Amplitude and phase response of the predictive FIR filter used for the zero crossing detection of the line voltage given with the transfer function (B.1.)
Using the samples \( \nu_{s,filt} \) of digitally processed line voltage \( \nu_s \) depicted in Figure B.2, the zero crossings are determined at each sampling instant. If the sign of signal \( \nu_{s,filt} \) has changed from negative to positive value over the last two sampling instants, a zero crossing of the line voltage has occurred. At that instant, the counter for the 60Hz sinusoidal output voltage reference look-up table is reset to zero. After the reset, at each upcoming sampling instant the next value of the sinusoidal look-up table prestored in the RAM memory of the TMS320C40 is loaded and used as the instantaneous output voltage reference.

In the case of the line voltage outage, the look-up table counter starts periodically (with the frequency of 60Hz) resetting itself, allowing the output voltage reference to free-run. The method for detecting the voltage outage is presented in Appendix C.

In the case of the line voltage recovery after the outage, the output voltage reference and line voltage are or can be phase-shifted. The only way to synchronize the reference signal to the line voltage in this case is to let the reference signal run with an increased frequency. So, after the line voltage recovery, the output voltage reference starts loading the values from the 61Hz look-up table, forcing the reference to slowly phase-shift with respect to the line. After some time, the zero crossings of the two waveforms will coincide. As soon as the reference and line are phase-locked, the reference starts again loading the values from the 60Hz look-up table. At this instant, the synchronizing condition to transfer to the line has been satisfied and synchronization flag sync_flag is set.

In order to demonstrate the operation of the synchronization algorithm, two special cases have been discussed and experimental results presented.

In the first case, the line voltage outage occurred at \( t = 0.1s \) and the voltage reference started free-running. This is shown in Figure B.4.
In the second case, the voltage reference has been free-running for some time, and the synchronization is performed after the line voltage recovery. This is shown in Figure B.5. It can be seen that the voltage reference is phase shifted approximately 90 deg from the line initially. In order to synchronize the voltage reference to the line, the voltage reference starts loading the values from the 61Hz look-up table (prestored in the DSP memory). At around $t = 0.34s$, the line and the reference are phase-locked and the synchronization flag sync_flag is set.

![Line Voltage Outage](image)

Figure B.4: The synthesized voltage reference $v_{ref}$ in the case of the line voltage outage.
Figure B.5: The synchronization of the voltage reference $v_{ref}$ to the line voltage $v_s$ in the case of the line voltage recovery.
The pseudo code for the synchronization algorithm proposed in this thesis is given below.

Initialization{
    Create 60Hz and 61Hz Look-Up Tables
    Initialize 60Hz Look-Up Table Counter to 0
    Initialize 61Hz Look-Up Table Counter to 0
    Reset Line-Voltage-In Flag
    Reset Sync-Procedure-In Flag
} /* end of initialization */
Sampling of the Line Voltage
Median Filtering of the Line Voltage
Predictive Filtering of the Median Filter Output
Checking if the Line Outage Occurred
If(Line Present Now && Line Absent Before &&
    System Not in Sync Procedure){
    Set Sync-Procedure-In Flag
    Phase-In 61Hz Look-Up Table
    Set Line-Voltage-In Flag
} /* end of if */
If(Line is Present Now && System Started Sync Procedure){
    Use 61Hz Look-Up Table for Voltage Reference
} /* end of if */
else{
    Use 60Hz Look-Up Table for Voltage Reference
} /* end of else */
If(Zero Voltage Crossing Detected && Line Present Now &&
    61Hz Look-Up Table Counter = 0 && System in Sync Procedure){
    Reset Line-Voltage-In Flag(synch_line_in=0)
    Reset Sync-Procedure-In Flag(set_vl_income=0)
Initialize 60Hz Look-Up Table Counter to 0
Initialize 61Hz Look-Up Table Counter to 0
} /* end of if */

If(Zero Voltage Crossing Detected && Line is Present Now &&
   System Not in Sync Procedure){
    Initialize 60Hz Look-Up Table Counter to 0
} /* end of if */

Increase 60Hz Look-Up Table Counter by one
If(60Hz Look-Up Table Counter > 60Hz Table Length){
    Initialize 60Hz Look-Up Table Counter to 0
} /* end of if */

If(61Hz Look-Up Table Counter > 61Hz Table Length){
    Initialize 61Hz Look-Up Table Counter to 0
} /* end of if */

The synchronization algorithm takes 35µs to execute on the UHP40 platform using
the TMS320C40 processor.
Appendix C

Line Disturbance Detection Method

In this appendix, a novel method for line disturbance detection has been proposed. This method is used in the CSI-VCS controller in order to acknowledge a request for transfer to the line-connected or the stand-alone mode. The proposed line disturbance detection method is implemented in software and is well suited for real-time applications in power electronics which are related to power quality issues.

Many line disturbance detection methods have been proposed lately in the literature [48, 49, 50, 53]. The analog method is proposed in [53], the floating-window algorithm in [49] and the wavelet analysis in [50]. All of these methods are used for line-disturbance off-line analysis of the collected data from the power quality nodes [1]. None of these methods discuss the real-time application of the line-disturbance detection method which can be used on-line. Therefore, the algorithm proposed in this thesis is dealing with detecting the line disturbances in real-time.

The line voltage disturbance detection block decides on the optimal mode of CSI-
VCS operation at any given time. Due to possible glitches in the distribution line and measurement noise, the appropriate filtering of the line voltage has been implemented as described in the Appendix B of this thesis. Using this filtered signal of the line voltage a novel procedure for reliable detection of the line disturbances is proposed in this appendix.

The algorithm structure used for line voltage disturbance detection is shown in the form of the block diagram in Figure C.1. The line voltage \( v_s \) has been sensed and further processed by the median and FIR filter. The digital signal processing stage including the filtering has been described in Appendix B.

![Figure C.1: The block diagram of the line voltage disturbance detection method proposed in this thesis.](image)

Next, the relative error of the line voltage \( \text{error}_{rel} \) is defined as follows:

\[
\text{error}_{rel} = \frac{v_{s,\text{filt}} - v_\text{ref}}{v_\text{ref}}, \tag{C.1}
\]

where \( v_{s,\text{filt}} \) is the output of the FIR predictive filter and \( v_\text{ref} \) is the output voltage reference obtained from the synchronization algorithm. This relative error is calculated only between 15 and 165 degrees of the output voltage reference sinusoid since the denominator in Eq.(C.1) tends to zero near zero-crossings, giving infinite error at these instants. The area under the sinusoid between 0-15deg and 165-180deg which
does not take part in the relative error calculation is compensated by multiplying the relative error by a constant factor. This factor is determined as the ratio of the rms values of the full sinusoid and a sinusoid defined only between 15 and 165 deg. It is easy to prove that the rms value of the full sinusoid is $\sqrt{6}=0.58$ times larger than the rms value of the sinusoid calculated between 15-165deg.

In order to evaluate the weight of the relative error of the line voltage defined in Eq.(C.1), the susceptibility curve of the electronic equipment which the CSI-VCS is conditioning has to be known in advance. The susceptibility curve for the industrial equipment is usually given as the graph of overvoltage/undervoltage-amplitude versus time.

It is important to emphasize at this point that the proposed procedure used in this thesis to evaluate the quality of the line voltage can be used for any design specifications and voltage tolerance limits. Only the weights imposed on the relative error are going to change according to the susceptibility specification of the given equipment. The method has been demonstrated in this appendix using the CBEMA curve shown in Figure C.2.

Based on the susceptibility curve, and using the proposed method, the proper weights on the voltage error are imposed so that the equipment voltage-tolerance limits are exceeded within the specified time. This means that the relative error is calculated at each sampling instant and that error is weighted in the following way. The weight is introduced for each value of the undervoltage/overvoltage in such a way that the weighted error i.e. relative error multiplied by its weight and integrated over time reaches the disturbance threshold limit exactly after the time interval specified by the equipment susceptibility curve. The example showing a few discrete calculated weights based on the CBEMA curve are shown in Table C.1 and Table C.2.
Figure C.2: The CBEMA curve introduced in the introduction, used here as an example for the equipment susceptibility curve in order to validate the line disturbance detection algorithm.
Table C.1: Positive weights used for the CBEMA curve by the line disturbance detection method in the case of the line overvoltage.

<table>
<thead>
<tr>
<th></th>
<th>Point 1</th>
<th>Point 2</th>
<th>Point 3</th>
<th>Point 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time duration of the disturbance</td>
<td>0.1s</td>
<td>8.3ms</td>
<td>1ms</td>
<td>100µs</td>
</tr>
<tr>
<td>Number of samples</td>
<td>800</td>
<td>66</td>
<td>8</td>
<td>1</td>
</tr>
<tr>
<td>Allowable disturbance amplitude</td>
<td>0.1</td>
<td>0.3</td>
<td>1.0</td>
<td>2.0</td>
</tr>
<tr>
<td>Weight</td>
<td>0.0125</td>
<td>0.05</td>
<td>0.125</td>
<td>0.5</td>
</tr>
</tbody>
</table>

Table C.2: Negative weights used for the CBEMA curve by the line disturbance detection method in the case of the line undervoltage.

<table>
<thead>
<tr>
<th></th>
<th>Point 1</th>
<th>Point 2</th>
<th>Point 3</th>
<th>Point 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time duration of the disturbance</td>
<td>0.5s</td>
<td>0.1</td>
<td>16ms</td>
<td>8.33ms</td>
</tr>
<tr>
<td>Number of samples</td>
<td>4000</td>
<td>800</td>
<td>133</td>
<td>67</td>
</tr>
<tr>
<td>Allowable disturbance amplitude</td>
<td>0.3</td>
<td>0.42</td>
<td>0.7</td>
<td>1.0</td>
</tr>
<tr>
<td>Weight</td>
<td>0.00083</td>
<td>0.00298</td>
<td>0.0107</td>
<td>0.015</td>
</tr>
</tbody>
</table>

As an example how the weights in these tables are calculated, look for the element in the second column and third row of Table C.1. If the overvoltage of 30% is detected, based on the CBEMA curve, after 8.3ms, the threshold limit should be reached. Since
the threshold limit is chosen to be 1 for a positive weight and -1 for the negative weight, the following equation has to be satisfied in order to determine the proper weight for the particular relative error:

\[ 1 = Weight \cdot DisturbanceAmplitude \cdot No. \ of \ Sampling \ Instants, \quad \text{(C.2)} \]

where

\[ No. \ of \ Sampling \ Instants = \frac{Allowable \ Disturbance \ Time}{Sampling \ Period}. \quad \text{(C.3)} \]

So, for the given example, from Eq.(C.3), we have:

\[ No. \ of \ Sampling \ Instants = \frac{8.33\text{ms}}{125\mu s} = 66, \quad \text{(C.4)} \]

for a sampling frequency of 8kHz. Using this result and Eq.(C.2), the following weight has been calculated:

\[ Weight = \frac{1}{0.3 \cdot 67} = 0.05, \quad \text{(C.5)} \]

and is shown as the element in the second column and fourth row of Table C.1.

So, based on the input data(first three rows) presented in Tables C.1 and C.2, the discrete values of positive and negative weights(fourth row) for any value of the relative error are calculated as described above. Then, using the curve fitting of given discrete weight points from the tables, it is possible to obtain continuous functions of positive/negative weights. The arguments of these weighting functions are relative errors and in the case of the CBEMA curve are given by following expressions:

\[ pos. \ weight = 0.1061error_{rel}^3 - 0.195error_{rel}^2 + 0.2167error_{rel} - 0.0026 \quad \text{(C.6)} \]

and

\[ neg. \ weight = -0.0676error_{rel}^3 + 0.1203error_{rel}^2 - 0.0422error_{rel} + 0.0045. \quad \text{(C.7)} \]

These weighting functions are calculated at each sampling instant and are presented in Figure C.3 as continuous functions of the line disturbance amplitude.
Figure C.3: The positive and negative weights used in the line disturbance detection method shown as functions of the disturbance amplitude.

The integration method used to integrate the weighted error in this algorithm in order to accumulate the effect of the voltage disturbance over time is based on a digital integrator presented in [42,43]. For floating point digital filters (such as TMS320C40 of Texas Instruments) there is a simple implementation of the integrator with the inherent limit of the integration time. Instead of realizing the pole $z = 1$ for an ideal digital integrator, it is sufficient to realize $z = 0.999 \cdots$, where the number of nines is determined by the dynamic range of the floating point representation as well as the integration time.

The simple comparator block is used after the integration for detecting if the line
voltage disturbance threshold limit has been reached, as shown in Figure C.1. If the absolute value of the integrated error is higher than one, that means that the threshold limit has been reached and that the line voltage is out of the specified limits. Setting the signal transfer, at that instant, initiates the request for the system to switch to stand-alone mode.

In the case of a voltage recovery after the outage, the integration error starts decreasing due to the limited integration time as described above. If the magnitude of the integral error drops under a specified level (lower threshold limit), the line voltage is assumed to be again within acceptable amplitude limits. At that instant, the transfer to the line-connected mode is initiated.

The pseudo code for the line disturbance detection algorithm used in this thesis is given below. Setting the variable Transfer is used to define if the transfer to the stand alone mode is requested by the algorithm and setting the variable Stand_Alone serves to indicate that the system is in the stand-alone mode of operation. The output of the FIR filter is denoted in the algorithm as FIR_out and the output voltage reference as Out_Vol_Ref. All other variables used in the pseudo code are descriptive and self explanatory.

```
Initialization{
    Transfer = 0
    Stand_Alone = 0
}/* end of initialization */
Sampling of the Line Voltage
Median Filtering of the Line Voltage
Predictive Filtering of the Median Filter Output
Calculating the Abs(Out_Vol_Ref)
If(15deg < Abs(Out_Vol_Ref) < 165deg){
    Relative Error = (FIR_out - Out_Vol_Ref)/Out_Vol_Ref
}/* end of if */
```
else{
    Relative Error = 0
}/* end of else */
If(Relative Error > 0){
    Weight = Positive Weight
}/* end of if */
If(Relative Error < 0){
    Weight = Negative Weight
}/* end of if */
Calculating the Weighted Error
Calculating the Integral Error
Limiting the Integral Error to +/-1
If(Integral Error >= 1 || Integral Error <= -1){
    Set Transfer
    Set Stand_Alone
}/* end of if */
If(Stand Alone == 0 && (-0.2 < Integral Error < 0.2){
    Transfer = 0
}/* end of if */

The synchronization algorithm takes 10μs to execute on the UHP40 platform using the TMS320C40 processor.

In order to demonstrate the line disturbance detection method proposed in this thesis, three characteristic cases are taken into account and experimental results presented.

In the first case, a 10% overvoltage has been detected on the line(at t=0.02s) and simulation/experimental results showing the characteristic waveforms of the algorithm are shown in Figure C.4(simulation results)/Figure C.5(experimental results). As can be seen, 140ms after the line disturbance occurred(at t=0.16s), the integral
error reached the threshold limit 1 and at that instant the transfer flag has been set by the algorithm. This detection time is equal to the time which is specified by the CBEMA curve in the case of 10% overvoltage. This can be seen in Figure C.2.

Figure C.4: Simulation Results: Line voltage, integral error and transfer flag waveforms in the case of 10% overvoltage occurring on the line.
Figure C.5: **Experimental Results:** Line voltage, integral error and transfer flag waveforms in the case of 10% overvoltage occurring on the line.
In the second case, an outage has been detected on the line (at $t=0.038s$) and simulation/experimental results showing the characteristic waveforms of the algorithm are shown in Figure C.6(simulation results)/Figure C.7(experimental results). As can be seen, half a cycle after the outage occurs (at $t=0.045s$), the integral error reaches the threshold limit 1 and at that instant the transfer flag is set by the algorithm. This detection time is equal to the time which is specified by the CBEMA curve in the case of 100% undervoltage. This can be seen in Figure C.2.

Figure C.6: Simulation Results: Line voltage, integral error and transfer flag waveforms in the case of the line outage.
Figure C.7: Experimental Results: Line voltage, integral error and transfer flag waveforms in the case of the line outage.
In Figure C.8, the line voltage dropped 70\% (at $t=0.02s$) and it recovered after a few periods (at $t=0.06s$). The disturbance threshold limit is reached at $t=0.036s$ and at that instant the transfer flag is set. This is exactly 16ms after the disturbance occurs on the line as specified by the CBEMA curve. After line voltage recovery (at $t=0.06s$), the integral error starts decreasing and at $t=0.11s$ it reaches the lower threshold limit. In this case the magnitude of the lower threshold limit has been set to 0.4. At that instant, the transfer flag is reset, indicating that the line is again within acceptable amplitude limits.

Figure C.8: Simulation Results: Line voltage, integral error and transfer flag waveforms in the case of 70\% undervoltage disturbance on the line occurring at $t = 0.2s$ and disappearing at $t = 0.6s$. 

173
The third case deals with the capacitive switching often present on the distribution line shown in Figure C.9. In this case we can see that the negative and positive weighted errors (due to the oscillations) are canceling each other giving the net value of the integral error which is not setting the transfer flag. This means that although the disturbance is present on the line the disturbance detection algorithm is not detecting it. This can be interpreted as the constant energy demand by the electronic equipment. In favor to this reasoning is the fact that the susceptibility curve is not represented as an absolute voltage amplitude tolerance specification, but the exponential amplitude versus time curve. Taking into account that the product of voltage and time is given in units of energy, the exponential dependence of the voltage versus time brings to ones mind the constant energy demand.

![Figure C.9: Line voltage and integral error waveforms in the case of the simulated capacitor switching on the distribution line occurring at $t = 0.2s$.](image-url)
The advantages of using the proposed line disturbance detection method are briefly discussed in the following paragraphs.

The first advantage of the proposed method is the possibility of independent setting of positive and negative weights. This is important since the susceptibility curves of the electronic equipment usually have distinct positive and negative tolerance bounds. In such a way the proposed algorithm can account for different reaction times for unipolar disturbances. Furthermore, by integrating the errors with positive and negative signs, the accumulated total error accounts only for the net disturbance.

The second advantage is the use of a simple integration method in the detection algorithm. The self-resetting feature of the integration method allows for continuous updating of the line voltage disturbance levels.

Finally, the last advantage of the proposed method is the possibility of setting the level of lower threshold limit in the case of the line voltage recovery independently of the other parameters in the algorithm. This brings another degree of flexibility to the proposed method.

The algorithm for line voltage disturbance detection proposed in this thesis is intended to be used by any power conditioning equipment used to backup sensitive electronic equipment. Based on this algorithm the transfer instant between line and power conditioner can be detected reliably.
Appendix D

Digital Implementation of PWM for DC-chopper and CSI

In this appendix, the implementation of the PWM modulators for the DC-chopper and CSI (described in Chapter 2) is presented. Both PWM modulators are implemented digitally in a programmable chip FLEX8000 from ALTERA. The design has been carried out using the MAX-PLUSII graphic design tool and is based on the design of 3-phase PWM modulator for VSI presented in the U of T/Power Group local documentation. The list of graphic design files and brief description of the files used in the design are given in the following paragraph and more details can be found in the U of T/Power Group local documentation. Also in this section the schematics of the graphic design files are presented.

The list of graphic design files (.gdf) used in the design of the PWM modulator for a DC-chopper and CSI and a brief description follow:

- system.gdf: Top design file.
- idcsipwm.gdf: Ideal PWM modulator for single-phase CSI without overlap-
time included.

- **id1qchop.gdf**: Ideal PWM modulator for one-quadrant DC-chopper.
- **sysbus16.gdf**: Data bus interface to the DSPC40.
- **overlap.gdf**: Block which provides overlap-time for the IGBT's in the same leg of the CSI.
- **pomoc.gdf**: Spurious block to enable the data bus to be bidirectional.
- **dummy.gdf**: Dummy processing of unused input FLEX pins in order to protect the device.
- **reg16.gdf**: 16-bit register.
- **count16.gdf**: 16-bit counter.
- **compar16.gdf**: 16-bit digital comparator.
- **switch16.gdf**: Multiplexer.
- **switch8.gdf**: Multiplexer.
- **io16.gdf**: 16-bit bidirectional input/output port.
- **biport.gdf**: 1-bit bidirectional input/output port.
- **fall-del.gdf**: Falling edge delay.
- **platform.gdf**: Block which limits the duration of gating signal to some minimum predetermined time.
- **watchdog.gdf**: C40 watchdog.
- **8count.gdf**: 8-bit counter.

The schematic diagrams of these graphic design files follow.
Figure D.1: The schematic diagram of the file system.gdf.
Figure D.3: The schematic diagram of the file id1qchop.gdf.
Figure D.4: The schematic diagram of the file sysbus16.gdf.
Figure D.5: The schematic diagram of the file overlap.gdf.

Figure D.6: The schematic diagram of the file pomoc.gdf.
Figure D.7: The schematic diagram of the file dummy.gdf.

Figure D.8: The schematic diagram of the file reg16.gdf.
Figure D.9: The schematic diagram of the file compar16.gdf.
Figure D.10: The schematic diagram of the file switch16.gdf.

Figure D.11: The schematic diagram of the file switch8.gdf.
Figure D.12: The schematic diagram of the file io16.gdf.
Figure D.13: The schematic diagram of the file biport.gdf.

Figure D.14: The schematic diagram of the file fall-del.gdf.
Figure D.15: The schematic diagram of the file platform.gdf.

Figure D.16: The schematic diagram of the file watchdog.gdf.
Bibliography


