CHARACTERIZATION
OF Gd$_2$O$_3$ HIGH-$K$
DIELECTRIC FILMS
ON Si(001)

by

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A Thesis
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TITLE: Characterization of Gd$_2$O$_3$ High-$K$ Dielectric Films on Si(001)

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For silicon MOSFETs (metal-oxide-semiconductor field effect transistors), silicon dioxide (SiO₂) films have served as the gate dielectric since the birth of integrated circuits. The traditional SiO₂ dielectric faces a number of problems and challenges as the feature size of the device is scaling down. A lot of research is now being focused on high-K dielectric materials to be replaced as the future gate dielectrics. Gadolinium oxide (Gd₂O₃), with a dielectric constant around 16, has been successfully passivated on GaAs surface with low interface state density, which has the potential use for optical communication applications.

Gd₂O₃ dielectric films have been deposited on Si(001) surface with electron-beam evaporation from a compressed powder Gd₂O₃ target. For material analysis, the stoichiometry of the Gd₂O₃ films was measured by X-ray photoelectron spectroscopy, whereas the depth profiling of the films was examined by Auger electron spectroscopy. The thickness of the film and structure were determined by conducting X-ray reflectivity measurement together with the aid of TEM micrographs. The electrical properties of the films were measured by forming Al gate capacitors. From the capacitance-voltage (CV) measurement, the dielectric constant of the films was calculated under strong accumulation at 100kHz, whereas the interface properties and the integrity of the dielectric films were investigated by the lateral shift in capacitance as a function of frequency and hysteresis, respectively. The leakage currents and their mechanisms were studied by current-voltage (IV) measurement.

The dielectric constant of the Gd₂O₃ films was determined to be 16.0, high enough to be considered as an alternate gate dielectric on Si(001). Nonetheless, annealing the films in oxygen with film thickness ≤ 10nm results in complicated 3-layer film structure. With the formation of parasitic SiO₂ layer next to the silicon substrate, the dielectric constant of the films decreases since SiO₂ has a lower dielectric constant of 3.9. However, post oxidation annealing of the Gd₂O₃ films is necessary to improve the leakage current.
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# TABLE OF CONTENTS

Abstract ........................................................................................................ ii
Acknowledgements ................................................................................ iv
Table of Contents ...................................................................................... v
List of Figures .......................................................................................... viii
List of Tables .............................................................................................. xvi

1 Introduction 1

1.1 Dielectric Constant and Capacitance ...................................................... 2
1.2 Basic Concept of Metal-Oxide-Semiconductor Field Effect
   Transistors (MOSFETs) ............................................................................. 3
1.3 Oxidation of Silicon ............................................................................... 5
1.4 Limitations of SiO₂ Gate Dielectrics ..................................................... 6
   1.4.1 Hot Carrier Degradation ................................................................. 6
   1.4.2 Impurity (Boron) Penetration ......................................................... 8
1.5 Oxynitrides as Gate Dielectrics ............................................................ 9
   1.5.1 Impurity Barrier Properties of Oxynitrides ..................................... 9
   1.5.2 Thermal Growth of Oxynitrides in Conventional
       Furnaces vs. Rapid-Thermal-Processing (RTP) ............................... 10
1.5.3 Growth of Oxynitride Dielectrics in N₂O ........................................ 11
   1.5.4 Electrical and Device Properties of Oxynitrides
       Grown in NO .................................................................................. 13
1.6 Direct Tunneling of Ultrathin Oxide/Oxynitride Films ......................... 17
1.7 High-K Dielectric Films ...................................................................... 18
   1.7.1 Concerns of High-K Materials ....................................................... 18
1.8 Gd₂O₃ as Future Gate Dielectrics ......................................................... 19
References .................................................................................................. 21
## LIST OF FIGURES

<table>
<thead>
<tr>
<th>Figure (1.1)</th>
<th>Schematic of a simple n-channel MOSFET.</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Figure (1.2)</td>
<td>Structure of a simple capacitor.</td>
<td>2</td>
</tr>
</tbody>
</table>
| Figure (1.3) | (a) Schematic illustration of the induced n-channel and the depletion region.  
(b) Drain current-voltage characteristics as a function of gate voltage. | 4    |
| Figure (1.4) | Mechanism of hot-carrier generation.   | 6    |
| Figure (1.5) | Characteristics of device degradation after substrate hot-carrier injection. | 7    |
| Figure (1.6) | Characteristics of device degradation after channel hot-electron injection. | 7    |
| Figure (1.7) | (a) CV characteristics for SiO₂ gate and BF₂-implanted polysilicon.  
(b) CV characteristics for 1050°C oxynitride gate and BF₂-implanted polysilicon. | 9    |
| Figure (1.8) | N depth profiles for three 1000°C oxides, all grown in N₂O. | 12   |
Figure (1.9) N depth profiles for a 54 Å RTP oxide grown in N₂O at 1000°C, and for a similar oxide which is subsequently reoxidized in O₂ by RTP to final thickness of 74 Å.

Figure (1.10) (a) Oxynitride film thickness as a function of anneal time. (b) Peak atomic concentration of nitrogen at the interface as a function of anneal time.

Figure (1.11) A comparison of annealed to as grown oxide layers. NO1 and ON2 annealing in NO for same temperature at 1150°C for different times of 1 and 5 minutes. (a) High frequency CV and (b) current voltage.

Figure (1.12) High frequency CV characteristics of annealed oxide layers. Annealing is with different ratios of NO to nitrogen as per the insert in the figure.

Figure (1.13) I_d vs. V_d characteristics (insert) and CV characteristics of MOS structures (a) NO-annealed, and (b) non-annealed.

Figure (1.14) (a) G_m vs. V_g for a 10nm thermal oxide nMOSFET. (b) G_m vs. V_g for a NO-annealed 10nm thermal oxide nMOSFET.

Figure (1.15) Lattice spacing and dielectric constant of rare-earth (L) oxides with the cubic bixbyite phase with composition L₂O₃.

Figure (2.1) Exploded view of an electron emitter assembly.
| Figure (2.2) | Exploded view of an electron beam source. | Page 24 |
| Figure (2.3) | Force experienced by electrons in a contained magnetic and electrostatic field. | Page 25 |
| Figure (2.4) | Self-accelerated gun with elongated cathodes and electromagnetic field deflection through 270°. | Page 25 |
| Figure (2.5) | Schematic representation of a typical electron beam evaporation source. | Page 27 |
| Figure (2.6) | Energy-level diagrams showing the electron transitions in XPS. | Page 28 |
| Figure (2.7) | Energy-level diagrams of Auger electron excitation. | Page 30 |
| Figure (2.8) | (a) Energy spectrum of electrons emitted from a surface bombarded by an electron beam.  
(b) The derivative of number of emitted electrons with respect to the energy. | Page 32 |
| Figure (2.9) | Experimental measurements of electron escape depths in various elements. | Page 33 |
| Figure (2.10) | Comparison of Auger electron escape depths with emission depths of backscattered electrons and X-rays. | Page 34 |
| Figure (2.11) | Ion milling a crater and performing AES on the exposed surface, thus allowing depth profiling with AES. | Page 34 |
Figure (2.12) The propagation of a plane wave in a layered structure.

Figure (3.1) A schematic diagram of the In-situ Processing (ISP) system used to deposited Gd$_2$O$_3$ films.

Figure (3.2) A blow view of electron-beam used to deposited Gd$_2$O$_3$ films. The beam features a standard 270° beam deflection geometry with the rod passing through a water-cooled block.

Figure (3.3) Plot of background pressure vs. deposition rate during the deposition of ISP962 deposited at room temperature without degassing the Gd$_2$O$_3$ rod source.

Figure (3.4) Plot of background pressure vs. deposition rate during the deposition of ISP1003 deposited at room temperature. The rod source was degassed for 1 hour prior to deposition.

Figure (4.1) XPS spectrum for Gd 4d peak excited by Mg Kα radiation. The Si 2s peak is also shown in the spectrum.

Figure (4.2) XPS spectra of Gd 4d and O 1s peaks for gadolinium oxide. The spectra were referred to the C 1s core level binding energy at 284.8eV.

Figure (4.3) XPS spectrum of O 1s peaks for Gd$_2$O$_3$ films under different conditions.

Figure (4.4) XPS spectrum of Si 2p peak for a thin film annealed in-situ at different temperatures.
Figure (4.5) XPS spectrum of Gd 3d peak as a reference to align all spectra for a thick and a thin films for the as-deposited condition.

Figure (4.6) XPS O 1s spectrum for both a thick and a thin films for the as-deposited condition. Note, 1eV shift in binding energy between thick and thin films was observed.

Figure (4.7) Auger depth profiles for Gd, O, and Si for Gd$_2$O$_3$ films deposited at room temperature and at a substrate temperature of 500°C both with no oxygen flowing during the deposition.

Figure (4.8) Auger depth profiles for the thick Gd$_2$O$_3$ film, ISP960 with nominal thickness of 230 Å, for pieces of as-deposited and 500, 700, and 780°C annealed samples.

Figure (4.9) Auger depth profiles for another thick Gd$_2$O$_3$ film, ISP906 with nominal thickness of 500 Å, for pieces of as-deposited and 500, 700, and 780°C annealed samples.

Figure (4.10) Auger depth profiles for a thin Gd$_2$O$_3$ film, ISP972 with nominal thickness of 80 Å. Strong intermixing of the film composition was observed for the annealed samples.

Figure (4.11) Schematic of the X-ray reflectivity instrument with Cu anode (\(\lambda=1.54\) Å) and a double-crystal channel-cut monochromator.
**Figure (4.12)** Schematic model of the postulated 3-layer structure in Gd$_2$O$_3$ films after annealing.

**Figure (4.13)** TEM micrographs for sample ISP972 under different conditions with nominal thickness of 80 Å deposited substrate temperature at 500°C.

**Figure (4.14)** X-ray reflectivity data (symbols) for the Gd$_2$O$_3$ film of ISP972 with different conditions as indicated. Solid lines denote the results of fitting. The datasets were offset by two decades for clarity.

**Figure (4.15)** Resultant film structure of Gd$_2$O$_3$ films after annealing at temperature ≥ 500°C in oxygen with RTP system.

**Figure (4.16)** Basic model for thermal oxidation of silicon.

**Figure (4.17)** AFM image of Gd$_2$O$_3$ film (ISP962) deposited at ambient temperature.

**Figure (4.18)** Cross section of a MOS capacitor.

**Figure (4.19)** Small ac voltage of amplitude $a$ superposed on the gate bias applied to the terminals of the MOS capacitor to measure its capacitance or admittance as a function of gate bias.

**Figure (4.20)** Dielectric constant of a 23nm thick (ISP960) Gd$_2$O$_3$ film as-deposited and annealed in oxygen for 10 min at 500, 700, and 780°C.
Figure (4.21) Dielectric constant of a 10nm thick (ISP974) Gd$_2$O$_3$ film as-deposited and annealed in oxygen for 10 min at 500, 700, and 780°C.

Figure (4.22) CV characteristics for sample ISP971 (8nm) deposited at 500°C with oxygen pressure of $2 \times 10^{-5}$ Torr during the deposition. The films were annealed in oxygen for 10 min. The as-deposited film was too leaky to obtain good CV characteristic and is not shown here.

Figure (4.23) CV characteristics of films deposited at ambient temperature (ISP962~10nm) and at 500°C (ISP972 ~80nm) both without oxygen flow during the deposition and given a POA at 700°C.

Figure (4.24) CV characteristics of ISP1003 (~8nm) annealed for 10 min in oxygen at 700°C.

Figure (4.25) Series capacitance model of a stack dielectrics consisting of SiO$_2$ and Gd$_2$O$_3$.

Figure (4.26) Estimate of the thickness of the SiO$_2$ interface layer from CV analysis for ISP971 (12.5nm) and ISP972 (8nm) films annealed in O$_2$. The anneals at 500 and 700°C were for 10 min and the anneal at 780°C was for 2 min.

Figure (4.27) J-V characteristic for a 12.5nm thick film (ISP971) annealed in O$_2$ for 10 min.
Figure (4.28) Energy-band diagram for the Frenkel-Pool (FP) emission.

Figure (4.29) Energy-band diagram for the Fowler-Nordheim (FN) tunneling.
# LIST OF TABLES

<table>
<thead>
<tr>
<th>Table (1.1)</th>
<th>Technology roadmap characteristics in the area of thermal/thin films.</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Table (3.1)</td>
<td>Sample summary for all the wafers deposited Gd$_2$O$_3$ films under different conditions.</td>
<td>43</td>
</tr>
<tr>
<td>Table (4.1)</td>
<td>The [Gd]/[O] ratio for the 16 wafers measured by In-situ XPS. The X-ray source is at 54.7° relative to the analyzer axis.</td>
<td>47</td>
</tr>
<tr>
<td>Table (4.2)</td>
<td>Summary of [Gd]/[O] ratio for Gd$_2$O$_3$ films under different conditions.</td>
<td>51</td>
</tr>
<tr>
<td>Table (4.3)</td>
<td>Optical constants and densities of several materials used for X-ray reflectivity measurements. The values for the silicate, Gd$_2$SiO$_5$ and Gd$_2$Si$_2$O$_7$, were calculated using linear combinations of the constants of Gd$_2$O$_3$ and SiO$_2$ in the ratios 1:1 and 1:2, respectively.</td>
<td>62</td>
</tr>
<tr>
<td>Table (4.4)</td>
<td>Results of the X-ray reflectivity analysis for ISP972. Thickness of each layer is denoted as $t_m$.</td>
<td>65</td>
</tr>
<tr>
<td>Table (4.5)</td>
<td>Comparison of interfacial SiO2 layer thickness obtained from CV analysis and TEM micrographs for sample ISP972 (8nm thick).</td>
<td>78</td>
</tr>
</tbody>
</table>
CHAPTER 1. INTRODUCTION

Since the ages of civilization are denoted by the dominant material of the time, we are now in the silicon age. The invention of silicon transistors and development of the integrated circuit have led to revolutions not only in technology but also in the economy. The key component of most VLSI devices nowadays involves the silicon MOSFET, metal-oxide semiconductor field effect transistor (Figure 1.1), which had its first demonstration marked forty years ago. As the 21st century approaches, the current trends in semiconductor manufacturing reveal the most interesting, exciting, profitable, and potentially risky period in the history of civilization. The phenomenal growth of the electronics industry has been largely due to the smaller, lighter, faster, and cheaper semiconductor products. In order to achieve the characteristics of higher speed, greater density (more devices/area), and lower power, each individual device (MOSFET) has to be reduced in size. The minimum feature size has dropped from tens of microns in the early 60s to the current value of 0.25μm and is projected to be below 0.05μm in about 15 years. For the gate dielectric, these numbers translate into a gate dielectric thickness of ~1-2μm in the early 60s, ~4-5nm in 1997, and an equivalent thickness of <1nm in 2012 as indicated in Table 1.1.

![Figure 1.1. Schematic of a simple n-channel MOSFET [1].](image_url)

<table>
<thead>
<tr>
<th>First Year of IC Production</th>
<th>1997</th>
<th>1999</th>
<th>2001</th>
<th>2003</th>
<th>2006</th>
<th>2009</th>
<th>2012</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRAM generation</td>
<td>256M</td>
<td>1G</td>
<td>1.7G</td>
<td>4G</td>
<td>16G</td>
<td>64G</td>
<td>256G</td>
</tr>
<tr>
<td>Minimum Feature Size, μm</td>
<td>0.25</td>
<td>0.18</td>
<td>0.15</td>
<td>0.13</td>
<td>0.10</td>
<td>0.07</td>
<td>0.05</td>
</tr>
<tr>
<td>Equivalent Oxide Thickness, nm</td>
<td>4 - 5</td>
<td>3 - 4</td>
<td>2 - 3</td>
<td>2 - 3</td>
<td>1.5 - 2</td>
<td>&lt; 1.5</td>
<td>&lt; 1.0</td>
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</tbody>
</table>
Silicon dioxide films have served as the gate dielectric since the birth of integrated circuits. The traditional SiO$_2$ dielectric faces a number of problems and challenges as the feature size of the device is scaling down. Dopant (boron) diffusion into and through the ultrathin oxide from the poly-Si gate becomes a critical issue. Oxynitride (SiO$_x$N$_y$) shows its strong potential to replace conventional “pure” silicon gate oxides for sub-0.25μm devices. Nitrogen incorporated into the oxide has been shown to form a barrier against boron diffusion in p+ gate MOSFETs. In addition, a small concentration of nitrogen near the interface appears to reduce hot-electron degradation and improve breakdown properties. However, the fundamental limit of ultrathin oxide/oxynitride films is direct tunneling (current) which grows exponentially with decreasing film thickness. To overcome the direct tunneling problem, the physical thickness of the dielectric should be kept large, much thicker than the direct tunneling limit. On the other hand, ULSI scaling is driving a reduction in thickness for next generation of fast switching devices. To ameliorate these conflicting needs, one can replace conventional SiO$_2$ by a material with a higher dielectric constant in order to increase the physical thickness of the film, while the “equivalent” electrical thickness with respect to pure SiO$_2$ and the direct tunneling current would be much reduced [1].

1.1. Dielectric Constant and Capacitance

The dielectric constant of a material is defined as the ability of a material to store charge when subject to an electric field that can be best illustrated by a parallel-plate capacitor which is shown in Figure 1.2. When voltage is applied to the both ends of

![Figure 1.2. Structure of simple capacitor [2].](image)
conducting plates, the dielectric material in between the parallel plates is polarized. The electrical charge $Q$ (in coulombs) stored on either plate is directly proportional to the applied voltage $V$ (in volts):

$$Q = C \times V$$

(1.1)

where the proportionality constant, $C$, is defined as the capacitance, with units of farads, $F$ (1 farad = 1 coulomb per volt). The capacitance contains both a geometrical and a material factor. The permittivity ($\varepsilon$) is the material factor that reflects the ability of the material to be polarized by the electrical field, whereas the geometric factor is the ratio of the capacitor area, $A$, to the separation distance, $d$, of the conducting plates. As a consequence, the capacitance is defined as,

$$C = \varepsilon \left(\frac{A}{d}\right)$$

(1.2)

Since the permittivity of a material is customarily described as its permittivity normalized to that of vacuum, the relative permittivity, or dielectric constant, $K$ is defined as,

$$K = \frac{\varepsilon}{\varepsilon_o} = \left(\frac{d}{A}\right)\left(\frac{C}{\varepsilon_o}\right)$$

(1.3)

where $\varepsilon_o$ is the permittivity of a vacuum and is equal to $8.85 \times 10^{-12}$ F/m. For gate dielectric materials used in sub-0.25$\mu$m devices, the dielectric constant for SiO$_2$ is around 3.9, whereas that for oxynitride is around 7.8. The material for sub-0.1$\mu$m devices requires the dielectric constant to be greater than 10 in most cases.

1.2. Basic Concept of Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs)

The basic MOS transistor is illustrated in Figure 1.1 for the case of an n-type channel formed on a p-type Si substrate. The $n^+$ source and drain regions are diffused or implanted into a relatively lightly doped p-type substrate, and a thin oxide layer separates the metal/poly-Si gate from the Si surface. In this device, the drain current is controlled by a voltage applied at the gate electrode that is isolated from the conducting channel by an oxide. No current flows from drain to source without a conducting n channel between them. However, when a positive voltage is applied to the gate relatively to the substrate, positive charges are in effect situated on the gate metal. In response, negative charges are
induced in the underlying Si by the formation of a depletion region and a thin surface region containing mobile electrons termed the inversion layer as shown in Figure 1.3a. These induced electrons form a conducting channel in the field-effect-transistor allowing current to flow from drain to source (electrons from source to drain) when a positive drain-source voltage is applied. The ohmic voltage drop in the channel results in the drain end of the channel having a smaller field normal to the surface than at the source end, hence the density of electrons decreases going from source to drain in the manner shown in Figure 1.3a. Since the potential difference between the channel and the substrate contact is greater at the drain end, the depletion width at the drain end will also be greater [3]. The drain current-voltage characteristics as a function of gate voltage is shown in Figure 1.3b. When the drain voltage is increased beyond a certain point, channel "pinchoff" occurs and the drain current saturates.

Figure 1.3 (a). Schematic illustration of the induced n-channel and the depletion region [4].

Figure 1.3 (b). Drain current-voltage characteristics as a function of gate voltage [4].

The minimum gate voltage required to induce the channel is called the threshold voltage $V_T$, and is an important parameter in MOS transistors. The positive gate voltage of an n-channel device must be larger than some value $V_T$ before a conducting channel is
induced. The transistor of this type that requires the applied gate voltage to be larger than $V_T$ to induce a conducting channel is called the enhancement-mode transistor. The MOS transistor is "normally off" with zero gate voltage. In contrast, a "normally on" device is called a depletion-mode transistor, since gate voltage is used to deplete a channel which exists at equilibrium. In other words, for the depletion-mode transistor the conducting channel already exists with zero gate voltage, and a negative gate voltage is required to turn the device off. Despite the fact that both n-channel and p-channel MOS transistors are in common usage, the n-channel type is generally preferred because it takes advantage of the fact that the electron mobility in Si is larger than the mobility of holes. The ability of the MOS transistor to switch from the "off" state to the "on" state is particularly useful in digital circuits [4].

1.3. Oxidation of Silicon

In industrial practice, gate silicon dioxide (SiO$_2$) layers are formed by thermal oxidation of the silicon surface within a resistance-heated furnace with a tubular quartz reactor at atmospheric pressures and elevated temperatures of typically 850 – 1100°C [5]. Before the wafer is placed in the furnace, it must be cleaned with an RCA cleaning method (most commonly employed) to remove any organic and inorganic contaminants that can degrade performance and reliability of the MOS devices made. Pure oxygen and water vapor are two types of oxidizing gases utilized to cause thermal oxidation of silicon. "Dry" and "wet" oxides are produced base on the following two equations:

$$\text{Si (solid)} + \text{O}_2 \rightarrow \text{SiO}_2 \text{ (solid)} \quad \text{"dry"} \quad (1.4)$$

$$\text{Si (solid)} + 2\text{H}_2\text{O} \rightarrow \text{SiO}_2 \text{ (solid)} + 2\text{H}_2 \quad \text{"wet"} \quad (1.5)$$

There is an initial phase for growth in dry oxygen, which is not fully understood, but applies over a range of thickness which may well overlap the range of thicknesses of the most advanced gates in CMOS and DRAM devices. The second region is associated with a constant growth rate that depends on the crystal orientation of the silicon surface. The growth rate and incidentally the density of interface traps depend on the rate of reaction of the oxidizing species at the silicon surface. The parabolic region is the region for thick oxide where the thickness is proportional to $x_r^{1/2}$ ($x_r$ is the thickness). When thin oxides are required as for faster devices, Rapid-Thermal-Processing (RTP) can be
employed to grow the SiO2 layers. However, the major feature of conventional furnace oxidation is ease with which batch processing is attainable.

1.4. Limitations of SiO2 Gate Dielectrics

1.4.1. Hot Carrier Degradation

The shrinkage of device dimension without corresponding reductions in supply voltages leads to very high electric fields near the drain of the device [6]. Such intensified electric fields cause some physical phenomena which impose fundamental design constraints on VLSI devices, resulting in deterioration of device reliability. Among these phenomena, hot-carrier injection into gate oxide is known for imposing one of the severest limitations on the miniaturization of MOSFET’s in VLSI’s. As a result of the high electric field, channel electrons are accelerated and produce impact ionization. The generated electrons and holes can be injected into the gate oxide, resulting in charge trapping and interface trap generation. For n-channel MOSFETs, usually found in VLSI circuits, hot electrons are emitted from the silicon into the gate oxide when applied voltages are sufficiently large. Hot electrons can originate from either the surface (conducting) channel or the silicon substrate. Some of the electrons, those which gain sufficient energy to surmount the Si-SiO2 interfacial energy barrier without suffering an energy-losing collision in the channel, are injected into the oxide, as shown in Figure 1.4.

Figure 1.4. Mechanism of hot-carrier generation [7].

Subsequent trapping of the injected electrons causes device instability, such as threshold-voltage shift and transconductance \( G_m = dI_d/dV_g \) degradation. Transconductance is defined as change in source-to-drain current \( I_{ds} \) with respect to change in applied gate voltage \( V_g \). Hot holes are generated as a result of impact ionization and can be injected into the oxide under the biasing conditions \( V_D > V_G > V_T \) as shown in Figure 1.4 [7].
Two kinds of damages that are likely induced by the injection of hot electrons for the n-channel MOSFETs are the local trapped charge and interface state. As mentioned, hot electrons can originate from either the surface channel or the silicon substrate. In the case of channel hot-electron injection, the average momentum of the high-energy electrons is largely parallel to the silicon/silicon oxide interface, and therefore the electrons are likely to be trapped at the interface resulting in higher interface state densities and this degrades transconductance. While in the substrate hot-electron injection case, the average momentum of the high-energy electrons is perpendicular to the interface so that the electron can penetrate deeper into the oxide and get trapped along the path. These locally trapped electrons result in a shift in threshold voltage. 

Figure 1.5

![Figure 1.5](image)

Figure 1.5. Characteristics of device degradation after substrate hot-electron injection: $V_b = -10V$, $V_g = 3V$ during stressing ($T_{ox} = 20\text{nm}$, $W = L = 100\mu\text{m}$) [8].

Figure 1.6

![Figure 1.6](image)

Figure 1.6. Characteristics of device degradation after channel hot-electron injection: $V_g = 3V$, $V_d = 6.5V$ during stressing ($T_{ox} = 15.5\text{nm}$, $W = 100\mu\text{m}$, $L = 2\mu\text{m}$) [8].
shows typical device degradation after substrate hot-electron injection. A parallel shift in threshold voltage after stressing is evidence that indicates that the local trapped charges are the major physical damage. However, some interface-state generation are generated as revealed in the slightly reduced transconductance ($G_m$) after stressing. In Figure 1.6, the channel hot-electron injection-induced degradation, however, shows very little parallel shift in threshold voltage and is mainly due to reduced channel mobility caused by interface-state generation that can be seen from the great reduction in transconductance after stressing [8].

1.4.2. Impurity (Boron) Penetration

Scaling of CMOS progresses down to submicron channel lengths greatly improves device density and circuit speed, but introduces many challenges in process technology. One difficulty is the scaling of the gate dielectric, particularly for the fabrication of $p^+$ polysilicon gate of p-channel MOS region for CMOS [9]. The use of boron doped $p^+$ polysilicon gate electrodes for deep submicrometer CMOS is of great interest due to the improvements as compared to conventional buried-channel PMOS FET’s with $n^+$ polysilicon gate electrodes. The improvements include reduced short-channel effects, better turn-off behavior, and improved hot-carrier reliability [10]. However, the major concern with the doped $p^+$ polysilicon gate electrodes is the penetration of boron impurity through the thin gate oxide into the channel region. Penetration of boron atoms into an SiO$_2$ film is further enhanced by high-temperature forming-gas annealing. Poor threshold voltage control, fluctuations in flat band voltage ($V_{FB}$) accompanied by increased PMOS subthreshold slope and electron trapping rate, and decreased low field mobility are the deleterious effects as a result of this impurity penetration [11]. Figure 1.7a shows the C-V characteristics for a PMOSFET’s with 125Å SiO$_2$ gate dielectric and BF$_2$ doped $p^+$ polysilicon gate electrode. The three curves plotted correspond to total annealing time in forming gas at 900°C of 10, 20, and 30 minutes. Note that the curves shift dramatically to the right and $C_{\text{min}}$ shows large increases with increasing thermal time. The flat-band voltage is shifted roughly 3V from its initial value as a result of the additional 20-minute time at 900°C, indicating a large amount of boron penetration into the channel.
1.5. Oxynitrides as Gate Dielectrics

1.5.1. Impurity Barrier Properties of Oxynitrides

In order to reduce damage at a drain region caused by channel hot electron injection, graded drain structures such as double-diffusion drain (DDD), and lightly-doped drain (LDD) structures, and other variations have been employed. These structures can reduce the electric field in the drain space region or change the locations of generated hot carriers. Nevertheless, when device dimensions are scaled down further, the damage caused by channel hot electron injection in short channel devices is still substantial in spite of the DDD and LDD structures used in the process. Therefore, a better approach to this damage is to improve the gate oxide and Si/SiO$_2$ interface quality and thus reduce the incidence of trapping during hot carrier injection. Oxynitrides have been shown to improve the MOS characteristics by producing surface protective layers against impurity penetration and by producing good interfacial characteristics. Nitrogen incorporation into the oxide has been shown to form a barrier against boron diffusion in p$^+$ gate MOSFETs. The C-V characteristics of an identical SiO$_2$ gate oxide as shown in Figure 1.7a but annealed in ammonia at 1050°C for 45 seconds to form oxynitride gate dielectric is shown in Figure 1.7b. The shift in flat-band voltage is reasonable small on the order of 250mV, and further the shift does not continue to increase with increasing thermal time, but saturates after the first 10-min cycle. These results indicate that the presence of nitrogen on the surface of pre grown oxide improves the impurity barrier properties to boron diffusion associated with the use of p$^+$ polysilicon gate. Moreover, a
small nitrogen concentration near the interface appears to reduce hot-electron degradation and improve breakdown properties as will be discussed later [1]. Although there are plenty of methods to grow the gate dielectric of ultrathin oxynitrides both thermally and non-thermally, thermal growth of oxynitride film will be discussed here.

![Figure 1.7. (b) CV characteristics for 1050°C oxynitride gate and BF₂-implanted polysilicon [10].](image)

1.5.2. Thermal Growth of Oxynitrides in Conventional Furnaces vs. Rapid-Thermal-Processing (RTP)

Thermal nitridation of SiO₂ is achieved conventionally by heating the pre-grown oxide in furnaces with NH₃ gas. In spite of a significant amount of nitrogen incorporated into the film, the main drawback of processing in ammonia is that too much hydrogen penetrates into the film. The large amount of hydrogen introduced into the dielectric film induces high-density electron traps that degrade the properties of MOSFETs. The laughing gas N₂O has replaced NH₃ since N₂O is considered to contain presumably no hydrogen, thus N₂O-nitrided oxides are expected to exhibit improved reliability and therefore will be discussed here. For VLSI, the annealing process should result in a minimum diffusion of dopants, while the temperature remains sufficiently high to obtain excellent removal of damage due to processing and a high degree of dopant activation. Thus, short-time processing is a possible solution to many VLSI processing steps [5]. Due to the long load/unload and heat-recovery times of wafer holders, conventional furnaces cannot be utilized for short-time processing. Rapid thermal processing (RTP), which utilizes incoherent light of tungsten-halogen lamps to heat the wafer by photoabsorption from above and below, is a promising technique to be utilized in VLSI
technology. RTP has the following advantages as compared with conventional furnaces in the point of view of gate-dielectric fabrication:

(A) An excellent controllability of the thermal process that ensures rapid heating and cooling rates with steady-state temperature ranges of 500°C – 1200°C and time ranges of 3 – 600s.

(B) A controllable process ambient which can be switched and purged in seconds due to very small heating chamber and the use of mass-flow controllers to accommodate advanced multi-gas processes such as oxidation-nitridation-reoxidation.

(C) The ambient is filled with inert gas and the wafer is cold enough during loading and unloading thus minimizing undesirable reactions to take place during RTP [5].

Nitridation of an oxide film, first of all, results in an incorporation of nitrogen atoms into SiO₂ configurations. The amount and location of N incorporated in the oxide by different growth conditions, namely furnace and RTP, in N₂O will be discussed. Following the nitridation of SiO₂, Post-Nitridation-Anneal (PNA) must be performed in order to improve the dielectric properties by reducing the fixed-charge density. PNA is defined as the high-temperature anneal in O₂ (reoxidation) or an inert gas such as N₂ (inert anneal) following nitridation and prior to gate-electrode deposition.

1.5.3. Growth of Oxynitride Dielectrics in N₂O

Since the electrical improvements have been linked to the amount and location of N incorporated in the oxide, it is important to understand the correlation between oxide growth conditions and the N location and concentration. It is reported in Ref. [12] that oxides grown in N₂O by furnace and rapid thermal processing (RTP) have distinctly different N concentration depth profiles. Here, thin SiO₂ film has been primarily grown on the (100) n-type silicon wafers prior to nitridation in N₂O. The nitridation temperature for these oxides is 1000°C, with final film thickness of 50-150 Å. It is shown in general furnace oxides have a more or less uniform distribution of N throughout the oxide, while the RTP oxides have a peak of N at the Si-SiO₂ interface as indicated in Figure 1.8. To determine whether the fast temperature cycle during RTP is affecting the N distribution, a furnace oxide identical to the one profile in Figure 1.8 is given a rapid thermal anneal in N₂O at 1000°C. A complete absence of N in the RTP reoxidized oxide at greater than
Figure 1.8. N depth profiles for three 1000°C oxides, all grown in N_{2}O [12].

35Å from the interface is observed. The nitrogen, which has been present due to the initial furnace N_{2}O oxidation, is removed from the bulk of the oxide by the RTP N_{2}O exposure. While RTP reoxidation in N_{2}O removes N from the bulk of the oxide, RTP reoxidation in O_{2} does not have this effect as shown in Figure 1.9. In Figure 9, the N depth profiles for a 54 Å RTP oxide grown in N_{2}O at 1000°C and the identical grown oxide reoxidized in pure O_{2} are shown. An additional 20 Å of oxide growth at the interface is obtained for the film that is reoxidized in O_{2}, causing the N peak to spread out away from the interface with the amount of N in the film remaining constant. The distance of the nitrogen-rich layer movement is approximately equal to the increase of the film thickness. This fact can be explained by the model that the nitrogen incorporation is enhanced by the interfacial strain, which is due to lattice mismatch between Si and SiO_{2}. Thus if the Si-SiO_{2} interface moves by interfacial oxidation, the peak of the nitrogen concentration follows it [5].

Figure 1.9. N depth profiles for a 54 Å RTP oxide grown in N_{2}O at 1000°C, and for a similar oxide which is subsequently reoxidized in O_{2} by RTP to a final thickness of 74 Å [12].
When elevated to a moderately high temperature, N₂O has been reported to decompose following the three reactions:

\[ \text{N}_2\text{O} \rightarrow \text{N}_2 + \text{O}, \]  \hspace{1cm} (1.6)

\[ \text{N}_2\text{O} + \text{O} \rightarrow 2\text{NO}, \]  \hspace{1cm} (1.7)

\[ \text{O} + \text{O} \rightarrow \text{O}_2. \]  \hspace{1cm} (1.8)

In the rapid thermal processing, the decomposition of the N₂O takes place at or near the surface of the wafer, rather than far away as is the case for a furnace process. This suggests that the O that is present in the intermediate step of N₂O decomposition may reach the wafer in the RTP system, and may be playing a role in the removal of N from the oxide [12]. It is further suggested that the N₂ does not react with the silicon at 1000°C, but instead it is the oxidation of the silicon by NO that is responsible for the incorporation of N in the oxide. As a result, the nitric oxide (NO) is the preferential nitridation gas for ultrathin films since there is no mechanism of nitrogen removal from the film. In addition, the thermal budget for NO processing is less than that for N₂O since it incorporates larger amounts of nitrogen at the interface, provides a hydrogen-free processing ambient, and provides for a more controlled process due to the self-limiting nature of the NO oxidation [13]. *Figure 1.10* further shows the effect of annealing temperature in N₂O with RTP in terms of film thickness and nitrogen concentration as a function of time. Increasing annealing temperature leads to increase in peak concentration of nitrogen. However, there is a saturation of nitrogen at the interface with temperature. It is also observed in the figure that the nitrogen concentration at the interface increases with time, but as the nitrogen accumulates at the interface, the growth of the dielectric layer (oxynitride) thickness has been slowed down. As mentioned, the nitrogen build up is caused by the diffusion of NO species that are decomposed from N₂O through the growing oxide, while the growth of oxide is mainly due to the O₂ in the decomposed gas.

1.5.4. Electrical and Device Properties of Oxynitrides Grown in NO

Experimentally, it has been shown that the growth rate of dielectric layers in an N₂O environment are much slower than that in pure oxygen under similar conditions. Furthermore, the growth rate is even slower in NO and displays distinctly limiting thickness characteristics. The limiting growth thickness of NO grown layers with time
Figure 1.10 (a). Thickness (nm) as a function of time (seconds). (b) Peak atomic percent of nitrogen at the interface [14].

and temperature provides little scope for variable thickness layers particularly when the maximum thickness is only a few nano meters [14]. This property is an excellent one for future generation integration where strict thickness control will be required over, for example, the entire area of a 400 mm diameter wafer. It is also this reason that NO has been more commonly used to anneal pre grown oxide layer. The improved electrical properties of SiO₂ oxide layer annealed in NO as compared to as grown condition are revealed in Figure 1.11. The layers are grown in O₂ at 950°C for 30 seconds in an RTP system and then subjected to an NO anneal for 1 and 5 minutes at 1150°C. The leakage current is considerably improved for both annealing conditions as compared to the as grown SiO₂ oxide, with a higher breakdown voltage for the longer annealed sample that represents higher nitrogen concentrations at the interface. Interesting results have been obtained in the C-V curves showing that the longer annealed sample has a larger flat band shift in spite of the fact that the surface state density for both annealing conditions remain the same. Nonetheless, neither of the annealed C-V curves show evidence of traps as is the case for the as grown oxide. Furthermore, Figure 1.12 indicates that increase the annealing NO concentration results in larger flat band shift. This suggests that the more nitrogen incorporated in the oxide layer the larger the flat band shift. As far as electrical characteristics are concerned, there is an optimum amount of nitrogen for surface state effects above which an increase in fixed charge density will result.

In order to examine the effects of annealing pre grown oxides in NO for device performance, 12nm thick conventional gate oxide without nitridation and 12.9nm thick oxynitride layer have been grown on p-type substrates for n-channel MOSFETs. Initial oxides are grown in dry oxygen at 800°C followed by annealing in N₂ for 30 minutes at
Figure 1.11. A comparison of annealed to as grown oxide layers. ON1 and ON2 annealing in NO for same temperature at 1150°C for different times of 1 and 5 min. (a) High frequency CV and (b) current voltage [14].

Figure 1.12. High frequency CV characteristics of annealed oxide layers. Annealing is with different ratios of NO to nitrogen as per the insert in the figure [14].

900°C. A thin oxynitride layer is then formed by annealing the pre grown oxide in pure NO ambient at 1150°C for 5 minutes with RTP. Electrical properties of devices before and after hot-carrier stress are measured with an HP 4145B semiconductor parametric analyzer. Stressing is performed with $V_g = 1.5$ volts and $V_d = 9.5$ Volts for nominally 2000 seconds. Figure 1.13 shows the $I_d$ versus $V_d$ (as inserted in figure) and the gate to drain capacitance, $C_{gd}$, versus gate voltage ($V_g$) curves for the n-channel MOSFETs ($W/L_{eff} = 25\mu m/0.85\mu m$). Gate-to-drain capacitance measurements can be used to characterize hot carrier degradation of MOSFETs. It is believed that the decrease in $C_{gd}$
in the strong inversion region is due to the generation of acceptor type interface states in the top half of the silicon bandgap, whilst the increase in $C_{gd}$ in the accumulation and depletion regions is due to the trapping of holes during stress [14]. From Figure 1.13,

![Figure 1.13. $I_d$ vs $V_d$ characteristics (insert) and CV characteristics of MOS structures (a) NO-annealed, (b) Non-annealed [14].](image)

the conventional gate oxide device shows considerably greater change in capacitance in both inversion and accumulation, whereas the NO annealed device shows little degradation in accumulation but more evident in the inversion area. Consequently, it is evident that NO annealing of MOSFETs significantly improves the "hot carrier" endurance. Moreover, it can be seen that the NO annealed $I_d$-$V_d$ characteristics do not change noticeably upon stressing while the non-annealed device undergoes significant degradation. This further proves that NO annealing of conventional SiO$_2$ dielectrics
results in better device performance. In addition to capacitance measurement, transconductance ($G_m$) measurement on the 10nm gate thickness devices is shown in

![Figure 1.14](image_url)

Figure 1.14. (a) 10nm thermal oxide nMOSFET W/L=25/1.0, (b) NO-annealed 10nm thermal oxide nMOSFET W/L=25/1.0 (both with stress conditions of $V_g=1.5V$, $V_d=9.5V$) [14].

Figure 1.14. It is observed that the NO annealed device has a lower peak $G_m$ than the conventional oxide device under low normal field, indicating a degradation of peak electron mobility as a result of presence of nitrogen at the interface. This degradation has been proposed as a major obstacle to the use of nitrogen. Too heavy nitridation is unfavorable from the performance point of view. On the other hand, the conventional gate oxide shows a large mobility degradation under high electric field while an improved high field value of $G_m$ is observed for NO annealed device. It is also shown from the curves that stressing has less effect on the NO annealed device than on conventional gate oxide one. Conclusively, in terms of device performances, nitridation achieves outstanding improvement of $G_m$ under high electric field but degrades the peak mobility of channel electron under low normal field. However, since most devices will be working into the high field regime, degradation of peak mobility under low normal field due to nitridation will not be considered to be a problem.

1.6. Direct Tunneling of Ultrathin Oxide/Oxynitride Films

As mentioned in the Introduction section, direct tunneling is one of the fundamental limits for ultrathin oxide/oxynitride films and grows exponentially with
decreasing film thickness. The direct tunneling is defined as tunneling of electrons from the Si substrate to the gate by surmounting the whole tunneling barrier when the Fermi level in the gate is opposite the silicon bandgap [15]. The basic problem is that a large tunnel current flows between the gate and the silicon when gate bias moves the Fermi level in the gate toward a position opposite either the majority or minority carrier band edge [16]. For oxide thickness below 3nm, direct tunneling becomes a limiting leakage mechanism in MOS technology. To overcome this problem, materials with higher dielectric constants can increase the "physical" thickness of the dielectric film thicker than the direct tunneling limit, while the "equivalent" electrical thickness with respect to pure SiO2 would be reduced.

1.7. High-K Dielectric Films

1.7.1. Concerns of High-K Materials

The best high-K materials to be used as a future gate dielectric must posses the following properties: (i) a high dielectric constant, (ii) high thermal stability with respect to Si, (iii) minimal intrinsic defects and traps in the film, (iv) a low interface state density and high stability of the interface during thermal treatments and external radiation, (v) high resistance to dopant diffusion, (vi) low leakage currents, (vii) large bandgap and an appropriate tunneling barrier height, (viii) a low thermal budget and defect free processing, and (ix) manufacturability and integration with silicon technology [1]. Several high-K materials have been extensively studied for DRAM applications due to their high dielectric constants and are looking their potentials to be used as gate dielectrics in MOSFET devices. They include Ta2O5, TiO2, Y2O3, ferroelectrics, CeO2, etc. However, thermodynamic data shows that all these binary oxides are unstable in contact with silicon. Direct growth of these oxides frequently accompanied by extensive interdiffusion or chemical reactions that degrade the properties of the oxide, the underlying silicon, or both [17]. Thus, a silicon-compatible buffer layer should be used for the growth of these oxides on silicon in order to provide a nonreactive diffusion barrier and a stable nucleation template for the subsequent growth of the overlying desired oxide. A very thin buffer layer of silicon oxide, oxynitride, or nitride is usually used to minimize interface states and to be a diffusion barrier between the layers since
they are highly compatible with silicon substrate. If a thin buffer layer is used, the equivalent thickness of the stacked dielectrics will have contributions from both the thickness of the buffer layer and the equivalent thickness of the high-\(K\) layer. In order for the equivalent thickness of the stack dielectric to be thin, the buffer layer should ideally consist of 1-2 atomic layers. Moreover, the interface between the buffer layer and the high-\(K\) material should be as good as the Si/Si\(_2\)O\(_2\) interface. The equivalent thickness of the high-\(K\) material is calculated as:

\[ T_{\text{ox}} = \text{thickness of the high-}K\text{ material} \times \left( \frac{K \text{ of } \text{SiO}_2}{3.83} \right) / K \text{ of high-}K\text{ material} \]

where \(T_{\text{ox}}\) is the equivalent SiO\(_2\) oxide thickness and \(K\) is the dielectric constant of the respective oxide. Since capacitors that contain stacked structures can be simply viewed as several capacitors with different dielectrics connected in series, the “total” equivalent thickness is a linear sum of the equivalent thickness of each individual oxide.

1.8. Gd\(_2\)O\(_3\) as a Future Gate Dielectric

The dielectric constants [18, 19] and lattice spacing [20] for the rare-earth (L) oxides with a cubic bixbyite phase of composition \(\text{L}_2\text{O}_3\) are shown in Figure 1.15. Gd\(_2\)O\(_3\) has a value of dielectric constant high enough to be considered as an alternate gate dielectric on Si(001). Further motivation for the study of the Gd\(_2\)O\(_3\)/Si(001) interface is provided by the fact that, as shown in Figure 1.15, the cubic phase of Gd\(_2\)O\(_3\) has an excellent lattice match at twice the lattice spacing of Si(001). Finally, epitaxial Gd\(_2\)O\(_3\) films have produced the best metal-insulator-semiconductor (MIS) interfaces on GaAs(001) [21].

In this thesis, characterization of gadolinium oxide deposited on Si(001) will be studied by using various analytical techniques, including X-ray photoelectron spectroscopy (XPS), Auger electron spectroscopy (AES), transmitted electron microscopy (TEM), X-ray reflectivity, and atomic force microscopy (AFM) for material analysis, whereas the electrical properties of the Gd\(_2\)O\(_3\) gate dielectrics will be studied with the capacitance-voltage (CV) and current-voltage (IV) measurements.
Figure 1.15. Lattice spacing and dielectric constant of rare-earth (L) oxides with the cubic bixbyite phase with composition $L_2O_3$. 
References


CHAPTER 2. THEORY AND APPARATUS

In this section, theory of some important instruments will be described. Fundamentals of an electron-beam evaporation used to deposit gadolinium oxide films from a compress target will first be discussed. Theoretical background of analytical techniques of X-ray photoelectron spectroscopy (XPS), Auger electron spectroscopy (AES), and X-ray reflectivity will also be described here.

2.1. Electron-Beam Evaporation

The main advantage of using electron-beam to deposit thin films is that it offers high evaporation rate, freedom from contamination, excellent economy, and high thermal efficiency. It has to be operated in a reasonable good vacuum with a pressure less than $10^{-5}$ Torr, known as the region of free molecular flow. This region is characterized by the fact that the residual gas molecules in the system are relatively so few in number, they rarely collide with each other even though they may strike the bounding surfaces of the vacuum chamber. It is also due to the insulating conditions of the free molecular flow region that steep voltage gradients can be maintained in the vicinity of a thermionic emitter. Figure 2.1 is the exploded view of an electron emitter assembly.

![Figure 2.1. Exploded view of an electron emitter assembly [1].](image_url)

A filament is heated by low voltage current to incandescence causing electrons to be emitted in random directions. The filament is located in the groove of a cathode beam former, both of which are connected to the negative terminal of a high voltage power supply. With the beam former negative charged, electrons emitted toward the back and sides of the beam former
are repelled, but those emitted toward the front are accelerated and attracted to the anode, which is at ground potential [1]. An exploded view of the electron beam source is shown in Figure 2.2 with some of the components identified. It can be seen that the permanent magnet located underneath the water-cooled copper crucible has large pole extensions on both sides of the crucible. They provide the magnetic field responsible for bending the electron beam through 270°. Since an electron in motion in a magnet field experiences a force perpendicular to its direction and to the magnetic field, the deflection of electron beam in the transverse beam gun can be understood by the left-hand rule indicated in Figure 2.3. The thumb points in the direction the electrons are initially going; the index points in the direction of the magnetic field north to south; the middle finger indicates the direction of the electrostatic force. The negative charged electrons emitted from the filament are accelerated by the anode at ground potential, and then get deflected and focused by the magnetic fields at 270° impinging on the surface of the evaporant to achieve evaporation. The self-accelerating gun with a 270° beam deflection system

Figure 2.2. Exploded view of an electron beam source [1].
solves the problems of shorting out electrically and coating over with evaporant of the beam emitter since it can be placed completely out of the path of falling debris as shown in Figure 2.4. A permanent magnet is sufficient to provide the main deflection field for a transverse beam gun of low power, but an electromagnet is often used for higher powers.

Figure 2.3. Force experienced by electrons in a contained magnetic and electrostatic field [1].

Figure 2.4. Self-accelerated gun with elongated cathodes and electromagnetic field deflection through 270° [1].

A current (100's of mA) is sent through a tungsten filament and heats it to the point where thermionic emission of electrons takes place. Thermionic emission of electrons is described by the Richardson equation:

\[ J = A T^2 \exp \left(-\frac{e\phi}{kT} \right) \]  

(2.1)
where

\[ J = \text{current density} \]
\[ A = \text{Richardson constant} \]
\[ T = \text{temperature degree K} \]
\[ e = \text{electron charge} \]
\[ \phi = \text{work function} \]
\[ K = \text{Boltzmann constant} \]

According to the above equation, the current density emitted increases as the temperature is increased for a material of a given work function. This range where current density increases with temperature is called the emission limited region. However, as the current increases, it is going to reach a point where the field generated by the cathode-anode spacing and voltage controls how much current can be obtained. The region where current increases with increasing voltage is known as the space charge limited region. Increase in cathode temperature has no effect on the current density. As the electron beam hits the surface of the evaporant, the kinetic energy of its motion is transformed to heat via the impact. The overall energy released is quite high so the hearth that holds the evaporant must be water-cooled to keep from melting. Figure 2.5 depicts a typical electron beam evaporation that utilizes 270° deflection of the beam and a water-cooled copper crucible, and the evaporant is replenished from the rod fed on the bottom. Generally, the evaporation rate for any material obeys the Langmuir-Knudsen relationship:

\[
\frac{\partial m}{\partial t} = kAP \sqrt{\frac{M}{T}}
\]

(2.2)

where

\[
\frac{\partial m}{\partial t} = \text{evaporation rate}
\]

A = area of evaporant surface
P = vapor pressure of evaporant
M = molecular weight
T = absolute temperature
k = constant
Vapor pressure $P$ is also a function of temperature $T$ according to:

$$\ln P = \text{const. } \frac{1}{T}$$

(2.3)

Therefore, a greater evaporation rate is obtained as the temperature is increased. In practice, the evaporation rate is usually kept large compared to the rate of bombardment of the substrate by residual gas molecules to reduce impurities on the surface caused by occluded gases and other contaminants.

Figure 2.5. Schematic representation of a typical electron beam evaporation source [1].

### 2.2. X-ray Photoelectron Spectroscopy (XPS)

XPS involves irradiating a solid in vacuum with monochromatic soft X-rays and analyzing the energy of the emitted electrons. The energy of the photons can be up to 10 keV and interact with the atomic electrons primarily via the photon absorption process [2]. At sufficient high energy, photons can penetrate within the solid and interact with the inner shell electrons, which is useful in identifying elements. In contrast, lower energy photons establish the visible spectra associated with the outmost loosely bound electrons. Since these loosely bound electrons are involved in chemical binding, they are not useful for elemental identification. Since the mean free path of electrons in solids is very small, the detected electrons originate from only the top few atomic layers, making XPS a unique surface-sensitive technique for chemical analysis [3]. Figure 2.6
Figure 2.6. Energy-level diagrams showing the electron transitions in XPS [4].

illustrates the electronic transition involved in XPS. First, an electron is ejected from one of the core electronic levels by an incident X-ray photon (Fig. 2.6a). The kinetic energy \( KE \) of the emitted core electron is:

\[
KE = h\nu - BE + \phi
\]  

(2.4)

where \( h\nu \) is the energy of the incident photons, \( BE \) is the binding energy of the atomic orbital from which the emitted electron originates, and \( \phi \) is spectrometer work function. After a core hole is produced, it is filled by an outer electron. With this electronic transition, energy is conserved by either the emission of a photon (Fig. 2.6b) or by the emission of a secondary electron through radiationless transition (Fig. 2.6c). The former emits a characteristic X-ray whose energy \( E_x \) is the difference in energy of the two levels involved in the transition with the addition of the work function. For example, if the transition is between the K and L energy levels, then:

\[
E_x = E_k - E_{L,3} + \phi
\]  

(2.5)

This transition, in which a photon is emitted, enables energy-dispersive X-ray analysis. In the case of a radiationless transition, the secondary electron emitted is the Auger electron. The energy released from one of the outer electrons to fill the core hole ejects
another electron from the atom. The discrete amount of energy is equal to the difference between the initial and final states giving the energy of the Auger electron \( (E_A) \) as:

\[
E_A = E_K - E_{L1} - E_{L2,3} + \phi
\]  

(2.6)

The transitions in which Auger emission and photon emission occur are mutually exclusive processes with total probability for their occurrence equal to one [4]. The kinetic energy of the Auger and photoemitted electrons is in the range of 50 to 2000eV. These low-velocity electrons have a high possibility of undergoing an inelastic collision with an atom in the matrix if they travel very far before leaving the surface. Sufficient energy of these electrons will be lost after a single collision making them difficult to be removed from the flux of electrons having energies given by Equations (2.4) and (2.6). Thus, only those electrons originating from the surface or a few atomic layers below the surface will contribute to an XPS peak. From peak heights or peak areas, quantitative data such as the relative concentration of the various constituents can be obtained, and identification of chemical states can be made from exact measurement of peak positions and separations.

2.2.1. XPS Sensitivity Factor

In order to calculate the relative concentration for each constituent, a sensitivity factor for each element has to be determined. For a sample that is homogeneous in the analysis volume, the number of photoelectrons per second in a specific spectral peak is given by:

\[
I = n f \sigma \theta \gamma \lambda A T
\]  

(2.7)

where \( n \) is the atomic concentration of the element (atoms/cm\(^2\)), \( f \) is the X-ray flux in photon/cm\(^2\)-sec, \( \sigma \) is the photoelectric cross-section for the atomic orbital in cm\(^2\), \( \theta \) is the instrumental angular efficiency factor based on the angle between the photon path and detected electron, \( \gamma \) is the photoelectron process efficiency for formation of photoelectrons of the normal photoelectron energy, \( \lambda \) is photoelectron mean free path in the sample, \( A \) is effective sample area from which photoelectrons are detected, and \( T \) is detection efficiency for electrons emitted from the sample. Rearranging Equation (2.7) gives:

\[
n = I / f \sigma \theta \gamma \lambda A T
\]  

(2.8)
The denominator in Equation (2.8) can be defined as the atomic sensitivity factor, S. The XPS intensities for elements 1 and 2 in the same matrix can be compared according to:

\[
\frac{n_1}{n_2} = \frac{I_1 / S_1}{I_2 / S_2}
\]

(2.9)

The expression may be used for all homogeneous samples if the ratio \(S_1/S_2\) is matrix-independent for all materials [3].

### 2.3. Auger Electron Spectroscopy (AES)

The Auger electron spectroscopy technique for chemical analysis of surfaces is based on the Auger radiationless process [5]. The process is the same as that for XPS radiationless process except it is excited by an electron beam, with energy up to 10keV, instead of a photon beam. *Figure 2.7* shows the nomenclature used to describe the Auger processes. If the energetic electron beam creates vacancies in the K shell, the Auger process is initiated when an outer electron such as an L\(_1\) electron fills the holes. The energy released can be transferred to another electron, such as another L\(_1\) or L\(_3\) electron,
to be ejected from the atom with outgoing energy of \( E_{\text{KL}L_1} = E_K - E_{L_1} - E_{L_1} \) if the ejected electron is \( L_1 \). The energy difference between these two states given to the ejected Auger electron will have a kinetic energy characteristic of the parent atom, making it possible to identify the composition of the solid surface if the Auger transitions occur within a few angstroms of the surface. The process that involves one K shell and two L shell electrons are termed KLL Auger transition in general, and more specifically denoted as KL\(_1\)L\(_1\) or KL\(_1\)L\(_2\). Evidently, three electrons must be involved to create one Auger electron; elements with fewer than three electrons (i.e. H and He) cannot emit Auger electrons, and hence cannot be detected with AES. If the vacancies happen in the L shell, Auger processes are initiated when an electron from the M shell fills the L hole and another M shell electron is ejected, an LMM Auger transition. The strongest Auger transitions are of the type KLL or LMM since electron-electron interactions are strongest between electrons whose orbitals are closest together [2].

Since the Auger peaks are superimposed on a rather large continuous background, the surface concentration of each element is calculated from the peak-to-peak magnitude of an Auger peak, with the energy distribution function \( N(E) \), in a differentiated spectrum. Thus, the conventional Auger spectrum is the function \( \frac{dN(E)}{dE} \) [5]. Figure 2.8 shows the energy spectrum of electrons emitted from a surface bombarded by an electron beam. The presence of Auger electrons is manifested as small peaks in the total energy distribution function. All of these electrons including secondary electrons, backscattered electrons, and Auger electrons can be collected, but only the Auger electrons are of interest. The secondary electrons are the lower energy electrons and are produced by inelastic collisions of the primary beam and the inner shell electrons of the sample atoms. Since they possess such low energies, only secondary electrons created close to the surface actually escape and are detected. In contrary to secondary electrons, backscattered electrons are those that have suffered elastic collisions with target atoms and thus still possess most of their incident energy. Thus they are also termed higher energy electrons with energies close to those of primary beam electrons. The secondary and backscattered electrons constitute strong noise, and in order to extract valid signal information about
emitted Auger electrons from raw data, signal processing methods, such as differentiation, must be performed to elucidate the Auger electron peaks. This differentiation is performed by electronic means using lock-in amplifiers. Nevertheless, the presence of the background electron signal places a lower bound on the sensitivity limits of Auger electron spectroscopy, only those elements with concentrations exceeding 0.1-1% at the sample surface can be detected [6].

Most Auger electron energies are between 20 and 2500eV, so the depth from which they can escape from the solid without losing a significant percentage of energy is quite shallow (< 50Å). Only those electrons from the near-surface region can escape without losing a significant portion of their energy and thus be identified as Auger electrons. The average depth from which electrons escape the solid without losing energy is referred to as inelastic mean free path (or escape depth), \( \lambda \), and is a function of the kinetic energy of the Auger electrons but independent of the primary electron energy used. Figure 2.9 shows the functional dependence of the inelastic mean free path on the kinetic energy of the Auger electrons in various elements. In the energy range of interest (20 to 2500eV), the inelastic mean free path varies from 2 to 10 monolayers, corresponding to the top 0.5 to 3 nm of the sample surface. The unique dependence of \( \lambda \).
Figure 2.9. Experimental measurements of electron escape depths in various elements [7].

on Auger electron energy distinguishes the top monolayer chemistry from the layers below [7]. Figure 2.10 shows the comparison of Auger electron escape depths with emission depths of backscattered electrons, secondary electrons, and X-rays. The escape depth of Auger electron is small compared to that of characteristic X-rays used in X-ray microprobe analysis. Thus, Auger electron spectroscopy is a technique that can only provide compositional data about the surface layers of samples. In order to provide lateral resolution (depth profile), ion sputtering with Ar⁺ on the sample surface is required to profile in-depth composition. AES data is taken from the bottom of a crater, ion sputtered into the surface as shown in Figure 2.11. Auger analysis is done by continuously sputtering and simultaneous electron spectroscopy, together with multiplexing of different element peaks and a display of the respective Auger peak-to-peak heights [8]. The depth profile can therefore be obtained by plotting the Auger peak heights as a function of milling time. However, depth profile by AES is a destructive technique since the ion sputtering will destroy the sample in the local area of the sample being examined.
Figure 2.10. Comparison of Auger electron escape depths with emission depths of backscattered electrons and X-rays [7].

Figure 2.11. Ion milling a crater and performing AES on the exposed surface, thus allowing depth profiling with AES [6].
2.4. X-ray Reflectivity

In the X-ray reflectivity method of film metrology, the specular reflectivity of X-rays from a film surface is measured as a function of incidence angle [9]. The thickness, density and roughness of a single film on a substrate or a stack consisting up to four layers can be obtained by analyzing these data with computer simulation. Since the optical constants for hard X-rays depend only on the composition and density of the film, there are fewer unknowns to fit than in ellipsometry, enable X-ray reflectivity method to be a powerful tool for thin film analysis. However, the underlying theory is quite complicated and will be only explained briefly here.

![Figure 2.12. The propagation of a plane wave in a layered structure [11].](image)

The theory of reflectivity of a multilayer structure is in general based on an iteration procedure with the use of a recurrent formula which connects the reflection amplitudes of X-ray waves in two nearest layers [10]. The formula is a direct consequence of the law of penetration and reflection of radiation at the boundary of two homogeneous media. Now, consider an artificial system which consists of plane parallel layers of different materials with abrupt boundaries between them as indicated in Figure 2.12. Each layer is assumed to be homogeneous along the surface which is parallel to the
The electric field vector in the layer with number \( m \) has the form [10]
\[
E_m(x, z, t) = E(x, t)[E_m \exp(i k_{z m} z) + E_m^R \exp(-i k_{z m} z)]
\]
where \( E(x, t) = \exp(ikx - i\omega t) \), \( E_m \) and \( E_m^R \) are the amplitudes of refracted and reflected waves in the middle of the layer and coordinate \( z \) is measured from the middle line of the layer. If the glancing incidence is of a small angle \( \theta \), at the top interface the wave vector may be approximated by \( k_{x 3} \approx k_3 \), and so
\[
k_{x 2} \approx k_3 (\theta^2 - 2\delta_2 - 2i\beta_2)^{1/2} \quad [12].
\]
The general relationship between the wave number of the \( m \)-th layer and that of vacuum is
\[
k_{z m} = k_3 f_m
\]
by adapting the notation.
\begin{equation}
\left(\frac{\partial^2}{\partial x^2} - 2\delta_m - 2\beta_m \right)^{1/2}
\end{equation}

Therefore, the conditions of continuity for the electric and magnetic fields at the boundary between the layers \( m \) and \( m-1 \) can be written as:

\begin{equation}
E_m C_m + E_m^R C_m^{-1} = E_{m-1} C_{m-1}^{-1} + E_{m-1}^R C_{m-1}
\end{equation}

\begin{equation}
k_m (E_m C_m - E_m^R C_m^{-1}) = k_{m-1} (E_{m-1} C_{m-1}^{-1} - E_{m-1}^R C_{m-1}).
\end{equation}

Here \( C_m = \exp \left( i k_m t_m/2 \right) \), where \( t_m \) is the thickness of the \( m \)-th layer [10]. Consequently, the reflection (\( R_m \)) and transmission coefficient (\( T_m \)) at the \( m \) and \( m-1 \) interface are defined as:

\begin{equation}
R_m = \frac{C_{m-1} E_m^R}{C_m E_m},
\end{equation}

and

\begin{equation}
T_m = \frac{C_{m-1} E_{m-1}}{C_m E_m}.
\end{equation}

The amplitudes \( C_m E_m, C_{m-1}^E, \) and \( C_{m-1} E_{m-1} \) are the values of the incident, reflected, and refracted beams, respectively, measured at the interface. This leads to the recursion relations

\begin{equation}
R_m = \frac{C_{m-1}^4 R_{m-1} + G_m}{C_{m-1}^4 R_{m-1} G_m + 1},
\end{equation}

and

\begin{equation}
T_m = \frac{1 + R_m}{1 + C_{m-1}^4 R_{m-1}},
\end{equation}

where

\begin{equation}
G_m = \frac{f_m - f_{m-1}}{f_m + f_{m-1}}.
\end{equation}

Therefore, reflection and transmission coefficients at every interface can be calculated if \( R \) at one interface is known. Since we have assumed there is no reflected beam that propagates in the substrate, \( R_0 = 0 \), \( R \) and \( T \) at every interface can be determined by applying the recursion relations to successive layers from bottom to the top. Consequently, the resultant reflectivity at the top surface (\( m=3 \)) is given by
\[ |R_3|^2 = \left| \frac{E^r_3}{E_3} \right|^2, \]  

with \( |C_3| = 1, f_3 = 0 \), and refractive index \( n_3 = 1 \).
References

CHAPTER 3. DEPOSITION AND ANNEALING OF GADOLINIUM OXIDE (Gd₂O₃) FILMS

Before the deposition of Gd₂O₃ on Si(001) surfaces (0.025 ohm-cm n-type), the wafers were given a standard HF-last RCA clean prior to insertion into the in-situ processing (ISP) system. A schematic diagram of the ISP system is shown in Figure 3.1. Wafers were transported in the ISP system with trolley moving through different tunnels with the background pressure of 1.8×10⁻⁷ Torr. The chamber for the deposition of Gd₂O₃ films is the Si e-beam chamber located near the end of the system with background pressure in the range of 2.5×10⁻¹⁰ to 1.2×10⁻¹⁰ Torr before the deposition. The base pressure after bake-out was dominated by hydrogen and the background water vapor pressure was <5×10⁻¹² Torr. Gd₂O₃ films were deposited using an electron-beam (e-beam) evaporator with 6mm diameter pressed-powder Gd₂O₃ rods (nominally 99.999% pure). The evaporation source, manufactured by Thermionics Inc, featured a standard 270° beam deflection geometry as described in Electron-beam Evaporation section 2.1 with the rod passing through a water-cooled block. Figure 3.2 shows the evaporation source of the e-beam used to deposit Gd₂O₃ films. Different deposition rates were chosen for thick and thin films. However, it was observed that the deposition rate does not stay constant during the deposition, so adjusting the depositing current is required to achieve a stable deposition rate. For a typical deposition rate of 2Å/sec, the depositing current is around 32mA. The background gases during deposition were monitored with a quadrupole mass spectrometer, and it was found that the O and O₂ pressures were each ~10⁻⁸ Torr for the usual deposition rate of 2Å/sec. It was also found that hydrogen and carbon monoxide pressure rose to 1×10⁻⁸ and 1×10⁻⁹ Torr, respectively, during deposition, due to stray heat from the electron gun. An external flowmeter allowed molecular oxygen gas to be introduced into the chamber, and depositions were carried out at pressures up to 10⁻⁴ Torr.

Table 3.1 lists all the wafers deposited with Gd₂O₃ films under different conditions. The films were deposited at different substrate temperatures held at ambient or heated to 500°C with a quartz-lamp heater. Two of the thin films, around 15Å
Figure 3.1. A schematic diagram of the In-situ Processing (ISP) system used to deposited Gd$_2$O$_3$ films.
Figure 3.2. A blow view of electron-beam used to deposit $\text{Gd}_2\text{O}_3$ films. The beam features a standard $270^\circ$ beam deflection geometry with the rod passing through a water-cooled block.
Table 3.1. Sample summary for all the wafers deposited Gd$_2$O$_3$ films under different conditions.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>lsp906</td>
<td>Room Temp, UHV</td>
</tr>
<tr>
<td>lsp912</td>
<td>Room Temp, UHV</td>
</tr>
<tr>
<td>lsp913</td>
<td>Room Temp&lt;br&gt;Annealed 300°C, 500°C, 800°C in situ</td>
</tr>
<tr>
<td>lsp915</td>
<td>Room Temp&lt;br&gt;Annealed 300°C, 500°C, 800°C in situ</td>
</tr>
<tr>
<td>lsp960</td>
<td>Room Temp, UHV</td>
</tr>
<tr>
<td>lsp961</td>
<td>500°C, UHV</td>
</tr>
<tr>
<td>lsp962</td>
<td>Room Temp, UHV</td>
</tr>
<tr>
<td>lsp971</td>
<td>500°C, 2×10^{-5} Torr O$_2$</td>
</tr>
<tr>
<td>lsp972</td>
<td>500°C, UHV</td>
</tr>
<tr>
<td>lsp975, 976</td>
<td>Room Temp, UHV</td>
</tr>
<tr>
<td>lsp973</td>
<td>500°C, 2×10^{-5} Torr O$_2$</td>
</tr>
<tr>
<td>lsp974</td>
<td>500°C, 1×10^{-4} Torr O$_2$</td>
</tr>
<tr>
<td>lsp989</td>
<td>500°C, 1×10^{-4} Torr O$_2$&lt;br&gt;on Dolf's Buffer</td>
</tr>
<tr>
<td>lsp980</td>
<td>Room Temp.&lt;br&gt;Low background pressure&lt;br&gt;Annealed 700°C in-situ</td>
</tr>
<tr>
<td>lsp1003</td>
<td>Room Temp.&lt;br&gt;Low background pressure</td>
</tr>
</tbody>
</table>
(ISP913 and ISP915), were annealed in-situ (under UHV condition) at 300, 500, 800°C. Excess oxygen was bled into the Si e-beam chamber during deposition of ISP971, 973, 974 and 989. For ISP980 and ISP1003, the gadolinium rod source was degassed just under threshold current for deposition (around 10mA) for one hour to get rid of the residual oxygen (or water) in the rod. Some samples (ISP975, 976, and 989) were deposited a very thin buffer layer of oxynitride prior to the deposition of Gd$_2$O$_3$ films.

*Figure 3.3 and 3.4 show the deposition rate and background pressure during the deposition of ISP962 and ISP1003 both deposited at room temperature, respectively. The background pressure of ISP1003 during deposition (low $10^{-7}$ Torr) was of one magnitude lower than that of ISP962 (low $10^{-6}$ Torr) since the rod source was degassed before the deposition. Nevertheless, same feature was observed for both samples, the deposition pressure followed the same trend as the deposition rate. With increasing deposition rate, the background pressure rose. The pressure rise (predominantly oxygen) was caused by the increase in deposition current to achieve vaporization and thermal dissociation of the oxide target during e-beam heating.*

![Figure 3.3 - Deposition Rate vs. Pressure](image)

*Figure 3.3. Plot of background pressure vs. deposition rate during the deposition of ISP962 deposited at room temperature without degassing the Gd$_2$O$_3$ rod source.*
Figure 3.3. Plot of background pressure vs. deposition rate during the deposition of ISP1003 deposited at room temperature. The rod source was degassed for 1 hour prior to deposition.

Post-deposition anneal for the as-deposited Gd$_2$O$_3$ films was done in a Heatpulse 610 (Steag RTP Systems) rapid thermal processing system. With rapid thermal anneal, the temperature was raised at a fast rate of 100°C/sec, stayed at desired temperature for input duration and then cooled down at a much slower rate. The reason for a slow cool down rate is to avoid thermal stress built up in the film that might cause the degradation of the film quality. The purpose of post-deposition anneal is to reduce some of the defects, such as voids in the film or dangling bonds at the interface. Samples were annealed with the RTP at 500, 700, and 780°C in O$_2$ for 10 minutes, while some of the films were only annealed at 780°C in O$_2$ for 2 minutes. In-situ annealing of two of the thin films at 300, 500, 800°C was done in ECR-CVD chamber of the ISP system under UHV condition.
CHAPTER 4. RESULTS AND DISCUSSION

In this section, material aspects and electrical properties of the Gd$_2$O$_3$ films deposited on Si(001) surface will be discussed. For material analysis, the stoichiometry of the film was measured by X-ray photoelectron spectroscopy, whereas the depth profiling analysis of the films was examined by Auger electron spectroscopy. Furthermore, the interface between Gd$_2$O$_3$ and Si substrate was resolved by transmitted electron microscopy (TEM) and the film surface roughness was inspected by atomic force microscopy (AFM). The thickness of the film and structure were determined by the method of X-ray reflectivity. In the electrical properties of the films, the dielectric constant ($K$) of Gd$_2$O$_3$ films was calculated. Some important characteristics of the capacitance-voltage (C-V) and current-voltage (I-V) measurements will be discussed. They include hysteresis measured at high and low frequency C-V, approximation of interface state density, gate leakage current and its mechanisms.

4.1. Material Analysis

4.1.1. Stoichiometry of the As-deposited Gadolinium Oxide

The stoichiometry of the as-deposited film was measured by the in-situ XPS machine with X-ray source located at 54.7° relative to the analyzer axis, giving sensitivity factors for O$_{1s}$ and Gd$_{4d}$ peaks of 0.711 and 2.484, respectively. The reason for studying the Gd$_{4d}$ peak instead of the Gd$_{3d}$ peak for gadolinium is that Gd$_{4d}$ has the strongest signal for the XPS spectrum. However, the spectral structure of Gd$_{4d}$ peak is quite complicated and is discussed in Ref. [1]. The stoichiometry of the film is then calculated by integrating the area under the peaks of O$_{1s}$ and Gd$_{4d}$ and with their sensitivity factors. This gives:

$$\frac{n_{Gd}}{n_O} = \frac{I_{Gd}}{I_O} \frac{S_{Gd}}{S_O} = \frac{S_{Gd}}{S_O} \frac{I_{Gd}}{I_O} = \frac{0.711}{2.484} \frac{I_{Gd}}{I_O} = 0.286232 \frac{I_{Gd}}{I_O},$$

where $n_{Gd}$ and $n_O$ are the atomic concentrations of Gd and O, and $I_{Gd}$ and $I_O$ are the intensity for Gd$_{4d}$ and O$_{1s}$ peaks, respectively. Table 4.1 lists the [Gd]/[O] ratio for the 16 wafers measured. The resultant value of [Gd]/[O] = 0.55 ± 0.07, indicates that the as-deposited film is stoichiometric Gd$_2$O$_3$. The small deviation from the expected [Gd]/[O] ratio of 0.67 is probably due to the accumulated moisture on the Gd$_2$O$_3$ film surface. The
The hygroscopic (moisture absorbing) property of the Gd$_2$O$_3$ films will be discussed in the next section. The [Gd]/[O] ratio of the two thin films (ISP913 and ISP915) cannot be calculated with the Gd$_{4d}$ and O$_{1s}$ spectrums due to the fact that Si$_{2s}$ peak positioned at 151eV contributed a strong signal that interfered with the signal of the Gd$_{4d}$ peak, as indicated in Figure 4.1. Moreover, the [Gd]/[O] ratio of sample ISP1003 cannot be obtained because the wafer was broken during the transfer into the in-situ XPS machine.

Table 4.1. The [Gd]/[O] ratio for the 16 wafers measured by In-situ XPS. The X-ray source is at 54.7° relative to the analyzer axis.

<table>
<thead>
<tr>
<th>Sample Number</th>
<th>$Gd/O$</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISP 906</td>
<td>0.54</td>
</tr>
<tr>
<td>ISP 912</td>
<td>0.53</td>
</tr>
<tr>
<td>ISP 913</td>
<td>-</td>
</tr>
<tr>
<td>ISP 915</td>
<td>-</td>
</tr>
<tr>
<td>ISP 960</td>
<td>0.52</td>
</tr>
<tr>
<td>ISP 961</td>
<td>0.62</td>
</tr>
<tr>
<td>ISP 962</td>
<td>0.55</td>
</tr>
<tr>
<td>ISP 971</td>
<td>0.52</td>
</tr>
<tr>
<td>ISP 972</td>
<td>0.53</td>
</tr>
<tr>
<td>ISP 973</td>
<td>0.53</td>
</tr>
<tr>
<td>ISP 974</td>
<td>0.54</td>
</tr>
<tr>
<td>ISP 975</td>
<td>0.58</td>
</tr>
<tr>
<td>ISP 976</td>
<td>0.62</td>
</tr>
<tr>
<td>ISP 980</td>
<td>0.58</td>
</tr>
<tr>
<td>ISP 989</td>
<td>0.53</td>
</tr>
<tr>
<td>ISP 1003</td>
<td>-</td>
</tr>
</tbody>
</table>
Figure 4.1. XPS spectrum for Gd 4d peak excited by Mg Kα radiation. The Si 2s peak is also shown in the spectrum.

Figure 4.2 shows the spectra of Gd₄d and O₁s. The two spectra have been referred to the C₁s core level binding energy at 284.8eV. For the O₁s spectrum, two O₁s peaks are clearly identified, one with binding energy at about 528.95eV and another one at about 531.49eV. The peak with higher binding energy at ~531.49eV is commonly observed for practically all ex-situ surfaces (i.e., oxide surface, which are exposed to air), and is generally produced by surface contaminants [2]. The intensity of this peak (referred as "adventitious O₁s peak" here after) varies with environment as in atmosphere or in UHV, and will be discussed in the next section. The second peak at ~528.95eV is attributed to O to Gd bonding, and the relative intensity of this peak is related to the film thickness. In the case of Gd₄d spectrum, it seems first there are two peaks. The main peak is at 141.1eV, while the secondary peak is at 146.5eV. However, as explained in Ref. [1], the spectral structure of Gd 4d is actually quite complicated and is attributed to multiplet splitting of the 4d hole with the 4f⁷ valence electrons, forming ⁹D and ⁷D final ionic states.
Figure 4.2. XPS spectra of Gd 4d and O 1s peaks for gadolinium oxide. The spectra were referred to the C 1s core level binding energy at 284.8 eV.

4.1.2. Hygroscopic Property of Gd₂O₃ Films

ISP906 was the first Gd₂O₃ film and had a thickness of 500Å. The change in composition of the film was analyzed by the in-situ XPS machine with Mg-Kα X-ray source and with pass energy of 29.35 eV. It is found that the peak of adventitious oxygen (surface contaminant) was at a minimum for the as-deposited condition, so essentially the whole area of the O₁s peak was attributed to O-Gd bonding. The [Gd]/[O] ratio was determined to be 0.54. The wafer was then taken out of the ISP system and left in a nitrogen container for 50 days. The composition of the same wafer was investigated again by the in-situ XPS in order to determine the change in composition as the film was exposed to atmosphere. The resultant [Gd]/[O] ratio was determined to be 0.35, taking the whole area under the two peaks of the O₁s spectrum. The adventitious peak for O₁s
increased in intensity compared with the film deposited under UHV, as shown in Figure 4.3. If curve fitting was performed to subtract the adventitious oxygen peak, the composition of the film was then calculated to be [Gd]/[O] = 0.96. The correct composition of the film cannot be determined simply by subtracting the adventitious peak for oxygen, since some oxygen atoms are both bonding to Gd and adventitious species. Nevertheless, it is conclusive that the Gd₂O₃ film absorbs a lot of moisture (hygroscopic) during exposure to atmosphere. In order to reduce the moisture content in the film, a quarter piece was annealed in ECR-CVD chamber at 800°C for 10 minutes in-situ. The annealed film exhibited the same composition compared to the film deposited under UHV, with [Gd]/[O] ratio of 0.56. Figure 4.3 also shows that the intensity of the adventitious O peak decreased to the same extent for the as-deposited film. Table 4.2 summarizes a series of calibrations on the composition of Gd₂O₃ film under different conditions.

Figure 4.3. XPS spectrum of O 1s peaks for Gd₂O₃ films under different conditions.
Table 4.2. Summary of [Gd]/[O] ratio for Gd₂O₃ films under different conditions.

<table>
<thead>
<tr>
<th>Condition</th>
<th>Mg source (in-situ XPS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Right after deposition</td>
<td>Pass energy: 29.35 eV</td>
</tr>
<tr>
<td>(in vacuum)</td>
<td>Gd/O ratio: 0.54</td>
</tr>
<tr>
<td>Left in N₂ container</td>
<td>Pass energy: 29.35 eV</td>
</tr>
<tr>
<td>for 50 days</td>
<td>Gd/O ratio (including the two peaks for O₁s): 0.35</td>
</tr>
<tr>
<td></td>
<td>Gd/O ratio (excluding the adventitious O peak): 0.96</td>
</tr>
<tr>
<td>Annealed at 800°C for 10 min in-situ</td>
<td>Pass energy: 29.35 eV</td>
</tr>
<tr>
<td></td>
<td>Gd/O ratio: 0.56</td>
</tr>
</tbody>
</table>

4.1.3. In-situ XPS Analysis

The National Technology Roadmap for Semiconductors states that an alternate gate oxide should have a high dielectric constant ($K$), be stable in contact with silicon (withstand an ~900°C annealing step), have a low density of electrically-active defects at the oxide/silicon interface ($D_{it}$) [3]. In order for the oxide to avoid reactions with silicon, it is highly desirable that the oxide/silicon interface be thermodynamically stable. This section discusses the stability of interface between Gd₂O₃ and Si(001) substrate by depositing a very thin Gd₂O₃ film so that the Si₂p spectrum can be resolved by the resolution depth of XPS. By carefully studying the chemical shift for both the Si₂p peak and the O₁s peak, the bonding structure at the interface can be extracted and therefore the thermodynamic stability of Gd₂O₃ film in contact with Si can be investigated.

Since the chemical composition in a thin film with a thickness no more than 20Å can be best studied using XPS, Gd₂O₃ films a few monolayers thick (≈14Å) were deposited on samples ISP913 and ISP915. The films were then in-situ annealed at different temperatures of 300, 500, and 800°C, with water vapor pressure rose to ~10⁻⁷ Torr during 800°C anneal. After each annealing step, Si₂p, O₁s, Gd₄d, and Gd₃d spectra were obtained by the in-situ XPS machine. For the Si₂p spectrum, it was observed that a secondary shoulder appeared at about 103.37eV for the as deposited condition with the reference Si₂p peak positioned at about 100.32eV. The intensity of the secondary shoulder increased with annealing temperature as indicated in Figure 4.4. A least-square
curve fitting was used to determine the chemical shift of this oxidation state, assuming the spin-orbit splitting of 0.612eV of the Si 2p_{1/2,3/2} peak [4]. The shift in binding energy for this oxidation state was determined to be 3.08eV. This shows that the chemical environment in the layer above the Si substrate had been changed during the deposition, causing the binding energy of the Si 2p level to shift by about 3.08eV. The oxidation state of this chemical shift of 3.08eV has yet to be determined. However, it is reported in Ref. [5] that for chemical shift of 2.6eV, the chemical state is Si^{+3}, whereas that for Si^{+4} (SiO₂) is 3.82eV towards higher binding energy. The concept of chemical shifts is explained by the fact that the inner electrons feel an alteration in energy due to a change in the valence shell contribution to the potential based on the outer electron chemical binding. The greater the electronegativity of the surrounding atoms, the more the displacement of electronic charge from the atom and the higher the observed binding energies of the core electrons [6]. The electronegativity is the relative tendency of an element to gain, or attract, an electron, and the electronegativity of O, Si, and Gd has been shown to be 3.44, 1.90, and 1.20, respectively.

Figure 4.4. XPS spectrum of Si 2p peak for a thin film (ISP915 ~14Å) annealed in-situ.
To identify the reaction that takes place at the interface of the Gd₂O₃ with the Si substrate, all possible reactions that can occur between Si and Gd₂O₃ need to be analyzed thermodynamically. To avoid reactions with silicon, it is desirable that the oxide/silicon interface must be thermodynamically stable. As suggested in Ref. [7], possible reactions for a binary oxide (MOₓ) in contact with silicon are:

\[ \text{Si} + \text{MO}_x \rightarrow \text{M} + \text{SiO}_2 \]  \hspace{1cm} (4.2)

and

\[ \text{Si} + \text{MO}_x \rightarrow \text{MSi}_x + \text{SiO}_2 \]  \hspace{1cm} (4.3)

if an element has multiple silicides, the most silicon-rich silicide (MSiₓ) should be used in Equation (4.3). The Gibbs free energy at room temperature (298K) for Si, Gd, Gd₂O₃, and SiO₂ can be found in Ref. [8] and [9], whereas that for the most silicon-rich gadolinium silicide (GdSi₁.₈⁹) in the temperature range of 830K to 960K is available in Ref. [10]. Due to the lack of thermodynamic data for GdSi₁.₈⁹ at room temperature, the Gibbs free energy of GdSi₁.₈⁹ for the above mentioned temperature range will be used to carry out the calculation. Increasing temperature will lead to a decrease in the Gibbs free energy (more negative since \( G = H - TS \)) of an element, therefore by overestimating the \( G^\circ_{298} \) for GdSi₁.₈⁹ at room temperature the thermodynamic calculation here will not be invalidated. In another words, since

\[ \Delta G^\circ_{298} = \sum \text{Products } G^\circ_{298} - \sum \text{Reactants } G^\circ_{298} \]  \hspace{1cm} (4.4)

the overestimated value of \( G^\circ_{298} \) for GdSi₁.₈⁹ (more negative) will give a conservative result for the calculation. If the calculated \( \Delta G^\circ_{298} \) for the reaction involving GdSi₁.₈⁹ is positive by using the \( G^\circ_{830-930} \) for GdSi₁.₈⁹, it implies that the actual value of \( \Delta G^\circ_{298} \) at room temperature will be more positive if \( G^\circ_{298} \) for GdSi₁.₈⁹ is known. The \( \Delta G^\circ_{298} \) per mole of GdO₁.₅ for the balance equations of

\[ 0.75\text{Si} + \text{GdO}_1.5 \rightarrow \text{Gd} + 0.75\text{SiO}_2 \]  \hspace{1cm} (4.5)

and

\[ 2.64\text{Si} + \text{GdO}_1.5 \rightarrow \text{GdSi}_1.89 + 0.75\text{SiO}_2 \]  \hspace{1cm} (4.6)

is calculated to be 53.039 kcal/mol and 55.51 kcal/mol, respectively, by using the thermodynamic data mentioned above. Since the magnitude of \( \Delta G^\circ_{298} \) indicates the direction of the reaction, the positive Gibbs free energy values mean that it is
thermodynamically unfavorable for the reaction to proceed to its products. The two reactions (4.5) and (4.6) are thus been ruled out from the thermodynamic calculation. If the M-Si-O system contains more than one MO\textsubscript{x} binary oxide, reactions involving MO\textsubscript{x} binary oxide on both sides of the equation must also be tested [7]. The additional reactions to be tested are:

\[ \text{Si} + \text{MO}_x \rightarrow \text{MO}_w + \text{SiO}_2 \]  

(4.7)

and

\[ \text{Si} + \text{MO}_w \rightarrow \text{MO}_x + \text{MSi}_z \]  

(4.8)

where MO\textsubscript{x} and MO\textsubscript{w} are the two binary oxides with MO\textsubscript{x} being the more oxygen-rich. Gadolinium is reported to form an oxygen-rich oxide GdO\textsubscript{2} [11, 12]. Tarsa et al. [12] suggested that Gd\textsubscript{2}O\textsubscript{3} reacts with silicon to form GdO\textsubscript{2} and gadolinium silicide, but no thermodynamic data is available for the GdO\textsubscript{2} phase. Furthermore, since three silicates of gadolinium have been identified [13], reactions involving the formation of silicates (ternary oxide MSi\textsubscript{x}O\textsubscript{y}) need to be considered [7] as follow:

\[ \text{Si} + \text{MO}_x \rightarrow \text{MSi}_z + \text{MSi}_x\text{O}_y \]  

(4.9)

\[ \text{Si} + \text{MO}_x \rightarrow \text{M} + \text{MSi}_x\text{O}_y \]  

(4.10)

\[ \text{Si} + \text{MO}_x \rightarrow \text{SiO}_2 + \text{MSi}_x\text{O}_y \]  

(4.11)

The +3.08eV shift in binding energy for the Si 2p level indicates that the resultant compound at the interface is not a silicide of GdSi\textsubscript{1.89}, but instead is a silicate. Silicides are binary compounds of silicon, usually with a more electropositive element such as gadolinium. The structures of silicates are based on (SiO\textsubscript{4})\textsuperscript{4-} tetrahedra linked from zero to four corner oxygens. If silicide is formed at the interface, the shift in binding energy should be negative since silicon is bonded to the more electropositive element. If silicon dioxide (SiO\textsubscript{2}) is formed, the shift should be \( \approx 4eV \) since silicon is bonded to 4 oxygen atoms having each Si-O bond contributing +1eV shift. However, we have to consider the next-nearest neighbor effect that would cause the shift in binding energy of SiO\textsubscript{2} to be less than 4eV if oxygen is also bonded to a more electropositive element. The formation of silicate can be further corroborated by the bonding structure of oxygen. The bonding structure of oxygen is determined by overlaying the oxygen spectrums for both a thick (~100Å) and a thin (~14Å) films for the as-deposited condition (ISP912 and ISP913).
ISP912 was deposited with 100Å Gd₂O₃, where ISP913 was with 14Å. The spectra were both obtained with Al Kα X-ray source, setting the pass energy to 5.85eV. Since the Gd₄d peak for ISP913 (thin film) was interfered by the strong signal of Si₂s peak, it is difficult to align spectra by using the Gd₄d peak as a reference. Thus, the Gd₃d peak is used instead to align all spectra for both ISP912 and ISP913 as shown in Figure 4.5. In spite of the alignment in binding energy, there is a 1eV shift in binding energy for the two oxygen peaks. Figure 4.6 shows that the oxygen peak for the thick film is positioned at ~529eV whereas that for thin film is positioned at ~530eV. The O spectrum for the thick film (ISP912) is attributed to Gd-O bonding while that for the thin film (ISP913) is associated with the bonding structure of oxygen near the interface. The +1eV shift for the thin film indicates that oxygen is not only bonded to Gd but also bonded to Si atoms at the interface since the electronegativity of Si (1.90) is higher than that of Gd (1.20). This further confirms that it is gadolinium silicate formed at the interface for the initial reaction for the as deposited Gd₂O₃ film under UHV.

![XPS spectrum of Gd 3d peak as a reference to align all spectra for a thick (ISP912) and a thin (ISP913) films for the as-deposited condition.](image-url)
Figure 4.6. XPS O 1s spectrum for both a thick (ISP912) and a thin (Isp913) films for the as-deposited condition. Note, 1eV shift in binding energy between thick and thin films was observed.

4.1.4. Auger Depth Profile of the Film Composition

Auger analysis was performed on a Physical Electronics Industries 650 instrument with a cylindrical mirror analyzer which operated with a 5kV electron beam 30° off normal. Sputter profiling was performed with a 1keV argon ion beam. Si LMM, C KLL, and O KLL lines were used to analyze the depth distributions of silicon, carbon, and oxygen in the films respectively, while the gadolinium profile was obtained from the valence (MNN) transition at 138eV. For the C KLL, Gd MNN and O KLL signals, the atomic concentration is directly related to the peak-to-peak height of the derivative spectra. The sensitivity factors for silicon, carbon, and oxygen used for the analysis were those provided by the instrument manufacture [14].
Figure 4.7 shows the Auger depth profiles for Gd, O, and Si for films deposited at room temperature (ISP962) and at substrate temperature of 500°C (ISP972) both with no oxygen flow during the deposition. No post-oxidation anneal was done to these films. The interface is indicated on the figure. It is worth noting that there is quite a long tail of gadolinium into the Si substrate, implying that the interface is not as sharp as anticipated. In addition, the interface quality does not improve with increasing substrate temperature. The long tail of gadolinium in the Si substrate can be caused by diffusion of gadolinium into the substrate or by a rough interface. If the interface between the Gd₂O₃ film and Si substrate is relatively rough, this artifact may result during sputtering through the film. However, sample ISP962 was measured to have a RMS (root-mean-square) roughness of 0.18nm by the atomic force microscopy, which indicates that the film was relatively smooth (refer to section 4.1.7). Nevertheless, the as-deposited films seem to be stoichiometric Gd₂O₃ with an atomic concentration of [Gd]:[O] of 2:3 from the Auger depth profile. Within the sensitivity of the instrument, no carbon was detected in the films.

Figure 4.7. Auger depth profiles for Gd, O, and Si for Gd₂O₃ films deposited at room temperature (ISP962) and at substrate temperature of 500°C (ISP972) both with no oxygen flow during the deposition.
The Auger depth profiles for Gd, O, and Si on one of the thick films, ISP960 with nominal thickness of 230Å, are shown in Figure 4.8 for pieces of as-deposited and 500, 700, and 780°C annealed samples. The post-oxidation of the samples was done by RTP in oxygen for 10 minutes. The sputter time has been adjusted for better comparison. This was accomplished by setting the sputter time at atomic concentration of 50% Si to be the same for all samples. The bulk of the film remained stoichiometric Gd₂O₃ upon annealing, despite the fact that a little increase in Si concentration near the interface was detected for the sample annealed at 780°C. Figure 4.9 shows the depth profiles for O, Gd, and Si for another thick film, ISP906 with a nominal thickness of 500Å. The film remains stoichiometric Gd₂O₃ upon annealing. Consequently, we can conclude that for Gd₂O₃ films with thickness ≥ 23nm deposited on Si(001), the composition of the films do not change with annealing temperature up to 780°C.

Figure 4.8. Auger depth profiles for the thick Gd₂O₃ film, ISP960 with nominal thickness of 230Å, for pieces of as-deposited and 500, 700, and 780°C annealed samples.
Figure 4.9. Auger depth profiles for another thick Gd$_2$O$_3$ film, ISP906 with nominal thickness of 500Å, for pieces of as-deposited and 500, 700, and 780°C annealed samples.

In comparison, thin films showed distinct structure in the O, Gd, and Si profiles as the films were annealed in oxygen with the RTP system. Figure 4.10 shows the Auger depth profiles for a thin film (ISP972), with nominal thickness of 80Å deposited with substrate temperature at 500°C, and films annealed at different temperatures in oxygen. For all of the annealed samples except for the as-deposited film, both the O and Gd profiles show a dip and rise when going from the surface to the silicon substrate, while the Si profile first rises and then falls before increasing in the Si substrate. This indicates that annealing results in a 3-layer structure in the film. The O KLL and Gd MNN peaks were observed to have relatively constant peak-shapes throughout the film, while the Si LMM peak varied substantially during sputtering through the film. The change in peak shape is attributed to the changes in the chemical environment of atoms, particularly when one or two valence electrons are involved in changes in chemical bonding. Since the peak shape could be related to the energy distribution of electrons in the valence band, the change in Si peak shape can be explained by the change in chemical bonding.
around Si atoms. Although good silicon concentrations cannot be obtained from the Si LMM Auger data, the results clearly show that silicon has diffused into the Gd₂O₃ film. Consequently, it is conclusive to say that annealing Gd₂O₃ films with thickness ≤ 100Å in oxygen will result in a 3-layer structure in the films. The structure and composition of the as-deposited and annealed films will be discussed in the next section.

Figure 4.10. Auger depth profiles for a thin Gd₂O₃ film, ISP972 with nominal thickness of 80Å. Strong intermixing of the film composition was observed for the annealed samples.

4.1.5. Determination of Film Structure and Thickness by TEM and X-ray Reflectivity

The structure of the films and the effect of annealing were observed directly in high-resolution TEM micrographs made on a Philips EM-430T instrument operating at 250 keV. Cross-sectional samples were made using a low-angle ion-milling technique. X-ray reflectivity measurements were made using a Cu anode (λ=1.54Å) and a double-crystal channel-cut monochromator as shown in Figure 4.11. The reflectivity scans were obtained by scanning in angle, θ, at glancing angle between 0 and 4°. The interpretation of reflectivity data from a multilayer structure makes use of a recursive procedure based.
on the Fresnel formulae [15,16] as described in the X-ray reflectivity section 2.4. Each layer with index \( m \) (\( m=0 \) for the substrate) is described by its thickness, \( t_m \) and its optical constants \( \delta_m \) and \( \beta_m \) which depend on the illuminating wavelength, \( \lambda \). In this notation the complex index of refraction is defined as \( n_m = 1 - \delta_m - i\beta_m \). The optical constants for materials of interest are listed in Table 4.3. Using the definitions \( f_m = (\delta^2 - 2\delta_m - 2i\beta_m)^{1/2} \) and \( C_m = \exp(i k_m t_m/2) \), where the wave vector, \( k = 2\pi/\lambda \), the recursion relations are expressed as

\[
G_m = \frac{f_m - f_{m-1}}{f_m + f_{m-1}}, \quad (4.12)
\]

and

\[
R_m = \frac{C_{m-1}^4 R_{m-1} + G_m}{C_{m-1}^4 R_{m-1} G_m + 1}, \quad (4.13)
\]

For three layers above a substrate, the measured reflectivity (in air, \( m = 4 \)) is \( \| R_4 \|^2 \), with \( \| C_4 \| = 1 \), \( f_4 = 0 \), and \( R_0 = 0 \) assuming no reflected wave travels in the substrate. The schematic model of the postulated 3-layer structure is illustrated in Figure 4.12.

![Schematic of the X-ray reflectivity instrument with Cu anode (\( \lambda=1.54\text{Å} \)) and a double-crystal channel-cut monochromator.](image)

Figure 4.11. Schematic of the X-ray reflectivity instrument with Cu anode (\( \lambda=1.54\text{Å} \)) and a double-crystal channel-cut monochromator.
Table 4.3. Optical constants and densities of several materials used for X-ray reflectivity measurements. The values for the silicates, Gd$_2$SiO$_5$ and Gd$_2$Si$_2$O$_7$, were calculated using linear combinations of the constants of Gd$_2$O$_3$ and SiO$_2$ in the ratios 1:1 and 1:2, respectively.

<table>
<thead>
<tr>
<th>Material</th>
<th>$\delta$ ($\times 10^7$)</th>
<th>$\beta$ ($\times 10^7$)</th>
<th>Density (g/cm$^3$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>76.03</td>
<td>1.728</td>
<td>2.327</td>
</tr>
<tr>
<td>SiO$_2$</td>
<td>71.35</td>
<td>0.9208</td>
<td>2.2</td>
</tr>
<tr>
<td>Gd$_2$O$_3$</td>
<td>174.8</td>
<td>34.83</td>
<td>7.407</td>
</tr>
<tr>
<td>Gd$_2$SiO$_5$</td>
<td>123.1</td>
<td>17.87</td>
<td>4.804</td>
</tr>
<tr>
<td>Gd$_2$Si$_2$O$_7$</td>
<td>105.8</td>
<td>12.22</td>
<td>3.936</td>
</tr>
</tbody>
</table>

Figure 4.12. Schematic model of the postulated 3-layer structure in Gd$_2$O$_3$ films after annealing.

Figure 4.13 shows the TEM micrographs for sample ISP972 as-deposited and after annealing, with a nominal thickness of 80Å deposited at substrate temperature of 500°C. Again, the annealing was done with RTP system in oxygen. The same feature was observed here in comparison with the results from Auger depth profiling. The film consisted of a 3-layer structure even for the as-deposited sample. From the figure, it is apparent that a thin interfacial layer was formed during the deposition process, and that each sample consisted of three distinct layers after annealing with thickness as indicated.
The topmost layer is polycrystalline Gd$_2$O$_3$ and the crystalline grain size increases upon annealing as shown in the figure. The composition of the topmost layer is confirmed by the X-ray diffraction data from the 500Å thick reference film (ISP906), which exhibits a peak due to a set of planes with spacing \( d = 3.12 \text{Å} \), a characteristic of the (222)-reflection in cubic Gd$_2$O$_3$ [17].

![TEM micrographs](image)

Figure 4.13. TEM micrographs for sample ISP972 under different conditions with nominal thickness of 80Å deposited with substrate temperature at 500°C.

Non-linear least-squares fits to the reflectivity data for the same sample are shown in Figure 4.14. From the contrast in the TEM micrographs and the electrical measurements (which will be discussed later), it is plausible that the layer nearest the silicon substrate is SiO$_2$. The fits are not sensitive to the thickness of the buried SiO$_2$ layer due to the fact that the electron density for SiO$_2$ (2.2 g/cm$^3$) and Si (2.327 g/cm$^3$)
are very close. Therefore, layer 1 was assumed to be SiO$_2$ with the thickness fixed at the value determined from the TEM measurement. Layer 3 was assumed to be Gd$_2$O$_3$ and the thickness was a free parameter in the fitting. The composition of layer 2 was determined from the X-ray optical constants, in which $\delta_2$ was allowed to vary while $\beta_2$ is a dependent variable related to $\delta_2$ through the Kramers-Kronig relations [18] and was adjusted manually in the least-square fitting. From the best fit value of $\delta_2$, the value of $\beta_2$ was found by supposing that the layer consists of a mixture of SiO$_2$ and Gd$_2$O$_3$, and the optical constants of the mixture are a linear combination of those for the two pure oxides. An iterative procedure was used to ensure the correspondence between these two parameters. The results of this analysis are summarized in Table 4.4. The SiO$_2$ contents were found to be 19, 21, and 33% for the samples annealed at 500, 700, and 780°C, respectively. For the as-deposited film, the data were analyzed by using a simpler Gd$_2$O$_3$/SiO$_2$/Si(001) structure since it was difficult to discern or fit separate layers probably due to the inhomogeneous film along the growth direction. This technique yields much better results for the annealed films where the contrast between successive layers is more pronounced [19]. The characteristic layer structure exhibited in sample ISP972 was observed for all the annealed and as-deposited samples with thickness $\leq 100\AA$ regardless of oxygen flow-rate during the deposition or deposition temperature for the ranges studied in this work. The resultant film structure after annealing at temperature $\geq 500^\circ$C is shown in Figure 4.15. The interfacial SiO$_2$ layer grows during oxygen annealing at a rate dependent on temperature and the thickness of the gadolinium oxide layer.
Figure 4.14. X-ray reflectivity data (symbols) for the Gd$_2$O$_3$ film of ISP972 with different conditions as indicated. Solid lines denote the results of fitting. The datasets were offset by two decades for clarity.

Table 4.4. Results of the X-ray reflectivity analysis for ISP972. Thickness of each layer is denoted as $t_m$.

<table>
<thead>
<tr>
<th>Sample ISP972</th>
<th>$t_1$ (Å)</th>
<th>$\delta_2$ ($\times 10^5$)</th>
<th>$\beta_2$ ($\times 10^7$)</th>
<th>$t_2$ (Å)</th>
<th>$t_3$ (Å)</th>
<th>$t_{total}$ (Å)</th>
</tr>
</thead>
<tbody>
<tr>
<td>as-deposited</td>
<td>5</td>
<td>-</td>
<td>-</td>
<td>59</td>
<td>64</td>
<td></td>
</tr>
<tr>
<td>annealed 500°C</td>
<td>15</td>
<td>155</td>
<td>28</td>
<td>15</td>
<td>50</td>
<td>80</td>
</tr>
<tr>
<td>annealed 700°C</td>
<td>23</td>
<td>153</td>
<td>28</td>
<td>16</td>
<td>48</td>
<td>87</td>
</tr>
<tr>
<td>annealed 780°C (10 min)</td>
<td>23</td>
<td>141</td>
<td>24</td>
<td>20</td>
<td>42</td>
<td>85</td>
</tr>
</tbody>
</table>
4.1.6. Growth Kinetics of Parasitic SiO₂ Layer

The growth kinetic of the interfacial SiO₂ layer can be explained by the well know Deal-Grove model for the oxidation process of silicon illustrated in Figure 4.16. As described in the model, for the oxidizing species to reach the Si-SiO₂ interface, they must go through consecutive steps:

1. They are transported from the bulk of the gas phase to the oxide-gas interface with the flux $F_1$,
2. They diffuse across the growing oxide layer toward the silicon substrate with the flux $F_2$, and
3. They react with the silicon atoms at the Si-SiO₂ interface with the flux $F_3$ [20].

Two growth laws can be obtained by assuming steady-state conditions (no build-up or depletion of oxidizing species) so that $F=F_1=F_2=F_3$. For long time oxidation (parabolic growth law), the thickness of the growing oxide, $d$, is defined as:

$$d^2 = Bt$$

(4.14)

where

$$B = \frac{2Dc^*}{N_1},$$

(4.15)
with $B$ referred to as the parabolic rate constant and $t$ is the oxidation time, $D$ is the diffusion coefficient of the oxidizing species in the oxide (Flux $F_2$), $C^*$ is the equilibrium concentration in the bulk of the oxide, and $N_1$ is the number of oxygen molecules incorporated into a unit volume of oxide ($2.2 \times 10^{22}$ for dry $O_2$ oxidation). On the other hand, for short oxidation times, the growth law is known as the linear growth law. The details on the derivation of the two relationships can be found in Appendix I.

![Figure 4.16. Basic model for thermal oxidation of silicon](image_url)

The formation of the interfacial $SiO_2$ layer with annealed $Gd_2O_3$ films can be best explained by the parabolic growth law. The parabolic rate constant, $B$, is proportional to the diffusion constant, $D$, of the oxidizing species through the existing oxide, or $Gd_2O_3$ oxide. This implies that the oxide growth in the parabolic regime is diffusion-controlled process. In other words, as the $Gd_2O_3$ oxide layer gets thicker, the oxidizing species must diffuse through a larger distance to arrive at the $Si/SiO_2$ interface. The reaction (flux $F_3$) of silicon atoms to form $SiO_2$ thus becomes limited by the rate at which the oxidizing species diffuses through the $Gd_2O_3$ oxide layer. This explains the absence of the complicated 3-layer structure with $SiO_2$ oxide at the interface for $Gd_2O_3$ film thickness $\geq 230\AA$ as observed in Auger analysis on the thick films. The diffusion coefficient, $D$, in flux $F_2$ is temperature dependent and is defined as:

$$D = D_0 \exp\left(-\frac{Q}{RT}\right)$$

(4.16)
where $D_0$ is a constant with units cm$^2$/s, $Q$ is the activation energy in J/mol for the diffusion process, $R$ is the gas constant equal to 8.314 J/mol-K, and $T$ is the oxidation temperature. The higher the oxidation temperature, the greater the diffusion coefficient, the more ease of the oxidizing species to diffuse through the Gd$_2$O$_3$ film to react with silicon substrate. Temperature dependence of the diffusion coefficient and thickness dependence of the ease of oxidizing O$_2$ molecules to reach at the Si/SiO$_2$ interface can explain the experimental fact that the interfacial SiO$_2$ layer grows at a rate dependent on temperature and the thickness of the Gd$_2$O$_3$ layer during oxygen annealing of the film.

4.1.7. Gd$_2$O$_3$ Film Roughness by AFM (atomic force microscopy) Analysis

*Figure 4.17* shows the AFM image on one of the Gd$_2$O$_3$ films (ISP962) deposited at ambient temperature without oxygen flow during the deposition. The instrument (AFM) was operated under tapping mode, and the basic fundamentals on how an AFM works can be found in Ref. [21], and will not be described here. The as-deposited film was quite smooth (RMS roughness = 0.18nm) without any pinholes or island growth detected. In addition, the smoothness of the films improved with annealing temperature in oxygen. The improvement in smoothness with annealing temperature can be explained by the fact that annealing Gd$_2$O$_3$ films in oxygen results in more dense films.

![AFM Image](image-url)

*Figure 4.17.* AFM image of Gd$_2$O$_3$ film (ISP962) deposited at ambient temperature.
4.2. Electrical Properties of Gd$_2$O$_3$ Films

In order to conduct the electrical measurements, Al gate capacitors were made by evaporating aluminum through a shadow mask. The back contacts (or ohmic contact) were made with In-Ga eutectic. The area of the capacitors, $-5 \times 10^{-4}$ cm$^2$, was measured to an accuracy of $\pm 2\%$ with a calibrated digitizing camera. Electrical measurements were conducted by probing the Al gates in a probe-station attached to two instruments, a multi-frequency LCR meter (HP Model 4275A), and a picoammeter/DC voltage source (HP Model 4140B) with the back contact grounded. The cross section of the MOS capacitor is shown in Figure 4.18. To measure capacitance as a function of gate bias in steady state, a small alternating component of voltage or ac voltage is superimposed on the gate bias as shown in Figure 4.19 [22]. The steady state here means the macroscopic parameters of a system are either time independent or varying sinusoidally in time with time independent amplitudes. Quasi-static CV measurements were made by ramping the voltage source of the picoammeter from inversion to accumulation (gate from $-ve$ to $+ve$ for n-type substrate) at a rate of 100 mV/s. High frequency CV measurements were made by stepping with 0.1 V steps each second, first from $-ve$ to $+ve$ and then $+ve$ to $-ve$ to look for hysteresis. IV characteristics were obtained with the picoammeter by stepping the voltage source from 0 volts in a positive direction (towards accumulation) until breakdown, which was characterized by a steep rise to currents above $10^{-2}$ A.

![Figure 4.18. Cross section of a MOS capacitor [22].](image)
Figure 4.19. Small ac voltage of amplitude $a$ superposed on the gate bias applied to the terminals of the MOS capacitor to measure its capacitance or admittance as a function of gate bias [22].

4.2.1. Dielectric Constant of Gd$_2$O$_3$ Films

The four general types of charges associated with the insulating oxide-Si system are fixed oxide charge, mobile oxide charge, oxide trapped charge, and interface trapped charge. The most popular method to measure the various charges is the capacitance-voltage (CV) measurement. The capacitance is defined as a change in charge due to a change of voltage. During a capacitance measurement, a small-signal ac voltage is applied to the device along with the gate bias. The resulting charge variation gives rise to the capacitance. For a MOS capacitor, the total capacitance can be represented as follow:

$$C = \frac{1}{\frac{1}{C_\text{ox}} + \frac{1}{C_s + C_\text{it}}}$$

(4.17)

where $C_{\text{ox}}$ is the oxide capacitance, $C_s$ is the semiconductor capacitance, and $C_{\text{it}}$ is the interface capacitance. For an n-type silicon substrate under positive gate bias, the silicon surface is heavily accumulated with electrons. Electron charge dominates on the silicon surface giving a very large value in $C_s$. This leads to $1/C_s+C_{\text{it}}$ to approach zero.
Excluding the effect of series resistance, the equivalent circuit of the MOS capacitor under strong accumulation will thus be $C_{ox}$. Since $C_{ox} = \text{dielectric constant/ thickness of the oxide}$, knowing the thickness of the oxide film, the dielectric constant ($K$) of the insulating oxide can be determined under strong accumulation as:

$$K = \left( \frac{C_{ox}}{A} \right) \left( \frac{d}{\varepsilon} \right)$$

where $A$ is the area of the capacitor, $d$ is the thickness of the oxide, and $\varepsilon_0$ is the permittivity of vacuum ($8.85 \times 10^{-12}$ F/m).

The dielectric constant of Gd$_2$O$_3$ was determined from a 23nm thick film (ISP960) deposited at ambient temperature without oxygen flow during the deposition. The thickness of the film was obtained by X-ray reflectivity measurements, whereas the strong accumulation capacitance was determined at 100kHz with +ve gate bias up to 3V at which the capacitance leveled off. The dielectric constant vs. annealing temperature for ISP960 is plotted in Figure 4.20, with samples annealed 10 minutes in oxygen. The value decreased slightly with annealing temperature, probably due to the formation of a thin interfacial layer of SiO$_2$ after annealing that has a lower dielectric constant of 3.9. Nevertheless, the dielectric constant stays roughly at 16 for the as-deposited film and annealed films. In a contrary, the dielectric constants of a thinner film with thickness of 10nm (ISP974) decrease significantly with annealing temperature as shown in Figure 4.21. This can be explained by the fact that thinner films result in thicker interfacial SiO$_2$ layer after annealing by the mechanisms described above. Since the dielectric constant of SiO$_2$ is 3.9, the total dielectric constant of the film will decrease with thicker SiO$_2$ layer at the interface.
Figure 4.20. Dielectric constant of a 23nm thick (ISP960) Gd$_2$O$_3$ film as-deposited and annealed in oxygen for 10 min at 500, 700, 780°C.

Figure 4.21. Dielectric constant of a 10nm thick (ISP974) Gd$_2$O$_3$ film as-deposited and annealed in oxygen for 10 min at 500, 700, 780°C.
4.2.2. C-V Characteristics of Gd_2O_3 Films

The CV characteristics of films deposited under different conditions will be discussed. The effect of substrate temperature and background oxygen pressure on the CV characteristics of Gd_2O_3 films will be investigated. Figure 4.22 shows the CV characteristics for sample ISP971 deposited at 500°C with an oxygen pressure of 2x10^{-5} Torr during the deposition given a 10-minute oxygen anneal at different temperatures. The as-deposited film was too leaky to obtain good CV characteristic and is not shown here. The best characteristic was obtained for the film annealed at 700°C since it possessed a larger quasi-static dip and a smaller lateral shift as a function of frequency, both indicative of lower interface state density. Films with post oxidation anneal (POA) at 700°C will be used as a reference to compare the effect of change in deposition condition on CV characteristics. Figure 4.23 shows the CV characteristics of films deposited at ambient temperature (ISP962) and at 500°C (ISP972) both without oxygen flow during the deposition and given a POA at 700°C. The film deposited at ambient temperature was too leaky to measure the quasi-static CV, whereas the film deposited at 500°C showed a dip in the quasi-static CV. This implies that depositing films with substrate temperature at 500°C improves the electrical properties of the Gd_2O_3 films. Nevertheless, a counterclockwise hysteresis of 0.1-0.2 V was observed for both films, indicative of charge trapping. Oxide traps, which are associated with defects in the oxide such as impurities and broken bonds, can cause a voltage shift of the MOS C-V curve. The oxide traps are usually electrically neutral, and are charged by introducing electrons and holes into the oxide [23]. The introduction of electrons and holes can be cause by the high electric field applied across an oxide layer by tunneling [24].

The best CV characteristics for any films produced so far were obtained for films deposited at room temperature with low background pressure (ISP1003). The Gd_2O_3 rod source was degassed for one hour before deposition to get rid of the residual oxygen (or water) in the target. Figure 4.24 shows the CV characteristics for film ISP1003 after annealing in oxygen for 10 min at 700°C. The characteristics have the smallest lateral shift as a function of frequency and the largest quasi-static dip, indicative of the lowest interface state density of any films produced so far. The characteristics do not
Figure 4.22. CV characteristics for sample ISP971 (8nm) deposited at 500°C with oxygen pressure of $2 \times 10^{-5}$ Torr during the deposition. The films were annealed in oxygen for 10 min. The as-deposited film was too leaky to obtain good CV characteristic and is not shown here.
Figure 4.23. CV characteristics of films deposited at ambient temperature (ISP962 ~10nm) and at 500°C (ISP972 ~80nm) both without oxygen flow during the deposition and given a POA at 700°C.

Figure 4.24. CV characteristics of ISP1003 (~8nm) annealed for 10 min in oxygen at 700 °C: (---) quasistatic, (---) 100 kHz, (-----) 1 MHz.
superimpose perfectly in accumulation because of leakage contributions to the quasi-static curve. The apparent dispersion in accumulation between 100kHz and 1MHz curves may be caused, at least in part, by the effect of probe inductance at higher frequencies. A small counterclockwise hysteresis of \( \sim 50 \text{mV} \) was observed between forward and reverse voltage scans. In a comparison to films deposited without degassing the Gd\(_2\)O\(_3\) rod source prior to deposition, the hysteresis reduces significantly for films deposited under low background pressure. This can be due to the fact that films deposited from degassed rod result in more dense films and thus less impurities and broken bonds attribute to oxide trap charges. Attempts to anneal the film in forming gas (4% hydrogen and 96% nitrogen) at 400°C after metal deposition to reduce the dangling bonds at the interface was prevented by the strong reaction between the aluminum and the gadolinium oxide. Thus, no accurate measurements could be performed on hydrogen-annealed samples.

### 4.2.3. Extraction of Interfacial SiO\(_2\) Layer Thickness from Capacitance

X-ray reflectivity measurements were used to determine the thickness of the top two layers, \( t_2 \) and \( t_3 \), for a 125Å thick film (ISP971) deposited at 500°C with an oxygen pressure of \( 2 \times 10^{-5} \) Torr. Assuming the two layers have the same dielectric constant, \( K_{Gd_2O_3} = 16.0 \), an estimate of the thickness of the SiO\(_2\) interface layer, \( t_{ox} \), can be obtained using the series capacitance model as indicated in Figure 4.25, so that

\[
\frac{1}{C_{total}} = \frac{1}{C_{SiO_2}} + \frac{1}{C_{Gd_2O_3}}
\]

(4.19)

and since

\[
\frac{C}{A} = \frac{\epsilon_O K}{t_{ox}},
\]

(4.20)

therefore

\[
\frac{1}{C_{total}} = \frac{t_{SiO_2}}{A\epsilon_O K_{SiO_2}} + \frac{t_{Gd_2O_3}}{A\epsilon_O K_{Gd_2O_3}}
\]

(4.21)

where \( \epsilon_O \) is the permittivity of vacuum, \( C \) is the measured capacitance in strong accumulation, \( A \) is the area of the capacitor, and \( K_{SiO_2} = 3.9 \) is the dielectric constant of silicon dioxide. The results of this analysis on film ISP971 (125Å) and a similar analysis...
on ISP972 (80Å) are shown in Figure 4.26 as a function of annealing temperature. The interfacial SiO₂ layer thickness increases with annealing temperature, and the two data points at 780°C happen to be lower because the films were annealed at 780°C for 2 minutes in oxygen instead of 10 minutes. Furthermore, the SiO₂ layer thickness obtained from the CV analysis appears to be thicker for thinner films, consistent with the hypothesis that the thinner film results in greater diffusion of oxygen through the film during annealing. The average dielectric constants, \( K \), were calculated using the total capacitance and thickness obtained from the reflectivity measurements and are shown in brackets above the data points in Figure 4.26. For sample ISP972, the 80Å thick film, the results can be compared with the estimate of the SiO₂ layer thickness obtained from the TEM analysis. As shown in Table 4.5, the thickness obtained from the CV analysis is slightly larger. The discrepancy between the SiO₂ layer thickness determined from the CV analysis and the TEM measurement is probably a result of the crude assumption that layers 2 and 3 have the same dielectric constant of 16.0.

**Dielectric Stacks**

![Diagram showing series capacitance model of a stack dielectrics consisting of SiO₂ and Gd₂O₃.](image)

**Figure 4.25.** Series capacitance model of a stack dielectrics consisting of SiO₂ and Gd₂O₃.
Figure 4.26. Estimate of the thickness of the SiO$_2$ interface layer from CV analysis for ISP971 (12.5nm) and ISP972 (8nm) films annealed in O$_2$. The anneals at 500 and 700°C were for 10 min and the anneal at 780°C was for 2 min.

Table 4.5. Comparison of interfacial SiO$_2$ layer thickness obtained from CV analysis and TEM micrographs for sample ISP972 (8nm thick).

<table>
<thead>
<tr>
<th>Sample ISP972 Condition</th>
<th>SiO$_2$ thickness from CV</th>
<th>SiO$_2$ thickness from TEM</th>
</tr>
</thead>
<tbody>
<tr>
<td>annealed at 500°C in O$_2$ for 10 min</td>
<td>20</td>
<td>15</td>
</tr>
<tr>
<td>annealed at 700°C in O$_2$ for 10 min</td>
<td>27</td>
<td>23</td>
</tr>
</tbody>
</table>
4.2.4. I-V Characteristics of Gd$_2$O$_3$ Films Annealed in Oxygen

*Figure 4.27* shows the current density through the 125Å thick film (ISP971) by applying the gate bias from 0 volts in a positive direction towards accumulation until breakdown. The as-deposited film is leaky but a 10-minute anneal in O$_2$ at 500°C resulted in a dramatic improvement, despite the fact that the film was deposited at 500°C with oxygen flow of $2 \times 10^{-5}$ Torr. The results were similar for films annealed at 700°C or 780°C for 10 minutes in oxygen. The breakdown voltage is characterized by a steep rise in the current density, and is $+6.2$V for film annealed at 500°C and $+7.2$V for films annealed at 700 and 780°C. It is worth noting that the breakdown voltage for the films annealed at 700°C in *Figure 4.27* occurs at potentials that correspond to a field in the SiO$_2$ interface layer of $-17$MV/cm. The detail calculation for the breakdown electric field of the interfacial SiO$_2$ layer is carried out in Appendix II. In comparison to the breakdown electric field for a 39Å thick SiO$_2$ of 15MV/cm [25], the electric field of the parasitic SiO$_2$ layer with thickness of 20Å at breakdown is remarkably high.

![J-V characteristic for a 12.5nm thick film (ISP971) annealed in O$_2$ for 10 min.](image-url)
The J-V characteristics possess two distinct slopes at low and high electric field, implying different mechanisms. The equations of leakage current density \( J \) as a function of electric field \( \xi \) for ohmic and ionic hopping conduction mechanisms [23] are:

\[
J \sim \xi \exp\left(-\Delta E_{ae} / kT\right) \quad \text{Ohmic} \tag{4.22}
\]

and

\[
J \sim \frac{\xi}{T} \exp\left(-\Delta E_{ai} / kT\right) \quad \text{Ionic hopping} \tag{4.23}
\]

where \( \Delta E_{ae} \) is the activation energy of electrons, \( \Delta E_{ai} \) is the activation energy of ions, \( T \) is temperature, and \( k \) is the Boltzmann's constant equal to \( 8.62 \times 10^{-5} \) eV/K. The leaky current density is linearly proportional to the electric field for both ohmic and ionic hopping conduction mechanisms. It is observed for all the annealed films, the IV characteristics are linear below 2V, characteristic of an ohmic or ionic hopping conduction mechanism. However, at higher voltages, attempts to fit the characteristics to either Frenkel-Poole (FP) or Fowler-Nordheim (FN) expressions [26] were complicated by the layered structure of the films and did not lead to meaningful conclusions. The energy-band diagrams for Frenkel-Poole (FP) and Fowler-Nordheim (FN) leakage current mechanisms are shown in Figure 4.28 and 4.29, respectively, with their current density equations. For Fowler-Nordheim tunneling, electrons tunnel into the conduction band of the oxide layer through a triangular energy barrier, whereas Frenkel-Poole emission is associated with trap-assisted tunneling in thin SiO₂ and high-permittivity gate dielectric stacks. The latter is more likely to be the dominant leakage current mechanism at higher electric field for the gate dielectric stacks consisting of SiO₂/Gd₂O₃ films.
Frenkel-Poole Conduction

Frenkel-Poole emission: \( J \sim \varepsilon \exp \left[ -\frac{q(\phi_B - \sqrt{q \varepsilon / \pi \varepsilon_s})}{kT} \right] \)

Figure 4.28. Energy-band diagram for the Frenkel-Poole (FP) emission.

Fowler-Nordheim Tunneling

\[
J_{FN} = \frac{q^3 \varepsilon_{ox}^2}{16\pi^2 \hbar \phi_{ox}} \exp \left( -\frac{4\sqrt{2m^* \phi_{ox}^3 / \hbar}}{3 \hbar q \varepsilon_{ox}} \right).
\]

Figure 4.29. Energy-band diagram for the Fowler-Nordheim (FN) tunneling.
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CHAPTER 5. CONCLUSIONS

Gd$_2$O$_3$ oxide layers were successfully deposited on Si(001) substrates using a rod-fed e-beam source with pressed powder Gd$_2$O$_3$ targets. The stoichiometry of the Gd$_2$O$_3$ films has been confirmed by in-situ XPS measurements with a small deviation due to the hygroscopic property (water accumulated on the top surface) of Gd$_2$O$_3$ films. The stoichiometry of Gd$_2$O$_3$ film does not change with film thickness $\geq$ 23nm after post-oxidation anneals with an RTP system in oxygen up to 780°C, as observed by Auger depth profiling on the thick films.

However, for Gd$_2$O$_3$ films $\lesssim$ 10nm thick, rapid thermal annealing produces a complicated multilayer structure. Transmission electron microscopy (TEM) and Auger depth profiling on thin films show the existence of an interfacial layer, most probably SiO$_2$, that grows during oxygen annealing at a rate dependent on temperature and thickness of the gadolinium oxide layer. From TEM analysis and X-ray diffraction measurements, the top layer of the film is polycrystalline Gd$_2$O$_3$ as-deposited and an increase in the polycrystalline grain size occurs on annealing. In addition, the Auger depth profiling and TEM analysis show that there is an intermediate layer between the surface Gd$_2$O$_3$ and interfacial SiO$_2$ layers after oxygen annealing in RTP system. X-ray reflectivity measurements have been successfully modeled by assuming the intermediate layer is a mixture of SiO$_2$ and Gd$_2$O$_3$. The intermediate “silicate” layer appears to be amorphous in the TEM micrographs and may be a mixture of the known silicate phases Gd$_2$Si$_2$O$_7$ and Gd$_2$SiO$_5$. The conversion of Gd$_2$O$_3$ to either of these silicates requires reaction with oxygen and silicon (the addition of either 2SiO$_2$ or SiO$_2$, respectively). From the initial reaction studied in In-situ XPS Analysis section 4.1.3, the gadolinium oxide reacts with the silicon substrate probably to form gadolinium silicate at the interface when the films were annealed in-situ under UHV condition. When the films were moved out from the In-situ Processing (ISP) system and annealed in oxygen with the rapid thermal annealing system, oxygen molecules diffuse through the films to form SiO$_2$ at the interface.
The dielectric constant of thick films as-deposited has been determined to be 16.0 ± 0.3, and is not significantly affected by oxygen annealing of the films. For thin films, the dielectric constant decreases with annealing due to the increase in thickness of a SiO$_2$ layer that has a lower dielectric constant of 3.9. With films produced so far, the best CV characteristics were observed for films deposited at room temperature with low background pressure achieved by degassing the Gd$_2$O$_3$ rod source prior to deposition. However, it is observed that depositing Gd$_2$O$_3$ films with substrates heated to 500°C improves the electrical properties by producing less leaky films. More work has to be done in order to improve the electrical property of Gd$_2$O$_3$ films deposited on Si(001) substrates by depositing films with substrate temperature held at 500°C with a degassed rod source. IV measurements show that annealing Gd$_2$O$_3$ films in oxygen at temperatures ≥ 500°C is required to reduce current leakage. Furthermore, CV and IV measurements show that the SiO$_2$ layer next to the Si substrate has excellent electrical characteristics after annealing in oxygen at 700°C or 780°C. The breakdown in the films occurs at applied voltages that correspond to fields in the SiO$_2$ barrier layer ≥ 15MV/cm. More work needs to be done to explain the detailed shape of the IV characteristics of the two (or three) layer structures.

Since it is difficult to eliminate the interfacial SiO$_2$ layer by manipulating the growth conditions, it is suggested that a very thin buffer layer (few monolayers) such as oxynitrides or silicon nitrides should be deposited on Si(001) substrates prior to the deposition of Gd$_2$O$_3$ films to act as a barrier in order to prevent reaction of gadolinium oxide and the silicon substrate and to improve the electrical properties of future gate dielectrics of Gd$_2$O$_3$. 
Appendix I

Silicon Oxidation Kinetics (Linear-Parabolic Model)

The model assumes that the oxidation process that occurs as a result of two fluxes ($F_1$ and $F_2$ as defined in the Growth Kinetics of Parasitic $SiO_2$ Layer section) that sequentially transport the oxidizing species from the gas to the $Si/SiO_2$ interface, where a third flux ($F_3$) is involved in the consumption of the oxidant by the reaction with the silicon. In steady-state condition (no build-up or depletion of oxidizing species), the three fluxes will be equal, i.e. $F=F_1=F_2=F_3$. The model continues by approximating each of these fluxes as they relate to physical quantities.

The oxidizing species are brought from the bulk of the gas stream to the wafer surface by a mass-transport process. $F_1$ occurs as a result of this transport, and is assumed to arise from the concentration difference between the oxidizing species in the bulk of the gas, $C_g$, and that at the oxide surface, $C_s$ [1]. $F_1$ is postulated to be linearly proportional to the concentration difference by the proportionality constant, $h_g$, which is defined as the mass-transfer coefficient, or:

$$F_1 = h_g (C_g - C_s).$$

(1)

To relate the equilibrium oxidizing species concentration in the oxide to that in the gas phase, we invoke Henry's law, which states that the concentration of a species dissolved in a solid at equilibrium is proportional to the partial pressure of the species at the solid surface, thus

$$C_o = H P_z$$

(2)

and

$$C^* = HP_g$$

(3)

where $C_o$ is the equilibrium concentration in the oxide at the outer surface, $C^*$ is the equilibrium bulk concentration in the oxide that would be in equilibrium with the bulk of the gas, $P_z$ is the partial pressure in the gas adjacent to the oxide surface, $P_g$ is the partial
pressure in the bulk of the gas, and $H$ is Henry's constant. Using Henry's law along with the ideal gas law, we get

$$F_1 = h(C^* - C_o)$$  \hspace{1cm} (4)$$

where $h$ is the gas-phase mass-transfer coefficient in terms of concentration in the solid given by $h = h_g / HkT$. Invoking Henry's law for this process implies that the oxidizing species moves through the oxide in molecular form, since the law does not hold under conditions of molecular dissociation.

Once inside the oxide layer the oxidants diffuse towards the Si/SiO$_2$ interface by the second flux $F_2$, which can be expressed under steady state as:

$$F_2 = D \frac{(C_o - C_i)}{d}$$  \hspace{1cm} (5)$$

in analogy with Fick's law, where $D$ is the diffusion coefficient of the oxidizing species in the oxide, $C_i$ is the oxidizing species concentration in the oxide adjacent to the oxide-silicon interface, and $d$ is the oxide thickness. Assuming that the flux corresponding to the Si-SiO$_2$ interface reaction is proportional to $C_i$,

$$F_3 = k_i C_i$$  \hspace{1cm} (6)$$

where $k_i$ is the rate constant of chemical surface reaction for silicon oxidation.

By setting $F_1 = F_2 = F_3$ for the steady state conditions and solving simultaneous equations, expressions for $C_i$ and $C_o$ can be obtained. Two limiting cases arise when the diffusivity is either very small or very large. When the diffusivity is very small, $C_i \to 0$ and $C_o \to C^*$, it is called the diffusion-controlled case, in which the flux of oxidant through the oxide ($F_2$) is small (due to $D$ being small) as compared to the flux corresponding to the Si-SiO$_2$ interface reaction ($F_3$). The second case, where $D$ is large leading to $C_i = C_o$, is called the reaction-controlled case, because an abundant supply of oxidant is provided at the Si-SiO$_2$ interface.
In order to calculate the rate of oxide growth, we define \( N_1 \) as the number of oxidant molecules incorporated into a unit volume of the oxide layer and is equal to \( 2.2 \times 10^{22} \text{ cm}^3 \) for dry oxygen. Combining various equations and assuming that an oxide may be present initially from a previous processing step or may grow before the assumptions in the model are valid, that is, \( d = d_i \) at \( t = 0 \), the following equation can be obtained:

\[
\frac{d}{A/2} = \left[ 1 + \frac{t + \tau}{A^2 / 4B} \right]^{1/2} - 1
\]  

(8)

One limiting case occurs for long oxidation times when \( t \gg \tau \) and \( t \gg A^2/4B \).

\[
d^2 = Bt \quad \text{(parabolic law)}
\]

(9)

Equation (9) is the parabolic law where \( B \) is the parabolic rate constant. The other limiting case occurs for short oxidation times when \( (t + \tau) \ll A^2/4B \).

\[
d = \frac{B}{A} (t + \tau) \quad \text{(linear law)}
\]

(10)

Equation (10) is the linear law where \( B/A \) is the linear rate constant [2]. Furthermore, the parabolic law describes the diffusion-controlled case, whereas the linear law describes the reaction-controlled case.
References


Appendix II

Calculation of Breakdown Electric Field for the Parasitic SiO₂ Layer

In discussing dielectric materials, we usually talk about the polarization \( P \) of the material, which is defined as the dipole moment per unit volume. If the number of molecules per unit volume is \( N \), and if each has a moment \( p \), it follows that the polarization is given by

\[
P = Np,
\]

where we have assumed that all the molecule moments lie in the same direction. When a medium is polarized, its electromagnetic properties change, and is expressed through the well-known equation

\[
D = \varepsilon_o \xi + P,
\]

where \( D \) is the electric displacement vector, \( \varepsilon_o \) the permittivity in vacuum, and \( \xi \) the electric field in the medium.

It is also well known that the displacement vector \( D \) depends only on the external sources producing the external field, and is completely unaffected by the polarization of the medium. Equation (2) is usually rewritten in the form

\[
D = \varepsilon \xi = \varepsilon_o K \xi,
\]

where the relative dielectric constant

\[
K = \varepsilon / \varepsilon_o \ [1].
\]

Therefore, for the two stacked dielectrics consisting of SiO₂ and Gd₂O₃, \( D_{ax} = D_{Gd₂O₃} \), that is

\[
\varepsilon_o K_{ax} \xi_{ax} = \varepsilon_o K_{Gd₂O₃} \xi_{Gd₂O₃}.
\]

Since \( \xi = V/d \), where \( V \) is the voltage across the dielectric stacks and \( d \) is the thickness of the corresponding oxide, assuming the voltage across the SiO₂ layer is \( V_{ax} \), the voltage across the Gd₂O₃ film is then \( (V-V_{ax}) \), equation (5) reduces to

\[
K_{ax} \frac{V_{ax}}{d_{ax}} = K_{Gd₂O₃} \frac{V-V_{ax}}{d_{Gd₂O₃}}.
\]

\[
K_{ax} \frac{V_{ax}}{d_{ax}} = K_{Gd₂O₃} \frac{V-V_{ax}}{d_{Gd₂O₃}}.
\]
Rearranging equation (7), we get

\[ V_{ox} \left( \frac{K_{ox}}{d_{ox}} + \frac{K_{Gd2O3}}{d_{Gd2O3}} \right) = \frac{K_{Gd2O3}}{d_{Gd2O3}} V, \]  

(7)

and if we divide both sides by \( d_{ox} \), then we have

\[ \frac{V_{ox}}{d_{ox}} \left( \frac{K_{ox}}{d_{ox}} + \frac{K_{Gd2O3}}{d_{Gd2O3}} \right) = \frac{K_{Gd2O3}}{d_{Gd2O3}} \frac{V}{d_{ox}}, \]  

(8)

thus the breakdown electric field in SiO₂ interface layer is then

\[ \frac{V_{ox}}{d_{ox}} = \frac{K_{Gd2O3}}{d_{Gd2O3}} \frac{V}{d_{ox}} \left( \frac{K_{ox}}{d_{ox}} + \frac{K_{Gd2O3}}{d_{Gd2O3}} \right). \]  

(9)

The thickness of the interfacial SiO₂ layer is determined to be 20.5Å from the capacitance method for ISP971 annealed at 700°C in oxygen for 10 minutes, whereas the thickness of the Gd₂O₃ layer is 125Å - 20.5Å = 104.5Å. Taking the breakdown voltage at 7.2V and dielectric constants for SiO₂ and Gd₂O₃ layers to be 3.9 and 16, respectively, the electric field for the SiO₂ interface layer at breakdown is determined to be ~17MV/cm using equation (9).

Reference