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UMI
5-V ONLY ZENER BASED FLASH E²PROM ARCHITECTURE AND PERIPHERAL CIRCUITS

by

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A thesis submitted in conformity with the requirements for a Degree of Master of Applied Science
Graduate Department of Electrical and Computer Engineering
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Master of Applied Science, 1995
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ABSTRACT

The objective of this thesis is to present the architecture and peripheral circuits suitable for the implementation of a 5V only ZE²PROM memory. First, the development of a large signal model of the cell for circuit simulations is presented. The proposed model is implemented as a subcircuit in the HSPICE simulator.

A novel “Shared Bit Line, Alternating Word Line” architecture is proposed to achieve high density for the memory. The peripheral circuits that can implement the read, program and erase modes of operations in this architecture are presented. High voltage issues in a low voltage process are addressed. The implementation of the positive and negative charge pump circuits that generate the required programming and erasing voltages using a 5V power supply are presented.
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# TABLE OF CONTENTS

## CHAPTER 1

**Introduction** ................................................................. 1

1.1 Review Of Flash E²PROM .................................................. 1
1.2 Flash Memory Architecture and Organization ....................... 4
1.3 Flash ZE²PROM Cell Structure .......................................... 7
1.4 Motivation and Outline of the Thesis .................................... 8

## CHAPTER 2

**Flash ZE²PROM Device Modeling** ..................................... 11

2.1 Introduction ........................................................................ 11
2.2 Cell Operation and Device Simulations ................................. 11
  2.2.1 Read Mode ............................................................. 11
  2.2.2 Program Mode ......................................................... 13
  2.2.3 Erase Mode ............................................................ 15
2.3 Equivalent Circuit Model .................................................... 16
2.4 Model Parameters ............................................................ 17
  2.4.1 Comparison of HSPICE and MEDICI Simulations ................ 18
2.5 Summary ........................................................................... 21

## CHAPTER 3

**ZE²PROM Architecture and Peripherals** ............................... 23

3.1 Introduction ........................................................................ 23
3.2 Architecture ........................................................................ 23
3.3 Memory Array ..................................................................... 25
3.4 Peripheral Functions ........................................................... 29
  3.4.1 Word Line Operation .................................................... 29
  3.4.2 Column Control Operation ............................................ 30
3.5 High Voltage Devices In BiCMOS Technology ....................... 32
  3.5.1 HSPICE Models for HVMOS Devices ............................... 34
 CHAPTER 4
Experimental High Voltage Building Blocks ........................................ 47
4.1 Introduction .................................................................................. 47
4.2 Implementation of High Voltage Devices ..................................... 47
4.3 Positive Charge Pump Circuits (PCP) .......................................... 51
4.4 Negative Charge Pump Circuits (NCP) ....................................... 59
4.5 Summary ...................................................................................... 63

 CHAPTER 5
Conclusions ....................................................................................... 65
5.1 Suggestions for Future Work ....................................................... 66

Appendix A
HSPICE Model of ZE²PROM Cell .................................................... 67

Appendix B
HSPICE Models of HV Devices ....................................................... 69

Appendix C
Vneg/Gnd Switch .............................................................................. 70

Appendix D
Isolated Diodes in BiCMOS and Improved NCP Circuit .................. 72
List of Figures

Chapter 1
Figure 1.1. ETOX cell structure .................................................................2
Figure 1.2. (a) Hot electron injection at the drain side during programming.
 (b) Removal of electrons from source side during erasure .....................3
Figure 1.3 Basic Flash E²PROM architecture and NOR array .......................5
Figure 1.4. Device structure and circuit symbol of ZE²PROM cell .................7

Chapter 2
Figure 2.1. Only the sense section of the ZE²PROM contributes to read operation...12
Figure 2.2. IV Characteristics of an unprogrammed cell obtained from MEDICI
 device simulations ................................................................................13
Figure 2.3. The hot electron generation occurs due to breakdown of the n⁺/p⁺
 junctions in active section during programming ........................................13
Figure 2.4. Hot Electron Injection current and threshold voltage shift during
 programming with \( V_{CG}=12V \) and \( V_S=V_D=4.7V \) ........................................14
Figure 2.5. The erase operation of the device ..............................................15
Figure 2.6. The tunneling current with \( V_{CG}=-15 \) and \( V_S=3V \) bias conditions and
 threshold voltage shift during erasing .......................................................16
Figure 2.7. A subcircuit representing the large signal model of the ZE²PROM ....17
Figure 2.8. Comparison of IV characteristics of the ZE²PROM obtained from
 MEDICI and HSPICE model .................................................................19
Figure 2.9. Breakdown characteristics of the p⁺/n⁺ junctions ........................19
Figure 2.10. Comparison of the threshold voltage shift of the ZE²PROM cell with the
 data obtained from MEDICI and HSPICE simulations: (a) During
 programming (b) During erasing .........................................................20

Chapter 3
Figure 3.1. A Flash ZE²PROM block diagram ..............................................24
Figure 3.2. ZE²PROM bitcell (a) Cell structure, (b) Cell layout ......................26
Figure 3.3. The circuit diagram and the corresponding layout of Array-A ..........27
Figure 3.4. The circuit diagram and the corresponding layout of Array-B ..........28
Figure 3.5. Word line control for program, read, erase and idle states .............30
Figure 3.6. Column control operation for read, program and erase states ..........31
Figure 3.7. The cross section of existing BiCMOS technology .......................32
Figure 3.8. The cross section of HVNMOS and its circuit symbol ...................33
Figure 3.9. The cross section of HVPMOS and its circuit symbol ........................................34
Figure 3.10. The simulated dc characteristics of HVMOS devices with HSPICE model
obtained by optimization of the low voltage model .................................................. 35
Figure 3.11. Program/Read switching circuit .................................................................. 36
Figure 3.12. HSPICE simulations showing Vpp and Vdd switching at the word line ..........37
Figure 3.13. Negative voltage connecting circuit and the HSPICE simulations ............... 38
Figure 3.14. Low voltage switches are used for bit line operation ................................. 39
Figure 3.15. Threshold voltage change of ZE2PROM cell for different current levels .... 40
Figure 3.16. Current source circuit to bias the source and the drain of ZE2PROM cell.
The Zener diodes model the Zener junctions at the source and the drain. .................. 41
Figure 3.17. HSPICE simulation showing the current through the zener junctions
during programming. The circuit is designed to supply 5μA per junction
resulting in 10μA per cell .............................................................................................. 41
Figure 3.18. Current sensing circuit for Flash ZE2PROM .............................................. 42
Figure 3.19. The input and the output of the inverter as a function of Icell when Iref is
45μA ............................................................................................................................ 43

Chapter 4
Figure 4.1. The rectangular layout of high voltage devices (a) HVNMOS and (b)
HVPMOS ....................................................................................................................... 48
Figure 4.2. The micrograph of a rectangular HVNMOS device ..................................... 49
Figure 4.3. Breakdown and IV Characteristics of HVNMOS when operating in
forward mode (W=40μm and L=3μm) .......................................................................... 49
Figure 4.4. Breakdown and IV Characteristics of HVPMOS when operating in
forward mode (W=260μm and L=3μm) ........................................................................ 50
Figure 4.5. Comparison of simulated and the experimental dc characteristics of
HV MOS devices with HSPICE model obtained by optimization the low voltage
........................................................................................................................................ 50
Figure 4.6. A typical n-stage voltage multiplier configuration ........................................ 52
Figure 4.7. PCP using diode connected HVNMOS devices .......................................... 53
Figure 4.8. HSPICE simulations of PCP circuit with different capacitive loads .......... 54
Figure 4.9. PCP with HVNMOS pass transistors and their feedback to provide gate
bias .................................................................................................................................... 54
Figure 4.10. HSPICE simulations of 2-stage PCP circuits ............................................. 55
Figure 4.11. Test set up for charge pump circuits .......................................................... 56
Figure 4.12. Comparison of simulated and experimental results for PCP circuit.
(Cl=5pF Clk=5MHz) .................................................................................................. 56
Appendix A

Figure A. 1. The ZE²PROM cell structure and the large signal model. ........................................67

Appendix C

Figure C. 1. The “Vneg/Gnd Switch” circuit .............................................................................70
Figure C. 2. HSPICE simulations showing Vneg and Gnd switching at the word line.71

Appendix D

Figure D. 1. The cross section and the layout of the BE-Diode ....................................................72
Figure D. 2. Micrograph of the BE-Diode ..................................................................................73
Figure D. 3. IV Characteristics of the BE-Diode ........................................................................73
Figure D. 4. Two device structures for isolated diodes in BiCMOS technology ......................74
Figure D. 5. The modified circuit diagram of NCP implemented with isolated diodes 75
List of Tables

Chapter 1
Table 1. 1 Flash ZE²PROM cell’s voltage requirements ...........................................8

Chapter 3
Table 3. 1 Flash ZE²PROM cell’s required voltages .............................................23
Table 3. 2 Comparison of the area per bitcell of two configurations. ..................29
Table 3. 3 Truth table for word line operation ......................................................29
Table 3. 4 Truth table for column control operation ............................................31

Chapter 4
Table 4. 1 The control gate current and equivalent capacitance of ZE²PROM cells .51
Table 4. 2 Simulated and measured rise times for PCP circuit with gate biased
     HVNMOS. ........................................................................................................57
Table 4. 3 Simulated and measured rise times for PCP with BJT diodes circuit. ......57
Table 4. 4 Simulated and measured fall times for NCP circuit. ...........................62
CHAPTER 1

INTRODUCTION

Read Only Memories (ROMs) are a major segment in the semiconductor memory market. Conventional mask programmable ROMs are nonvolatile and allow permanent storage of information [1]. However, they require special masks to define the stored information. Electrically Programmable Read Only Memories (EPROMs) can be programmed electrically but require UV light for erasure. Electrically Erasable Programmable Read Only Memories (E²PROMs) allow both electrical programming and erasing, but have low density due to large area memory cell.

The challenge for the semiconductor industry is to fabricate memory with electrical erasability, high density, good memory retention, high read/write speed and cycling capability. The development of Flash Memory is a response to these requirements [2].

Flash memories have received industry-wide attention since their appearance in the late 1980's. They are now available in densities up to 32M bits with random access times of 60ns [3]. Combined with complete nonvolatility, this capacity makes the chips a potential fit in many applications. Some of these applications include small capacity hard disk drives and memory cards for portable computers.

1.1 Review Of Flash E²PROM

Flash E²PROMs are derived from E²PROM. They are programmed a bit or a byte at a time and erased a block at a time. The “flash” designation comes from the ability to erase the entire memory array or sections of it at once. First generation flash memories use dual power supplies, typically 5V/12V. The second generation uses on-chip charge pump circuits to achieve 5V-only operation [4].
Most flash memories are programmed using hot-electron injection techniques and are electrically erased by tunneling. The E\(^2\)PROM's individual byte erasure is made possible by the addition of a second select transistor to each memory cell. By eliminating the select transistor flash erasure is obtained. Therefore, flash memories can be built in much higher densities than E\(^2\)PROM.

Different suppliers of flash memories have taken slightly different approaches to the cell design. The ETOX\(^TM\) (EPROM Tunnel Oxide)\(^1\) cell is the simplest and smallest. It employs a single field-effect transistor with a floating gate storage and is programmed and erased through different areas of the gate oxide [2]. The ETOX flash E\(^2\)PROM transistor resembles an ordinary MOS transistor, except for the addition of the floating gate, buried in the insulator between the substrate and the ordinary control gate as illustrated in Fig 1.1. Very high densities can be achieved with flash E\(^2\)PROM since the floating storage gate and the control gate are both stacked directly above the transistor channel.

![ETOX cell structure](image)

Figure 1.1. ETOX cell structure

---

1. ETOX is a trademark of Intel
The cell is programmed and erased by injecting and removing electrons from the floating gate. The charge stored in the floating gate alters the threshold voltage, $V_{TH}$, of the device as seen by the control gate. A programmed cell has a high $V_{TH}$ which is considered as a logic "0" state. An unprogrammed or an erased cell has a low $V_{TH}$ which represents a logic "1" state.

For programming, 12V is applied between the source and the control gate and approximately 6V between the source and the drain as illustrated in Fig. 1.2.(a). The source-drain voltage generates hot electrons in the channel. The high voltage on the control gate attracts the electrons across the thin tunneling gate oxide and results in their accumulation on the floating gate. The electrons accumulated shifts the threshold voltage of the cell, thus switching it from its "1" to its "0" state.

Electrical erasure of ETOX flash memory is accomplished by Fowler-Nordheim (FN) tunneling of the electrons from the floating gate. During this operation, the drain is left open and the control gate is grounded. Application of 12V to the source creates an electric field across the thin oxide between the floating gate and the source and pulls the electrons off the floating gate as illustrated in Fig 1.2.(b). When all the excess electrons are removed from the floating gate of the cell, the $V_{TH}$ returns to its initial value. This effectively changes the state of
the cell back to a logic "1". If more electrons are removed than were added, the threshold voltage can go below its intrinsic level. In the extreme case, this would result in a depletion mode transistor. When this ‘over-erasure’ occurs the cell always remains ‘on’.

To sense the content of the ETOX flash cell, supply-voltage levels are applied to the control gate and the drain of the cell while the source is grounded. In an erased cell, the control gate voltage is sufficient to overcome the transistor’s threshold voltage \( V_{TH} \) and a drain-to-source current is detected by the sense circuitry and is translated into a logic “1”. In a programmed cell, however, the transistor’s \( V_{TH} \) is high so that the applied voltage on the control gate is not sufficient to turn the cell on. The absence of current results in a logic “0” at the corresponding data output.

### 1.2 Flash Memory Architecture and Organization

A typical 5V-only Flash E\(^2\)PROM using the ETOX memory cell is shown in Fig. 1.3. The highlighted blocks involve high voltage levels. The memory array uses a NOR architecture [6].

Control circuitry makes the necessary connections to the memory array for read, program and erase operations. The control signals for the different modes of operation are output enable (\( OE \)) and write enable (\( WE \)). The control input chip enable (\( CE \)) selects the memory chip in the system.

In the read mode, the row and column decoders send low voltage signals to the control gate and the drains of all the cells connected to the selected word line and bit line respectively. The sense amplifier detects the state of the cell and data is transferred to the output. In the program mode, the cell to be programmed is selected in the array by simultaneously raising its control gate and its drain. The high voltage drivers provide the connection of high voltage pulses which are generated by charge pump circuits, to the word line when they are selected by the row decoder. Similarly, the bit line is raised to the necessary voltage. For block erasure, all the word lines are grounded and all the bit lines are raised to a high voltage in that particular block.
In flash E²PROM, the complete block is erased before new data is programmed. However, application of the erase pulse to the array will cause the cells in "1" state to lose more charge than originally stored, resulting in over-erasure. Preprogramming or preconditioning a block to "0"s puts an equal number of electrons on the
floating gate of each cell in the block before all are erased in parallel. This technique ensures uniform and dependable erasure and prevents over-erasure.

There are some limitations in ETOX technology. These are:

1) The channel hot electron injection method for programming requires biasing the drain of the device at a high drain voltage (6 to 8V) to generate hot electrons. This biasing condition results in high programming current (300–450μA/cell).

2) The charge pump or bootstrap circuits that generate these voltages from the 5V power supply will occupy large area due to the high current requirement during programming.

3) The high programming current limits the number of cells that can be programmed at one time.

4) The high current also increases the power consumption.

5) It has a slow programming time (~10μs).

6) During the erase operation, the high voltage (+12V) applied to the source terminal generates holes which get trapped in the gate oxide. These trapped holes cause threshold voltage degradation.

7) Improvements in programming time require shorter channel length (fine line photolithography) to enhance the hot electron injection.

8) Overerasure is controlled with preprogramming before erasing. The complete programming algorithm word by word is repeated before bulk erasure resulting in a long erase time of the memory.

In order to address some of the above problems, a new Flash E²PROM cell has been developed [8] and is being fabricated at University of Toronto. This new memory cell has different requirements than a conventional ETOX cell, therefore it needs a new architecture and peripheral circuitry. In addition, high density, low power consumption and availability of a 5V single power supply must be considered.
1.3 Flash ZE²PROM Cell Structure

In conventional flash E²PROM cells, a higher programming speed is achieved by using a scaled MOS technology with a reduced channel length and applying high drain voltages to obtain a higher electric field between source and drain regions.

In the ZE²PROM cell [8] designed and developed at The University of Toronto, high programming speed is achieved by using two zener junctions implemented by the addition of p⁺ regions on both sides of source and drain diffusions under the channel. The complete cell structure and the proposed circuit symbol is shown in Fig 1.4. The application of a positive voltage to both drain and source regions while the substrate is grounded, cause the zener junctions to breakdown. This generates a large number of electron-hole pairs. The electrons can be attracted to the floating gate by applying a high positive voltage to the control gate. The holes recombine in the substrate resulting in a substrate current flow.

![Device structure and circuit symbol of ZE²PROM cell](image)

Figure 1.4. Device structure and circuit symbol of ZE²PROM cell

The electrical erasure of the flash ZE²PROM is the same as a conventional source-gate erasure scheme where a positive voltage is applied at the source and a high negative voltage is applied at the gate. The high electric field from the
source to the control gate causes the electrons to tunnel out of the floating gate. One limitation due to the zener junctions is that the positive voltage at the source cannot exceed the zener breakdown voltage.

For the read operation of the flash ZE^2PROM cell, the conductivity of the cell determines the information stored in the cell. To obtain cell conductivity, a channel needs to be created by applying gate and drain voltages. Since the presence of the p^+ regions under the gate effectively terminates the conduction channel, the structure is merged with an ETOX cell to allow the current flow for read operation as illustrated in Fig 1.4. During read operation the bias voltage at the drain junction is kept below the zener breakdown voltage.

The voltage requirements of ZE^2PROM cell for different modes of operation are listed in Table 1.1. To achieve 5V-only operation, the ZE^2PROM memory must have on-chip voltage generators. The positive and negative high voltage levels can be generated using positive (PCP) and negative (NCP) charge pump circuits respectively. In addition, driver circuits that can handle the high voltages and control circuitry to switch the necessary voltage levels to the ZE^2PROM cell are also needed.

<table>
<thead>
<tr>
<th>Mode</th>
<th>Control Gate</th>
<th>Source</th>
<th>Drain</th>
</tr>
</thead>
<tbody>
<tr>
<td>Program</td>
<td>+12V</td>
<td>+5V</td>
<td>+5V</td>
</tr>
<tr>
<td>Erase</td>
<td>-15V</td>
<td>+3V</td>
<td>Float</td>
</tr>
<tr>
<td>Read</td>
<td>+5V</td>
<td>GND</td>
<td>+3V</td>
</tr>
</tbody>
</table>

### 1.4 Motivation and Outline of the Thesis

The objective of this thesis is to investigate the design of the peripheral circuitry required to implement a 5V-only Flash Memory using the novel ZE^2PROM cell, which is compatible with CMOS/BiCMOS technology.

Chapter 2 focuses on the development of an HSPICE model of the cell. This model is necessary for circuit simulations and design of the peripheral circuitry. The HSPICE model predictions are compared to those provided by a two dimensional device simulator.
Chapter 3 covers the design considerations of the ZE2PROM array to achieve a high density and low power dissipation. An architecture that optimizes the area occupied by the array and the peripheral circuitry that can implement the ZE2PROM cell’s read, write and erase modes of operation are proposed.

Chapter 4 includes the design and implementation of experimental building blocks that generate the high voltages using a conventional low voltage CMOS/BiCMOS process. These are the positive charge pump (PCP) and the negative charge pump (NCP) circuits. Different circuit configurations are described and experimental results are presented.

Conclusions and suggestions for future work are given in Chapter 5.
References


2.1 Introduction

The purpose of this chapter is to develop an equivalent model of the novel ZE²PROM cell suitable for circuit simulations. The availability of an accurate model is essential to the design and optimization of the peripheral circuits to achieve the required design specifications.

In this chapter, the development of a simple large signal model for a ZE²PROM cell suitable for HSPICE simulations will be described. Due to the unavailability of the experimental results at the time of this work, two dimensional device simulator results are used as guidelines [1]. The main purpose is to demonstrate the methodology of the model development so that it can be modified to fit experimental results.

2.2 Cell Operation and Device Simulations

The ZE²PROM cell structure consists of two parts, the active and the sense section (see Fig 1.4.). Each section contributes to the programming, erasing and reading operation differently. To model the device accurately, it is necessary to identify their behavior individually for three modes of operation. Therefore, the device structure and its behavior based on the simulation results obtained from a two dimensional device simulator must be considered.

2.2.1 Read Mode

In read mode, the ZE²PROM cell behaves like an ordinary transistor with a threshold voltage determined by the charge accumulated on the floating gate. The initial condition where a small amount of charge is present on the floating
gate corresponds to the unprogrammed or "1" state. When charge is accumulated on the floating gate, the cell is in the "0" state. The unprogrammed cell will turn on when the supply voltage is applied to the control gate and the read voltage level is applied at the drain. For a programmed cell the transistor will not turn on resulting in zero current flow.

Current flow occurs only in the sense section of the structure as illustrated in Fig 2.1. This current is detected in the read operation. The conductivity of an unprogrammed ZE²PROM cell can be observed from its IV characteristics. The IV characteristics of the sense section obtained using the two dimensional device simulator MEDICI¹ are illustrated in Fig 2.2. The control gate bias voltage ranges from 0V to 5V in 1V steps and the drain voltage is swept from 0 to 3V. The reason for the drain voltage limitation is the presence of the zener junctions at the drain with a 4.2V breakdown voltage.

![Diagram](image)

(W/2, L)

Figure 2.1 Only the sense section of the ZE²PROM contributes to the read operation.

---

¹. MEDICI, TMA Two Dimensional Device Simulator
Figure 2. 2. IV Characteristics of an unprogrammed cell obtained from MEDICI device simulations.

2.2.2 Program Mode

In program mode the active section of the device contributes to the programming as shown in Fig 2.3.

Figure 2. 3. The hot electron generation occurs due to breakdown of the n⁺/p⁺ junctions in the active section during programming.
To generate the electrons for programming, 5V are applied to the source and drain of the structure. With this bias condition, the n+/p+ junctions breakdown and a large number of electron-hole pairs are generated. By applying a high positive voltage at the control gate, the electrons are attracted to the floating gate and the holes flow in the substrate. This results in a hot electron injection \( I_{\text{HEI}} \) current to the floating gate and a substrate current. The electrons accumulated in the floating gate alter the threshold voltage of the device with respect to the control gate. The change in threshold voltage \( \Delta V_{\text{TH}} \) can be approximated by

\[
\Delta V_{\text{TH}} = -\frac{\Delta Q_{\text{FG}}}{C_{\text{FG}}}
\]  

where \( \Delta Q_{\text{FG}} \) is the change in the amount of the charge on the floating gate and \( C_{\text{FG}} \) is the floating gate capacitance. The hot electron current and the threshold voltage shift during programming are shown in Fig 2.4.

![Figure 2.4](image)

**Figure 2.4.** Hot Electron Injection current and threshold voltage shift during programming with \( V_{\text{CG}}=12\text{V} \) and \( V_S=V_D=4.7\text{V} \)

It is observed that the threshold voltage shift is a function of \( I_{\text{HEI}} \) which in turn is a function of the zener current, the control gate voltage and its duration.
In addition, the thickness of the interpoly and tunneling oxides are parameters that effect the programming time of the device.

2.2.3 Erase Mode

In the erase mode, the accumulated charges tunnel from the floating gate to the source junction of the device as shown in Fig 2.5. The voltage applied to the control gate and the source are -15V and 3V respectively while the drain is left open. The high electric field generated between the control gate and the source cause the electrons that are present in the floating gate to tunnel to the source of the device. This results in the Fowler Nordheim Tunneling current (I_{FNT}) and the reduction in the threshold voltage of the device.

![Diagram of erase mode](image)

Figure 2.5. The erase operation of the device.

The device simulations of the tunnelling current and the threshold voltage shift during erasing are shown in Fig 2.6. The erasing time is a function of the tunneling current which in turn depends on the control gate voltage pulse, the source voltage pulse and their durations, and the oxide thickness of the device.
2.3 Equivalent Circuit Model

The equivalent circuit model is implemented as a SPICE subcircuit with elements corresponding to the physical structure of the $\text{ZE}^2\text{PROM}$ cell. The basic structure of the device is represented by the capacitor, $C_{\text{FG}}$, and an NMOS transistor which are connected in series. They model the floating gate capacitor and the MOS transistor of the sense section respectively. The zener diodes model the $n^+/p^+$ junctions present in the active section. The current sources $I_{\text{HEI}}$ and $I_{\text{FNT}}$ represent the hot electron injection current and the tunneling current during programming and erasing respectively. The switches $S_1$ and $S_2$ are inserted to turn on the corresponding current sources for programming and erasing.

The proposed HSPICE subcircuit model of the $\text{ZE}^2\text{PROM}$ cell with the elements corresponding to its structure is illustrated in Fig 2.7.
To implement the subcircuit in HSPICE, it is necessary to obtain the model parameters of the elements.

The value of the capacitance $C_{FG}$ depends on the oxide thickness between the control gate and the floating gate, and the area of the device. Therefore, it can easily be modeled in HSPICE with the parameters interpoly oxide thickness $T_{ox2}$, the channel length $L$, and channel width $W$ respectively. Accordingly, the equivalent capacitance will be calculated by the simulator as

$$C_{FG} = \frac{e_{ox}}{T_{ox2}} (W \times L)$$  \hspace{1cm} (2.2)

The NMOS transistor can be modeled by the conventional HSPICE model. To get an accurate model for the NMOS transistor, the structure with a 100Å tunnel oxide was simulated in MEDICI. The zero bias threshold voltage $V_{TO}$ and transconductance parameter $K_P$ were extracted. The physical parameters such
as junction depth $X_J$, substrate doping concentration $NSUB$ and lateral diffusion length $LD$ were obtained from the device structure. The $VTO$ and $KP$ parameters of the NMOS transistor were optimized to fit the DC characteristics of the cell [2].

The zener junctions were modeled as diodes with a specified reverse breakdown voltage. The subcircuit elements obtained according to its physical structure models the device in a predetermined state, programmed or erased. To model the complete operation, the circuit must be modified to include the threshold voltage change of the device during programming and erasing. This is done by the addition of the current sources, $I_{HEI}$ and $I_{FNT}$ to charge or discharge the floating gate node and thus change the threshold of the structure with respect to the control gate.

The hot electron current, $I_{HEI}$ and tunneling current, $I_{FNT}$ were implemented as current sources with piece wise linear (PWL) functions to fit the data obtained from the device simulator's results. The current sources are activated with switches to perform programming and erasing respectively. The detailed listing of the model parameters are included in Appendix A.

2.4.1 Comparison of HSPICE and MEDICI Simulations

The complete subcircuit was simulated with HSPICE and its performance was compared with the MEDICI results.

The IV characteristics of the subcircuit were obtained with transient analysis. DC analysis was not possible due to the presence of the control gate capacitor. Therefore, pulse voltages of 0V, 1V, 2V, 3V, 4V and 5V were applied at the control gate while the drain voltage was ramped slowly from 0 to 3V for each gate voltage. The current values were printed for specified times when the transient analysis were performed. The comparison of the IV characteristics obtained from device simulations of the real structure and HSPICE simulations of its equivalent subcircuit is shown in Fig 2.8. It was observed that the simulation results were in agreement to MEDICI simulation results within 10%.

The comparison of the breakdown characteristics of the zener junctions are illustrated in Fig 2.9. The HSPICE simulation results are also within 10% compared to MEDICI results.
Figure 2.8. Comparison of IV characteristics of the ZE²PROM obtained from MEDICI and HSPICE model.

Figure 2.9. Breakdown characteristics of the p^+/n^+ junctions.
To observe the programming of the device, the hot electron current source was switched on and transient analysis was performed. The voltage levels at the floating gate were recorded for different time intervals. These values were used as the initial condition at the floating gate to extract the threshold voltage of the subcircuit with respect to the control gate. The threshold voltage was measured with a conventional 0.1V drain bias and a linear sweep at the control gate [2].

The same procedure was used for the erasing of the cell. Using the last floating gate voltage obtained from the programming simulations as the initial condition, the $I_{FNT}$ current source was switched on and a transient analysis was performed. The floating gate voltage levels were recorded and used to extract the threshold voltage of the circuit. The simulation results for threshold shift during programming and erasing are illustrated in Fig 2.10. HSPICE simulations showed threshold voltage deviation within 20% in a given time compared to MEDICI results.

![Figure 2.10](image.png)

*Figure 2.10. Comparison of the threshold voltage shift of the ZE$^2$PROM cell with the data obtained from MEDICI and HSPICE simulations: (a) During Programming (b) During Erasing.*
The proposed model gives good results for the complete ZE²PROM cell's behavior. The components used in the subcircuit correspond to the actual physical structure of the device. The model can be used for an accurate simulation of the memory peripherals.

2.5 Summary

In this chapter, a large signal model for the ZE²PROM cell suitable for circuit simulations was developed. The model was implemented in HSPICE as a subcircuit corresponding to the cell's physical structure. It has been shown that the model is in good agreement with the device simulator's large signal characteristics. The methodology used to develop the model was presented. This methodology can be used to extract the parameters from the experimental results as well. The proposed model includes the threshold voltage shift of the device during programming and erasing. The proposed model is used for HSPICE simulations of the peripheral building blocks, which will be described in the next chapter.
References


CHAPTER 3

ZE2PROM ARCHITECTURE AND PERIPHERALS

3.1 Introduction

The purpose of this chapter is to demonstrate the feasibility of a memory using the ZE2PROM cell. First, an architecture that can implement the different modes of operation is considered. An array to achieve high density is proposed. The circuits that can implement some of the building blocks are included. The objective is to demonstrate the functionality of the circuits. They must be optimized according to the required specifications.

3.2 Architecture

A system that implements a 5V-only ZE2PROM memory taking into account the cell’s voltage requirements as listed in Table 3.1 is considered. There are four states of operation for a ZE2PROM bitcell. For programming a cell, "0" data is written in the selected cell by altering its threshold voltage to a high value. All the data in a block or a complete array is erased when a change in data is required. This is done by applying the required voltage levels to all the cells in a selected block to reduce their threshold voltages to a low value.

Table 3.1 Flash ZE2PROM cell's required voltages.

<table>
<thead>
<tr>
<th>Mode</th>
<th>Control Gate</th>
<th>Source</th>
<th>Drain</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read</td>
<td>+5V</td>
<td>GND</td>
<td>+3V</td>
</tr>
<tr>
<td>Idle</td>
<td>GND</td>
<td>Float</td>
<td>Float</td>
</tr>
<tr>
<td>Erase</td>
<td>-15V</td>
<td>+3V</td>
<td>Float</td>
</tr>
<tr>
<td>Program</td>
<td>+12V</td>
<td>+5V</td>
<td>+5V</td>
</tr>
</tbody>
</table>
resulting in a "1" state. During read operation the conductivity of the cell in a particular word line and bit line determines the data stored in it. This data is transferred to the output through the bit lines. The idle state is referred to as the state of the cell when it is not selected. The block diagram of a ZE²PROM memory of $2^n \times 2^n$ bits is illustrated in Fig 3.1.

![Block Diagram](image)

**Figure 3.1** A Flash ZE²PROM block diagram

Row and column address inputs and decoders select the correct bit in the memory array. The control circuit generates the logic for different modes of operations.
under the control of two signals PRGM (program) and READ (read). Since there are four states of operation, two control signals are sufficient to implement the logic. There is also a CE (chip enable) control signal which selects the memory chip in the system, however for simplicity it is not included in the design.

The 'Word Line Control' block switches the control gate voltages of the cells in a selected word line. It switches high voltage levels which are generated internally by the charge pump circuits during programming and erasing respectively. In addition, the circuit connects the control gates of the cells in the selected word line to the voltage supply and the remaining ones to a ground level to perform read operation.

The 'Bit Line-R/W Control' or "bit line and read write control line" circuit is an interface between the column decoder and the memory array. It performs the switching of the required voltages at the drain and the source junctions of the cells in a selected column.

Sense amplifiers sense the stored data in the array, amplify and transfer it to the data buffers. One sense amplifier is required for each column. Data buffers are needed to transfer data to the output during read operation and to the input during program operation.

The above covers the basic building blocks of a 5V-only flash ZE²PROM. To implement the system, the memory array must occupy a small area [1] and it must be implementable in a 5V CMOS/BiCMOS process. In addition high speed and low power consumption are also the design objectives. To achieve high density, a bitcell that achieves the smallest die area will be considered first.

### 3.3 Memory Array

The ZE²PROM bitcell structure and its layout according to 0.8μm BiCMOS¹ design rules, are shown in Figs 3.2 (a) and (b) respectively.

---

1. BNR/NTE 0.8μm BATMOS Process
To operate a selected $ZE^2PROM$ cell without affecting any other cell it must have a control line on the drain, source and gate. The circuit diagram and the layout of a 4x2 array referred as "Array-A" are shown in Fig 3.3. In this configuration, the $ZE^2PROM$ cells are placed in a NOR array with a single word line per row and two access lines per column. One of the access lines is the "R/W control line" and the other is the single "bit line".
Since high density is an important parameter, other architectures were investigated to reduce the area per bitcell. Using the virtual ground concept [2-4] where the two columns share a metal line and considering the symmetrical structure of the cell and its operations, a novel array suitable for the ZE^2PROM is proposed. In this configuration, the sources and the drains of cells of two consecutive columns share an n^+ diffusion eliminating the LOCOS isolation between them. However, if these cells are placed in a single word line the neighboring cell will be unintentionally programmed one side when a particular cell is programmed. This will also apply to the erase operation. To resolve this problem, a second word line per row is introduced. The second word line connects the control gates of the alternating
cells in a row resulting in even (wle) and odd (wlo) word lines. The circuit diagram and the layout of this configuration (Array-B) is shown in Fig 3.4. It can be referred as the “Shared Bit Line, Alternating Word Line NOR” configuration.

Figure 3.4. The circuit diagram and the corresponding layout of Array-B.
Using the 0.8µm BiCMOS process design rules, the area per bit cell was calculated for both configurations A and B. The reduction in the area is significant when the shared bit line configuration (Array B) is used as shown in Table 3.2.

Table 3.2 Comparison of the area per bitcell of two configurations.

<table>
<thead>
<tr>
<th></th>
<th>Array-A</th>
<th>Array-B</th>
<th>Area Reduction</th>
</tr>
</thead>
<tbody>
<tr>
<td>32.00µm²</td>
<td>22.40µm²</td>
<td></td>
<td>30%</td>
</tr>
</tbody>
</table>

Therefore, the Shared Bit Line, Alternating Word Line NOR configuration (Array B) will be used as the basis for the discussion in the remainder of this chapter.

3.4 Peripheral Functions

In this section, the control logic necessary to implement the ZE²PROM operations are described. First, the word line operation which controls the cells’ control gates in a row will be considered. It will be followed by a discussion of the column control operation.

3.4.1 Word Line Operation

The ZE²PROM cell’s voltage requirements on the control gate are implemented with two control inputs, \( \text{Prgm} \) and \( \text{Read} \). The truth table is shown in Table 3.3. The block diagram that implements the word line operation is shown in Fig 3.5.

Table 3.3 Truth table for word line operation.

<table>
<thead>
<tr>
<th>Operation</th>
<th>Prgm</th>
<th>Read</th>
<th>Applied Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read</td>
<td>0</td>
<td>0</td>
<td>Vdd</td>
</tr>
<tr>
<td>Idle</td>
<td>0</td>
<td>1</td>
<td>GND</td>
</tr>
<tr>
<td>Erase</td>
<td>1</td>
<td>0</td>
<td>Vneg</td>
</tr>
<tr>
<td>Program</td>
<td>1</td>
<td>1</td>
<td>Vpp</td>
</tr>
</tbody>
</table>
Figure 3.5. Word line control for program, read, erase and idle states.

The control circuit generates the low voltage control signals for the switching circuits. Signals P and R control the Vpp/Vdd switch to obtain Vpp, Vdd or high impedance at the word line for program, read or other operations respectively. The high positive voltage Vpp, is generated by the Positive Charge Pump (PCP). The negative voltage Vneg is generated by the Negative Charge Pump (NCP). Signal E starts the negative charge pump to pull all the word lines to Vneg. The negative switch isolates the word lines from each other when the negative charge pump is not in use. The Idle signal controls the low voltage M_{ni} transistor to connect the unselected word line to the ground level to implement the idle state. The high voltage transistor M_{pi} isolates M_{ni} when the negative voltage is established at the word line.
3.4.2 Column Control Operation

The truth table for the corresponding column control operations is shown in Table 3.4. The block diagram that implements the logic is illustrated in Fig 3.6.

Table 3.4 Truth table for column control operation.

<table>
<thead>
<tr>
<th>Operation</th>
<th>Prgm</th>
<th>Read</th>
<th>R/W Line</th>
<th>Bit Line</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read</td>
<td>0</td>
<td>0</td>
<td>GND</td>
<td>3V</td>
</tr>
<tr>
<td>Idle</td>
<td>0</td>
<td>1</td>
<td>Float</td>
<td>Float</td>
</tr>
<tr>
<td>Erase</td>
<td>1</td>
<td>0</td>
<td>3V</td>
<td>Float</td>
</tr>
<tr>
<td>Program</td>
<td>1</td>
<td>1</td>
<td>Vdd</td>
<td>Vdd</td>
</tr>
</tbody>
</table>

Figure 3.6. Column control operation for read, program and erase states.

The control circuit generates the voltage levels to implement the truth table similar to the word line operation. In the column control circuits the highest voltage applied is the 5V supply voltage. Therefore, all the circuits involving the column control can be implemented with existing low voltage devices. Program switches are PMOS transistors which connect both the R/W and the bit lines to
the supply voltages under control of ProgEn signal. The current sources are included to limit the current through the zener junctions which will be described in section 3.7. The erase and read switches connect 3V or ground levels with the control of EraEn and Read signals respectively.

With the building blocks identified, the circuits that can implement them will be considered. These circuits involve both high and low voltages and therefore require the availability of the devices that can sustain the required voltages in the process to be implemented. The availability of low voltage BiCMOS process technology is assumed. The description of the process and the high voltage devices will be described next.

3.5 High Voltage Devices In BiCMOS Technology

The existing BiCMOS technology is designed and optimized for maximum 5V applications. It has complementary MOS devices and bipolar NPN devices with breakdown voltages of around 8V. A brief description of the BiCMOS technology is as follows.

Fig 3.7 illustrates the cross section of a typical submicron BiCMOS technology. The process begins with the formation of twin buried layers and the growth of a very lightly doped epitaxial layer. The double n- and p- wells are formed by self-aligned phosphorus and boron implantation. Polysilicon buffered local oxidation of silicon (LOCOS) is used for isolation to achieve a minimum device well spacing of 1.4μm. A threshold voltage adjust implant is carried out after growth of a 175 Å gate oxide. Masked lightly doped diffusion, n- LDD and p- LDD implants are used in the CMOS devices to enhance reliability by suppressing hot electron injection effects. Polysilicon layers are used for the gates of the MOS devices, the emitter of NPN bipolar transistor and the top plate of the double polysilicon capacitor. The process permits selective self-aligned silicidation of all the polysilicon levels, MOS source/drain and NPN extrinsic bases. After planarization, contacts and vias are filled with tungsten plugs. The tungsten plugs allow fully stacked contacts and vias. Three metal layers are available for interconnections. Besides the active devices, high performance resistors and capacitors are also available.
One way of increasing the breakdown voltage of NMOS or PMOS transistors is to use lightly doped extended regions between the drain and channel. These structures can be implemented in the existing BiCMOS technology by making use of the lightly doped n-well and p-well regions with simple layout manipulations [5]. The cross sections of high voltage NMOS and PMOS transistors and their circuit symbols are illustrated in Fig 3.8 and Fig 3.9 respectively. The p regions are highlighted to emphasize the existing connection paths to the common grounded p-substrate.
The performance of the high voltage device is characterized by its breakdown voltage ($B_{VDS}$) and specific on resistance ($R_{ON}$). Since the process parameters are fixed, the only parameters that can be optimized for the best performance are the layout parameters. They are channel length ($L$), device well spacing ($L_{ds}$) and the extended gate field plate over the thin and thick oxide ($L_{gp}$) and ($L_{fp}$) respectively as illustrated in the cross section of the devices. The simulated breakdown voltage obtained for those devices are $+30V$ and $-30V$ respectively [5].

Both of the devices are suitable for flash $ZE^2$PROM applications. To use them in circuit simulations, it is necessary to develop simple HSPICE models for them.

### 3.5.1 HSPICE Models for HVMOS Devices

The high voltage devices have the same structure as the low voltage devices except for the additional drift region as illustrated in their cross sections. This drift region is formed by a lightly doped n-well region for HVNMOS and a lightly doped p-well regions for HVPMOS as seen in the corresponding cross sections. It can be modeled by a lump resistor connected in series to the drain terminal of an ordinary MOS.
The low voltage NMOS and PMOS devices used in BiCMOS technology have well developed Level=3 HSPICE empirical models. The high voltage devices can be modeled with the existing low voltage model parameters with some modifications. The drain resistance parameter $R_D$ which is included in the low voltage model can be adjusted to model the drift regions. In addition to $R_D$, other parameters can be optimized to fit device simulators data using the HSPICE optimization analysis. The model parameters of both HVNMOS and HVPMOS obtained after optimization are listed in Appendix B. The simulated IV characteristics are shown below in Fig 3.10.

The availability of both low voltage and high voltage devices in the low voltage BiCMOS process makes the implementation of the peripheral circuits possible. The circuits that can implement the word line and the column line operation will be considered next.

![Figure 3.10](image)

**Figure 3.10.** The simulated dc characteristics of HVMOS devices with HSPICE model obtained by optimization of the low voltage model.

### 3.6 Word Line Switching Circuits

There are two major circuits that are involved in word line operation. One is a circuit that can switch the programming voltage $V_{pp}$ and the supply voltage $V_{dd}$. The other one is the negative switch that connects the erasing voltage $V_{neg}$.
3.6.1 Vpp/Vdd Switch

The circuit diagram of the Vpp/Vdd switch [6] is shown in Fig 3.11. The voltage levels at the word line \( \text{wl} \) according to the control signals \( P \) and \( R \) are also included. The row select (RS) signal selects the switch that corresponds to the word line.

Basically, the circuit is a high voltage inverter with a feedback transistor. The operation of the circuit is as follows: For the read operation the \( P \) and \( R \) control signals are low. The low signal \( R \) is transferred through \( M_{n2} \) and \( M_{p2} \) turns on pulling the word line (wl) to \( \text{Vdd} \). In the meantime, \( P \) signal is transferred to the input of a high voltage inverter through the pass transistor \( M_{n1} \) which turns \( M_{pinv} \) on pulling the output of the inverter to Vpp. This turns off \( M_{p1} \) and the program voltage level Vpp is isolated from the word line.

![Circuit Diagram](image)

**Figure 3.11. Program/Read switching circuit.**

For program operation, the \( P \) and \( R \) signals are both high. This turns \( M_{p2} \) off, disconnecting \( \text{Vdd} \) from the \( \text{wl} \). The high input transferred though \( M_{n1} \) results in a low level at the output of the inverter turning on \( M_{p1} \) and the word line.
is pulled to Vpp. $M_{\text{piso}}$ ensures that $M_{\text{p2}}$ stays off during programming. Without this transistor, $M_{\text{p2}}$ will turn on when program is enabled and the voltage level at the word line will be the average value of Vpp and Vdd. When P is high and R is low, $M_{\text{piso}}$ is off isolating WL from Vdd. A high input to the inverter results in Vpp at the word line. When P is low and R is high both $M_{\text{p1}}$ and $M_{\text{p2}}$ are off resulting in a high impedance Z at the word line.

The Vpp/Vdd switching circuit was simulated using HSPICE to illustrate the functionality of switching the voltage levels at the word line. The circuit was simulated with a single cell as a load. The simulation results are shown in Fig 3.12. The dimensions of the devices were chosen to be minimal and must be optimized according to all requirements.

![HSPICE simulation results showing Vpp and Vdd switching at the word line.](image)

**Figure 3.12.** HSPICE simulation results showing Vpp and Vdd switching at the word line.

### 3.6.2 Negative Switch

For the erase operation, a negative switching circuit is necessary to switch the word line to the negative voltage, which is generated by the negative charge pump circuit (NCP). The complement of the Vpp/Vdd switch can be designed as a Vneg/Gnd switch to implement the erase and idle states. However, this circuit will require the availability of an HVNMOS device that is isolated from the grounded substrate. The proposed Vneg/Gnd switch is described in Appendix C.
Since HVN MOS devices are not available in BiCMOS technology, other ways of connecting the negative voltage to the word lines was considered. One way is to pull down all the word lines when the negative voltage is generated. In this case the word lines must be isolated from each other when the NCP is not in use.

The circuit diagram of a negative switch is illustrated in Fig 3.13. One negative switch is required per word line. The circuit has two states of operation. When the negative charge pump circuit is activated, $M_{p2}$ turns on and pulls the word line to $V_{neg}$. For the other state, $V_{neg}$ is zero. When the word line is $V_{pp}$ or $V_{dd}$, $M_{p1}$ turns on and the connection path occurs through the resistor $R$. To not draw current, the value of $R$ must be high. In this circuit configuration, the operation of the NCP to start negative voltage generation is controlled with the $E$ signal. The HSPICE simulation results are also included in Fig 3.13. The dimensions of the devices and the value of the resistor must be optimized according to the current capability and design specifications.

![Circuit Diagram and HSPICE Simulation Results](image)

**Figure 3.13.** Negative voltage connecting circuit and the HSPICE simulation results.

This concludes the discussion of the control circuits that switch the voltage levels to the control gate of the cells to implement all the operation modes. To
select the correct bit, the column in which the cell resides in must also be raised to the corresponding voltage levels at the same time as the word line.

3.7 Column Switching Circuits

The sources and drains of the ZE²PROM cells in one column are connected with a R/W control line and a bit line. In the proposed "Shared Bit Line, Alternating Word Line NOR" array, the two neighboring columns are folded and they form the mirror image of each other.

The R/W control and bit line switching circuits are shown in Fig 3.14. The 3V supply voltage required during read and erase operations can be generated internally from the 5V supply voltage. The 3V supply is chosen to avoid zener breakdown during erasing and reading. For example, 3.5V obtained by two diode voltage drops can be used. The diodes can be implemented using both NPN or NMOS transistors.

![Diagram of R/W control and bit line switching circuits](image)

**Figure 3.14. Low voltage switches are used for bit line operation**

An important design consideration when supplying the program voltage is the presence of the zener diodes at both source and drain regions. The programming speed of the ZE²PROM cell is enhanced with the generation of a high number of electron-hole pairs when breakdown occurs. When operating in this region, the
current of the zener diode is very sensitive to the voltage variations. The sensitivity can be avoided by limiting the current at both the source and drain junctions. Furthermore, if the current is limited the power dissipation will be reduced as well. The current limitation is also necessary for safe operation of the device. Therefore, it is necessary to bias both the source and the drain terminals of ZE²PROM cell using current sources.

In order to specify the value of the current source per cell during programming, the threshold voltage dependence on the current level obtained from the device simulations is considered. It can be seen in Fig. 3.15 that when the current level is limited to 10µA the programming time of the ZE²PROM cell is 300ns compared to 150ns for 80µA. This programming speed is still faster than a conventional flash E²PROM cell by an order of magnitude. In addition, the current reduction will result in preprogramming the cells in flash or blocks before erasure. This is not possible with the ETOX cell array, because programming of the cell requires high current levels (~400µA/cell) to generate hot electrons.

![Figure 3.15. Threshold voltage change of ZE²PROM cell for different current levels.](image-url)
For program operation, switches are used to connect the current sources which are controlled by the ProgEn signal as shown in Fig 3.14. The current source can be implemented using basic cascode current mirror configuration [10] and can be mirrored to each R/W control and bit line. The circuit diagram of the current source is shown in Fig. 3.16. The circuit was designed and simulated to implement 5μA current sources at the drain and source junctions of a cell to obtain 10μA of zener current per cell. The HSPICE simulation results in Fig 3.17 show the limited current through the zener junctions switched by a PMOS transistor under control of the ProgEn signal.

When the complete array is designed, the value of the current sources to be chosen will depend on the number of cells per column, programming time and power dissipation requirements. When the R/W and bit lines are raised to the programming voltage, all the zener junctions of the cells in that particular column will break down and will draw current from the current sources. Therefore, the current sources must be scaled to supply the required current. To reduce the power dissipation the bit lines can be divided in subbitlines.

Figure 3.16. Current source circuit to bias the source and the drain of ZE²PROM cell.
Figure 3.17. HSPICE simulation showing the current through the zener junctions during programming. The circuit is designed to supply 5μA per junction resulting in 10μA per cell.

3.8 Sensing Circuit

During the read operation, the data stored in the array must be sensed and translated to the output. The current drive of the cell is 1/2 compared to a conventional cell. The time to charge the parasitic bit line capacitances to a certain potential level will be long if voltage sensing is considered. Therefore, a current sensing scheme is proposed. With this circuit the stored data is obtained by sensing the current drawn by the on cells when the read voltages are applied. This current on each bit line is mirrored and compared with a reference current, Iref.

The circuit diagram of a proposed sense amplifier is illustrated in Fig 3.18. When the next cell sharing the same bit line is read, the role of the source and the drain terminals of neighboring cells interchange as depicted in Fig 3.18. The sensed data still corresponds to the correct bit.

The read current of an unprogrammed cell is 87μA under 5V at the control gate and 3V at the drain as shown in the read characteristics in Fig 2.2. To illustrate the functionality of the sense circuit, it was simulated in HSPICE. Iref was set to 45μA and the Icell was swept from 0 to 100μA. The input of the
inverter and the data output is shown in Fig 3.19. The output data will correspond to "0" when the read current is larger than 50µA and "1" when it is less than 40µA. To obtain the conventional logic "0" and "1", the output must be further inverted.

Figure 3.18. Current sensing circuit for Flash ZE²PROM.

Figure 3.19. The input and the output of the inverter as a function of Icell when Iref is 45µA.
The remaining building blocks except the charge pump circuits can be implemented by logic gates available in the standard cell library of the technology used. The design of the charge pump circuits requires the high voltage devices in the low voltage CMOS/BiCMOS process. The issues involving the high voltage generation will be covered in the following chapter.

3.9 Summary

In this chapter, a ZE\textsuperscript{2}PROM architecture and the peripheral circuitry required to implement the basic cell operations were presented. Since most of the area in a memory chip is occupied by the memory array, its configuration must be designed to minimize the area per bitcell. Two arrays were considered and a “Shared Bit Line, Alternating Word Line NOR” configuration suitable for ZE\textsuperscript{2}PROM was proposed. With this array a 30% higher density can be achieved.

The ZE\textsuperscript{2}PROM cell requires the application of different voltage levels during different modes of operations. The control logic to implement read, write, program and idle states was described. The circuitry necessary to implement these states were presented and their functionality were illustrated with HSPICE simulation results. High density and low power dissipation were the main objectives.
References


CHAPTER 4

EXPERIMENTAL HIGH VOLTAGE BUILDING BLOCKS

4.1 Introduction

When a \( \text{ZE}^2\text{PROM} \) cell is programmed and erased, high voltages are only applied to the control gate. This results in pure capacitive loads for the high voltage generator and thus very low current requirement. Therefore, on chip charge pump circuits which are used to boost the voltage levels above the power supply level can be much smaller in area and capacity, compared to a conventional flash \( \text{E}^2\text{PROM} \).

To implement the above circuits, the devices that can sustain the required high voltages must be available. In the previous chapter it was shown that when a low voltage technology is used, it is desirable to implement these devices without a process change. This simplifies the integration of both the high voltage and the low voltage implementations on the same design.

In this chapter, the design and the implementation of positive charge pump (PCP) and negative charge pump (NCP) circuits in low voltage CMOS/BiCMOS technology that are suitable for programming and erasing \( \text{ZE}^2\text{PROM} \) cells will be described.

4.2 Implementation of High Voltage Devices

The implementation of the high voltage devices described in the previous chapter using BiCMOS will be considered first. Traditionally, high voltage devices are implemented in interdigitated layouts with circular geometries to avoid possible breakdown voltage degradation caused by curvature effects. This is not a concern
for the flash ZE²PROM application since the estimated breakdown voltages are much higher than the required voltage levels. Therefore, both the HVN莫斯 and HVPMOS transistors can be implemented in rectangular layouts as illustrated in Fig 4.1.

Figure 4.1. The rectangular layout of high voltage devices (a) HVN莫斯 and (b) HVPMOS

HVNmos devices were easily implemented by overlapping n-diffusion, the n-well and the gate poly design layers to realize the corresponding extended drain and field plate regions. The micrograph of the HVNmos device is shown in Fig 4.2. The same manipulation applies to HVPMOS, however it requires an additional n⁺ buried mask layer that surrounds the devices for isolation from the common grounded p-substrate. Due to the unavailability of this layer at the time of the design, these devices were not implemented.

The breakdown voltage and dc characteristics of the HVNmos device were measured using the HP4145 Semiconductor Parameter Analyzer. The experimental results are shown in Fig 4.3. The measured breakdown voltages were 30V for 0V gate bias and 22V for 5V gate bias condition.
Figure 4.2. The micrograph of a rectangular HVNMOS device.

Figure 4.3. Breakdown and IV Characteristics of HVNMOS when operating in forward mode (W=40μm and L=3μm)

The HVPMOS experimental results [1] also showed a -30V breakdown voltage. The measured breakdown and IV characteristics when the device is operating in forward mode are shown in Fig 4.4.
The HSPICE models of the devices were verified with the experimental results. The simulated IV characteristics were in agreement within 5% with the measured results as shown in Fig 4.5.
Both HVNOMOS and HVPMOS devices were used in the implementation of the HV building blocks. The design and the development of the PCP circuits that can generate the high programming voltages required for programming the flash \( \text{ZE}^2\text{PROM} \) cells will be described in the next section.

4.3 Positive Charge Pump Circuits (PCP)

During programming, a high voltage is applied at the control gate of the \( \text{ZE}^2\text{PROM} \) cell. The load for the positive charge pump circuit is the equivalent control gate capacitance of the total \( \text{ZE}^2\text{PROM} \) cells to be programmed at once. The equivalent gate capacitance of a minimum size (1.4\( \mu \text{m} \times 0.8\mu \text{m} \)) \( \text{ZE}^2\text{PROM} \) is calculated to be approximately 3fF. The simulated gate current during programming is approximately 90nA per \( \mu \text{m} \) width and 2.0\( \mu \text{m} \) channel length. According to the programming mechanism, the gate current is the result of the charge generated by zener breakdown of both \( n^+/p^+ \) junctions and attracted to the floating gate by the applied voltage. Since the injection occurs at the sides of the gate structure, the programming current is proportional to the area of the \( p^+ \) region in the active section only. According to this assumption the programming gate current for a unit cell designed in 0.8\( \mu \text{m} \) BiCMOS technology is about 30nA. The total gate current and capacitance of the selected group of cells during programming can be approximated as follows.

Table 4.1. The control gate current and equivalent capacitance of \( \text{ZE}^2\text{PROM} \) cells.

<table>
<thead>
<tr>
<th>( \text{ZE}^2\text{PROM} ) Cell Density</th>
<th>( I_{CG} )</th>
<th>( C_{CG} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 bit</td>
<td>30nA</td>
<td>3fF</td>
</tr>
<tr>
<td>8 bits</td>
<td>240nA</td>
<td>24fF</td>
</tr>
<tr>
<td>16 bits</td>
<td>480nA</td>
<td>48fF</td>
</tr>
<tr>
<td>32 bits</td>
<td>1( \mu \text{A} )</td>
<td>96fF</td>
</tr>
<tr>
<td>1K bits</td>
<td>31( \mu \text{A} )</td>
<td>3pF</td>
</tr>
<tr>
<td>2K bits</td>
<td>62( \mu \text{A} )</td>
<td>6pF</td>
</tr>
<tr>
<td>8K bits</td>
<td>248( \mu \text{A} )</td>
<td>24pF</td>
</tr>
</tbody>
</table>

The values listed in Table 4.1 provide \( \text{ZE}^2\text{PROM} \) design specifications for the PCP circuits that will be considered next.
Positive high voltages can be generated on chip by using the n-stage voltage multiplier circuit introduced by Dickson [2]. The basic structure is shown in Fig 4.6. This circuit makes use of capacitors that are interconnected by diodes and coupled in parallel with two nonoverlapping clock signals. The multiplier operates by pumping packets of charge along the diode chain as the coupling capacitors are charged and discharged during each half of the clock cycle. The average node potentials increase progressively from the input to the output of the diode chain after each clock cycle.

![Diagram of n-stage voltage multiplier circuit](image)

**Figure 4.6. A typical n-stage voltage multiplier configuration**

The actual voltage obtained at the output is a function of the number of diode/capacitor stages, the voltage drop on the diodes, the amplitude of the clock and the load current. When \( V_\emptyset \) is equal to \( V_{IN} \), the open circuit output voltage can be approximated as follows [2].

\[
V_{OUT} = (n + 1) (V_{IN} - V_D)
\]

where \( V_{IN} \) is the input voltage, \( V_D \) is the forwardbiased diode voltage, \( V_\emptyset \) is the amplitude of the clock and \( n \) is the number of stages.

The total charge pumped by each diode per clock cycle is \( CV_{OUT} \). The current supplied at the output due to charge transfer at a period of time is a function of the clock frequency \( f \), storage capacitor \( C \) and the output voltage \( V_{OUT} \). It can be approximated as [2]
The number of the stages and the value of the storage capacitor can be calculated according to the voltage and the current requirements at the output. The maximum voltage swing across the diode of each stage is approximately $2V_{IN} - V_D$, therefore the reverse breakdown voltages of diodes must be higher than this value. In addition, the process must be able to handle the peak voltage level at the last stage.

The diodes shown in the n-stage voltage multiplier circuit in Fig 4.6 can be implemented with diode connected NMOS transistors. When this configuration is used, the diode voltage $V_D$ can be replaced by the threshold voltage $V_{TH}$ in equation 4.1 to estimate the number of the stages required for certain voltage. However, this will not be a good approximation when an n-well CMOS/BiCMOS technology is used. The threshold voltage of the devices at each stage will differ due to the body effect, as the node voltages increase. This, in turn will increase the number of stages. For programming a flash $ZE^2$PROM cell, the application of 12V is required. Accordingly, a minimum 3-stage voltage multiplier is required when $V_\phi$ and $V_{DD}$ are 5V and $V_{TH0}$ of the HVNMOS transistor is 0.75V. The circuit diagram is shown in Fig 4.7.

![Figure 4.7. PCP using diode connected HVNMOS devices.](image)

The circuit was simulated with HSPICE for different capacitive loads of 5pf, 10pf, 20pf. The storage capacitors are 10pf and the clock has 5V (Vdd)
amplitude and 5MHz frequency. The simulation results are shown in Fig 4.8. The rise times for the capacitive loads are 1.85µs, 2.47µs and 3.50µs respectively.

![Simulation Results Graph](image)

Figure 4.8. HSPICE simulations of PCP circuit with different capacitive loads.

The problem with this circuit is that the open circuit output voltage depends on the $V_{TH}$ of the NMOS devices, which in turn increases for each stage due to bulk effect. The performance of the circuit can be improved using HVNMOS pass transistors and supplying gate bias with feedback as shown in Fig 4.9.

![Circuit Diagram](image)

Figure 4.9. PCP with HVNMOS pass transistors and their feedback to provide gate bias.
In this configuration the conductivities of the switching transistors are controlled by four clocks of 5V amplitude and different phases and improved with the aid of feedback transistors. Each stage consists of four transistors and four storage capacitors. The operation of the circuit is as follows: Assuming zero initial voltage at all of the nodes, as Clka1 goes high, 5V appears at node a. Then Clka2 goes high and M1 turns on and results in charge distribution between Ca1 and Cb1. When Clkb1 goes high at the same time that Clka1 and Clka2 go low, M1 turns off. Voltage at node b is boosted up due to the previous charge. In the meantime, Mf1 turns on resulting in charge transfer from Ca1 to Ca2 and keeping M1 off. This charge transfer is necessary to turn on M1 at the next cycle, since node b goes higher than the gate voltage and the clock voltage will not be enough to turn on the transistor. The same procedure repeats for the second part of the circuit during the next cycle and a high voltage is established at the output. The output voltage is boosted up to a higher voltage by transferring charges from one stage to the next one and to the load. Two stages are necessary to obtain 12V at the output. The HSPICE simulations results are shown in Fig 4.10.

![Diagram of PCP circuit](a)

![Graph of HSPICE simulations](b)

Figure 4.10. HSPICE simulations of 2-stage PCP circuits.

The PCP circuit was implemented and tested using the set up shown in Fig 4.11. The comparison of the simulated and measured output voltage is illustrated
in Fig 4.12. The measured output voltage is within 10% in agreement with the expected value. The simulated and measured rise times for different load capacitors are listed in Table 4.2.

![Diagram of test setup for charge pump circuits](image)

**Figure 4.11.** Test set up for charge pump circuits.

![Graph comparing simulated and experimental results for PCP circuit](image)

**Figure 4.12.** Comparison of simulated and experimental results for PCP circuit. (Cl=5pF Clk=5MHz).
The disadvantages of this configuration are the large number of transistors and capacitors resulting in large area and the requirement for four nonoverlapping clocks. The performance of both configurations can be improved by replacing the diode with a diode connected NPN transistor. In this configuration the diode’s forward voltage is the same for all the stages since there is no bulk effect.

An improved PCP was designed and implemented using diode connected NPN transistors is illustrated in Fig 4.13. The base collector junction was used to ensure high reverse breakdown [4]. \( BV_{CBO} \) was measured to be 19V and collector to substrate breakdown voltage as 33V. The circuit was tested using the same set up as before. The simulated and measured output values are illustrated in Fig 4.14 and the rise times for different load capacitors are listed in Table 4.3.

![Circuit Diagram](image)

Figure 4.13. The circuit diagram of the PCP with BJT diodes.

<table>
<thead>
<tr>
<th>( T_r ) (μs)</th>
<th>( C_L=5)pF</th>
<th>( C_L=10)pF</th>
<th>( C_L=20)pF</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>HSPICE</strong></td>
<td>2.85</td>
<td>3.15</td>
<td>4.45</td>
</tr>
<tr>
<td><strong>Measured</strong></td>
<td>4.40</td>
<td>5.04</td>
<td>8.55</td>
</tr>
</tbody>
</table>

Table 4.2. Simulated and measured rise times for PCP circuit with gate biased HVNOMOS.

<table>
<thead>
<tr>
<th>( T_r ) (μs)</th>
<th>( C_L=5)pF</th>
<th>( C_L=10)pF</th>
<th>( C_L=20)pF</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>HSPICE</strong></td>
<td>0.80</td>
<td>1.00</td>
<td>1.65</td>
</tr>
<tr>
<td><strong>Measured</strong></td>
<td>1.02</td>
<td>1.45</td>
<td>2.20</td>
</tr>
</tbody>
</table>

Table 4.3. Simulated and measured rise times for PCP with BJT diodes circuit.
Figure 4. 14. Comparison of simulated and experimental results for PCP-Bipolar circuit. (Cl=5pF Clk=5MHz)

Figure 4. 15. Micrograph of the experimental chip.
The output voltage is 14V which is 15% higher than the required programming voltage and will further improve the programming time of the cell. This configuration gives the best performance compared to the previous ones. The PCP with BJT diodes consist of two stages, occupies the smallest area, has the shortest rise time and uses only one clock.

4.4 Negative Charge Pump Circuits (NCP)

High negative voltage is required for the erase operation. The n-stage multiplier circuit can be modified as shown in Fig 4.16. The operation of the circuit is similar to its positive counterpart except the average node potentials decrease progressively towards the output after each clock cycle.

![Voltage multiplier configuration to obtain negative output voltage.](image)

The open circuit output voltage can be approximated as

\[ V_{OUT} = -n (V_{\phi} - V_D) \]  \hspace{1cm} (4.3)

An important consideration for this circuit when implemented in n-well technology is to ensure the isolation of the coupling devices from the common grounded p-substrate.

It can be implemented by using diode connected HVPMOS devices with high voltage handling capability similar to its positive counterpart. However, since the substrates of HVPMOS devices are connected to the highest voltage level
(5V $V_{DD}$), the bulk effect altering the $V_{TH}$ of the devices will be higher than the HVNMOS devices for the corresponding stages. This in turn will increase the number of stages to generate the required output. Negative 15V can be obtained with six stages. The circuit diagram of the NCP circuit is shown in Fig 4.17.

![Circuit Diagram](image)

**Figure 4.17.** NCP using diode connected HVPMOS devices.

![Simulation Graph](image)

**Figure 4.18.** HSPICE simulations of NCP circuit with different capacitive loads.

The circuit was simulated with HSPICE for capacitive loads of 5pf, 10pf, 20pf. The storage capacitors are 10pf and the clock has 5V amplitude and 5MHz frequency.
frequency. The simulation results are shown in Fig 4.18. The fall times for the capacitive loads are 6.30μs, 7.40μs and 9.75μs respectively.

The problem with this circuit is the sensitivity of $V_{TH}$ of the PMOS devices to the bulk effect. The performance of the circuit can be improved by supplying a gate bias voltage similar to the PCP. The corresponding NCP circuit is obtained by replacing the HVNMOs devices with HVPMOS devices and inverting the input clocks as shown in Fig 4.19. The operation of the circuit is the same and each node is discharged to the previous one generating a negative voltage at the output instead.

![Diagram showing NCP with PMOS pass transistors and their feedback providing gate bias.](image)

Figure 4.19. NCP with PMOS pass transistors and their feedback providing gate bias.

At the time of designing the negative charge pump circuits, HVPMOS devices were not available. This circuit was implemented using long channel low voltage PMOS devices. The measurements performed on long channel devices showed drain to source breakdown voltage ($BV_{DS}$) of -12V and drain or source to p-substrate ($BV_{DSUB}$) of -17V. Three stages were implemented to generate -12V at the output due to the limitations of the process. The NCP circuit was tested using a similar set up as the one used for the PCP circuits. The comparison of the experimental and simulated results are shown in Fig 4.20. The simulated and measured fall times are listed in Table 4.4.
Table 4.4. Simulated and measured fall times for NCP circuit.

<table>
<thead>
<tr>
<th>$T_f$ (µs)</th>
<th>$C_L=5\text{pF}$</th>
<th>$C_L=10\text{pF}$</th>
<th>$C_L=20\text{pF}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>HSPICE</td>
<td>28.0</td>
<td>34.5</td>
<td>49.5</td>
</tr>
<tr>
<td>Measured</td>
<td>7.40</td>
<td>16.8</td>
<td>18.8</td>
</tr>
</tbody>
</table>

Figure 4.20. Comparison of simulated and experimental results for NCP circuit. (Cl=5pf and Clk=5MHz).

Figure 4.21. Micrograph of the experimental NCP.
The experimental results showed better performance than the simulations as can be observed in Fig 4.20. This could be due to the fact that the available HSPICE models are optimized for 5V applications. However, this circuit has similar disadvantages as its positive counterpart.

The performances of previous NCP configurations can be improved by using isolated diodes. In the PCP case the diodes were implemented using diode connected NPN transistors. However, this is not possible when negative voltages are involved. The NPN transistor's collector and the grounded substrate forms a diode which clamps the negative voltages; see the cross section of BiCMOS structure in Fig 3.7. To implement the NCP circuit in BiCMOS technology with coupling diodes, it is necessary to have floating diodes isolated from the p-substrate and it is desirable to obtain them without a process change. The base emitter junction of the existing bipolar NPN was investigated as an isolated diode. The observations and suggestions on isolated diodes in a BiCMOS process and proposed NCP circuit are described in Appendix D.

### 4.5 Summary

In this chapter, the design and the implementation of the positive and negative charge pump circuits required to generate the high programming and erasing voltages for ZE²PROM was presented. The high voltage issues in a low voltage BiCMOS process was addressed and high voltage devices suitable for high voltage circuits were described.

Different circuit configurations were considered and comparison of their performances were covered. The simulated and measured data obtained from the experimental designs implemented in BiCMOS technology were presented. It has been shown that the best performances in both PCP and NCP circuit configurations are obtained when they are implemented in diode configuration.
References


CHAPTER 5

CONCLUSIONS

In this thesis, the architecture and the design of the peripheral circuitry suitable for a zener based (ZE\textsuperscript{2}PROM) flash memory has been investigated. The cell achieved 150ns programming time and 50ms erasing time. The cell uses a 5V supply and has different requirements for read, program and erase operations from a conventional flash E\textsuperscript{2}PROM cell and thus requires a new architecture and peripheral building blocks. The contributions of the thesis include:

First, a simple model for the ZE\textsuperscript{2}PROM cell suitable for circuit simulations was developed. An HSPICE subcircuit with elements corresponding to the cell's physical structure was proposed. The model included the transient threshold voltage shift of the device during programming and erasing. The proposed model was used in the circuit simulations when the peripheral building blocks were considered.

A ZE\textsuperscript{2}PROM architecture and the peripheral circuitry required to implement the basic cell operations were presented in Chapter 3. Since most of the area in a memory chip is occupied by the memory array, its configuration was designed to minimize the area per bitcell. A novel "Shared Bit Line, Alternating Word Line NOR" configuration suitable for ZE\textsuperscript{2}PROM was proposed and 30% higher density was achieved. The circuitry to implement read, write, program and idle states was described. The word line and the column control operations were demonstrated. The detailed circuitry to implement the switching of the voltage levels were presented. Current sources were proposed for the current control of zener junctions during programming to avoid the variations of the current due to supply voltage changes. The proposed architecture and the peripheral circuits achieve high density, low power dissipation and uses 5V single power supply.
The high voltage issues in a low voltage BiCMOS process were addressed and high voltage devices suitable for high voltage circuits were used. The positive and negative charge pump circuits which can be used to generate the high programming and erasing voltages for ZE²PROM were presented. Different circuit configurations were considered and compared. Experimental designs implemented in a BiCMOS technology were presented. It was shown that the best performance in both PCP and NCP circuit configurations is obtained when they are implemented using a diode configuration.

5.1 Suggestions for Future Work

Modeling improvements:

- The current sources in the HSPICE subcircuit that model the threshold voltage shift during programming and erasing can be further developed to model the zener current and control gate voltage variations.

Device improvements:

- The erase time of the ZE²PROM cell can be investigated to improve the overall programming and erasing of the memory array.

- Implementation of an isolated diode in BiCMOS technology can be further investigated.

Circuits and system work:

- An experimental ZE²PROM memory using the proposed architecture and peripheral circuits should be implemented to confirm the expected functionality.

- Implementation of program and erase algorithms with preprogramming in blocks can be investigated.
Appendix A

HSPICE Model of $\text{ZE}^2\text{PROM}$ Cell

Model parameters for elements of the $\text{ZE}^2\text{PROM}$ cell are provided below. The device parameters are obtained from the MEDICI structure. The electrical parameters were extracted from the device simulation. Both active and sense sections sizes are $L=2\mu\text{m}$ and $W=1\mu\text{m}$.

![Figure A.1. The $\text{ZE}^2\text{PROM}$ cell structure and the large signal model.](image)

```
.MODEL CAPFG C
THICK=300E-10, L=2U, W=1U
```
.MODEL MNEPROM NMOS

LEVEL=3, ACM=2, VTO=0.250, TOX=100E-10,
NSUB=6E16, LD=0.35E-6, XJ=0.5E-6, RS=968.4,
RD=968.4, RSH=0.0, KP=72E-6

.MODEL DZ D

BV=4.15V, IBV=1.2058U, N=0.01, RS=10
RZ=5K

IHEI PWL (0 0 1ns 90.05nA 256ns 50.75nA)

IFNT PWL (0 0 2us 15.28pA 32us -14.3pA
256us -9.577pA 2.048ms -.11pA 7.612ms -.512pA
52.46ms -67.73fA 100ms -23.51fA)
Appendix B

HSPICE Models of HV Devices

In this section HSPICE model parameters for high voltage devices with 2\(\mu\)m channel length are provided.

```
.MODEL HVNmos NMOS
LEVEL=3, ACM=2, VTO=750.8E-3, UO=401,
TOX=17.52E-9, NSUB=3.231E16, NFS=819.9E9, DELTA=0.1,
THETA=9.8E-3, WD=0.00, PB=0.9236, LD=55E-9,
LDIF=940.5E-9, XJ=247.9E-9, VMAX=1.045E6, ETA=521E-3,
KAPPA=0, RS=595.6, RD=9.463E3, RSH=0,
HDIF=1.2E-6, GAMMA=491E-3, JS=5.0E-4, JSW=5.5E-9,
CJ=250.0E-6, MJ=0.50, CJSW=2.50E-12, MJSW=0.30,
CGSO=273.9E-12, CGBO=570.9E-12, CGDO=273.9E-12

.MODEL HVPMOS PMOS
LEVEL=3, ACM=2, VTO=-0.870, UO=166,
TOX=17.5E-9, NSUB=2.800E16, NFS=540E9, DELTA=0.695,
THETA=1.23, WD=85.76E-9, LD=1.00E-9, LDIF=999.0E-9,
XJ=91.79E-9, VMAX=7.63K, ETA=4.76E-6, KAPPA=13.5,
RS=1.200E3, RD=124K, RSH=0.0, HDIF=2.2E-6,
JS=5.0E-4, JSW=5.5E-10, CJ=450.0E-6, MJ=0.61,
CJSW=170.0E-12, MJSW=0.26, CGSO=214.8E-12, CGBO=586.E-12,
CGDO=214.8E-12
```
Appendix C

Vneg/Gnd Switch

Vneg/Gnd switch is the complement of the Vpp/Vdd switch and requires the availability of isolated HVNMOS devices. One way of implementing isolated HVNMOS device is to insert an n-subwell above the p-substrate to isolate the device. However, this requires an extra mask to the existing BiCMOS process.

The proposed circuit to perform Vneg/Gnd switching is shown in Fig C.1.

![Circuit Diagram]

Figure C. 1. The “Vneg/Gnd Switch” circuit.

The RS (Row Select) signal enables the pass transistor $M_{pe}$ to transfer $E$ (Erase) signal to the input of the inverter and $I$ (Idle) signal to the input of the low voltage switch. When both signals are high, the $wl$ is pulled down to the negative voltage for the erase operation. The $wl$ is grounded for the idle state of operation of the unselected word line. The operation of the circuit is
similar to its positive counterpart. The feedback transistor $M_{nf}$ makes the input of the inverter swing between $V_{dd}$ and $V_{neg}$. $M_{niso}$ is inserted in order to prevent the $M_{ni}$ to turn on when the wl is being pulled down. Since the erase operation is done in flash or blocks all of the word lines of the array or the particular block are selected by the row decoder.

The circuit was designed and simulated with a single cell as a load to illustrate its functionality. The simulation results are shown if Fig C.2. The dimensions of the devices must be rescaled according to the number of the cells and parasitic capacitances.

![Inverter simulation](image)

**Figure C. 2.** HSPICE simulations showing $V_{neg}$ and Gnd switching at the word line.
Appendix D

Isolated Diodes in BiCMOS and Improved NCP Circuit

In this section, the investigation of the base emitter junction of an NPN transistor as an isolated diode in BiCMOS process is described. Suggestions for isolated diodes in BiCMOS technology and improved NCP circuit that use these diodes are also included.

It was observed that the only PN junction isolated from the grounded substrate in BiCMOS process was the base-emitter junction of the NPN transistor. It can be used as a diode when the collector is left floating. To characterize the BE-diode, measurements on NPN devices were carried out using the HP4145 Semiconductor Parameter Analyzer. The reverse breakdown voltage of the junction was measured to be approximately 5.5V to 6V as expected due to the highly doped n⁺ poly emitter. The HSPICE model parameters were extracted for circuit simulations. The layout of the BE diodes were designed and implemented using emitter, p-base and nwell design layers and by removing n⁺sinker layer following the minimum design rules as shown in Fig D.1. The micrograph of the device is shown in Fig D.2.

![Figure D.1. The cross section and the layout of the BE-Diode.](image)
Figure D. 2. Micrograph of the BE-Diode.

The simulated IV characteristics based on the extracted model parameters and measured data are shown in Fig D.3.

Figure D. 3. IV Characteristics of the BE-Diode.
The implemented diodes were tested in to confirm the required specifications. The reverse breakdown voltages were approximately 6V as expected and the IV characteristics were in agreement with the data obtained from the NPN transistors. However, more testing showed a thyristor behavior between the n+ emitter and grounded p-substrate with a base terminal behaving as its gate due to the existing four layer n^+ pnp structure. This problem could be resolved by layout manipulation to prevent the device from turning on.

There are other possible ways to implement isolated diodes in BiCMOS process. Two suggested structures require the availability of p+ poly which requires one additional mask layer to the existing process. The cross section of the suggested structures are shown in Fig D.4.

Figure D. 4. Two device structures for isolated diodes in BiCMOS technology.

The device structure shown in (a) is a PNP transistor in a diode connected configuration. The other structure is a simple p^+/n^+ diode implemented with poly layers which can be isolated with thick oxide [1]. The device characteristics should be optimized to meet the high voltage requirements in order to be used in NCP circuits.

In all of the above structures the reverse breakdown voltage is expected to be low due to high doping concentrations of the poly layers. For example, in the BE-diode the measured breakdown voltage was approximately 6V. To implement the NCP circuit in the diode configuration, the circuit must be modified. This is
necessary since the voltage swing across the diodes are approximately 9V when 5V supply and clock voltages are used.

The NCP circuit can be implemented by placing two diodes in series to reduce the voltage drop on each diode to 4.5V which is less than the measured reverse breakdown voltage. This will change the fall times of the output and increase the number of stages. The open circuit output can be approximated as

\[
V_{OUT} = -n(V_{DD} - 2V_D)
\]  

(D.1)

The modified circuit diagram and the HSPICE simulation results using the models developed for the BE-diode are shown in Fig D.5.

![Diagram of NCP circuit with isolated diodes and HSPICE simulation results](image)

Figure D. 5. The modified circuit diagram of NCP implemented with isolated diodes and HSPICE simulation results.
The simulated fall times are $4.20\mu$s, $5.40\mu$s and $7.30\mu$s for 5pf, 10pf and 20pf capacitive loads respectively. This configuration gives the best performance compared to the previous NCP circuits.
References