Design and Implementation of a 16kbit 1T1C Ferroelectric Random Access Memory Testchip

by

Joseph Wai-Kit Siu

A thesis submitted in conformity with the requirements for the degree of Master of Applied Science in the Department of Electrical and Computer Engineering University of Toronto

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Master of Applied Science, 2001

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Abstract

This thesis presents design and implementation of a novel reference generation scheme and a current-steering sense amplifier. The reference generation scheme balances fatigue among memory cell capacitors and reference cell capacitors on the same row. The sense amplifier design allows a reference current to be shared among eight adjacent columns in the memory array.

A 16kbit 1T1C ferroelectric random access memory (FeRAM) testchip has been designed and fabricated in a 0.35μm CMOS technology with integration of planar ferroelectric capacitors. Testchip functionality was verified by both simulation and measurement results.
Acknowledgments

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<th>Description</th>
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<tr>
<td>FeRAM</td>
<td>Ferroelectric Random Access Memory</td>
</tr>
<tr>
<td>DRAM</td>
<td>Dynamic Random Access Memory</td>
</tr>
<tr>
<td>EEPROM</td>
<td>Electrically Erasable Programmable Read-Only Memory</td>
</tr>
<tr>
<td>1T1C cell</td>
<td>One Transistor, One Capacitor Cell</td>
</tr>
<tr>
<td>2T2C cell</td>
<td>Two Transistor, Two Capacitor Cell</td>
</tr>
<tr>
<td>CCSA</td>
<td>Cross-Coupled Sense Amplifier</td>
</tr>
<tr>
<td>CSSA</td>
<td>Current-Steering Sense Amplifier</td>
</tr>
<tr>
<td>ICSSA</td>
<td>Improved Current-Steering Sense Amplifier</td>
</tr>
<tr>
<td>BL</td>
<td>Bit-Line</td>
</tr>
<tr>
<td>RBL &amp; RBL</td>
<td>Reference Bitline Pair</td>
</tr>
<tr>
<td>WL</td>
<td>Word-Line</td>
</tr>
<tr>
<td>PL</td>
<td>Plate-Line</td>
</tr>
<tr>
<td>CBL</td>
<td>Parasitic Bitline Capacitance</td>
</tr>
<tr>
<td>CFE</td>
<td>Ferroelectric Cell Capacitance</td>
</tr>
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</table>
| VBL | Voltage on the Memory Bitline BL (VBL=V1 if the stored data is ‘1’ or VBL=V0 if the stored data is ‘0’)
| VRBL | Voltage on the Reference Bitline RBL (=V0) |
| VRBL | Voltage on the Reference Bitline RBL (=V1) |
| ΔVBL | Differential Bitline Voltage (=V1-V0) |
Recent emergence of portable electronic devices, such as contactless smartcards and digital cameras, requires nonvolatile data storage with low power consumption and fast write time. Low power is critical in contactless smartcard application because the smartcard has no internal battery and uses power delivered by RF signals from a card reader. Low power and fast write access are both required in digital cameras to prolong camera's battery lifetime and to store pictures in memory chips respectively. Ferroelectric random access memory (FeRAM) is a promising nonvolatile memory candidate for applications requiring low power consumption and fast write time [1].

1.1 Motivation

Semiconductor memories are classified into two groups: volatile memories and nonvolatile memories. Volatile memories retain data only when power is supplied while nonvolatile memories can retain data without power. Examples of nonvolatile memories are EEPROM, Flash Memory, and FeRAM.

EEPROM and Flash Memory store binary data in form of electrical charge on the floating gate of a transistor [2]. The stored charge is retained on the floating gate even after power is removed. The charge transferring to or from the floating gate, however, requires a strong electric field generated from a voltage in the range of 10V to 18V. In addition, the stored charge must be cleared first before writing new data to an EEPROM cell or to a Flash Memory cell. This makes write access time (~1ms) several orders of magnitude larger than read access time (50ns).
contrast. an FeRAM in today’s technology uses 3V power supply, and has equal read and write access time of 100ns. FeRAM uses a ferroelectric capacitor, which has a thin film of ferroelectric material sandwiched between two electrodes, to store binary data. Ferroelectric material has two stable spontaneous polarizations that represent two distinct states in its crystal structure. These two states can be easily reoriented (for write and read) by applying a voltage in the range of 1V to 3V.

Characteristics of EEPROM, Flash memory, and FeRAM are compared in Table 1-1 [3] [4]. It is observed that FeRAM has slower read access time and limited read endurance when compared with EEPROM and Flash Memory. On the other hand, FeRAM is superior in write access time, energy consumption, and write endurance. Therefore, FeRAM is suitable in applications that demand frequent memory write at fast speed and low energy dissipation.

<table>
<thead>
<tr>
<th>Nonvolatile Memory</th>
<th>Write (Read) Access Time</th>
<th>Energy / 32b Write (Read)</th>
<th>Write (Read) Endurance</th>
</tr>
</thead>
<tbody>
<tr>
<td>EEPROM</td>
<td>1ms - 10ms (50ns)</td>
<td>1μJ (150pJ)</td>
<td>10^6 (Infinity)</td>
</tr>
<tr>
<td>Flash Memory</td>
<td>10μs - 100μs (50ns)</td>
<td>2μJ (150pJ)</td>
<td>10^6 (Infinity)</td>
</tr>
<tr>
<td>FeRAM</td>
<td>100ns (100ns)</td>
<td>1nJ (1nJ)</td>
<td>10^{12} (10^{12})</td>
</tr>
</tbody>
</table>

Table 1-1: Characteristics of EEPROM, Flash Memory, and FeRAM

1.2 Thesis Objective

A use of one transistor and one ferroelectric capacitor memory cell (1T1C cell) is a key factor of achieving high density FeRAM. In this research, a 1T1C FeRAM testchip is designed and fabricated for the following three objectives:

1. To implement a fatigue-tracking reference generation scheme

A 1T1C FeRAM requires a reference signal for data sensing. Previous reference generation schemes tend to fatigue reference cells faster than memory cells [4]. The fatigue-tracking reference generation scheme is implemented in the testchip to balance fatigue effect evenly between reference cells and memory cells.
2. To design a current-steering sense amplifier compatible with the fatigue-tracking reference generation scheme

The current-steering sense amplifier design allows a reference current to be shared among several memory columns in the 1T1C FeRAM, and hence reduces the area overhead of reference generation.

3. To find a range of bitline-to-cell-capacitance ratio that maximizes the differential bitline voltage for sensing

The differential bitline voltage is correlated to the number of cells connected to each bitline and to the size of the ferroelectric capacitor in the cell.

1.3 Thesis Outline

The thesis is categorized into six chapters: Chapter 1 provides a brief introduction of FeRAM and defines research objectives. Chapter 2 introduces ferroelectric material characteristics, demonstrates how to use a ferroelectric capacitor to form a nonvolatile memory, and investigates FeRAM circuit design in cell structure, reference generation scheme, and sense amplifier. Chapter 3 provides design details of the memory array and its corresponding row circuitry in the testchip. Chapter 4 provides design details of the sense amplifier, the writeback circuit, the associated column circuitry, and two test structures in the testchip. Chapter 5 presents simulation and measurement results of the testchip. Finally, Chapter 6 gives conclusions of this research and provides directions for future work.
A nonvolatile memory cell is capable of storing two stable states that can be retained without power. Memory cells in FeRAM use ferroelectric capacitors to obtain this nonvolatile data storage characteristic.

This chapter provides a background for FeRAM design. Section 2.1 describes properties of ferroelectric materials. Section 2.2 introduces Q-V characteristic of a ferroelectric capacitor. Section 2.3 shows a ferroelectric fabrication process and illustrates two different ferroelectric capacitor structures. Section 2.4 discusses FeRAM circuit design, consisting of cell structure, memory architecture, reference generation scheme, and sense amplifier design. In addition, Section 2.4 illustrates two basic cell operations (write and read) with timing diagrams and shows a relationship between the differential bitline voltage (developed in read operation) and memory core parameters.

2.1 Ferroelectric Material

The bistability of ferroelectric material is a key factor of nonvolatile binary data storage. This characteristic is reviewed in this section. Then, the structures of two well-known ferroelectric materials are illustrated.

When a dielectric is placed in an electric field, positive and negative charges in the dielectric are displaced from their original positions. This charge displacement is called polarization. In normal dielectric, polarization disappears when the electric field is removed. In contrast,
ferroelectric materials have two spontaneous polarizations inherent to the crystal structure of materials. Spontaneous polarization can be retained when the electric field goes to zero. In addition, the direction of polarization can be reversed by changing the electric field orientation. As a result, the ferroelectric materials have two nonvolatile switchable stable states for data storage.

One of the well-established ferroelectric materials is lead zirconate titanate (PZT), with the formula of Pb(Zr,Ti)O₃. Central atom in a cell of PZT is either zirconium (Zr) or titanium (Ti), depending on the their proportions in the chemical formula. As shown in Figure 2-1 [4], PZT cell has two stable states named state ‘0’ and state ‘1’.

![Figure 2-1: Two stable states in PZT material: (a) state ‘0’ and (b) state ‘1’](image)

Another group of ferroelectric materials, investigated in recent years, is known as layered perovskites. One well-studied example is bismuth-layered perovskite (SBT), with the formula of SrBi₂Ta₂O₉. As shown in Figure 2-2 [5], bismuth oxide (BiO) layers are interleaved with
ferroelectric material in SBT. BiO layers help to minimize an interaction between the ferroelectric material and an electrode of a ferroelectric capacitor, which uses a film of ferroelectric material as dielectric.

![Figure 2-2: SBT crystal structure](image)

Compared to SBT, PZT provides larger polarization and requires lower process temperature [6]. On the other hand, SBT works well at lower voltage and gives better reliability characteristics compared to PZT [5]. Due to lower process temperature requirement, PZT is extensively used in present FeRAM manufacturing. Our testchip is also fabricated using PZT.

### 2.2 Q-V Characteristics of Ferroelectric Capacitor

Q-V characteristic of the ferroelectric capacitor, known as hysteresis loop, is characterized using a Sawyer-Tower circuit. The circuit, shown in Figure 2-3, is composed of a series connection of a ferroelectric capacitor ($C_{FE}$) and a linear capacitor ($C_{linear}$). When a sinusoidal voltage input ($V_{in}$) is applied to this series connection, an identical incremental charge ($Q$) appears on both $C_{FE}$ and $C_{linear}$ such that $Q$ is the product of $C_{linear}$ and $V_{out}$. When making $C_{linear}/C_{FE}$ greater than 100 [7], the voltage across $C_{FE}$ ($V_{cfe}$) can be approximated by $V_{in}$. 
Hysteresis loop of a ferroelectric capacitor is illustrated in Figure 2-4. It has two important parameters: a saturation charge ($Q_s$) and a remanent charge ($Q_r$). $Q_s$ is defined as charge on the capacitor when a maximum voltage ($V_{\text{max}}$) is applied across $C_{\text{FE}}$, and $Q_r$ is defined as charge remained after $V_{\text{cfe}}$ becomes 0V. As observed from the hysteresis loop, $C_{\text{FE}}$ has a charge of $+Q_r$ or $-Q_r$ when $V_{\text{cfe}}$ is 0V. By convention, $+Q_r$ corresponds to state ‘0’ and $-Q_r$ corresponds to state ‘1’. State ‘0’ switches to state ‘1’ when applying a negative voltage pulse across $C_{\text{FE}}$. The charge on $C_{\text{FE}}$ changes along $A \rightarrow B \rightarrow C$. Similarly, state ‘1’ switches to state ‘0’ by applying a positive voltage pulse across $C_{\text{FE}}$. The charge on $C_{\text{FE}}$ changes along $C \rightarrow D \rightarrow A$. 
The hysteresis loop usually shrinks with repeated cycling, a phenomenon referred to as fatigue [4]. Fatigue is one of ferroelectric capacitor degrading characteristics, and is defined as the gradual loss of charge with repeated cycling of the capacitor. As illustrated in Figure 2-5, both \( Q_s \) and \( Q_r \) of the hysteresis loop reduce with cycling. From memory circuit point of view, fatigue causes often-accessed cells to degrade faster than less-accessed ones [4]. In Section 2.4.4, a circuit scheme is proposed to balance the access rate of memory cells in FeRAM, and hence minimize the effect of fatigue.

![Figure 2-5: Effect of fatigue on hysteresis loop](image)

**2.3 Ferroelectric Fabrication Process**

Ferroelectric fabrication process consists of few steps that are ordered based on process temperature. As illustrated in Figure 2-6, the first step is the standard CMOS fabrication process, followed by adding ferroelectric layers and interconnects. This fabrication order avoids cross-contamination among different layers and allows for reliable integration of ferroelectric capacitors with standard CMOS transistors [3].

Ferroelectric layers can be used to fabricate either a planar capacitor or a stacked capacitor. The planar capacitor, shown in Figure 2-7(a) [3], is laid beside an access transistor. Mask area of this structure is the sum of capacitor area and transistor area. A top electrode in the planar capacitor is connected to the transistor’s storage node through metal interconnects and a bottom electrode is connected to a plateline.
The stacked capacitor, illustrated in Figure 2-7(b) [3], is placed on top of an access transistor. Mask area of this structure is less than the sum of capacitor area and transistor area. A top electrode in the stacked capacitor is connected to a plateline and a bottom electrode is connected to the transistor's storage node through a contact plug. To protect the contact plug from oxidation, an extra layer, an electrically conducting oxygen diffusion barrier, is added in the fabrication process [3].

Compared to a stacked capacitor, a planar capacitor uses a less complicated fabrication process. On the other hand, the stacked capacitor has higher mask area efficiency compared to the planar capacitor. Our testchip is fabricated using planar ferroelectric capacitors along with a conventional 0.35µm CMOS technology.
2.4 FeRAM Circuit Design

In this section, two basic memory cell structures that use ferroelectric capacitors for nonvolatile data storage are introduced. Then, two memory cell operations (write and read) are explained along with their timing diagrams. In addition, the differential bitline signal developed during read
operation is shown to be related to two memory core parameters: the bitline capacitance and the ferroelectric capacitance. Lastly, an architecture of a memory core is illustrated, followed by discussions of reference generation scheme and sense amplifier design.

2.4.1 FeRAM Cell

An FeRAM cell, similar to a DRAM cell, consists of an access transistor and a storage capacitor. Two well-known cell structures are 2T2C and 1T1C, as shown in Figure 2-8.

![Figure 2-8: FeRAM cell structure: (a) 2T2C and (b) 1T1C](image)

A. 2T2C cell structure

Each 2T2C cell consists of two ferroelectric capacitors, $C_{FE}$ and $C_{FE}$, and two access transistors. Bottom plates of the capacitors are connected to a common plateline (PL), and top plates are connected to a bitline pair (BL and $\overline{BL}$) via access transistors. $C_{FE}$ and $C_{FE}$ always store complement binary data: one is considered as a data bit and the other one as a reference for data sensing. During a read access, the differential voltage is developed between BL and $\overline{BL}$. By assuming $V_1$ as a bitline signal for data ‘1’ and $V_0$ as a bitline signal for data ‘0’, the differential voltage of $V_1-V_0$ is available for data sensing.
Each 1T1C cell is composed of one ferroelectric capacitor \( C_{FE} \) and one access transistor. The bottom plate of the capacitor is connected to a plateline (PL), and the top plate is connected to a bitline (BL) via an access transistor. Depending on the stored data, either \( V_1 \) or \( V_0 \) appears on the bitline in each read access. For data sensing, 1T1C cells require a reference voltage. Ideally, the reference voltage is an average of \( V_1 \) and \( V_0 \), which provides equal noise margin for data '1' and data '0'. The sensing voltage, therefore, becomes \( V_1/2 - V_0/2 \), half of the value found in the 2T2C cell.

Compared to the 1T1C cell, the 2T2C cell has doubling of sensing voltage that eases a sense amplifier design for 2T2C cells. On the other hand, the 1T1C cell (including overhead circuits of reference voltage generation) has smaller area because it uses half number of transistors and capacitors when compared to the 2T2C cell. Since cell area is critical in high density FeRAM, the 1T1C cell is expected to be employed in FeRAM beyond 1Mb [4]. In our testchip, all memory cells are in the 1T1C cell structure.

2.4.2 Memory Cell Operations

To use \( C_{FE} \) as a storage element in an FeRAM cell, the storage state in \( C_{FE} \) must be both writable and readable. The cell write operation and the cell read operation are described separately in the following.

A. Cell write operation

Each cell write operation involves five steps, as shown in Figure 2-9.
The steps are as follows:

I. BL is driven to $V_{DD}$ in writing data ‘1’ or to 0V in writing data ‘0’. At this moment, the initial state of $C_{FE}$ can be either ‘1’ or ‘0’.

II. WL is asserted to turn on the access transistor and to create a connection between BL and $C_{FE}$. A voltage of $-V_{DD}$ then appears across $C_{FE}$ for writing data ‘1’.

III. PL is pulsed to $V_{DD}$, and therefore $+V_{DD}$ appears across $C_{FE}$ for writing data ‘0’. PL is then pulled back to 0V.

IV. BL is driven to 0V while WL is still activated, and hence the voltage across $C_{FE}$ becomes zero. $C_{FE}$, therefore, moves to state ‘1’ if writing data ‘1’, or to state ‘0’ if writing data ‘0’.

V. WL is deactivated to turn off the access transistor, hence disconnecting $C_{FE}$ from BL.
B. Cell Read Operation

Each cell read operation involves six steps, as shown in Figure 2-10.

The steps are as follows:

I. BL is precharged to 0V when PRE is active.

II. WL is asserted to create a capacitor divider, consisting of $C_{BL}$ and $C_{FE}$, between PL and ground. $C_{BL}$ represents the parasitic capacitance of BL that is mainly due to the diffusion capacitance of access transistors on BL. $C_{FE}$, on the other hand, is a data-dependent
capacitance that can be approximated by $C_1$ if the stored data is '1' or $C_0$ if the stored data is '0', as shown in Figure 2-11.

When $PL$ is pulsed, $V_{DD}$ is divided between $C_{BL}$ and $C_{FE}$. BL rises from 0V to $V_{BL}$ which is either $V_1$ or $V_0$.

$$V_1 = \left[ \frac{1}{1 + C_{BL}/C_1} \right] \times V_{DD} \quad \text{for the stored data '1'} \quad \text{Equation (a)}$$

$$V_0 = \left[ \frac{1}{1 + C_{BL}/C_0} \right] \times V_{DD} \quad \text{for the stored data '0'} \quad \text{Equation (b)}$$

where $C_{FE}$ is approximated by either $C_1$ or $C_0$, depending on the stored data.

III. Sense amplifier is activated to drive BL to $V_{DD}$ if $V_{BL}$ is $V_1$ or to 0V if $V_{BL}$ is $V_0$. Since $C_{FE}$ has lost its storage state, the sensed data must be restored to an accessed cell. When restoring data '0', $+V_{DD}$ is applied across $C_{FE}$.

IV. WL remains active to restore data '1' to the accessed cell, such that $-V_{DD}$ is applied across $C_{FE}$.

V. BL is driven to 0V while WL is still activated, and hence the voltage across $C_{FE}$ becomes zero. $C_{FE}$, therefore, moves back to state '1' if the stored data is '1' or to state '0' if the stored data is '0'.

VI. WL is deactivated to turn off the access transistor, and hence disconnecting $C_{FE}$ from BL.
As indicated by Equations (a) and (b), both $V_1$ and $V_0$ are functions of $C_{BL}/C_{FE}$. The difference between $V_1$ and $V_0$, denoted as $\Delta V_{BL}$, is also a function of $C_{BL}/C_{FE}$ [8]. Figure 2-12 shows typical values of $V_0$, $V_1$, and $\Delta V_{BL}$ over a range of $C_{BL}/C_{FE}$. In Chapter 5, measurement results of $V_0$, $V_1$, and $\Delta V_{BL}$ vs. $C_{BL}/C_{FE}$ from our designed testchip are provided.

![Graph](image)

Figure 2-12: $V_0$, $V_1$, and $\Delta V_{BL}$ vs. $C_{BL}/C_{FE}$

### 2.4.3 FeRAM Architecture

FeRAM architecture is similar to DRAM architecture since both memories use similar cell structures, consisting of an access transistor and a storage capacitor. On the other hand, FeRAM architecture is distinct from DRAM architecture because the plateline in an FeRAM cell is pulsed during memory operation while the plateline in a DRAM cell is held at a constant voltage, such as $V_{DD}/2$. Therefore, FeRAM requires an implementation of a plateline pulsing circuit.

One well-known FeRAM architecture places platelines parallel to wordlines (WL/PL) in the memory core, as shown in Figure 2-13. In each cell operation, a row address decoder is shared to
select a pair of wordline and plateline, and hence a simple driver is added on each row to pulse the selected plateline. An advantage of the WL//PL architecture over the BL//PL (the bitline-parallel-plateline) architecture [4] is that unaccessed cells are not disturbed by selected wordlines and platelines. The designed testchip uses the WL//PL architecture in the memory core.

![WL//PL FeRAM architecture](image)

Figure 2-13: WL//PL FeRAM architecture

### 2.4.4 Reference Generation Scheme

A robust reference should be provided for distinguishing \( V_0 \) or \( V_1 \) developed during read operation. In the 2T2C cell structure, a reference is generated inside the cell. In contrast, the 1T1C cell structure requires an external reference generation. A constant reference voltage \( V_{ref} \), the average of \( V_0 \) and \( V_1 \), is not a good choice because \( V_0 \) and \( V_1 \) are both process-dependent and time-dependent. As indicated by Equations (a) and (b) in Section 2.4.2, \( V_0 \) and \( V_1 \) are functions of \( C_{BL}/C_{FE} \), where \( C_{BL} \) is a process-dependent capacitance and \( C_{FE} \) is a time-dependent capacitance due to fatigue [4]. Therefore, exact values of \( V_0 \) and \( V_1 \) are hard to determine. A variable reference, generated from dedicated reference cells in the memory core, is a preferred choice as the reference can track both process variations and fatigue. Reference generation
schemes for 2T2C cells and 1T1C cells are discussed below:

A. Reference generation scheme for 2T2C cells

The 2T2C cell has two ferroelectric capacitors storing complement binary data: one is used as a data bit and the other one as a reference for data sensing. Ferroelectric capacitors in the cell are always accessed simultaneously, and therefore are fatigued evenly. Moreover, physical proximity of the capacitors provides better process matching characteristics. A disadvantage of this scheme is double in cell area when compared with the 1T1C cell.

B. Reference generation scheme for 1T1C cells: using two reference rows

Figure 2-14 shows the conventional approach [9] of generating a reference voltage for the 1T1C FeRAM. Two reference rows are added in the memory core along with their dedicated reference wordlines (RWL_odd and RWL_even) and platelines (RPL_odd and RPL_even). RWL_even and RPL_even control access to a row of reference cells that are connected to BL_i, and the reference row is activated when any even-numbered memory row is selected. Similarly, RWL_odd and RPL_odd control access to a row of reference cells that are connected to BL_i, and the reference row is activated when any odd-numbered memory row is selected. Therefore, each sense amplifier has a memory bitline voltage and a reference voltage as inputs for data sensing.

In this scheme, memory cells and reference cells are accessed at different rates, and hence are fatigued at different rates. For example, when accessing n sequential even-numbered memory rows in the core, each reference cell is accessed n times more than each memory cell. As a result, this reference generation scheme is susceptible to a fatigue imbalance between memory cells and reference cells.
C. Reference generation scheme for ITIC cells: using a reference column pair

This scheme includes a dedicated pair of reference columns (RBL and $\overline{RBL}$) in the memory core [7], as shown in Figure 2-15(a). Reference cells, assigned to each row, have the same access rate as those of memory cells. Therefore, this reference generation scheme is immune to fatigue imbalance between memory cells and reference cells.

As seen in Figure 2-15(b), each reference cell pair consists of a cell connected to RBL and a cell connected to $\overline{RBL}$. Cells on RBL always have a stored data ‘1’, and cells on $\overline{RBL}$ always have a stored data ‘0’. During read operation, $V_1$ is developed on RBL and $V_0$ is developed on $\overline{RBL}$. The read voltage on BL is either $V_1$ or $V_0$ if there is a capacitive balance among BL, RBL, and $\overline{RBL}$. A reference voltage $V_{\text{ref}}$, obtained by shorting RBL and $\overline{RBL}$, becomes the average of $V_1$ and $V_0$. 

![Figure 2-14: Reference generation scheme using two reference rows](image-url)
V_{ref} is usually shared among several memory columns to reduce memory core area. In this reference generation scheme, a pair of RBL and RBL is connected to several sense amplifiers, and each BL is fed to one sense amplifier. The sense amplifier adds its input capacitance to the pair of RBL and RBL, and therefore there is a capacitive imbalance among RBL, RBL, and BL. In Chapter 4, a sense amplifier is designed to solve this bitline loading mismatch problem.

### 2.4.5 Sense Amplifier Design

During read operation, the sense amplifier determines the logic value of the stored data by comparing the bitline voltage (V_{BL}) against a reference voltage (V_{ref}). This voltage difference is amplified to V_{DD} if V_{BL} is larger than V_{ref} (for the stored data ‘1’) or to 0V if V_{BL} is smaller than V_{ref} (for the stored data ‘0’). The full-swing output (V_{DD} or 0V) is then passed to the memory column circuit for “data read” and to the writeback circuit for “data restore”.

A sense amplifier in FeRAM must satisfy two general requirements:

1. It must reproduce the stored data for writeback, such that BL is driven to V_{DD} to restore data ‘1’, or to 0V to restore data ‘0’.
2. It must have a compact layout to fit in the column pitch. Alternatively, several adjacent sense amplifier layout are merged to share the column pitch of several columns.

Sense amplifiers used in the 2T2C FeRAM and the 1T1C FeRAM are described in the following.

A. *Cross-Coupled Sense Amplifier (CCSA) for the 2T2C FeRAM*

A schematic of the CCSA is shown in Figure 2-16. It has a pair of cross-coupled inverters, such that control signals ‘sap’ and ‘san’ turn on connections to $V_{DD}$ and ground respectively. The CCSA has a total of six transistors and its small silicon area allows it to easily fit in a column pitch [10].

![Cross-coupled sense amplifier](image)

Cells in the 2T2C FeRAM provide differential bitline signals on BL and $\overline{BL}$, which are connected to internal nodes ‘sen’ and ‘senn’ of the CCSA. When data sensing is complete, full-swing signals are generated on BL and $\overline{BL}$ automatically for data writeback.

B. *Current-Steering Sense Amplifier (CSSA) for the 1T1C FeRAM*

The CSSA is designed for the 1T1C FeRAM. Signals on BL, RBL, and $\overline{RBL}$ are buffered to the
CSSA indirectly, and hence remain unchanged until data sensing is done. This feature allows sharing of a reference signal among multiple BLs in the memory core. A schematic of the CSSA [7] is shown in Figure 2-17.

The circuit operation is described in the following.

1. Both nodes 'sen' and 'senn' are precharged to 0V before data sensing starts.
2. During read operation, $V_1$ develops on RBL and $V_0$ develops on $\overline{RBL}$. $V_{\text{ref}}$ is then generated
by shorting RBL and RBL. At the same time, \( V_x \) develops on BL. When the signal ‘sdn’ is asserted, \( V_x \) and \( V_{\text{ref}} \) are buffered to the CSSA to generate \( I_x \) and \( I_{\text{ref}} \) respectively.

3. \( I_x \) feeds to the node ‘sen’ and \( I_{\text{ref}} \) feeds to the node ‘senn’. \( I_x \) and \( I_{\text{ref}} \) then compete to pull up their corresponding nodes. Since the larger current can pull up its corresponding node faster, \( \Delta V \) is created between ‘sen’ and ‘senn’.

4. The signal ‘sapn’ is asserted to activate the cross-coupled inverter in the CSSA, which eventually pulls one node to \( V_{\text{DD}} \) and the other node to ground.

As mentioned in Section 2.4.4, a capacitive imbalance exists among BLs, RBLs, and \( \overline{\text{RBL}} \)s. A pair of RBL and \( \overline{\text{RBL}} \) feeds to several sense amplifiers, such that each sense amplifier contributes its input capacitance to the pair. Therefore, the pair has an aggregate extra loading \( C_{sa} \) as illustrated in Figure 2-17. One proposed solution [7] is to add an extra capacitance \( (C_{\text{ext}}) \) on each BL to compensate for \( C_{sa} \). This solution, however, is hard to implement since it is difficult to estimate \( C_{sa} \) accurately.

In the testchip, an improved current-steering sense amplifier (ICSSA) [4] is designed to solve this bitline loading mismatch problem. Design details of the ICSSA will be discussed in Chapter 4.

2.5 Summary

A \( \text{IT\text{IC}} \) ferroelectric memory cell consists of a ferroelectric capacitor and an access transistor, where the capacitor stores a binary data in the form of bistable and switchable charge. The capacitor charge decreases as a result of repeated cycling, a phenomenon known as fatigue.

FeRAM circuit design involves choosing cell structure, memory architecture, reference generation scheme, and sense amplifier. Our designed FeRAM testchip uses (1) a \( \text{IT\text{IC}} \) cell because of small cell size, (2) a WL/PL architecture because of no disturbance on unaccessed cells, (3) a dedicated column pair for reference generation because of immunity to fatigue imbalance among memory cells and reference cells, and (4) an ICSSA because of capacitive balance among BLs, RBLs, and \( \overline{\text{RBL}} \)s.
Chapter 3

Testchip Design: Memory Core and Row Circuitry

A testchip architecture, as shown in Figure 3-1, is proposed to implement and evaluate the design objectives outlined in Chapter 1. This chapter presents the design details of the memory core and its corresponding row circuitry to implement a fatigue-tracking reference generation scheme and correlate the differential bitline signal with memory core parameters. Next chapter will present the design details of remaining blocks in the testchip.

3.1 Memory Core

The memory core is an array of 1T1C cells in 256 rows and 64 columns. Moreover, there are
eight pairs of reference columns, such that each pair is assigned to eight memory columns shown in Figure 3-2. Since reference cells and memory cells on the same row share the same pairs of wordline (WL) and plateline (PL), both have identical fatigue on their ferroelectric capacitors [4].

Figure 3-2: Reference cells in the memory core

Figure 3-3 illustrates the memory core architecture, which implements a range of bitline capacitance ($C_{BL}$) and a range of ferroelectric cell capacitance ($C_{FE}$). The memory core is designed to have four distinct bitline lengths and four different sizes of cell capacitor. The shortest bitline corresponds to 64 rows of 1T1C cells while the longest bitline corresponds to 256 rows of 1T1C cells. $C_{BL}$, therefore, can take one of four values: from one to four times the minimum $C_{BL}$. Similarly, the smallest capacitor area is $1\mu m^2$ (1X) and the largest area is $4\mu m^2$ (4X), such that all cells have a row pitch of 5.5$\mu m$ and a column pitch of 2.75$\mu m$. $C_{FE}$, therefore, can take one of four values: from one (1X) to four times (4X) the minimum $C_{FE}$. When the testchip is in the test mode, up to three rows can be accessed among four adjacent rows, and hence the maximum available $C_{FE}$ is increased to 8X.
Using the designed memory core, a total of 32 \( C_{BL}/C_{FE} \) are provided for experimental purposes. The \( C_{BL}/C_{FE} \) range is from 0.1 to 2.98, as shown in Figure 3-4.

3.2 Row Circuitry

The row circuitry, as shown in Figure 3-5, is used to select an addressed row and activate its corresponding WL and PL in the memory core. It is composed of a row shift register, a row predecoder, a row decoder, WL drivers, and PL drivers.
A. Row Shift Register

The row shift register is composed of two different master-slave flip-flops: DFF1 and DFF0. Schematics of DFF1 and DFF0 [11] are shown in Figure 3-6. When DFFs are in normal mode, an input ‘D’ shifts to an output ‘Q’ at the falling edge of clock ‘ϕ’. When DFFs are in reset mode, DFF1 is initialized to have a high output and DFF0 is reset to have a low output.

A 64-bit row shift register, shown in Figure 3-7, is implemented to address 256 rows in the memory core. The shift register is composed of one DFF1 and 63 DFF0s connected in a loop, in which each DFF points to one row block (a set of four adjacent rows). When the signal ‘resetn’ is
asserted, DFF1 has a high output while all other DFF0s have low outputs. Hence, the first block (rows 1 to 4) is selected. When 'resetn' is deactivated, the active high output of DFF1 shifts sequentially along the register with each cycle of 'rowclk' and points to the next row block.

\[ \text{Figure 3-7: 64-bit row shift register} \]

\[ \text{Figure 3-7: 64-bit row shift register} \]

**B. Row Predecoder**

The schematic and the truth table of the row predecoder are provided in Figure 3-8. The predecoder has three inputs 'a1' to 'a3', in which 'a3' is low in normal mode and high in test mode. When the circuit is in normal mode, only one row is accessed in the selected row block. When the circuit is in test mode, two or three rows are accessed simultaneously to have parallel-connected ferroelectric cell capacitors. For instance, an equivalent $C_{FE}$ is 5X when a 1X cell and a 4X cell are accessed at the same time.
C. Row Decoder, WL Driver, and PL Driver

The row decoder, shown in Figure 3-9, activates the selected pair(s) of WL and PL in the memory core using four control signals: the row shift register output ('Q'), row predecoder outputs ('s1' to 's4'), a WL strobe input ('wlstb'), and a PL strobe input ('plstb'). 'Q' selects one of 64 row blocks in the memory core while 's1' to 's4' select up to three rows in the selected row block. When 'wlstb' and 'plstb' are asserted, the corresponding pair(s) of WL and PL is buffered to access the selected row(s). The WL driver is designed to provide equal rise time and fall time of
Ins for WL while the PL driver is designed to provide equal rise time and fall time of 10ns for PL.

Among components in the row circuitry, the PL drivers take the largest area. In order to pitch match the PL driver with the row pitch of the memory core (5.55\(\mu\)m), WL and PL drivers of two consecutive rows are laid out to share the row pitch of two rows, as illustrated in Figure 3-10.
3.3 Summary

The memory core and its corresponding row circuitry of the designed testchip are described. Highlights of these two circuits are:

- **Memory Core**
  
  Each reference column pair is assigned to eight memory columns in the core to balance fatigue among reference cells and memory cells.
  
  Memory columns and reference columns are designed to provide four distinct $C_{BL}$.
  
  Memory cells and reference cells are designed to provide four distinct $C_{FE}$.

- **Row Circuit**

  The row predecoder can activate up to three rows in the selected row block to extend the range of $C_{FE}$ by a factor of 2 for experimental purposes.
Chapter 4

Testchip Design: Sense Amplifier and Column Circuitry

The testchip architecture is shown in Figure 4-1 again. The previous chapter presented the design details of the memory core and its corresponding row circuitry. This chapter presents the design details of the sense amplifier, the writeback circuit, and their associated column circuitry.

4.1 Sense Amplifier

In Section 2.4.5, the current-steering sense amplifier design (CSSA) is found to have a bitline loading mismatch problem. In the testchip, an improved current-steering sense amplifier design (ICSSA), as illustrated in Figure 4-2, is implemented. The ICSSA is incorporated with a
reference column pair (RBL and \overline{RBL}) shared by eight memory columns (BLs). RBL and \overline{RBL} are connected to memory cells with stored data '1' and '0' respectively. The voltage developed on BL, \(V_1\) for a stored '1', and \(V_0\) for a stored '0', are identical to those of RBL and \overline{RBL} because cells on BL, RBL, and \overline{RBL} share the same WL and PL, and fatigue evenly.

![Diagram of memory cells and sense amplifiers](image)

Figure 4-2: Improved current-steering sense amplifier

At the beginning of sensing operation, ‘pre’ is activated to reset nodes ‘sen’ and ‘senn’ of the ICSSA to ground. After asserting ‘sdn’, the voltage developed on BL (\(V_x\)), RBL (\(V_1\)), and \overline{RBL} (\(V_0\)) are converted to \(I_x\), \(I_1\), and \(I_0\) using same-sized PMOS transistors. \(I_1\) and \(I_0\) are then summed to produce \(I_{\text{ref}}\). By activating ‘sapn’, \(I_x\) and \(I_{\text{ref}}\) are mirrored to generate \(I_{\text{mx}}\) and \(I_{\text{mref}}\), such that \(I_{\text{mx}}\) is equal to \(I_x\) and \(I_{\text{mref}}\) is half of \(I_{\text{ref}}\). \(I_{\text{mx}}\) and \(I_{\text{mref}}\) start sinking charge from opposite drain nodes (‘sen’ and ‘senn’) of the cross-coupled PMOS pair in the ICSSA and compete to pull their respective nodes down. The difference between \(I_{\text{mx}}\) and \(I_{\text{mref}}\) creates \(\Delta V\) between ‘sen’ and senn’, and finally the cross-coupled inverter pulls one node to \(V_{DD}\) and the other one to ground.
In this sensing scheme, BL, RBL, and RBL buffer their bitline voltages to ICCSA via identical PMOS transistors, and hence the capacitive balance is maintained among BL, RBL, and RBL. This bitline voltage buffering isolates RBL and RBL from output signals of ICCSA, and therefore Iref can be shared among several BLs in the memory core. The sensing speed of this design is limited by the capacitive load at the common node ‘share’ of the reference current mirror, which is proportional to the number of BL mirroring Iref. A larger number of BL implies higher capacitance at ‘share’, and hence longer rise time for the voltage at ‘share’. In the testchip, each pair of RBL and RBL is assigned to eight BLs to achieve a cycle time of 100ns in simulations.

![Figure 4-3: ICSSA simulation results: (left) read ‘1’ and (right) read ‘0’](image)

Results of HSPICE simulation, shown in Figure 4-3, illustrate critical currents and node voltages in the ICSSA as functions of time. In reading data ‘1’, I.mx is smaller than I_mref, and hence V_sen is charged up faster than V_senn and pulled up to VDD. In reading data ‘0’, I_mx is larger than I_mref, and therefore V_sen is pulled down to ground. In both cases, the sense operation is completed less than 6ns from the time of activating ‘sdsn’.

### 4.2 Writeback Circuit

Since FeRAM read operation is destructive, the writeback circuit, as shown in Figure 4-4, is designed to restore data to accessed cells at the end of operation. During data writeback, a control
signal ('wb') and its complement ('wbn') are asserted. For the reference column pair, $V_{DD}$ is
gated to RBL through a PMOS transistor while ground is gated to $\overline{RBL}$ through an NMOS
transistor. The cells on RBL and $\overline{RBL}$ are, therefore, restored as data '1' and '0' respectively.
The writeback circuit on the memory column has an inverting property, and thus the circuit input
is connected to 'senn' of the ICSSA. In order to balance capacitive loading between 'sen' and
'senn', a data read buffer is connected to 'sen'.

![Figure 4-4: Writeback circuit schematic (in solid lines)](image)

### 4.3 Column Circuitry

The column circuitry, as shown in Figure 4-5, is used to activate a memory operation (data read,
data write, bitline signal monitor, or bitline signal overwrite) on the selected column in the
memory core.

A 16-bit column shift register, similar to the row shift register discussed in Section 3.2, uses
'colclk' and 'resetn' to access a column block (a set of four adjacent columns) in the memory
core. The predecoder then chooses one column in the selected block using 'b1' and 'b2'. After
that, the column decoder generates a control signal to initiate a memory operation on the
addressed bitline based on 'rwn' (read/write signal), 'wb' (writeback signal), and 'feed' (bitline
overwrite signal). Before each memory access, all BL, RBL, and RBL are reset to ground. This zero voltage precharge scheme ensures a sufficient voltage exists across the accessed ferroelectric cell capacitor for full switching [7]. Details of the column circuitry are provided in Appendix C.

In the testchip, a monitor circuit and an overwrite circuit are designed for experimental purposes. The monitor circuit, shown in Figure 4-6, is used to measure voltages on RBL and RBL (V_{RBL} and V_{RBL}). The circuit is a PMOS source follower (consisting of a PMOS transistor, a transmission gate, and an off-chip resistor 1MΩ), and has an input V_{RBL} (V_{RBL}) and an output V_{RBL} (V_{RBL}). V_{RBL} and V_{RBL} (V_{RBL} and V_{RBL}) have a one-to-one correspondence because the monitor circuit demonstrates a simulated linear V_in - V_out relationship over an input voltage range of 0V and 2.1V, such that V_{RBL} (V_{RBL}) is within this range. As a result, V_{RBL} (V_{RBL}) can be determined by a measured output V_{RBL} (V_{RBL}). In the testchip, V_{RBL} (V_{RBL}) is multiplexed to serve all RBLs (RBLs) in the memory core to reduce the number of package pins. The voltage on the selected RBL and (RBL) is monitored after the transmission gate TG1 turns on.

![Figure 4-5: Column circuitry block diagram](image-url)
The overwrite circuit, as shown in Figure 4-6, is used to feed an external analog voltage to the selected bitline. In normal memory operation, the circuit is kept idle, and hence the bitline voltage is not interrupted. In case of a cell failure, the circuit is activated to supply analog inputs to the ICSSA for measuring its sensitivity. Similar to the monitor circuit, a set of overwrite circuit’s inputs (V_{BLi} and V_{BLj}) is multiplexed to serve all bitlines in the memory core. The voltage on the selected bitline is overwritten after the transmission gate TG2 turns on.

![Diagram of Monitor and Overwrite Circuits](image)

**Figure 4-6: Monitor and overwrite circuits**

### 4.4 Test Structures

**A. Ferroelectric Capacitor**

Ferroelectric capacitors, as shown in Figure 4-7, were implemented in the test chip for hysteresis loop measurement. The capacitors, organized in an array of eight by eight, are connected in parallel to include peripheral parasitic capacitance in the measurement [12]. The parallel-connected capacitors are characterized using the Sawyer-Tower circuit (refer to Section 2.2) along with a 10nF linear capacitor and a 1kHz sinusoidal source with 3V amplitude.
B. **Ring Oscillator**

A ring oscillator was included in the testchip to monitor the process delay characteristics. The circuit is composed of 101 minimum-sized inverters ($W_p/L_p = 2.2\mu m/0.5\mu m$ and $W_n/L_n = 1.1\mu m/0.4\mu m$) along an output buffer, as shown in Figure 4-8. A large number of inverters ensures the oscillation period be in a measurable range [13].

![Figure 4-7: Ferroelectric capacitor sample](image)

![Figure 4-8: Ring oscillator](image)

### 4.5 Layout Design

**A. Layout of the ICSSA and the column circuitry**

In order to pitch match the ICSSA with the column pitch of the memory core ($2.75\mu m$), the ICSSA and the column circuitry of each four adjacent BLs are laid out to share the column pitch.
of five columns (4 BLs plus 1 of RBL or RBL). For example, the circuits of BL1 (labelled as ‘A’ and ‘C’ in Figure 4-9) share the column pitch of BL1-BL4 and RBL. Figure 4-9 also shows that the circuits of RBL and RBL (labelled as ‘E’) are placed at the center and have the column pitch of ten columns (BL1-BL8, RBL, and RBL).

<table>
<thead>
<tr>
<th>Label</th>
<th>Block</th>
<th>Bitline</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>ICSSA, Writeback, Read &amp; Write, Monitor, and Overwrite</td>
<td>BL1</td>
</tr>
<tr>
<td>B</td>
<td>ICSSA, Writeback, Read &amp; Write, Monitor, and Overwrite</td>
<td>BL1</td>
</tr>
<tr>
<td>C</td>
<td>Column Decoder</td>
<td>BL1 &amp; BL2</td>
</tr>
<tr>
<td>D</td>
<td>ICSSA, Writeback, Read &amp; Write, Monitor, and Overwrite</td>
<td>BL1</td>
</tr>
<tr>
<td>E</td>
<td>ICSSA, Writeback, Read &amp; Write, Monitor, and Overwrite</td>
<td>BL1</td>
</tr>
<tr>
<td>F</td>
<td>Column Decoder</td>
<td>BL5 &amp; BL6</td>
</tr>
<tr>
<td>G</td>
<td>V-I converter of ICSSA, Writeback, Monitor &amp; Overwrite, and Column Decoder</td>
<td>RBL &amp; RBL</td>
</tr>
<tr>
<td>H</td>
<td>ICSSA, Writeback, Read &amp; Write, Monitor, and Overwrite</td>
<td>BL3</td>
</tr>
<tr>
<td>I</td>
<td>ICSSA, Writeback, Read &amp; Write, Monitor, and Overwrite</td>
<td>BL4</td>
</tr>
<tr>
<td>J</td>
<td>Column Decoder</td>
<td>BL3 &amp; BL4</td>
</tr>
<tr>
<td>K</td>
<td>ICSSA, Writeback, Read &amp; Write, Monitor, and Overwrite</td>
<td>BL7</td>
</tr>
<tr>
<td>L</td>
<td>ICSSA, Writeback, Read &amp; Write, Monitor, and Overwrite</td>
<td>BL8</td>
</tr>
<tr>
<td>M</td>
<td>Column Decoder</td>
<td>BL7 &amp; BL8</td>
</tr>
</tbody>
</table>

Figure 4-9: Layout of ICSSA and a column circuitry (for two column blocks)
B. Entire testchip layout

A layout and a die picture of the testchip are shown in Figure 4-10. The testchip occupies a total area of \(0.9\text{mm}^2\) \((0.47\text{mm} \times 1.91\text{mm})\). A pie chart of the area distribution shows that 46\% of the testchip area is used for data storage.

\[
\text{Row Circuitry: } 7.5\%
\]
\[
\text{Column Circuitry: } 9.0\%
\]
\[
\text{Amplifiers: }
\]
\[
\text{Memory Core: } 46.0\%
\]

Figure 4-10: (top) testchip layout, (bottom left) die picture, and (bottom right) area distribution.

† Testchip package assignment is provided in Appendix A.
4.6 Summary

The sense amplifier, the writeback circuit, the associated column circuitry, and two test structures of the designed testchip are described. Highlights of these circuits are:

- **Sense Amplifier**
  The sense amplifier converts bitline voltages to current signals before data sensing to (1) maintain balanced capacitive loading among memory bitlines and reference bitlines, (2) generate an equal noise margin reference current, and (3) allow the reference current to be shared among eight memory columns in the memory core.

- **Writeback Circuit**
  The writeback circuit restores data to accessed cells at the end of read cycle.

- **Monitor Circuit**
  The monitor circuit captures a signal on the selected bitline for bitline voltage measurement.

- **Overwrite Circuit**
  The overwrite circuit overwrites a signal on the selected bitline for characterizing the sense amplifier design.

- **Test Structures**
  Parallel-connected ferroelectric capacitors are implemented for hysteresis loop measurement. In addition, the ring oscillator is included for monitoring the process delay characteristics.
Chapter 5
Simulation and Measurement Results

This chapter presents simulation and measurement results of the designed testchip. Simulations are performed using HSPICE in conjunction with a pulse-based, parallel-element macromodel for ferroelectric capacitors [12], and measurements are performed using VXI test system at the University of Toronto (refer to Appendix B).

There are five types of simulations and measurements performed on the testchip.

1. Functional Test: to verify the design functionality
2. Bitline Voltage Measurement: to identify the differential bitline voltage ($\Delta V_{BL}$) as a function of $C_{BL}/C_{FE}$
3. Sense Amplifier Measurement: to determine the operating region of the improved current-steering sense amplifier design (ICSSA)
4. Hysteresis Loop Measurement: to characterize ferroelectric capacitor samples
5. Ring Oscillator Measurement: to determine the process delay characteristics

5.1 Functional Test

The designed testchip supports two memory operations: data write and data read. Control signal waveforms of these two operations are shown in Figure 5-1. As mentioned in Section 3.1, the memory core is composed of cells with four distinct ferroelectric capacitor sizes and four different bitline lengths. To verify circuit functionality on all types of cells, each cell in the memory core is subjected to a sequence of six operations: Write ‘1’ (W1) $\rightarrow$ Read (R) $\rightarrow$ Read (R) $\rightarrow$ Write ‘0’ (W0) $\rightarrow$ Read (R) $\rightarrow$ Read (R). The first R after each W1 or W0 is to confirm a
Write/Read Cycle

1. precharge a bitline and a sense amplifier
2. drive a wordline and a plateine
3. activate a sense amplifier
4. activate a writeback circuit
5. activate a data write circuit
6. activate a data read circuit

Figure 5-1: Control signal waveforms of data write and data read

successful data write while the second R is to confirm a successful data writeback.

Waveforms of 'data_in' (data input for W) and 'data_out' (data output of R) for one memory cell are shown in Figure 5-2. Both simulation and measurement results confirm that 'data_out' in R are consistent with 'data_in' in both W1 and W0.

Simulation results suggest an access time of 50ns and a cycle time of 100ns. Measurement results, however, provide slower speed characteristics due to the minimum time step of the VXI tester (= 6.25ns). The measured access time and cycle time are found as 62.5ns and 130ns respectively.
One of the design objectives for this research is to investigate the relationship between $\Delta V_{\text{BL}}$ and $C_{\text{BL}}/C_{\text{FE}}$. In the designed testchip, a monitor circuit was included for bitline voltage measurement (refer to Section 4.3) and the memory core was implemented to provide 32 $C_{\text{BL}}/C_{\text{FE}}$ (refer to Section 3.1).

$\Delta V_{\text{BL}}$ is the difference of two reference bitline voltages ($V_{\text{RBL}}$ and $V_{\overline{\text{RBL}}}$). $V_{\text{RBL}}$ and $V_{\overline{\text{RBL}}}$ are mapped from the monitor circuit outputs of RBL and $\overline{\text{RBL}}$ ($V_{\text{RBL0}}$ and $V_{\overline{\text{RBL0}}}$) based on the circuit DC characteristic. In the testchip, an extra copy of the monitor circuit was implemented.
for characterization. The circuit input and output, as shown in Figure 5-3, are connected to ‘refin’ and ‘refout’ respectively. A set of DC voltages, ranging from 0V to 3V in steps of 0.1V, was applied to ‘refin’ and the corresponding output was recorded from ‘refout’. Results of simulation and measurement for two test samples demonstrates a linear DC characteristic of the monitor circuit over an input range of 0V - 2.1V.

![Figure 5-3: DC characteristic of the monitor circuit](image)

When measuring $V_{\overline{RBL}}$ and $V_{\overline{RBL}}$ from RBL and $\overline{RBL}$, the sense amplifiers and writeback circuits in the testchip are disabled to prevent interruptions on $V_{RBL}$ and $V_{\overline{RBL}}$. Control signals of measuring $V_{RBL}$ and $V_{\overline{RBL}}$ are shown in Figure 5-4.

![Figure 5-4: Control signals of bitline voltage measurement](image)

1. precharge a bitline and a sense amplifier
2. drive a wordline and a plateline
3. keep a sense amplifier and a writeback circuit be off
4. activate a bitline monitor circuit
Simulated and measured results of $V_{RBL}$, $V_{RBL}'$, and $\Delta V_{BL}$ vs. $C_{BL}/C_{FE}$ are shown in Figure 5-5. Two points are observed: (1) $V_{RBL}$ and $V_{RBL}'$ decrease as $C_{BL}/C_{FE}$ increases, and (2) a range of $C_{BL}/C_{FE}$ exists for each value of $\Delta V_{BL}$ between 0.2V and 0.8V. As an example, a range of $C_{BL}/C_{FE}$ was identified to produce $\Delta V_{BL}$ greater than 0.4V. Results, summarized in Table 5-1, show that both simulations and measurements have the similar size of range, where the minimum (maximum) $C_{BL}/C_{FE}$ corresponds to the fastest speed (the highest density) implementation.

Discrepancies found between the simulated and measured curves are partly due to process variations and partly due to deviation in ferroelectric capacitor characteristics.
### Table 5-1: A range of $C_{BL}/C_{FE}$ for $\Delta V_{BL}=0.4V$

<table>
<thead>
<tr>
<th></th>
<th>$\Delta V_{BL} &gt; 0.4V$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>From $(C_{BL}/C_{FE})$</td>
</tr>
<tr>
<td>Measurement (Sample 1)</td>
<td>0.2</td>
</tr>
<tr>
<td>Measurement (Sample 2)</td>
<td>0.21</td>
</tr>
<tr>
<td>Simulation</td>
<td>0.2</td>
</tr>
</tbody>
</table>

#### 5.3 Sense Amplifier Measurement

An overwrite circuit is implemented to characterize the ICSSA. As shown in Figure 5-6, $V_{BLi}$ is applied to overwrite signals on BL and RBL while $V_{BLi}$ is supplied to overwrite signals on RBL.

During the ICSSA measurement, a set of DC voltages, ranging from 0.25V to 2V in steps of 0.25V, was applied to $V_{BLi}$. For each value of $V_{BLi}$, a range of $V_{BLi}$ was determined to have ICSSA outputs as '0' and '1'. As illustrated in Figure 5-7, the maximum $V_{BLi}$ for each $V_{BLi}$ (marked by symbol 0) was identified to have the output '0' and the minimum $V_{BLi}$ (marked by
symbol x) was identified to have the output '1'. The dashed area (the region between the straight lines with symbols 0 and x) is a meta-stability region of the ICSSA, where ICSSA output is undetermined. Ideally, the ICSSA has the output '0' if $V_{BLi}$ is smaller than $V_{BLi}$ and has the output '1' if $V_{BLi}$ is larger than $V_{BLi}$. This characteristic is represented by the equation of $V_{BLi} = V_{BLi}$ (or $\Delta V_{BL} = 0$) and shown as a thick straight line in Figure 5-7.

From ICCSA measurements, the values of $V_{BLi}$ farthest from the ideal line are 0.4V (for output '0') and 0.22V (for output '1'). Considering these two cases, the ICSSA guarantees to function properly when $\Delta V_{BL}$ is smaller than -0.4V (threshold line for output '0') or larger than 0.4V (threshold line for output '1').

The asymmetry of the meta-stability region observed in Figure 5-7 is due to mismatches of the V-to-I converters and the current mirrors in the ICSSA (refer to Figure 4-2). V-to-I converters and
current mirrors have been laid out with the same orientation. However, their physical separation (each pair of RBL and RBL is shared by eight BLs) introduces mismatch in their circuit characteristics [14]. In addition, the matching accuracy of simple current mirrors is susceptible to the effect of channel-length modulation. To reduce this adverse effect, cascode current mirrors can be used in the design at the price of larger circuit area.

In Figure 5-7, bitline voltage measurement results of 1X cells to 4X cells are also plotted. It is observed that all measured values (‘+’, ‘0’, ‘Δ’, and ‘□’) are far away from the meta-stability region, and therefore the ICSSA has an adequate noise margin of data sensing.

### 5.4 Hysteresis Loop Measurement

Ferroelectric capacitor samples were implemented for hysteresis loop measurement using the Sawyer-Tower circuit (refer to Section 4.4). This measurement provides a mean to re-calibrate the ferroelectric capacitor model for future designs. Hysteresis loops obtained from both measurements and simulations are shown in Figure 5-8. It is observed that the measured hysteresis loops are shifted up slightly from the simulated ones. However, this does not create significant error in simulations. As illustrated in Table 5-2, the simulated values of $Q_1$ and $Q_0$ (the capacitor charge transferred to BL during reading data ‘1’ and ‘0’ respectively) are found to be very close to their corresponding measured values. Small difference in percentage (~8%) confirms the simulated $V_{RBL}$ (or $V_{RBL}$) be similar to the measured $V_{RBL}$ (or $V_{RBL}$).

![Figure 5-8: Hysteresis loop measurement results](image-url)
A ring oscillator with 101 minimum-sized inverters was implemented to measure the inverter delay. This delay measurement is employed as a metric for comparing the transistor model and the actual process. The measured delay values for three test samples are summarized in Table 5-3. Comparison of the inverter delay values among measurements and three corner simulations is shown in Figure 5-9. It is observed that the percentage of difference between the average measured delay and the typical corner simulated delay is 4.2%. This small difference suggests that the transistor model characterizes the process accurately.

<table>
<thead>
<tr>
<th></th>
<th>Sample 1</th>
<th>Sample 2</th>
<th>Sample 3</th>
<th>Average</th>
</tr>
</thead>
<tbody>
<tr>
<td>Delay per Inverter (ps)</td>
<td>82.3</td>
<td>80.8</td>
<td>81.2</td>
<td>81.4</td>
</tr>
</tbody>
</table>

Table 5-3: Delay measurement results

5.6 Summary

Functionality and performance of the designed testchip have been verified in both simulations and measurements. Results are summarized as below:

- Functional Test
  Measurement results confirm the functionality of the fatigue-tracking reference generation
scheme and the ICSSA design. The results also show that the designed testchip has an access time of 62.5ns and a cycle time of 130ns.

- **Bitline Voltage Measurement**
  
  \( V_{RBL} \), \( V_{RBL} \), and \( \Delta V_{BL} \) are strongly related to \( C_{BL}/C_{FE} \), such that (1) both \( V_{RBL} \) and \( V_{RBL} \) decrease as \( C_{BL}/C_{FE} \) increases, and (2) a range of \( C_{BL}/C_{FE} \) can be identified to produce a specific \( \Delta V_{BL} \) for data sensing.

- **Sense Amplifier Measurement of the ICSSA**
  
  The ICSSA operates properly when \( |\Delta V_{BL}| \) is greater than 0.4V.

- **Hysteresis Loop Measurement**
  
  Discrepancies of simulated results and measured results suggest a re-calibration in the ferroelectric capacitor model.

- **Ring Oscillator Measurement**
  
  A close match of the simulated and measured inverter delay values suggests that the transistor model characterizes the process accurately.
This thesis has presented design and implementation of a 1T1C FeRAM testchip. Functionality of the testchip has been verified by both simulation and measurement results.

### 6.1 Contributions of the Thesis

Three contributions of this thesis to FeRAM design are:

1. A reference generation scheme was designed to eliminate fatigue imbalance in ferroelectric capacitors among memory cells and reference cells. Measurement results confirm the functionality of this reference generation scheme.

2. An improved current-steering sense amplifier (ICSSA) was designed to allow a reference current to be shared among eight adjacent memory columns in the memory core. Measurement results show that the ICSSA operates properly when a magnitude of the differential bitline voltage ($|\Delta V_{BL}|$) is greater than 0.4V.

3. Measurement results show that $\Delta V_{BL}$ is strongly related to memory core parameters $C_{BL}/C_{FE}$, such that an optimum range of $C_{BL}/C_{FE}$ can be identified to produce the maximum $\Delta V_{BL}$ for data sensing.

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† Technical collaborations with Yadollah Eslami, Department of Electrical and Computer Engineering at the University of Toronto, towards this contribution are acknowledged.
6.2 Topics for Future Work

Three suggested research areas in FeRAM design are: (1) sense amplifier design, (2) sensing scheme, and (3) ferroelectric capacitor modeling.

1. Sense amplifier design
The ICSSA implemented in this testchip occupies a relatively large area (refer to Section 4.5) and requires extra time for data writeback (refer to Section 4.2). An alternative sense amplifier is a cross-coupled sense amplifier (CCSA), which is smaller in size and enjoys an automatic writeback operation. Using the CCSA in the ITIC FeRAM, however, requires additional analog circuits to buffer the reference voltage to several CCSAs. A design challenge of this idea is to build a small and fast voltage buffer.

2. Sensing scheme
$\Delta V_{BL}$ is strongly related to $C_{BL}/C_{FE}$, and therefore a sense amplifier is redesigned for improving its sensitivity when there are changes in the memory architecture. It is worthwhile to develop a sensing scheme that frees the sense amplifier design from $C_{BL}/C_{FE}$. One novel scheme [15] was proposed to detect data using the charge stored on a capacitor rather than measuring $\Delta V_{BL}$. The proposed scheme, however, requires several preliminary operations prior to data sensing. In order to reduce the memory cycle time, the number of operations should be minimized and the circuits in each operation must be simplified.

3. Ferroelectric capacitor modeling
Precise behavioral modeling of the ferroelectric capacitor is essential to FeRAM circuit design [12]. The accuracy of the capacitor model used in this design can be improved by incorporating the hysteresis loop measurement results into the model (refer to Section 5.4). For achieving further accuracy, the ferroelectric material imperfections, such as fatigue, aging, relaxation, and imprint, should also be incorporated into the model [7].
Appendix

Testchip Package

The LT1C FeRAM testchip is packaged in a 32-pin DIP (only 28 pins are used). Testchip pin assignment and description are provided in Figure A-1.

<table>
<thead>
<tr>
<th>Pin Types</th>
<th>Pin</th>
<th>Descriptions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power &amp; Ground</td>
<td>$V_{DD}$</td>
<td>Power supply (3V)</td>
</tr>
<tr>
<td></td>
<td>$g_{nd}$</td>
<td>Ground (0V)</td>
</tr>
<tr>
<td>Digital input</td>
<td>rowclk, resetn, a1, a2, a3, wlstb, &amp; distb</td>
<td>Memory row addressing</td>
</tr>
<tr>
<td></td>
<td>colclk, resetn, b1, &amp; b2</td>
<td>Memory column addressing</td>
</tr>
<tr>
<td></td>
<td>pre</td>
<td>Bitline precharge</td>
</tr>
<tr>
<td></td>
<td>wb, rwn, feed</td>
<td>Memory operation control signals: data write, data read, bitline overwrite, and bitline monitor</td>
</tr>
<tr>
<td></td>
<td>$s_{dn}$, $s_{apn}$</td>
<td>Sense amplifier control signals</td>
</tr>
<tr>
<td></td>
<td>in</td>
<td>Input of data write</td>
</tr>
</tbody>
</table>

Figure A-1: Testchip pin assignment and description
<table>
<thead>
<tr>
<th>Digital output</th>
<th>out</th>
<th>Output of data read</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>ring_osc</td>
<td>Ring oscillator output</td>
</tr>
<tr>
<td>Analog input</td>
<td>( V_{\text{BLI}}, V_{\text{BLI}} )</td>
<td>Inputs of bitline overwrite</td>
</tr>
<tr>
<td></td>
<td>refin</td>
<td>Input of a monitor circuit (for characterization)</td>
</tr>
<tr>
<td>Analog output</td>
<td>( V_{\text{BLO}}, V_{\text{RBLO}}, V_{\text{RBL0}} )</td>
<td>Outputs of bitline monitor</td>
</tr>
<tr>
<td></td>
<td>refout</td>
<td>Output of monitor circuit (for characterization)</td>
</tr>
</tbody>
</table>

Figure A-1: Testchip pin assignment and description
Appendix

Test System

A test system setup is shown in Figure B-1. Users provide input control signals (pattern input & timing control) to a test sample through VXI tester, then the sample generates digital and analog outputs. The digital output of functional test is sent back to the tester for checking while the analog output of bitline voltage measurement is measured using an oscilloscope and a multimeter. A PCB board has been designed to interface the test sample with test equipment. A floorplan of the PCB board is illustrated in Figure B-2.

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Figure B-1: Test system setup

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Figure B-2: PCB board floorplan

- power connector
- 0.1µF
- 10µF
- 1MΩ
- header pin
- 1 DIP socket
- 2 timing module
- 3 I/O module
- 4 I/O module
A. Column Shift Register

A 16-bit shift register (similar to the row shift register mentioned in Section 3.2) is applied to address 64 memory columns in the memory core, as shown in Figure C-1. The shift register consists of one DFF1 and 15 DFF0s connected in a loop, in which each DFF points to one column block (a set of four adjacent columns). When the signal 'resetn' is asserted, DFF1 has a high output and all other DFFs have low outputs. Therefore, the first column block (columns 1 to 4) is selected. When 'resetn' is deactivated, the active high output of DFF1 shifts sequentially along the register with each cycle of 'colclk' and points to the next column block.

![Figure C-1: 16-bit column shift register](image)

B. Column Predecoder

The predecoder uses two address bits ('b1' and 'b2') to select one memory column in the selected column block. Its schematic and truth table are shown in Figure C-2.
C. Column Decoder

The column decoder is used to generate a control signal for initiating a memory operation on the selected column. The circuit, shown in Figure C-3, has five control inputs: two adjacent column DFF outputs (‘Q_A’ and ‘Q_B’), column predecoder outputs (‘t1’-‘t4’), a read/write signal (‘rwn’), a writeback signal (‘wb’), and an overwrite signal (‘feed’). During column addressing, either ‘Q_A’ or ‘Q_B’ is activated to select a column block and its corresponding reference column pair in the memory core. ‘t1’-‘t4’ then select one memory column in the selected column block.

The cells on memory columns have four operating modes: data read, data write, bitline signal monitor, and bitline signal overwrite. In contrast, the cells on reference column pairs have two modes: bitline signal monitor and bitline signal overwrite. Control signals ‘write_X’ and ‘over_X’ are generated to initiate data write and bitline signal overwrite. A control signal ‘read_X’ is produced to activate either data read or bitline signal monitor, such that the sense amplifier turns on during data read and off during bitline signal monitor.
D. Data Write and Data Read Circuits, as shown in Figure C-4

During write operation, differential inputs ('data_in' and 'data_inn') are applied to nodes 'sen' and 'senn' to flip the ICSSA to a proper state. After asserting 'wb', 'data_in' is passed to the selected bitline for writing a cell. During read operation, a stored data in the accessed cell is detected and found at 'sen'. The data is then routed to the output pin 'data_out' through a data read buffer.
Figure C-4: Precharge, data write, and data read circuits (in solid lines)
References


