MULTIPHASE OPTIMAL RESPONSE
MIXED-SIGNAL CURRENT PROGRAM MODE
CONTROLLER

by

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A thesis submitted in conformity with the requirements for the degree of
Master of Applied Science
Graduate Department of Electrical and Computer Engineering
University of Toronto

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ABSTRACT

Multiphase Optimal Response Mixed-Signal Current Program Mode Controller

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2009

The primary focus of this thesis is to present a simple and practical implementation of an optimal-time (OT) response controller for multiphase interleaved dc-dc switch-mode power supplies (SMPS). This novel solution enables equal current sharing between phases not only in steady-state, but also during load transients, as well as bump-less transition between those two states. Digital voltage loop and multiple analog peak current programmed mode current loops are combined to implement a capacitor charge balance control algorithm with a fairly simple hardware. This algorithm provides recovery from a disturbance in a single on-off switching action, which is performed in virtually fastest possible time, i.e. in optimal time.

The hybrid interface between the loops is provided through a structure combining a sample-and-hold circuit and a relatively slow successive-approximation D/A converter that provides control signals for all the loops in the system. Consequently, this enables equal current sharing under all operating conditions. Furthermore, for operation under light load conditions, the controller automatically switches into simply implemented pulse-frequency mode (PFM) of operation.

The effectiveness of the controller is demonstrated on a two-phase, 5V-to-1.8V, 20W, interleaved buck converter operating at a 1MHz switching frequency. The experimental results verify equal current sharing under all operating conditions, bump-less transition between the
modes, and demonstrate that upon a transient, the converter reaches new steady state through in
the virtually fastest possible time.
Acknowledgments

I would like to first thank my supervisor Aleksandar Prodic. Throughout the time that we have known each other, he has been a really great guidance not only in the academic field, but also in other aspects of my life. He always knew how to push me, challenge me, and put me into situations where I can get the most of myself. Professor Prodic always seemed to have a solution for every problem, regardless of how trivial it might be. But more importantly, he was always friendly, approachable and supportive. His positivity, leadership and work ethic have truly been inspiring.

Secondly, I wish to thank all my colleagues of Energy Systems Graduate Office and especially my Low-Power Management and Integrated SMPS Lab longtime friends Zdravko, Amir, Massimo, Aleks, Frank, Andrija, Jason, Damien and Francis. They all made my research experience more enjoyable. I will cherish the moments and memorable experiences that we have shared together.

I thank all my friends that supported me all the time during my pursuit of this degree and a special thank you goes to the Toshiba Corporation for sponsoring the project.

Finally, I want to dedicate this thesis to my family. I am grateful for the support they gave me and the sacrifices they made for me during these times. They have pushed me to challenge myself everyday while providing valuable guidance for resiliency and perseverance. Their love and support have been the most compelling source of motivation.
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Interleaved multiphase dc-dc switched-mode power supplies (SMPS) are being utilized in a wide range of low-power systems today [1-4]. Applications include power supplies for communication systems, computers, consumer and portable electronics, and other devices consuming power in the range of several watts to several hundreds of watts. The reason for this is the numerous advantages that multiphase SMPS are offering over the single-phase counterparts. Those include: i) a reduced output current ripple, which is translated into a smaller output filter; ii) an improved dynamic response; iii) a better cost efficiency reflected from equal thermal stress due to interleaving; and iv) possibility modularity. However, multiphase systems are more challenging to control because of more complex dynamics, requirements for balanced current sharing between the phases, and smooth mode transition, [5-9], in upcoming multi-mode systems for efficiency optimization. Considering the complexity of the control task, digital implementations appear to be the more feasible choice compared to the analog solutions. Digital controllers for multiphase already have proved their superiority in precise matching of multiple duty-pulses and in scalable systems [10-11]. Moreover, digital controllers offer other attractive features such as programmability and possibility for nonlinear control [12-22].

Although the advantages of digital implementation have been recognized, in multiphase systems, analog controllers are predominantly used. One of the main reasons is faster controller action that allows for minimization of costly reactive components of the power stage. In single-
phase SMPS, this problem has been solved with the utilization of various proximity optimal-time control methods [23-36]. These mixed-signal or digital time-optimal control solutions cannot be simply transferred to multiphase applications. Among the main reasons are: the complexity of the present solutions, which require costly hardware for implementation; and the need for an equal current sharing among the phases under all operating conditions.

1.1 Thesis Objective

The main goal of this thesis is to introduce a hardware efficient mixed-signal solution for the optimal control of multiphase interleaved dc-dc SMPS. The novel system, provides not only recovery from a load transient in virtually minimal possible time, but also proper dynamic current sharing during transients and bump-less transition between the modes, which has proven to be a challenging design problem in both single-phase and multiphase systems. Furthermore, the control method prevents inductor saturation, not common for numerous other methods.

As it will be described soon, due to its mixed-signal realization, at light loads, the controller also allows automatic transition to a more efficient pulse frequency mode (PFM) of voltage regulation.
CHAPTER 1 – INTRODUCTION

1.2 THESIS OVERVIEW

A brief review of the previous art in the related area, alongside the motivations leading to the research work included in the thesis, is reported in Chapter 2. In Chapter 3, the new mixed-signal controller architecture and its principle of operation are described. Three distinctive modes of controller operation (steady state, dynamic, and light-current mode) are also explained. The algorithm used to obtain a fast transient response in dynamic mode, by calculating current control references for single phase systems, is described in Chapter 4.

Chapter 5 describes how the combination of a Continuous-Time Digital Controller (CT-DC) and a Successive Approximation DAC (SA-DAC) can results in time-optimal and current-balanced transient responses for interleaved multiphase power converters.

Details about system operation at light loads, for improved overall power efficiency, are given in Chapter 6. The highlighted benefits of the thesis along with the conclusive remarks and proposed suggestions for future improvements are provided in Chapter 7.
CHAPTER 2 – PREVIOUS ART AND RESEARCH MOTIVATION

An overview of the previous art in the related area, along with the main motivations that inspired the research work done in this thesis, are reported in this chapter. First, a comparative analysis of voltage and current control methods for regulating operation of multiphase dc-dc converters is given. Then the chapter reviews optimal control methods, which are mostly developed for single-phase systems. Problems related to the implementation of optimal control methods in multiphase systems are addressed, and the need for solving the same are presented as the main motivation of this thesis.

2.1 VOLTAGE MODE VS. CURRENT MODE

The following comparative analysis shows that, for the targeted multiphase application, the voltage mode control, shown in Fig. 2.1, is less preferable to the current programmed mode based architectures, which general block diagram is shown in Fig. 2.2.
CHAPTER 2 – PREVIOUS ART AND RESEARCH MOTIVATION

Fig. 2.1: Voltage mode digital controller

Fig. 2.2: Mixed-signal current program mode controller
Since, as shown in Fig. 2.1, the regulation is performed only based on the output voltage value and information about the current is not available, parallel voltage mode controllers behave as voltage sources connected in parallel, as shown in the equivalent circuit of Fig. 2.3. In the circuit, for each phase, the switching network, left of the node $v_x(t)$ (Fig. 2.1), is replaced with a voltage source. Here, the current sharing usually relies on a good matching of converter components as well as on that of the controllers regulating operation of the individual phases. In other words, to achieve equal current sharing, the equivalent voltage sources need to be absolutely the same. The components mismatches often result in large variations between phase currents and, in some cases, cause negative currents in some of the phases. As a consequence, the phases taking large portions of the total current suffer damage due to overly high current and/or thermal stress.

![Voltage Mode](image1)

**Voltage Mode**

![Current Mode](image2)

**Current Mode**

Fig. 2.3: Equivalent circuits of a paralleled voltage mode and current program mode converter

On the other hand, in the current programmed mode controller, the output voltage is regulated indirectly [24], and as described below, the individual phases behave as current sources.
In the system of Fig. 2.2, based on the difference between the output voltage $V_{out}(t)$ and the desired reference $V_{ref}$, error signal is created. The error is then passed to a compensator, which creates a control signal $i_{ctrl}[n]$, used to set the peak inductor current in each switching cycle and, simultaneously control the amount of current delivered to the output. In a mixed-signal implementation as shown here, the transfer of the control signal $i_{ctrl}[n]$ into a peak current reference is performed through a digital to analog converter (DAC) and a comparator. In this way, the inductor is forced to behave as a voltage controlled current source, making paralleling of the current programmed mode (CPM) converter much simpler. As it is shown in Fig. 2.3, a multiphase CPM-controlled converter behaves as a set of parallel current sources charging a connection of the load and the output capacitor. By its nature, this configuration easily achieves desired current sharing and is almost insensitive to the converter parameter mismatches. Furthermore, compared to the voltage mode control, the CPM allows much simpler implementation of pulse-frequency modulation (PFM) control mode, which at light loads improves power processing efficiency.

For a voltage mode controller, the implementation of a PFM controller usually requires a specific functional block. As it will be shown in this thesis, to achieve the PFM operation in a current program mode no additions to the existing hardware are needed.
2.2 PREVIOUS FAST TRANSIENT RESPONSE CONTROLLERS

In low-power dc-dc SMPS used for supplying various portable and consumer electronics devices, the speed of the recovery time after a load transient is of key importance. By reducing the time the SMPS needs to reach the new steady-state after a transient, the size of the output filter of this cost-sensitive device can be significantly reduced. With the ultimate goal of achieving the fastest possible response for a given power stage, i.e. recovery through a single on-off action of the power switches, numerous methods have been developed. Those methods are known as time-optimal control methods and they include trajectory path methods [25], [26], non-linear/linear controllers [27-33], and methods based on the capacitor charge balance [23, 34-36].

Implementation of the optimal control methods has proven to be challenging, due to the sensitivity to parameter variations, and relatively high hardware complexity required for the controller implementation. Also the controllers, which usually run as conventional PI or PID controllers in steady-state and activate a separate mode of control during transients, often suffer from mode transition problems. In [34], [35], the methods require two LUT compensators and three powerful ADC respectively, which consume a considerable amount of power. The voltage mode controllers that utilize asynchronous ADC to sample the output voltage [23], [30], and [34], cannot provide current protection and require a DPWM, which can be very hard to synchronize for transient response in multiphase. The methods presented in [31] and [32] rely at the fact that the threshold voltage to activate transient mode is very small, which is unrealistic and can lead to mode transition problems due to the activation of the transient control mode.
when it is not desired. Moreover, the methods do not provide a solution for current changes during transient. The analog solution to time optimal control that is presented in [37] does not have constant current protection and cannot respond to dynamic load changes.

### 2.3 Previous Multiphase Controllers

In power supplies for microprocessor, also known as voltage regulator modules (VRM), where multiphase converters are most often used, it is essential to have balanced current sharing, precise voltage regulation and current protection. To achieve these characteristics, many innovative digital control techniques and solution [5-11], have been proposed in recent years. Those include techniques for achieving regulation and balanced current sharing, modularity and scalability, and operation with odd-number of phases. However, very little attention have been paid to the problems related to obtaining an optimal transient response in multiphase systems, even though the speed of the response is one of the most critical parameters.
2.4 Fast Transient Response Digital Controllers for Multiphase Systems

The previous two sections gave an overview of the previous art done to obtain fast transient response controller and digital interleaved multiphase controllers, respectively. Most of the optimal-time response methods utilize recent advances in digital control of low-power SMPS to implement relatively sophisticated algorithms with the scope of minimizing the response time in single-phase systems. While the digital optimal controllers have proven superior dynamic performance compared to analog solutions, their operation in multiphase systems has not been demonstrated in the above listed previous art.

Two problems can be correlated to the absence of the digital optimal control solutions for the multiphase systems: hardware complexity required for implementation and a lack of solution for equal current sharing during load transients. The optimal controllers usually rely on the instantaneous matching of the output load and inductor current, which, in the interleaved multiphase system, is challenging to achieve. Due to the phase shift between the phases, a large mismatch between instantaneous inductor current values usually exists. This causes difficulties in matching the sum of inductor currents to that of the load and, equally importantly, in providing equal current sharing during transients. Furthermore, mode transition problems, causing possible instability that has been noticed in numerous single-phase implementations [23-36], in multiphase systems, become even more complex.
CHAPTER 2 – PREVIOUS ART AND RESEARCH MOTIVATION

Targeting possible solutions to the above mentioned concerns is the primary objective of this thesis work.
This chapter gives a detailed explanation of system’s architecture and operation. Fig. 3.1 shows the block diagram of the developed multiphase current program mode controlled converter and Fig. 3.2 shows a more detailed diagram of the controller.

Fig. 3.1: A continuous-time CPM mixed-signal controlling the operation of a multiphase buck converter.
3.1 SYSTEM OVERVIEW

The controller can operate at three distinctive modes. At light loads, the controller behaves as a pulse-frequency modulation controller while at heavier loads it operates as a conventional mixed-signal current-programmed mode (CPM) system. During load transients, the continuous-time digital controller (CT-DC), i.e. dynamic mode, is active to achieve optimal-time transient response.

![Detailed block diagram of the multi-phase optimal controller](image)

Each phase operates as follows: the output voltage is sampled continuously by a windowed flash ADC which, after being subtracted to the digital representation of the reference voltage, produces a digital error signal, $e[n]$. For small errors, i.e. $|e[n]| \leq 1$, the controller operates in steady-state, either as a pulse-frequency modulator (PFM), or as a current

**Fig. 3.2: Detailed block diagram of the multi-phase optimal controller**
programmed mode (CPM) controller. The StateTransient signal (Fig. 3.2) enables the output of the DAC to be fed-back through the analog MUX to the dual-mode ADC creating a “successive-approximation DAC” (SA-DAC). This DAC sets the reference for the current loop, which, as shown in Fig.3.1, is analog. The digital value of the current reference signal $i_{\text{ctrl}}[n]$ determines whether the converter operates as a PFM or a CPM regulator. For medium and heavy loads, the current reference is calculated by a digital compensator (Fig.3.1) implementing the following control law:

$$i_{\text{ctrl}}[n] = K \cdot e[n] + i_{\text{ctrl}}[n-1]$$

(3.1)

where $K$ is a programmable proportional gain.

After being converted to its analog domain, the current control reference is compared with the sensed inductor current. When the sensed value exceeds that of the current reference the SR latch (Fig. 3.1), which was set at the beginning of a switching cycle, is reset.

Since the information about the peak inductor current is maintained at all times, this mode of control is convenient for the targeted application.

### 3.1.1 Compensator Design

Since the system is in CPM, the converter behaves as a single-pole plant [24] that can be regulated with a simple PI compensator. Fig. 3.3 shows the Bode plots of the uncompensated and
digitally compensated system when a buck converter is the power stage. To avoid limit cycle oscillation, the resolution of the successive approximation DAC is selected as:

\[
DAC_{\text{resolution, min}} > \log_2 \left( \frac{V_{DAC_{\text{MAX}}}}{\Delta V_{ADC} \cdot Gain} \cdot \frac{2L_f}{\sqrt{1 - D + D^2}} \right),
\]  

following the design procedure described in [38].

![Bode-plot of the CPM buck converter](image)

**Fig. 3.3:** Bode-plot of the CPM buck converter a) uncompensated; b) digitally compensated

To minimize the power consumption of the controller, in steady state, the dual-mode ADC is sampled at a lower rate than the switching frequency. This is due to the fact that the compensator is utilized only to maintain the output voltage value in steady-state and during slow transients. During load transients, the CT-DC of Fig. 3.1 is active and it brings the output voltage back to steady-state before switching back to a steady-state mode.
3.1.2 IMPLEMENTATION CONSIDERATIONS

While compared to voltage mode systems, CPM systems have advantages regarding current protection and simpler dynamics, they are more susceptible to noise. The reason for this is the unwanted switching of the comparator that sets the latch. To avoid this, a blanking signal and an AND logic circuit are used, as shown in Fig. 3.4. Also, in order to have the system stable at $D \geq 0.5$ and avoid period doubling problem [24], a digital ramp of slope $m_a > \frac{V_{out}(t)}{2L}$ is added to the current control command before it is supplied to the DAC.

![Diagram](image)

**Fig. 3.4: Blanking the undesired switching from the comparator**

The output voltage is sampled using a windowed flash ADC, formed of a set of comparators. For a tight output voltage regulation a small quantization step of the ADC is needed. This requires comparators with a small threshold voltage that can quickly react to voltage changes. Such a comparator requires large bias current, i.e. power consumption, and a significant silicon area. To minimize the requirements for the comparators, a pre amplifier stage, similar to the one of Fig.3.4, increasing the analog equivalent of the error signal, is inserted.
As it can be noted from (3.3), the output voltage and the reference voltage are passed through two consecutive summer stages. As a result, the difference of the output voltage to the reference is amplified by a controllable gain, $R_2/R_1$, therefore making the triggering of the comparators more sensible to the small variations of the output voltage.

**3.1.3 Interleaved Multiphase Operation with Equal Current Sharing**

The system of Fig. 3.1 can operate in interleaved multiphase fashion with equal current sharing.

Since the phases share the same voltage feedback loop, the same current control reference is provided to the SA-DAC of each phase, ideally, providing equal current sharing. The interleaved operation is achieved by digitally programming the switching clocks that set the SR
latches such that they are shifted in phase between each other by $T_S/N$, where $T_S$ is the switching period and $N$ the number of phases.

### 3.2 Pulse – Frequency Mode

The controller enters the pulse-frequency mode when the peak control signal $i_{ctrl}[n]$ falls below a predefined value $i_{PFM}[n]$, which is set to be smaller than the amplitude of the inductor current ripple. To achieve this, the output of the successive approximation DAC is set to a fixed value, the clock generator is suspended, and the SR latch is clocked by the asynchronous ADC for output voltage measurement. The regulation of the output voltage is now performed with a modified hysteretic technique.

When the output voltage error $e[n]$ exceeds the value of 1 the ADC triggers the SR latch and the main switch is turned on. This causes the inductor current to rise and, consequently, leads to an increase in the output voltage. When the inductor current reaches the value set by the DAC, the SR latch is reset and the switch is turned off. The next switching cycle starts when the load discharges the output capacitor such that the error is once again larger than 1.

It should be noted that, unlike in the voltage mode, this implementation of PFM virtually does not introduce any hardware overhead, thereby minimizing the overall cost of the controller implementation.
3.3 Dynamic Mode

Load transient, i.e. dynamic, mode of operation can be described by observing diagrams of Figs. 3.1 and 3.2. Transients are sensed and activated by the mode control logic block (MCL), at the time instant when the absolute value of the output voltage error exceeds 1, i.e. $|e[n]| \geq 2$. If a light-to-heavy load transient is detected, at that point, the main switch is immediately turned on; for the heavy-to-light transient it is turned off. Simultaneously, the StateTransient signal enables the amplified sensed current voltage to go to the input of the dual-mode ADC, which is sampled faster now, and activates the min/max detector & the optimal $\Delta i[n]$ calculator block. To achieve recovery through a single on-off switch action, this block calculates the peak value of the inductor current, in accordance with the capacitor-charge balance based algorithm described in the following section. The algorithm results in the virtually fastest possible charge recovery to the new steady-state value. The algorithm also results in a bump-less transition to a new steady-state.
CHAPTER 4 – SINGLE-PHASE OPTIMAL-TIME TRANSIENT RECOVERY

In this chapter, the operation of the optimal-time transient response controller in single-phase CPM system, Fig. 4.1, is explained. The concept is then extended to multiphase applications in the following chapter. The method utilizes a capacitor-charge balance algorithm implemented with a continuous-time digital controller (CT-DC), and a successive-approximation digital-to-analog converter (SA-DAC). The result is virtually the fastest possible recovery time for a transient and a bump-less transition back to steady-state.

Fig. 4.1: Single-phase continuous-time peak current program mode controlled dc-dc buck converter
4.1 Fast Transient Response in CPM Based on Capacitor-Charge Algorithm and CT-DC

Compared to the voltage mode control [23], implementation of a time-optimal controller in CPM is significantly simpler. The reason for this is that, instead of calculating optimal on and off times indirectly through forming relation between the inductor current and duty ratio value, the inductor current is directly used. Furthermore, to achieve bump-less transition, only two current control reference values are necessary, namely the after-transient new steady-state value and the peak current value during transient. The direct calculation also results in a lower delay, and therefore, a faster potential response. The operation of the proposed CPM CT-DC can be explained using the diagrams of Fig. 4.2. They show the key waveforms of the optimal recovery process for the system of Fig. 4.1 during a light-to-heavy load transient.
The CT-DC algorithm is inactive during steady-state operation, but, as soon as a load transient is detected, the main power switch is turned on or off depending on whether the load current is stepping up or down, respectively. Also, at this time instant, the compensator is turned off, the current reference is set to the maximum allowable current value, and the optimal control
sequence generator is activated. The initial setting of the current value provides protection from the inductor current saturation during the optimal generator operation. The generator provides two current reference values. The first is the actual peak current reference resulting in the time-optimal response. The second value is the peak current reference for the new steady-state, established upon the transient response is completed. It should be noted that the two references are obtained in a reversed order and that only the peak value is calculated. The new steady-state value is captured during the transient using the dual-mode ADC of the SA-DAC shown in Fig. 4.1. At the instant when the valley point is detected, the value of the amplified sensed current is sampled and held in a digital register. As it can be seen from the diagram of Fig. 4.2, this value corresponds to the new steady-state current, \(i_{\text{ctrl, new}}\). This process is followed by the calculation of \(\Delta i\), the current increment needed to replace the lost capacitor charge caused by the load transient. During the calculation time, the sampling rate of the SA-DAC is increased. This is performed so that the speed of digital to analog conversion can be increased such that the reference for the peak current value is set before \(i_L(t)\) actually reaches it. The digital peak current reference is calculated as:

\[
i_{\text{peak}}[n] = i_{\text{ctrl, new}}[n] + \Delta i[n]
\]  

(4.1)

It should be noted that the ability of this system to capture the new steady state of the inductor current completely eliminates stability problems related to transition between optimal and steady-state mode. As mentioned before, the mode transition in voltage mode systems is one of the main obstacles for a successful implementation of the optimal-time response algorithms [23].
The actual calculation of the current increment is performed using a simple capacitor charge balance based algorithm, starting from the equation stating that the loss of capacitor charge due to voltage variation needs to be equal to the extra charge brought by the inductor, i.e.

\[ Q = C \Delta v = \frac{1}{2} \Delta i(t_{on} + t_{off}) \]  

(4.2)

Where the relations between the transistor \( t_{on} \) and \( t_{off} \) times and \( \Delta i \) are given with the following equations:

\[ \Delta i = a_r \cdot t_{on} = \frac{V_g - V_{out}}{L} \cdot t_{on} \quad \text{and} \quad \Delta i = a_f \cdot t_{off} = \frac{V_{out}}{L} \cdot t_{off} \]  

(4.3)

\[ \frac{t_{on}}{t_{off}} = \frac{V_{out}}{V_g - V_{out}} \Rightarrow t_{on} = \frac{V_{out}}{V_g - V_{out}} \cdot t_{off} \]  

(4.4)

Where \( a_r \) and \( a_f \) are the rising and falling slopes, respectively. So, inserting (4.4) into (4.2) we have:

\[ Q = \frac{1}{2} \Delta i \cdot \left( t_{off} + \frac{V_{out}}{V_g - V_{out}} \cdot t_{off} \right) = \frac{1}{2} \Delta i \cdot t_{off} \left( \frac{V_g}{V_g - V_{out}} \right) \]  

(4.5)

But:

\[ \Delta i = \frac{V_{out}}{L} \cdot t_{off} \Rightarrow t_{off} = \frac{\Delta i \cdot L}{V_{out}} \]  

(4.6)

Therefore by combining (4.5) and (4.6) together we have:
\[ Q = \frac{1}{2} \Delta i^2 L \left( \frac{V_g}{V_{g_{out}} - V_{out}^2} \right) \]  

(4.7)

Also we know that:

\[ Q = C \cdot \Delta v \]  

(4.8)

\[ \therefore C \cdot \Delta v = \frac{1}{2} \Delta i^2 L \left( \frac{V_g}{V_{g_{out}} - V_{out}^2} \right) \]  

(4.9)

\[ \Delta i^2 = \frac{2C \cdot \Delta v}{L} \left( \frac{V_{g_{out}} - V_{out}^2}{V_g} \right) = \frac{2C \cdot \Delta v \cdot V_{out}}{L} \left( \frac{V_g - V_{out}}{V_g} \right) \]  

(4.10)

\[ \Delta i^2 = \frac{2 C \cdot \Delta v \cdot V_{ref}}{L} (1 - D) \]  

(4.11)

Therefore, for an ideal buck converter the expression for \( \Delta i \) becomes:

\[ \Delta i = \sqrt{\frac{2C(1 - D)V_{ref} \Delta v}{L}} \]  

(4.12)

It should be noted that, in this architecture of the controller, even when the voltage recovery is not optimal, the current reaches its proper steady-state value at the end of the on-off cycle. This is because, as described earlier, the new steady-state value of the current is not determined through calculation, but rather by capturing the value of the inductor current at peak/valley point.
4.2 MULTIPLE TRANSIENTS RECOVERY

One of the main problems of commonly used time-optimal controllers is inability to react to successive load transients occurring during on/off sequence calculation. This subsection shows that the proposed time-optimal CPM control methods does not suffer from the previously mentioned problem.

In this system, if a transient happens before the steady-state is reached, it is simply treated as a new transient, Fig. 4.3. When the voltage reaches the valley point again, the same process is repeated with the second transient, \(i_{ctrl, new}[n]_2\) and \(i_{peak}[n]_2\) are captured and calculated. These two new references are the current references to perform full system recovery as the charge balance is maintained. Therefore optimal-time recovery can be obtained even if the system is hit by theoretically an infinite number of consecutive transients.

\[
i_{peak, 1} = \sqrt{\frac{2C(1-D)V_{ref} \Delta V_1}{L}} + i_{ctrl, new, 1} \tag{4.13}
\]

\[
i_{peak, 2} = \sqrt{\frac{2C(1-D)V_{ref} \Delta V_2}{L}} + i_{ctrl, new, 2} \tag{4.14}
\]
Fig. 4.3: Output voltage, inductor current and current control reference waveforms during a dynamic load change
4.3 System Verification through Simulation Results

The system of Fig. 4.1 was simulated to verify the single-phase transient operation of the controller using the mixed-signal NCLAUNCH simulator of the Cadence package [39]. All the analog parts of the system were developed using Verilog AMS and the digital parts were in Verilog HDL. Simulations verification was performed for a single-phase 5.5V-to-1.8V; 10W buck converter operating at 1MHz. The inductor of the converter is 1.5\(\mu\)H and the output capacitor is 30\(\mu\)F. The simulations are used both to verify functionality and to perform a comparative analysis of system’s performances for different quantization levels of the output’s ADC as well as for different sampling rates. The comparative analysis is performed with the ultimate goal to minimize hardware requirement for the ADC.

The first two figures (Fig. 4.4 and 4.5) show the transient response of the system to a 4A load current step when the output voltage was sampled by an ADC with 4mV quantization step and an oversampling rate of 20 times larger than the switching frequency. Fig. 4.4 one shows the light-to-heavy transient response. The undershoot of the output voltage was 72mV and the transient period, until the voltage reached its new steady-state, was only 2.4\(\mu\)s. The heavy-to-light transient response is shown in Fig. 4.5. The deviation of the voltage during transient was 150mV and the recovery time was 4\(\mu\)s. The following two figures show a comparison, with respect to Fig. 4.4, in worst case performances obtained with 10mV and 20mV quantization voltage, respectively. In the third simulation test, Fig. 4.6, transient recovery performance on the worst case scenario, i.e. transient hit in the “worst” time during switching cycle, for the 4A load
current step is shown. It is obvious that the output voltage has an overshoot right after it reaches the steady-state after transient. The deviation is 25mV, which is caused by the maximum error (3%) in captured value from ADC. The last figure shows the worst case light-to-heavy performance when 40mV quantization voltage was used to sample the output voltage. The negative effect in this case, is an 8% error in captured value from ADC, which is translated in 75mV overshoot in output voltage following the transient.

Fig. 4.4: CT-DC transient response on light-to-heavy 4A load change step. The circled value shows the instantaneous current value captured by the SA-DAC.
CHAPTER 4 – SINGLE-PHASE OPTIMAL-TIME TRANSIENT RECOVERY

Fig. 4.5: CT-DC transient response on heavy-to-light 4A load change step. The circled value shows the instantaneous current value captured by the SA-DAC.

Fig. 4.6: CT-DC worst case transient response on light-to-heavy 4A load change step when the output quantization voltage was 10mV. The after-transient overshoot is caused by a 3% maximum error in the captured value from SA-DAC.
CHAPTER 4 – SINGLE-PHASE OPTIMAL-TIME TRANSIENT RECOVERY

4.4 EXPERIMENTAL SETUP AND SYSTEM VERIFICATION

The system of Fig. 4.1 was verified experimentally on a 5.5V to 1.8V, 10W buck converter operating at 1MHz. Table 1 gives a summary of all the specifications of the setup. The digital part of the continuous-time controller feedback loop was built on an Altera DE2 FPGA board and an ADC with a threshold voltage $V_{th} = 4$ mV was used to sample the output voltage. The output voltage was oversampled by 20 times to resemble the asynchronous flash ADC. Fig.
4.8, and its zoomed version Fig. 4.9, show the transient response during a 4A light-to-heavy load step, where the output voltage returns to its steady state in 2.3μs. The heavy-to-light performance of the controller is shown in Fig. 4.10. In both cases, the results also show smooth transition between optimal-response and steady-state control mode. Fig. 4.11 shows the optimal time recovery after the system is hit by two consecutive transients. The first transient is 2.2A and the other 2A. In the figure it is also shown that once the valley point is detected, the other transient hits and the system returns to steady state in 3.7μs. This shows that while keeping current protection, the controller produces very fast transient responses. The last two figures of this section show that voltage deviation during a load transient step can be reduced even more so if the steady-state voltage bin is reduced. Figs. 4.12 and 4.13 show the performance of the system when the steady-state voltage bins were 15mV and 10mV, respectively.

<table>
<thead>
<tr>
<th><strong>TABLE I</strong></th>
<th><strong>EXPERIMENTAL SETUP SPECIFICATION</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Parameter</strong></td>
<td><strong>Value</strong></td>
</tr>
<tr>
<td>( V_{\text{IN}} )</td>
<td>5.5V</td>
</tr>
<tr>
<td>( V_{\text{OUT}} )</td>
<td>1.8V</td>
</tr>
<tr>
<td>( f_{\text{Switching}} )</td>
<td>1MHz</td>
</tr>
<tr>
<td>( P_{\text{MAX}} )</td>
<td>10W</td>
</tr>
<tr>
<td>( V_{\text{Quantization}} )</td>
<td>4mV</td>
</tr>
<tr>
<td>( V_{\text{Steady-State}} )</td>
<td>20mV</td>
</tr>
<tr>
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<td>1.5μH</td>
</tr>
<tr>
<td>Capacitor</td>
<td>30μF</td>
</tr>
<tr>
<td>Load Step</td>
<td>4A</td>
</tr>
</tbody>
</table>
Fig. 4.8: CT-DC transient response on 4A load change step. The waveforms from top to bottom are: output voltage (100mV/div); amplified inductor current (1V/div); current control reference (1V/div); load change command signal (5V/div). The time scale is 5μs/div.
Fig. 4.9: The zoomed version of the transient response using CT-DC. The undershoot voltage deviation on a 3.6A load step change is 75mV and the settling time to the new steady-state is 2.3μs. The waveforms from top to bottom are: output voltage (50mV/div); amplified inductor current (1V/div); current control reference (1V/div); load change command signal (5V/div). The time scale is 1μs/div.
Fig. 4.10: CT-DC transient response on 4A heavy-to-light load change step. The waveforms from top to bottom are: output voltage (100mV/div); current control reference (1V/div); amplified inductor current (2V/div); load change command signal (5V/div). The time scale is 2μs/div.
Fig. 4.11: Two consecutive transients using CT-DC. A second switching sequence happens once the valley point of the first one is detected. Maximum deviation is 47mV and recovery time is 3.7μs. The waveforms from top to bottom are: output voltage (50mV/div); amplified inductor current (1V/div); current control reference (5V/div); the first load change command signal (5V/div). The time scale is 2μs/div.
Fig. 4.12: Operation of the CT-DC on a light-to-heavy 4A load current step when the steady-state voltage bin was 15mV. The waveforms from top to bottom are: output voltage (100mV/div); amplified inductor current (1V/div); current control reference (1V/div); load change command signal (1V/div). The time scale is 5μs/div.
Fig. 4.13: Operation of the CT-DC on a light-to-heavy 4A load current step when the steady-state voltage bin was 10mV. The waveforms from top to bottom are: output voltage (20mV/div); amplified inductor current (1V/div); current control reference (1V/div); load change command signal (5V/div). The time scale is 1μs/div.

### 4.5 Fast Transient Response with a Conventional ADC

For a medium-to-high power SMPS operating at lower switching frequencies compared to those of the low power systems, an optimal-time transient response can be achieved with an off-shelf simple digital-to-analog converter (DAC).

To achieve this, two additional changes are necessary: i) a digital register to save the integrator part of the current command (i[n-1]) should be part of the digital part of the feedback
controller; ii) the new after-transient current control reference should be calculated instead of being captured by a fast ADC. To calculate the after-transient new steady-state current value, Fig. 4.2, the time the output voltage needs to reach the valley point, $t_1$, is measured. Then, the increment of the old $i_{\text{ctrl,old}}$, i.e., value before the transient is found as:

$$ i_{\text{diff}} = \left( \frac{V_g - V_{\text{out}}}{L} \right) \cdot t_1 = \frac{V_g \left( 1 - \frac{V_{\text{out}}}{V_g} \right)}{L} \cdot t_1 $$

Then, the difference in current reference is either added or subtracted to the old current reference depending on whether it is a light-to-heavy, or heavy-to-light load transient step, respectively. And therefore, the current control value at the end of the transient is:

$$ i_{\text{ctrl, new}} = i_{\text{diff}} \pm i_{\text{ctrl, old}} $$

There is a tradeoff, however, opposite to the benefit that the system is more efficient in terms of power, considering the fact that an ADC is not used anymore in the feedback loop. Since the values of the new current control commands are pre-calculated and entered in a look-up table (LUT) controlled by a digital counter that measures time $t_1$, there is more room for errors. Since the values in the LUT are distinct, there is a higher chance that the captured value from the LUT is not the exact necessary value. This leads into a mode transition voltage overshoot or undershoot when the system goes from nonlinear to linear mode.
4.5.1 EXPERIMENTAL RESULTS

To verify the operation of the control system, when the new current control value is calculated instead of being captured by an ADC, the following experimental results are shown. The controller was tested on a 5.5V-1.5V buck converter switching at 500 kHz. The output voltage was sampled continuously by a set of sixteen comparators. The quantization voltage between two consecutive comparators was 40mV and the comparators were sampled every 100ns, which is a sufficiently small time to detect all the changes in the comparators. Table II gives a summary of all the specifications of the setup used to test the control method experimentally. This also shows that the system can work even when there is high capacitance at the output of the converter.
Fig. 4.14, and its magnified version Fig. 4.15, show response to a 3A light-to-heavy load transient, it can be seen that the steady state is regained after only one on-off switching action confirming the validity of the proposed algorithm. Fig. 4.16 shows yet another advantage of the current program mode controller, through the operation of the current limiter. The limiter does not allow inductor saturation. It can be seen that, when a pre-defined current limit is reached, the main switch briefly turns off and turns on again, never allowing current to exceed the maximum value. This process is repeated until the charge balance is achieved. It can also be seen that even when the maximum current is limited the controller achieves transient response that is significantly faster than that of conventional solutions.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$</td>
<td>5.5V</td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>1.5V</td>
</tr>
<tr>
<td>$f_{Switching}$</td>
<td>500KHz</td>
</tr>
<tr>
<td>$P_{MAX}$</td>
<td>10W</td>
</tr>
<tr>
<td>$V_{Quantization}$</td>
<td>40mV</td>
</tr>
<tr>
<td>$V_{Steady-State}$</td>
<td>60mV</td>
</tr>
<tr>
<td>Inductor</td>
<td>1.5μH</td>
</tr>
<tr>
<td>Capacitor</td>
<td>200μF</td>
</tr>
<tr>
<td>Load Step</td>
<td>3A</td>
</tr>
</tbody>
</table>
Fig. 4.14: Load transient response on 3A load change step. The waveforms from top to bottom are: output voltage (200mV/div); amplified inductor current. The time scale is 5μs/div. (2V/div); current control reference (5V/div); load change command signal (10V/div). The time scale is 20μs/div.
Fig. 4.15: Zoomed diagram of the transient response. The waveforms from top to bottom are: output voltage (100mV/div); amplified inductor current (2V/div); current control reference (5V/div); load change command signal (10V/div).
Fig. 4.16: Operation of the current protection. The waveforms from top to bottom are: output voltage (200mV/div); amplified inductor current (2V/div); current control reference (5V/div); load change command signal (10V/div). The time scale is 20\(\mu\)s/div.
CHAPTER 5 – MULTIPHASE OPTIMAL-TIME TRANSIENT RECOVERY

In this chapter, the operation of the single-phase optimal-time transient response in CPM systems is extended to multiphase applications. The most important feature of this control method is that it provides equal current sharing at all times, even during transients. For the purpose of explaining operation of the multiphase controller, block diagram of the controller is shown in Figs. 5.1 and Fig. 5.2. The first part of this chapter explains the method to obtain time-optimal transient recovery in multiphase systems. The following two parts show the results of system verification through mixed-signal simulation and experiments.
Fig. 5.1: A continuous-time CPM mixed-signal controller controlling the operation of a multiphase buck converter.
5.1 Fast Transient Response in Multiphase CPM Systems Based on SA-DAC and CT-DC

With regards to a balanced current sharing, a CPM controlled system makes parallel operation simpler than a voltage mode system. This is due to the fact that the inductors of individual phases behave as voltage-controlled current sources. Therefore, a multiphase converter behaves as a set of current sources charging a parallel combination of the output capacitor and the load resistor. Thus, in a multiphase mixed-signal CPM system, interleaved operation can be simply achieved by providing each phase with the same current control.
reference and by phase-shifting their respective switching clocks in an interleaved manner, according to the number of phases. However, the main obstacles in implementing an optimal-time controller for multiphase systems are maintaining balanced current sharing between the phases during transients and establishing a bump-less transition to the new steady state after the transient mode is completed. To resolve this, a modified successive-approximation DAC and a set of sample-and-hold capacitors are used.

Fig. 5.3: Output voltage, inductor current and current control reference waveform description in a two-phase system
The controller operates as follows: when the valley/peak point is detected, the new steady-state current commands for each phase are captured by the respective sample-and-hold capacitors, labeled as $C_0$ to $C_2$ in Fig. 5.2. Since as shown in Fig. 5.3, due to the phase shift, the instantaneous currents of the phases are not the same, the sampled values, which define new steady state current, cannot be fed the comparators directly. To solve for this problem, the fact that the sum of the instantaneous phase currents is equal to the output current is used. Hence, in order to obtain equal current sharing after the transient, an average value of all the currents should be found directly. For this reason, all captured values that are held in the capacitors are averaged and then fed to the comparator. In this way, the same new value of the steady-state current after the transient is ensured.

Averaging is simply done by briefly short-connecting the sample and hold capacitors, such that the same value of all the voltages is obtained. This process happens right after the transient state is detected. It should be noted that all the sample-and-hold capacitors have all the same value, which is small, so the amount of charge transferred between them, i.e. current through short connection switches, is small as well.

The following simulation verifies that the maximum current that can flow in the branch, when two capacitors are tied together, is less than 3mA. The test was done on two 5pF capacitors with a 2V voltage difference between them (worst case scenario for the considered operation) and an NMOS transistor ($L = 5\mu m$, $W = 20\mu m$) was used as a switch.
Fig. 5.4: Simulation result for the worst case, i.e. maximum branch current, when short-connecting two 5pF capacitors

Averaging can be obtained in the digital domain as well, after the new control values have been digitized. However, doing digital averaging for odd numbers (3, 5, 7,... phases) is not trivial and does require a considerable time, when the converter is operated at a high switching frequency.

\[
i_{ctrl\_new\_A} = i_{ctrl\_new\_B} = \text{Average}\left\{i_{\text{captured\_A}}, i_{\text{captured\_B}}\right\}
\]  

(5.1)
Therefore, the new after-transient current control reference is the same for all phases and is the digital average of all the captured values in the respective SA-DACs.

5.2 SYSTEM VERIFICATION THROUGH SIMULATION RESULTS

To verify the multiphase transient operation, the system of Fig. 5.1 was simulated using the mixed-signal NCLAUNCH simulator of the Cadence package. All the analog parts of the system were described using Verilog AMS, while the digital parts were in Verilog HDL. Simulations verification was done for a 2-phase, 3-phase, and 4-phase interleaved 5.5V-to-1.8V buck converter operating at 1MHz. The inductor in each phase of the converter is 1.5\mu H and the output capacitance was 30\mu F. The following simulation figures show the transient response of the system to an 8A light-to-heavy load step on a two-phase system, 12A load current step on a three-phase system, and 16A load current step on a four-phase system, respectively. This was done with the purpose that the load step that each phase would see is 4A. Also, this shows that as the number of phases is increased and the current load step is increased accordingly, the optimal-time transient performance obtained with the controller is the same. The quantization voltage that the output voltage was sampled was 4mV and the steady-state voltage bin was 20mV. Fig. 5.5 shows the response obtained when an 8A load change step was applied on a 2-phase system. The new steady-state current command value was obtained by digitally averaging the instantaneous current values that were captured by the respective SA-DAC. The transient state is 2.6\mu s and undershoot is only 76mV. Fig. 5.6 and Fig. 5.7 show the performance of the controller when on a 3-phase and 4-phase when 12A and 16A were applied, respectively. In both cases, the new
current control command value was obtained by short-connecting the sample-and-hold capacitors of all phases, as explained in the previous section. It can be seen that the performance of the controller is the same in all cases and that the balance between the phases is maintained at all times. Moreover, it is shown that optimal-time transient recovery is obtained in one single on-off sequence of the main switch.

Fig. 5.5: CT-DC transient response on a 2-phase interleaved system when a 8A load change step was applied to the output voltage. The load is shared equally between the phases. The circled values show each phase’s instantaneous current value captured by the SA-DAC and their averaged value, which was done digitally.

The output voltage recovers in 2.6μs and its undershoot is 76mV.
Fig. 5.6: CT-DC transient response on a 3-phase interleaved system when a 12A load change step was applied to the output voltage. The load is shared equally between the phases. The circled values show each phase’s instantaneous current value captured by the SA-DAC and their averaged value, achieved by short-connecting all the sample-and-hold capacitors. The output voltage recovers in 2.6μs and its undershoot is 74mV.
Fig. 5.7: CT-DC transient response on a 4-phase interleaved system when a 16A load change step was applied to the output voltage. The load is shared equally between the phases. The circled values show each phase’s instantaneous current value captured by the SA-DAC and their averaged value, achieved by short-connecting all the sample-and-hold capacitors. The output voltage recovers in 2.5μs and its undershoot is 78mV.

5.3 EXPERIMENTAL SETUP AND SYSTEM VERIFICATION

The system of Fig. 5.1 was verified experimentally on a two-phase 5.5V to 1.8V, 20W interleaved buck converter operating at 1MHz. The output capacitor is 30μF and the phase
inductors are 1.5$\mu$H. The digital part of the continuous-time controller feedback loop was built on an Altera DE2 FPGA board and an ADC with a threshold voltage $V_{th} = 4$ mV was used to sample the output voltage. The output voltage was oversampled by 20 times to resemble the asynchronous flash ADC and the steady-state voltage bin was 20 mV. Fig. 5.8 shows the transient response during an 8A light-to-heavy load step, where the output voltage returns to its steady state in 2.2$\mu$s and the undershoot is 75 mV. The current is shared equally between the phases, so the current load step that each phase sees is 4A. The instantaneous reference current averaging is performed by short-connecting the sample-and-hold capacitors. It is obvious that there is a balanced dynamic current sharing and that there is no mode transition problem in either phase, which reinforces one of the main objectives of this thesis. Fig. 5.9 shows the transient performance of the controller on the same load step, but this time the instantaneous reference current averaging, in order to obtain the after-transient current reference, is done digitally. Although experimental verification was performed on a two-phase system only, its consistency with respect to the simulation results described in the previous section, confirms that the same result can be expected even if the controller is tested in a three-phase, four-phase, or n-phase interleaved converter.
Fig. 5.8: Transient response on a two-phase interleaved buck converter when a 8A load change step was applied to the output voltage. The load is shared equally between the phases. The after-transient steady state current control reference is achieved by short-connecting all the sample-and-hold capacitors. The output voltage recovers in 2.2μs and its undershoot is 75mV. The waveforms from top to bottom are: output voltage (100mV/div); amplified inductor current (1V/div); current control reference (1V/div); load change command signal (5V/div). The time scale is 2μs/div.
Fig. 5.9: Transient response on a two-phase interleaved buck converter when a 8A load change step was applied to the output voltage. The load is shared equally between the phases. The after-transient steady state current control reference is achieved by digital averaging. The output voltage recovers in 2.2μs and its undershoot is 75mV. The waveforms from top to bottom are: output voltage (100mV/div); amplified inductor current (1V/div); current control reference (1V/div); load change command signal (5V/div). The time scale is 2μs/div.
When a power converter is operating at light current loads, pulse-frequency modulation (PFM) is usually the preferred mode of operation. The reason for this is that the switching losses are minimized, making the control method more power efficient.

In this chapter, the operation of the controller in pulse-frequency modulation is explained. The method does not require any additional hardware; it is only achieved through a simple modification of the existing controller. The first part of this chapter explains the method for obtaining pulse frequency modulation with the proposed controller. The following part shows verification of the PFM operation through experimental results.
6.1 Pulse-Frequency Mode of Operation

At light current loads the controller operates as a pulse-frequency modulation regulator. Fig. 6.1 shows a block diagram of the controller configured for pulse-frequency modulation.

![Block diagram of pulse-frequency modulation controller](image)

Fig. 6.1: A continuous-time CPM mixed-signal controller operating in pulse frequency modulation
The system operates as follows: as long as the current control command is smaller than predefined value $i_{PFM}[n]$, the main switch is in on state, the compensator and CT-DC are inactive and a fixed current command, which is smaller than the inductor current ripple, is fed to the DAC. Fixing the current control reference below the inductor current ripple has two functions: i) it ensures that the system is always in discontinuous conduction mode (DCM), which is essential for pulse-frequency operation; and ii) for a constant input voltage, it provides constant on-time of the main power switch, since the rising slope of the current is always the same.

The SR latch of Fig.6.1 is reset when the inductor current becomes larger than the reference and, consequently, the main switch is turned off. The new switching cycle is initiated by the flash ADC that samples the output voltage. Every time the error signal, $e[n]$, becomes larger than 1, it sets the SR latch and the main power switch is turned on. This way, a modified hysteretic-type of a loop is created to keep the output voltage regulated, whereas the switching pulses vary in frequency. It should be noted that, unlike in voltage mode conventional DPFM-s [40], [41], this implementation virtually does not introduce any hardware overhead, minimizing the overall cost of the controller implementation.

When the average load current increases above the threshold, the controller switches back to continuous conduction mode (CCM). A digital counter keeps track of the frequency of the PFM pulses. When the frequency is larger than a pre-defined threshold value, $f_{PFM}$, the compensator is activated and normal CPM operation is resumed.
6.2 EXPERIMENTAL SETUP AND SYSTEM VERIFICATION

The system of Fig. 6.1 was verified experimentally on a single-phase 5.5V to 1.8V buck converter. The output capacitor is 30μF and the inductor is 1.5μH. The digital part of the continuous-time controller feedback loop was built on an Altera DE2 FPGA board and an ADC with a threshold voltage $V_{th} = 4\text{mV}$ was used to sample the output voltage. The output voltage is sampled by a 20 MHz clock to resemble the asynchronous flash ADC and the steady-state voltage bin is 20mV. Fig. 6.2 shows the controller steady-state operation in pulse-frequency mode when the output load current is 15mA. The output voltage is zoomed in order to better observe the voltage ripple caused by the hysteretic loop. Fig 6.3 and Fig 6.4 show a heavy-to-light and light-to-heavy transient transitions for a 2A current load step, respectively. It can be seen that during the transition the current command boundary is surpassed and, therefore, the controller switches from CCM to DCM, i.e. pulse frequency mode of operation, – if the current step is + 2A it switches vice versa. It should be noted that for the last two figures the fast transient response controller is deactivated to display better the transitions when the threshold boundaries are crossed for PFM.
Fig. 6.2: Steady state pulse-frequency mode of operation. The load inductor current is 15mA and the switching frequency is almost 83 kHz. The waveforms from top to bottom are: output voltage (100mV/div); amplified inductor current (500mV/div); gate-drive signal (5V/div). The time scale is 5μs/div.
Fig. 6.3: PFM load transition on 2A load transient. When the load inductor current is 60mA and the switching frequency is almost 250 kHz. The waveforms from top to bottom are: output voltage (200mV/div); amplified inductor current (500mV/div); load step signal (5V/div). The time scale is 10μs/div.

Output Voltage = 1.8V

2A

60mA

CCM Operation

DCM Operation

Load step

Measurement Menu
Fig. 6.4: DCM-to-CCM load transition on 2A load transient. The waveforms from top to bottom are: output voltage (200mV/div); amplified inductor current (500mV/div); load step signal (5V/div). The time scale is 10μs/div. 

Output Voltage = 1.8V

60mA

DCM Operation

Load step

2A

CCM Operation
CHAPTER 7 – CONCLUSION AND FUTURE WORK

In this chapter, an overall summary and the conclusive remarks for the work reported in this document are provided. Also, possible extensions of this work are given.

7.1 THESIS SUMMARY AND CONTRIBUTIONS

An optimal-time control method and system for multiphase interleaved converters are introduced in this thesis report. The controller is implemented as a mixed-signal system, where the voltage loop is digital and the current loops are implemented in analog manner. The optimal response is obtained utilizing a simplified version of the capacitor charge balance algorithm [24]. To ensure proper current sharing during transients and bump-less transition between different control modes, a simple solution based on sample-and-hold capacitor circuits was introduced. The novel system provides not only recovery from a load transient in virtually minimal possible time but also proper dynamic current sharing during transients. Furthermore, due to its mixed-signal realization, at light loads, controller allows automatic transition to more efficient pulse-frequency mode (PFM) of voltage regulation. The modification to achieve pulse-frequency modulation does not require any hardware addition in the control loop.
The effectiveness of the controller is demonstrated on a two-phase experimental FPGA-based prototype. The experimental results demonstrated both virtually the fastest possible transient response for a given power stage and equal current sharing in all operating modes, including transients.

7.2 Future Work

The future work proposed here entails options for better calibration of CT-DC calculations and on-chip implementation considerations.

7.2.1 Auto-Tuning Procedure

As it already has been reported, auto-tuning is a procedure in which LC parameter values are extracted dynamically and the controller is tuned accordingly to achieve a better performance [42-45]. This method can be very efficient in linear/non-linear controllers that utilize capacitor charge balance calculations to obtain an optimal-time transient recovery. In this project, a range of peak current references during transient were pre-calculated using the equations (4.1) and (4.12) and were stored in LUT. However, variations from the nominal values of the parameters used in the formulae can lead to a non-perfect transient recovery. For this reason, if an auto-tuning component was augmented to the controller for calibration of the current command values in the LUT-s, a better and more robust performance can be obtained.
7.2.2 **ON-CHIP IMPLEMENTATION**

The biggest drawback of a current-programmed mode controller is bandwidth limitation due to the current sensing circuit. For operation at high switching frequencies the method requires a power-hungry high gain-bandwidth amplifier to amplify the sensed current.

The sensing method, utilized to prove the concept in this thesis, was the combination of a sense resistor in series with the inductor followed by an amplifier. The reason for this is that the targeted switching frequency used to demonstrate the operation of the proposed controller was not very high, and the drawback coming from the sensing circuit was not considerable. However, a modification of an on-chip current sensing technique, which is an augmentation to the power switches, (SenseFET) [10, 46-47] can reduce the requirements of a high gain-bandwidth amplifier. The result can be a more power efficient controller, even for operation at high switching frequencies.
REFERENCES


REFERENCES


REFERENCES


REFERENCES


REFERENCES


[39]  Cadence design Systems available online at http://www.cadence.com


APPENDIX A

APPENDIX A - EXPERIMENTAL SETUP PICTURES

A.1. SINGLE-PHASE EXPERIMENTAL SETUP WITH ALTERA FPGA
A.2. **TWO-PHASE EXPERIMENTAL PRINTED CIRCUIT BOARD**
APPENDIX B

APPENDIX B – MOST IMPORTANT CONTROLLER HDL BLOCKS

B.1. MODE CONTROL LOGIC FSM BLOCK

`timescale 1ns / 1ps

`include "error_logic.v"
`
include "PI_compensator.v"
`
include "rslatch.v"
`
include "blank_clock.v"
`
include "Peak_LUT.v"
`
include "freq_gen.v"
`
include "Transient_Valley.v"

module CTDC
(reset,clock,enable,cntrl_sig,duty_out,dac_out,dac_clk,adc_out,adc_clock,error,icn_adc,error2,sw_clock,bl_clk,DeltaV,stateTr,valleyDetected,fixit,Icsn,Ipek,FSM_State,deltaI,switchON);

/* This is the digital part of the feedback part of the controller designed for simulation purposes where the main part is a FSM that controls the current control reference. The quantization voltage is 4mV and the zero error bin is 12mV. The compensator is LUT based based on the law ic[n] = ic[n-1] + Ke[n]. All the clocks are synchronized with each other through the freq_generator block. */

parameter n = 7;

parameter m = 9;

input clock,reset,enable,cntrl_sig;// reset is active at LOW
APPENDIX B

input [m:0] adc_out;
input [n:0] icn_adc;

output duty_out;
output dac_clk,adc_clock,sw_clock;
output [n:0] dac_out;
output stateTr, valleyDetected;
output [4:1] FSM_State;
output [n:0] Icsn, Ipeak;
output fixit;
output [n+1:0] deltaI;
output [3:0] error, error2, DeltaV;
output switchON;

wire clk_1M, clk_20M, clk_50M, clk_250M, clk_500M;
wire [n:0] icn;
wire duty, bl_clk, transientSW, switchON;
wire [n:0] Ipeak;
wire [n:0] deltaI;
reg [n:0] dac_out, PI_newRef, Icsn;
reg [8:0] counter1, counter2, counter3;
reg [14:0] counter, counter_error;
reg freezePI, fixit, duty_out;
reg temp;
assign reset_signal = (cntrl_sig & bl_clk);

freq_gen   FG   (reset,clock,clk_1M,clk_20M,clk_50M,clk_250M);
error_logic  EL  (enable,clk_1M,adc_out,error);
error_logic  EL2 (enable,clk_50M,adc_out,error2);
PI_compensator  PI (enable,7'd12,clk_1M,error,icn,freezePI,PI_newRef);
  // the compensator is LUT based
blank_clock   BC  (reset,clk_50M,clk_1M,bl_clk);
rslatch   RS  (enable,reset_signal,clk_1M,duty);
Peak_LUT   PE  (switchON,DeltaV,Ipeak,Icsn,deltaI,fixit);

Transient_Valley  TV
  (enable,clk_50M,error2,DeltaV,adc_out,stateTr,valleyDetected);

reg   [3:0] FSM_State;
parameter   [3:0] StA = 4'd0, StB = 4'd1, StC = 4'd2, StD = 4'd3, StE = 4'd4,
               StF = 4'd5, StG = 4'd6, StH = 4'd7, StI = 4'd8, StJ = 4'd9,
               StX = 4'd10;

  // This FSM is built to test the functionality of the circuit based on a
  predetermined range of values of current.
always @ (posedge clk_50M or negedge enable or posedge fixit or posedge
  cntrl_sig or posedge stateTr)
begin
  if (enable == 0)
    begin
      FSM_State <= StX;
      counter_error <= 15'd0;
      counter <= 12'd0;
APPENDIX B

counter1 <= 9'd0;
counter2 <= 9'd0;
counter3 <= 9'd0;
temp <= 1'd0;
end
else
  case (FSM_State)
  StX: begin
    dac_out <= icn;
    freezePI <= 1'b0;
    if (stateTr == temp && temp == 1'b0)
      begin
        temp <= stateTr;
        if (counter_error < 15'd3000)
          begin
            FSM_State <= StX;
            counter_error <= counter_error + 15'd1;
          end
        else
          begin
            FSM_State <= StA;
            counter_error <= 15'd0;
          end
      end
  end
end
else
  begin


APPENDIX B

FSM_State <= StX;
counter_error <= 15'd0;
temp <= stateTr;
end
end

StA: begin
dac_out = icn;
counter1 = 9'd0;
counter2 = 9'd0;
freezePI = 1'b0;
PI_newRef = icn;
if (stateTr == 1'b1 && DeltaV[3] == 1'b1)
    FSM_State <= StB;
else FSM_State <= StA;
end

StB: begin
counter2 = counter2 + 9'd1;
dac_out = 8'd255;
if (fixit == 1'b1)/
    FSM_State <= StC;
else FSM_State <= StB;
end

StC: begin
counter1 = counter1 + 9'd1;
counter2 = 9'd0;
dac_out = Ipeak;
if (cntrl_sig == 1'b1)
    FSM_State <= StD;
else FSM_State <= StC;
end
StD: begin
    counter = counter + 15'd1;
    counter1 = 9'd0;
    freezePI = 1'b1;
    PI_newRef = Icsn;
    dac_out = Icsn;
    if (counter >= 15'd150)
        FSM_State <= StE;
    else FSM_State <= StD;
end
StE: begin
    counter = 15'd0;
    dac_out = icn;
    freezePI = 1'b0;
    PI_newRef = icn;
    if (stateTr == 1'b1 && DeltaV[3] == 1'b0)
        FSM_State <= StF;
    else FSM_State <= StE;
end
StF: begin
    counter2 = counter2 + 9'd1;
    dac_out = 8'd0;
if (fixit == 1'b1 && icn_adc == 8'd0 && stateTr == 1'b0)
    FSM_State <= StG;
else FSM_State <= StF;
end

StG: begin
    counter = counter + 15'd1;
    counter2 = 9'd0;
    freezePI = 1'b1;
    PI_newRef = Icsn + 8'd4;
    dac_out = Icsn + 8'd4;
    if (counter >= 15'd2000)
        FSM_State <= StH;
    else FSM_State <= StG;
end

StH: begin
    counter1 = counter1 + 9'd1;
    counter = 15'd0;
    dac_out = icn;
    freezePI = 1'b0;
    PI_newRef = icn;
    if (counter1 >= 9'd50)
        FSM_State <= StA;
    else FSM_State <= StH;
end

default:    FSM_State <= StA;
endcase
end

always @ (posedge clk_50M or negedge enable)
begin
if (enable == 1'b0) begin
fixit <= 1'b0;
Icsn <= 8'd0;end
else if (transientSW == 1'b0) begin
fixit <= 1'b0;
Icsn <= 8'd0;end
else if (valleyDetected == 1'b1 && fixit == 1'b0) begin
Icsn <= icn_adc + 8'd9; //adding the ripple to the captured value
fixit <= 1'b1;end
else begin
Icsn <= Icsn;
fixit <= fixit;end
end

always @ (posedge clk_50M or negedge enable)
// during light-to-heavy the main switch is turned on
// during heavy-to-light the main switch is turned off
begin
if (enable == 1'b0)
duty_out <= 1'b0;
else if (FSM_State == StB ||(FSM_State == StC && !cntrl_sig))
duty_out <= 1'b1;
else if (FSM_State == StF)
    duty_out <= 1'b0;
else
    duty_out <= duty;
end

assign    adc_clock = ((transientSW || stateTr) && FSM_State != 4'd10) ?
clk_50M : clk_20M;

assign    transientSW =(FSM_State == StB || FSM_State == StC || FSM_State ==
StF || FSM_State == StG || FSM_State == StD);

assign    switchON = (stateTr || valleyDetected) && transientSW;

assign    dac_clk = clk_20M;
assign    sw_clock = clk_1M;

endmodule

B.2. PI COMPENSATOR BLOCK

timescale 1ns / 1ps
`include "error_register.v"
`include "ae_lut.v"
`include "product_adder.v"
`include "gain_multi.v"
`include "product_adder.v"
`include "saturation.v"
`include "d_register.v"
module PI_compensator(reset,gain,clock,error,icn,freeze,newRef);

    input  reset,clock;
    input  [6:0] gain;
    input  [3:0] error;
    input  freeze;
    input  [7:0] newRef;
    output [7:0] icn;

    wire   [3:0]  error_old;
    wire   [16:0] ae_product,be_product,ab_sum,ab_sum_New,gainProduct_New;
    wire   [16:0] gainProduct,ic_old,ic_new,ic_limited;
    wire   [3:0] error_New;
    wire   [16:0] ic_limNew;

    assign ic_limNew = (freeze) ? {1'b0,(newRef),ic_old[7:0]} : ic_old;
    assign error_New = (freeze) ? 4'b0000 : error;
    assign ab_sum_New = (freeze) ? 17'd0 : ae_product;
    assign gainProduct_New = (freeze) ? 17'd0 : gainProduct;

    error_register   e1  (reset,clock,error_New,error_old);//e[n-1]
    ae_lut       t1  (reset,error_New,ae_product);// A*e[n]
    gain_multi       gml1 (reset,gain,ab_sum_New,gainProduct);// K*A*e[n]
APPENDIX B

    product_adder    a2 (reset,gainProduct_New,ic_limNew,ic_new);
        //K*A*e[n]+ i[n-1]

    saturation       s1 (reset,ic_old,ic_new,ab_sum_New[16],ic_limited);

    d_register       dl (reset,clock,ic_limited,ic_old);// i[n-1] register

    d_buffer         db1 (reset,clock,ic_limited[15:8],icn);

    // MSB is the sign so it is rejected. Then we take the 8 msb-s.

endmodule
Quantization voltage is 10mV and the sense gain is 30%.

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