INTEGRATED DISTORTION SUPPRESSION CIRCUIT
FOR A HIGH FIDELITY DIGITAL CLASS-D AUDIO AMPLIFIER

by

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Department of Electrical and Computer Engineering
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Abstract

Due to the lack of feedback networks, digital class D amplifiers operating in open loop typically have inferior performance when compared to analog class D amplifiers in closed loop configuration. This thesis presents an integrated distortion suppression circuit design for digital class D amplifiers, which forms a feedback loop around the output stage. This circuit suppresses the output stage distortion and noise by equalizing the modulator effective duty ratio and the output stage effective duty ratio. The suppression circuit is integrated with the class D modulator. An integrated class D amplifier output stage is implemented separately using a 0.35μm HV-CMOS technology. Experimental results confirm that the closed loop PSRR is improved by 15dB. The THD+N value is reduced by a factor of 2 to 30. The minimum THD+N is 0.03%, which is among the state of the art class D amplifiers.
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List of Abbreviations

AES  Audio Engineering Society
APIB  Audio Precision Interface Bus
BTL  Bridge Tied Load
DAC  Digital to Analog Converter
ΔΣ  Delta-Sigma Modulation
DSP  Digital Signal Processing
DUT  Device Under Test
FFT  Fast Fourier Transform
FIR  Finite Impulse Response
I²S  Integrated Inter-chip Sound
NPWM  Natural-Sampling PWM
NTF  Noise Transfer Function
OSR  Over-Sampling Ratio
PCB  Printed Circuit Board
PWM  Pulse-Width Modulation
PSRR  Power Supply Rejection Ratio
PTAT  Proportional To Absolute Temperature
PVT  Process Voltage and Temperature
SNR  Signal to Noise Ratio
STF  Signal Transfer Function
THD  Total Harmonic Distortion
THD+N  Total Harmonic Distortion Plus Noise
UPWM  Uniform-Sampling
CHAPTER 1

Introduction

1.1 OVERVIEW

Power amplifiers are a family of circuits that can provide power gain to the input signals. They can be classified as class A, B, AB, C, D, E, etc., according to their output stage topology.

Audio amplifiers are a subset of power amplifiers designed to amplify audio signals in the range of 20 Hz to 20 kHz (the human range of hearing). They are widely used in car audio systems, home entertainment systems, PC audio systems, and professional audio systems. Traditionally, most audio amplifiers are linear amplifiers operating in class A, B or AB. Recently, class D amplifiers have become a popular choice for audio amplifiers. They are switching amplifiers that offer many advantages over class B or AB amplifiers, such as higher efficiency (theoretically can be as high as 100%), smaller size and weight, smaller (or no) heat sinks, and lower cost.

1.2 BASICS OF CLASS D AMPLIFIER

A class D amplifier consists of a modulator and an output stage. The modulator generates a train of pulses modulated by the audio signal. The modulation process used in class D amplifier is typically Pulse Width Modulation (PWM). One possible implementation of the PWM is as shown in Figure 1.1. The PWM signal results from
comparing the input signal and a high frequency sawtooth carrier signal. The PWM signal contains the frequency content of both the input signal and the carrier signal.

![Diagram of PWM](image)

**Figure 1.1** One possible implementation of the PWM.

An H-bridge output stage is commonly used in class D amplifiers. The output stage consists of four power transistors and LC filters (see Figure 1.2). The output stage works as follows: during phase $\Phi_1$, transistor M2 and M3 turn ON, and current starts to flow from VDD to GND, shown as the solid lines in Figure 1.2. During phase $\Phi_2$, transistor M1 and M4 turn ON, resulting in current flowing in the opposite direction. The net result is that the input train of pulses is replicated with larger amplitude. When the amplified PWM waveform passes through the second order LC filter, the carrier signal is filtered out and the audio signal is recovered.
Figure 1.2 Operation of an H-bridge class D amplifier output stage.

There are two approaches to implement a class D amplifier modulator, namely analog and digital. Analog modulators use analog building blocks, such as op-amps and comparators to realize the PWM modulation, as shown in Figure 1.3. Integrated analog modulators require custom layout, and need to be redesigned for different technologies. Some of them are designed to include a feedback network in order to improve the performance. The feedback network implementation is straightforward because both the input and the output are analog signals. For consumer electronics applications, audio data is typically stored, processed, and transmitted in digital form. To use an analog class D amplifier, a DAC is required to convert the audio from digital to analog domain. The overall system performance, of course, will depend on the quality of DAC. It should be noted that most analog class D amplifiers reported are tested with analog input.
An alternative approach is to implement the modulator using digital signal processing. The digital modulator is able to accept digital inputs from storage media and generate modulation signals directly (see Figure 1.4). Adding a feedback network, in this case, is difficult because the input and output are across different signal domains. As a result, due to the lack of feedback networks, digital class D amplifiers operating in open loop typically have inferior performance, comparing to analog class D amplifiers in closed loop. On the other hand, digital class D amplifiers are more robust to process variations, more economical, easier to migrate between different technologies, more immune to noise and compatible with digital input directly.

The focus of this thesis is to develop a digital class D amplifier that can operate in closed loop configuration to obtain better performance. Specifically, the objective is to design and implement a feedback network for a digital class D amplifier. The target performance must be at least comparable to the analog versions.
1.3 LITERATURE SURVEY

Some of the major performance indicators of a class D amplifier include efficiency, audio quality and Power Supply Rejection Ratio (PSRR). The focus of this work is to improve the audio quality and PSRR for digital class D amplifiers. To test the audio quality, the input test tone is typically set to 1 kHz, and the Total Harmonic Distortion plus Noise (THD+N) is measured at the output. THD+N is defined as the ratio of the sum of the powers of all harmonic components plus noise to the power of the fundamental frequency (1.1).

\[
THD + N = \frac{\sum Harmonic Power + Noise Power}{Total Output Power}
\] (1.1)

The THD+N value is not constant across all input frequencies and output power levels. Therefore, THD+N is typically plotted against output power and input frequency. The performance between class D amplifiers can be compared by looking at the minimum THD+N for all output levels above 1W using 1 kHz input. Figures 1.5 shows the literature survey of recently published or manufactured class D audio
power amplifier performance based on the minimum THD+N. It can be seen from
Figure 1.5 that analog class D amplifiers in closed loop [1] [2] achieved the lowest
THD+N value.

1.4 THESIS ORGANIZATION

In the following chapters, a feedback network design for digital class D amplifiers is discussed. Chapter 2 covers the system level design considerations and simulation results. Chapter 3 shows the details of implementation using CMOS technology. Chapter 4 presents the output stage design. Finally, experimental results are shown in Chapter 5 and a summary is presented in Chapter 6.
2.1 CLASS D MODULATOR

2.1.1 PWM modulation

Class D amplifiers typically use PWM modulation to modulate the audio signal. PWM modulation has a few variations. In an analog class D amplifier, Natural-Sampling PWM (NPWM), shown in Figure 2.1, is often used. The sampling point occurs when the input signal and the carrier intersect and there is no base-band distortion introduced. In a digital system, however, uniform sampling has to be used due to its discrete nature. The Uniform-Sampling PWM (UPWM) introduces base band distortion, as shown in Figure 2.1.

Figure 2.1 Comparison of the NPWM and UPWM.
One method to correct the UPWM distortion is to employ the time domain interpolation. Figure 2.2 shows one implementation using linear time domain interpolation. Shown in Figure 2.2, the difference between Pseudo-Natural PWM (PNPWM) and NPWM are significantly reduced. PNPWM is employed in this design.

The above discussion is focused on left edge aligned PWM. An alternative approach is called center-aligned double-edge-modulated PWM, which is used in this work because this scheme offers lower distortion [17]. In a center-aligned double-edge-modulated PWM, both the falling and rising edges are modulated with reference to the center of switch period, and two different input samples are used in every switching period to modulate the two edges independently (see Figure 2.3).
2.1.2 Modulator design

The digital audio signal has very long word length (14, 16 or 24 bits), hence, direct PWM modulation is not practical because the frequency of the digital clock required would be well beyond the GHz range. A delta-sigma modulator can be inserted before the PWM modulator such that fewer bits are required to represent the same signal due to noise shaping. However, delta-sigma modulation requires oversampling, therefore, up-sample and interpolation also needs to be performed before the delta sigma modulation.

The class D modulator incorporates all the digital signal processing techniques discussed above, and the functional block diagram is shown in Figure 2.4. The delta-sigma modulator is supplied by Asahi Kasei EMD Corporation, and other circuit blocks are directly taken from [18].
2.2 ORIGIN OF DISTORTION

A few factors contribute to the class D amplifier signal distortion. Error in the PWM signal from the modulator due to limited resolution and timing jitters introduces PWM imperfection. Timing errors are also introduced by the gate driver due to finite rise/fall time, and finite turn ON/OFF time of the power transistors in the output stage. In addition, for audio power amplifiers, researchers have found that dead time is one of the major sources of distortion [19]. Dead time is a brief period of time during a switching cycle when both the high side and low side switches are off (see Figure 2.5). It is purposely introduced to the switching waveform to prevent shoot-through current from flowing between VDD and GND. This shoot-through current will reduce efficiency and in the extreme case, may lead to device breakdowns. For example, in an H-bridge configuration (see Figure 2.6), after transistors M2 and M3 turn OFF, a dead time period is required before transistors M1 and M4 to turn ON.
However, during the dead time period, the switching nodes are not driven. Inductor current starts to flow through the body diodes (see Figure 2.6). The voltage across the load now depends on the inductor current and its direction. It is out of the control of the modulator. The output waveform could be corrupted, leading to harmonic distortion.

The output stage is also very sensitive to the power supply noise. In an open-loop class D amplifier, the Power Supply Rejection Ratio is typically very poor [20]. The power supply noise becomes another major source of distortion if the output stage is operated without using a well-regulated power supply.

Finally, parasitics in the output stage as well as the power MOSFET on-resistance are also distortion contributors. In general, their effects are secondary compared to dead time and power supply noise. However, the selection on the type of inductors and capacitors could greatly influence the amount of distortion. This may not be immediately obvious to inexperienced class D amplifier designers.
The linearity of the LC filter inductor and capacitor is very important. THD+N could degrade as much as 10 times at certain frequency range or output power range with certain types of inductors and capacitors. Figures 2.7 and 2.8 show the performance impacts of different inductor choice and capacitor choice. In Figure 2.7, inductor 1 gives much better performance, especially at high output power. In Figure 2.8, poly film capacitor gives constant THD+N performance in the audio band, whereas ceramic capacitor introduces peaking at high frequencies. Note that the THD+N versus frequency response has a dip at around 6.7 kHz. More details on this topic will be presented in Chapter 4.

The dominant distortion contributors such as dead time and power supply noise are the focus of this work. A proposed feedback network is placed between the class D modulator and the output stage in order to suppress the distortion originated from the output stage. The new class D modulator design is shown in Figure 2.9.
Figure 2.7 Performance impact of the inductor choice.

Figure 2.8 Performance impact of the capacitor choice.
2.3 METHOD OF COMPENSATION

2.3.1 Effective duty ratio

Although the PWM switching waveform consists of rectangular pulses, the actual switching waveform at the switching nodes of the output stage could be corrupted as shown by the solid line in Figure 2.10 due to reasons discussed in section 2.2.

Before proceeding with the discussion on methods to compensate this discrepancy between the modulator PWM and output stage PWM, it is useful to define the effective duty ratio. The effective duty ratio $D_{\text{eff}}$ is the average voltage of a
pulse during each switching period divided by the nominal supply voltage (2.1).

\[ D_{\text{eff}} = \frac{1}{T_s} \int_0^{T_s} \frac{V_{\text{saw}}(t)}{V_{\text{nom}}} \, dt \]  

(2.1)

The effective duty ratio greatly simplifies the analysis on switching waveforms.

Two switching waveforms can be considered to be similar to each other if their effective duty ratios are the same, even though their shapes are different. Distortion at the output stage can be essentially modeled as an error term in the effective duty ratio. The modulator PWM duty ratio can be defined as \( D_{\text{mod}}[n] \). After passing through the output stage, \( D_{\text{dist}}[n] \) is added to \( D_{\text{mod}}[n] \), and the output stage duty ratio \( D_{\text{out}}[n] \) becomes \( D_{\text{mod}}[n] + D_{\text{dist}}[n] \), as shown in (2.2).

\[ D_{\text{out}}[n] = D_{\text{mod}}[n] + D_{\text{dist}}[n] \]  

(2.2)

Distortion can be suppressed, as long as the effective duty ratio of the output stage output matches the effective duty ratio of the modulator output, i.e. \( D_{\text{out}}[n] = D_{\text{mod}}[n] \). In other words, by equalizing \( D_{\text{out}}[n] \) and \( D_{\text{mod}}[n] \), the output voltage waveform at the load will match the modulated audio signal, after low pass filtering. Note that, in practice, \( D_{\text{dist}}[n] \) cannot be eliminated due to physical and electrical limitations.

2.3.2 Compensation in time domain

In order to achieve the goal of equalizing \( D_{\text{out}}[n] \) and \( D_{\text{mod}}[n] \), \( D_{\text{mod}}[n] \) cannot be used to drive the output stage anymore. It seems logical to use \( D_{\text{mod}}[n] - D_{\text{dist}}[n] \) to drive the output stage. However, this would require exact knowledge on the value of \( D_{\text{dist}}[n] \). In a real system, however, \( D_{\text{dist}}[n] \) cannot be obtained before passing through the output stage. One option is to use \( (D_{\text{mod}}[n] - D_{\text{dist}}[n-1]) \) to drive the output stage [18]. Since the PWM frequency is much higher than the signal frequency, \( D_{\text{dist}}[n-1] \)
would be very close to $D_{\text{dist}}[n]$. After passing through the output stage, $D_{\text{out}}[n]$ then becomes $(D_{\text{mod}}[n] - D_{\text{dist}}[n-1]) + D_{\text{dist}}[n]$, as shown in (2.3). As a result, the difference between $D_{\text{out}}[n]$ and $D_{\text{mod}}[n]$ are reduced significantly. Equation (2.3) is the fundamental of this work.

$$D_{\text{out}}[n] = (D_{\text{mod}}[n] - D_{\text{dist}}[n-1]) + D_{\text{dist}}[n] \quad (2.3)$$

2.3.3 Frequency domain modeling

Equation (2.3) seems reasonable in the time domain. However, the system behavior needs to be analyzed in the frequency domain as well to prove its functionality. The analysis in the frequency domain is presented in this section.

Applying Z-transform to (2.3), the following can be obtained.

$$D_{\text{out}}(Z) = D_{\text{mod}}(Z) + (1 - Z^{-1})D_{\text{dist}}(Z) \quad (2.4)$$

In general, $\text{Output}(Z) = \text{STF}(Z) \times \text{Input}(Z) + \text{NTF}(Z) \times \text{Noise}(Z)$, whereas $\text{STF}(Z)$ is the signal transfer function and $\text{NTF}(Z)$ is the noise transfer function. Comparing with (2.4), it is straightforward to realize that $\text{STF}(Z)$ is 1, whereas $\text{NTF}(Z)$ is $(1 - Z^{-1})$.

Since the STF is 1, the input signal is not altered in amplitude or phase. However, the distortion is shaped by $(1 - Z^{-1})$, which is the same NTF of a Delta-Sigma MOD1. This NTF has +20dB/decade slope in its frequency response (see Figure 2.11). If a PWM switching frequency of 384 kHz is used, then the NTF has a suppression effect on all the noise within audio band, as shown in Figure 2.11. Note that the NTF has more suppression effect on low frequency signals than high frequency signals.
To facilitate a system level simulation, a Z-domain model is constructed (see Figure 2.12) [18].

Comparing to (2.4), \( C(Z) \) and \( H(Z) \) can be obtained, as shown in (2.5).

\[
\begin{align*}
\begin{cases} 
H(Z) = Z^{-1} \\
C(Z) = \frac{1}{1-Z^{-1}}
\end{cases}
\end{align*}
\]  

(2.5)
2.3.4 MATLAB simulation

The system level simulation is performed in MATLAB and SIMULINK. In MATLAB, a train of center-aligned PWM pulses is generated. The effective duty ratio of each pulse is calculated and stored in an array. It is then passed to the distortion suppression model in SIMULINK. The resulting duty ratios are fed back into MATLAB and the PWM pulses are reconstructed. FFT is performed on the output signal after low pass filtering in order to avoid aliasing. The entire simulation procedure is as shown in Figure 2.13.

![Figure 2.13 System level simulation procedure.](image)

The SIMULINK model of the distortion suppression circuit is as shown in Figure 2.14. It is built based on Figure 2.12 and (2.5). The saturation block makes sure that no output duty ratio is larger than 1 or less than 0. The noise generator introduces disturbance to the duty ratios, to model the power stage non-idealities and power supply noise. Since THD+N measures the combined effects of harmonic distortion and noise, it is worthwhile to investigate the system's behaviour with different noise types.
1) Gaussian distributed noise

A Gaussian distributed noise source is added to the distortion suppression model. To introduce a moderate amount of distortion, the mean value and the variance are set to be 0.05 and 0.0004 respectively. A time domain plot of the PWM duty ratio noise is shown in Figure 2.15.

After simulation, three FFT plots are obtained in Figure 2.16. It can be seen that the Modulator PWM only has the fundamental frequency component (1 kHz) and the noise floor is low and flat. However, after introducing the Gaussian noise, the output stage PWM has a much higher noise floor, which appears flat in the audio band as well. With the help of distortion suppression technique, the output stage PWM achieves 20dB/decade distortion suppression within the audio band. It should be noted that the distortion suppression technique cannot achieve lower noise floor than the noise that is already embedded in the original input signal by the modulator PWM.
Figure 2.15 Gaussian distributed PWM duty ratio noise.

Figure 2.16 Comparison of the output stage PWM w/ and w/o distortion suppression.
2) Harmonic distortion

A harmonic distortion source is added to the distortion suppression model. It consists of the 3rd, 5th, 7th and 9th harmonics of the fundamental frequency 1 kHz. Figure 2.17 shows a time domain plot of the PWM duty ratio error.

Similarly, three FFT plots are obtained (Figure 2.18). After introducing the harmonic distortion, the output stage PWM shows 4 extra frequency tones at 3 kHz, 5 kHz, 7 kHz, and 9 kHz. With the help of distortion suppression technique, the output stage PWM has 27 dB lower 3rd harmonic tone. Referring back to Figure 2.11, it can be seen that the NTF is also around -27 dB at 3 kHz, which proves that the distortion suppression technique is capable of reducing the 3rd harmonic by -27 dB in the ideal case, if the input frequency is set to 1 kHz. Other harmonic tones are suppressed less than -27 dB because the NTF has 20 dB/decade frequency response. This is not an issue because the 3rd harmonic typically dominates the THD+N and higher order harmonics are already much lower than the 3rd harmonic before
distortion suppression.

Figure 2.18 Comparison of the output stage PWM w/ and w/o distortion suppression.

Figure 2.19 Comparison of the output stage PWM w/ and w/o distortion suppression.
When both the Gaussian noise and harmonic distortion are present, the 3rd harmonic tone can still be suppressed by 27dB and the noise floor also has 20dB/decade suppression (see Figure 2.19).

2.4 SYSTEM REALIZATION

To realize the distortion suppression technique in a real system, an integrator is required to obtain the effective duty ratio $D_{\text{out}[n]}$ and $D_{\text{mod}[n]}$. If a PWM switching waveform with effective duty ratio $D_{\text{eff}}$, and a nominal voltage of $V$ is integrated over the period $T_s$, the result would be $V_{\text{out}}(T_s) = D_{\text{eff}}T_sV$ (see Figure 2.20). $D_{\text{eff}}$ can be extracted from $V_{\text{out}}(T_s)$ easily by removing the constant $T_sV$.

![Figure 2.20 Integration of a PWM waveform.](image)

Referring to Figure 2.21, a proposed algorithm [18] to realize (2.3) is presented as follows:

1. In cycle 0, the modulator output $D_{\text{mod}[0]}$ is integrated positively with respect to time and $D_{\text{mod}[0]}VT_s$ is obtained.

2. The output stage duty ratio $D_{\text{out}[0]}$ is then integrated negatively on the same integrator and $-D_{\text{out}[0]}VT_s$ is obtained.

3. The integrator now stores the difference $D_{\text{mod}[0]}VT_s - D_{\text{out}[0]}VT_s$, which is
essentially $-D_{\text{dist}}[0]VT_s$.

4. In cycle 1, without resetting the integrator, continue to integrate $D_{\text{mod}}[1]$ positively, and use the net result $D_{\text{mod}}[1]VT_s - D_{\text{dist}}[0]VT_s$ to drive the output stage in cycle 1. Of course, $D_{\text{mod}}[1]VT_s - D_{\text{dist}}[0]VT_s$ is a voltage value, and the duty ratio information embedded, which is $D_{\text{mod}}[1] - D_{\text{dist}}[0]$, needs to be extracted and the PWM waveform needs to reconstructed from the duty ratios.

![Figure 2.21 A distortion suppression algorithm in time domain.](image)

Note that $D_{\text{dist}}[n]$ can be either positive or negative because the distortion could be due to the energy lost or stored in the parasitic components in the output stage.

The above algorithm can be realized using integrators and comparators, and the detailed block diagram is shown in Figure 2.22 [18]. An analog integrator is used to perform the integration function mentioned above. The PWM waveform is reconstructed using a comparator, and an inverting circuit is used to obtain a negative integral. A multiplexer (MUX) is also required to select different input signals.
for integration.

The implementation shown in Figure 2.22 is suitable for a left-edge aligned PWM modulation scheme. However, center aligned PWM modulation is used in this work. Hence, two separate circuits are required to process both the rising edge and the falling edge. The system block diagram is shown in Figure 2.23 [18].

A possible circuit implementation is proposed in [18], and is as shown in Figure
2.24. The resistor network on the left is used to attenuate the high voltage swing of the output stage switching waveform. The upper circuit is used to process the PWM rising edge and the bottom circuit is used to process the PWM falling edge. Integrators are reset with RST_R and RST_F at the very beginning to zero the capacitor voltage. FB_R and FB_F control the output stage PWM feedback signal flow. PWM_L_R, PWM_L_F, PWM_H_R and PWM_H_F control the modulator PWM signal flow. A MUX is used to combine the rising edge and falling edge of the compensated PWM, which goes through a digital deglitch block to remove possible glitches. All control signals are generated digitally.

The system design and considerations for the digital class D amplifier distortion suppression circuit have been presented in this chapter. The IC implementation of this circuit is presented next.
CHAPTER 3

IC Implementation

3.1 OVERVIEW

The distortion suppression circuit is integrated with a digital class D amplifier modulator using a standard 0.35μm CMOS technology. The block diagram for the digital modulator chip is as shown in Figure 3.1. The PLL, delta-sigma modulator (inside digital core) and reference circuit (REVBLK) were supplied by Asahi Kasei EMD Corporation. The distortion suppression circuit is highlighted in the figure, which includes the analog feedback block, de-glitch block, D flip-flop arrays, and PWM generators with switch control.

The distortion suppression circuit is realized using a mixed signal approach. The PWM integration and reconstruction process are implemented by the analog feedback block. The de-glitching, PWM generation and switch controls are built from digital logic. This chapter presents the detailed design of each circuit block.

3.2 ANALOG FEEDBACK DESIGN

The most important design for this work is the analog feedback block. Its schematic is re-captured in Figure 3.2. The top integrator integrates the rising edge of the modulator PWM and output stage PWM signals. A 2.5V reference voltage is used as the virtual ground reference. The integrator’s input is tied to 5V or 2.5V
during reference phase, depending on the logic level of the modulator PWM. During the feedback phase, FB_R turns on and allows the attenuated output stage PWM to be integrated in the negative direction.

![Figure 3.1 Digital class D amplifier modulator with distortion suppression circuit.](image)

Similarly, the bottom integrator integrates the falling edge of the modulator PWM and the output stage PWM signals. However, the attenuated output stage PWM, which has 0 to 2.5V voltage swing, is below the virtual ground (2.5V). In order to perform positive integration, a pull-up resistor is introduced to increase the voltage levels from 0V-2.5V to 2.5V-3.75V. After pulling up, however, the voltage swing is reduced by half, which needs to be compensated at the integrator by reducing the input resistor by half. As a result, the feedback branch and reference branch are
separated. Notice that the feedback branch (FB_R) is tied to the virtual ground (2.5V) when reference branch is active. This guarantees that the feedback branch has no contribution to the integral when the modulator PWM signal is being integrated.

Figure 3.2 Block diagram of the analog feedback block [18].

3.2.1 Op-amp design

There are a few op-amp topologies available to analog designers. A comparison of performance of various op-amp topologies is shown in Table 3.1 [21]. Since op-amps typically consume most of the power in an analog circuit, in order to maintain the high efficiency merit of the class D amplifier, it is desirable to use power efficient op-amps. In addition, the integrator output demands high voltage swing in order to handle the full duty ratio 100%.

Table 3.1 Comparison of performance of various op-amp topologies [21].

<table>
<thead>
<tr>
<th></th>
<th>Gain</th>
<th>Output Swing</th>
<th>Speed</th>
<th>Power Dissipation</th>
<th>Noise</th>
</tr>
</thead>
<tbody>
<tr>
<td>Telescopic</td>
<td>Medium</td>
<td>Medium</td>
<td>Highest</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>Folded-Cascode</td>
<td>Medium</td>
<td>Medium</td>
<td>High</td>
<td>Medium</td>
<td>Medium</td>
</tr>
<tr>
<td>Two-Stage</td>
<td>High</td>
<td>Highest</td>
<td>Low</td>
<td>Medium</td>
<td>Low</td>
</tr>
<tr>
<td>Gain-Boosted</td>
<td>High</td>
<td>Medium</td>
<td>Medium</td>
<td>High</td>
<td>Medium</td>
</tr>
</tbody>
</table>
Based on the above requirements, the two-stage op-amp topology is selected for high voltage swing and medium power consumption. In addition, the consideration for low noise further re-enforced the choice for this topology.

The schematic of the two stage op-amp is as shown in Figure 3.3 with transistor sizing and DC operating condition annotated. The compensation resistor and capacitor are included to improve the phase margin. Performance specifications are summarized in Table 3.2.

![Figure 3.3 Two stage op-amp with source follower.](image)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition/Comments</th>
<th>Simulated Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slew Rate</td>
<td>Max integrator output swing 2V (62pF &amp; 50k)</td>
<td>0.8V/μs</td>
</tr>
<tr>
<td>Gain Bandwidth Product</td>
<td>Smaller the settling time, the better</td>
<td>100MHz</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>Output ringing must be avoided</td>
<td>85 °</td>
</tr>
<tr>
<td>Power consumption</td>
<td>As low as possible</td>
<td>2.5mW</td>
</tr>
<tr>
<td>Layout Area</td>
<td>As small as possible</td>
<td>80μm x 80μm</td>
</tr>
</tbody>
</table>
The integrator’s time domain behavior was verified using Hspice simulations. The transient response is as plotted in Figure 3.4. The integrator output waveform is clean and free of ringing.

![Integrator transient simulation result.](image)

3.2.2 Comparator design

The comparator used in this design is shown in Figure 3.5. The circuit performs preamp and positive feedback at the first stage, and converts differential signal to single-ended signal at the second stage. Finally, the inverter chain restores the logic level to rail to rail.

Simulation results of the comparator are summarized in Table 3.3, and a transient simulation is shown in Figure 3.6.
Table 3.3 Comparator performance summary.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition/Comments</th>
<th>Simulation Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Swing</td>
<td>Rail to rail is required</td>
<td>Rail to Rail</td>
</tr>
<tr>
<td>Propagation Delay</td>
<td>As small as possible to reduce PWM duty</td>
<td>F: 7.6ns</td>
</tr>
<tr>
<td></td>
<td>cycle limitation</td>
<td>R: 7.3ns</td>
</tr>
<tr>
<td>Rise/Fall Time</td>
<td>Fast transition to reduce jitter</td>
<td>F: 0.89ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>R: 0.94ns</td>
</tr>
<tr>
<td>Power consumption</td>
<td>As low as possible</td>
<td>0.5mW</td>
</tr>
<tr>
<td>Layout Area</td>
<td>As small as possible</td>
<td>80μm x 70μm</td>
</tr>
</tbody>
</table>

3.2.3 Biasing circuit design

The biasing circuit should exhibit little dependence on power supply noise and process variation, and can be classified as follows [21]:

1) Proportional To Absolute Temperature (PTAT)

2) Constant transconductance

3) Temperature independent
The op-amp and comparator designs assume a 15μA reference current. The question is: how to generate this current $I_{\text{ref}}$? The biasing circuit should only rely on itself to generate this current with minimum dependence on power supply noise, i.e. the biasing circuit should somehow bias itself. Option 2 discussed above is able to provide this $I_{\text{ref}}$.

A simple circuit that can bias itself is shown in Figure 3.7 (a). If transistor M3 and M4 are sized to be $K$ times larger than M1 and M2, then $I_{\text{out}} = KI_{\text{ref}}$. Note that this circuit is able to support arbitrary current level after start-up. In order to uniquely define this current, a modification as shown in Figure 3.7 (b) is required. The resistor $R$ helps to introduce another constraint to the circuit, hence uniquely defining the current. Notice that $I_{\text{out}}$ is not a function of VDD, but can be affected by temperature and process parameters [21].
Taking the circuit in Figure 3.7 (b) one step further, using wide swing cascode current mirror can minimize most of the second-order imperfections. The complete circuit diagram is shown in Figure 3.8 [22].

Biasing circuit may have the possibility of having zero current in the loop upon start-up. A start-up circuit is necessary to bring the circuit out of this state and turns off itself once the biasing circuit is working properly. One possible implementation of the start-up circuit is as shown in Figure 3.8. In case there is zero current in the self-biased current mirror, the gate voltage of M10 and M11 is close to GND, which implies that transistor M19 is off. The weak pull-up transistor M5 will pull the gate of M17 and M18 high and subsequently turn them ON. Current starts to flow through M17 and M18, hence lowering the gate voltage $V_{bp1}$ of M2/M3 and $V_{bp2}$ of M6/M7. Once $V_{bp1}$ and $V_{bp2}$ are low enough, transistor M2/M3 and M6/M7 turn on, and bring the self-biased current mirror out of the zero current state.
After stable current has been established in the loop, \( V_{bn2} \) is high enough to turn on transistor M19, which subsequently turn off transistor M17 and M18 by lowering their gate voltage. In this state, the start-up circuit does not interfere with the biasing circuit any more, except for a small amount of constant current flowing through M5. In order to keep this quiescent current low, the transistor M5 should have very small W/L ratio. In addition, small transistor M5 also makes sure that when both transistor M5 and M19 are on, the drain voltage of M5 will be pulled to low by a stronger transistor M19.

### 3.2.4 Switch design

The easiest way to implement a switch is to use a single NMOS or PMOS transistor. The disadvantage of this approach is that the on-resistance of a single MOSFET is not constant with respect to the input voltage. Specifically, the PMOS transistor's on-resistance becomes prohibitively large when the input is close to GND. NMOS switch has the same disadvantage when the input is close to VDD. In order to achieve a relatively constant on-resistance, a transmission gate is typically used.

For this design, the on-resistance of the switch has to be low, to avoid large voltage drop across the switch. The switches on the output stage feedback path are sized to have \( R_{on} \) of 10\( \Omega \), whereas the switches on the reference path are sized to have \( R_{on} \) of 50\( \Omega \). The relative large transistor sizes imply large charge injection during switching. One way of cancelling the charge injection effect is to include a dummy switch, which is half of the size of the actual switch. This approach is not used in order to reduce the parasitic capacitance on the signal path. Another
approach is to use the transmission gate, which is used in this design. By using a parallel connection of both a NMOS and a PMOS switch, opposite charge packages cancel each other, as shown in Figure 3.9.

![Figure 3.8 The biasing circuit with start-up circuitry [22].](image)

![Figure 3.9 Use of complimentary switch to reduce charge injection [21].](image)
The exact cancellation of charge injection only occurs at one input voltage, and (3.1) [21] has to be satisfied. With other input voltages, this approach still offers significant cancellation. Note that, in this design, the input resistance of the integrator is high; hence most of the charge injected flows to the other side of the switch, which is low impedance.

\[ W_n L_n C_{ox} (V_{ck} - V_{in} - V_{thn}) = W_p L_p C_{ox} (V_{in} - |V_{thp}|) \]  

(3.1)

Inverter chains are used to drive the large gate capacitance of the transmission gate. Complementary clock signals are required, and their timing has to be matched in order to turn ON or OFF two switches simultaneously. A delay cell [21] (see Figure 3.10) is introduced to balance the clock skew. Hspice simulation shows that the clock skew is not noticeable after fine tuning the delay.

![Diagram of transmission gate and its gate driver](image)

Figure 3.10 Transmission gate and its gate driver.

3.2.5 Layout design

Although the top and bottom capacitors used in the integrators are not required to be matched precisely, it is desirable for them to have similar capacitance.
Therefore, layout matching technique is applied. Instead of laying out two separate capacitors, they are laid out with unit cells. Shown in Figure 3.11 (a), capacitor 1 and capacitor 2 are laid out in a checker board pattern. In this way, variation along all directions can be compensated and mismatch between capacitor 1 and 2 is minimized. In addition, dummy cells are surrounded around the core area to minimize the capacitance variation at the core edges, as shown in Figure 3.11 (b).

The input resistors for the falling edge integrator require good matching ratio 2:1. Since process variation is possible along any directions, the two resistors are laid out using the inter-digitated technique. As a result, both resistors experience the same variation and the mismatch between them can be minimized. A small portion of the layout is as shown in Figure 3.12. The left most and right most two columns are dummy resistors.

Figure 3.11 (a) Capacitor layout matching technique. (b) Dummy cells.
3.3 DIGITAL CIRCUIT DESIGN

The PWM generator and switch control block are coded in Verilog, and are implemented using the standard cell approach. The design flow is automated using synthesis tools and automatic place & route tools. Figure 3.13 shows the functional block diagram of these two circuit blocks and their interconnection. The PWM generator requires a clock frequency that is 4096×fs (48 kHz × 4096 = 196.608 MHz). This can be generated by an on-chip PLL or supplied off-chip. The reset switch is used to reset all internal flip-flops and prepares for the circuit to start up.

The switch control block generates the switch control signals for the analog feedback block. It also provides an option to turn off the distortion suppression circuit by asserting OL_LOOP signal low.
Figure 3.13 The PWM generator and switch control block.

The timing diagram of the switch control signals is as shown in Figure 3.14. The modulator PWM has a frequency of $8f_s$ ($48 \text{ kHz} \times 8 = 384 \text{ kHz}$). The RST_R and RST_F signals reset the integrator when they are high, and are subsequently lowered after the main RST goes low. The PWM_H_R and PWM_L_R control the rising edge reference switches, whereas the PWM_H_F and PWM_L_F control the falling edge reference switches. When $SW_F$ is active, the falling edge of the output stage PWM is on feedback and the rising edge of the modulator PWM is on referencing. When $SW_R$ is active, the rising edge of the output stage PWM is on feedback and the falling edge of the modulator PWM is on referencing.
The deglitch block (see Figure 3.15) filters the glitches in PWM waveforms and guarantees that only one pulse exists in one period. It is essential because the comparator output is prone to glitches.

The schematic of the dead time generator is enlarged in Figure 3.15, which is realized using inverter chains. Based on the simulation result, the dead time is 20ns, which can be turned to 0ns if required.

3.4 SYSTEM INTEGRATION

Consumer electronics industry demands multi-channel audio amplifiers. This prototype supports stereo operation, where the left channel and the right channel may have independent audio inputs. Shown in Figure 3.16, duplicated output stage
Hardware is required to amplify the left channel and the right channel independently. Each channel has two switching networks, namely side A and side B. Hence, four feedback circuits in total are required.

![Figure 3.16 Stereo class D amplifier output stage.](image)

Each feedback circuit consists of two feedback networks. As a result, there are 8 feedback networks that need to be controlled. One of the design challenges is to make sure that each of them is at the correct state, reference or feedback, depending on the status of output stage PWM and modulator PWM. To visualize this, Figure 3.17 (a) and (b) show two possible circuit states during normal operation. To minimize the digital hardware, the switch control signals are shared among feedback network by using appropriate digital logic manipulation.

![State (a)](image)
3.5 DESIGN FOR TESTABILITY

It is a good practice to design an integrated circuit that is testable and can be debugged easily. For a complex system, it is useful to have a test chip where individual modules are laid out separately, and the module I/Os are made available as chip I/Os. Digital designs should have some critical points of interests available as chip I/Os by using buffers. Typically, the number of critical points is much more than the number of the available chip pins. In this case, multiplexers can be used. However, for analog designs, digital buffers cannot be used. Hence, a unity gain amplifier (see Figure 3.18) is used in order to drive the large capacitance seen at the bond pad/bonding wire and test probes. This design includes a few unity gain buffers for testing and debugging purposes.
Referring to Figure 3.19, the attenuation resistor network (R5 and R6) are not integrated on chip. This is done intentionally such that R5 and R6 can be adjusted for different output stage power supply voltage. Resistors R1-R4 are integrated on chip to reduce parasitic capacitance at the internal nodes of the circuit. The pull-up resistor R4 is made adjustable by using an integrated trimming resistor shown in Figure 3.20, so that the effect of R4 variation can be studied. By selectively turning on transistors M1 to M4, different resistors are made in parallel and the total resistance can be adjusted in fine steps. Note that variation on R4 can also be adjusted by changing the resistance value of R5 and R6 proportionally. Therefore, the trimming resistor is not really required.

3.6 MISMATCH ANALYSIS

Integrated circuit technology provides a platform for implementing accurately matched capacitors. Using good layout techniques, capacitance can be matched to 0.1%. However, resistors cannot be matched with precision.
Referring again to Figure 3.19, resistors do not have to be precisely matched between feedback networks. However, resistor R2 and R3 have to be matched with 1:2 ratio in order to implement (2.3) correctly. Note that (2.3) can be rewritten as (3.2). With layout matching technique discussed in 3.2.5, matching results can be significantly improved, but not to a degree that can be ignored. Performance impacts of R2 and R3 mismatch need to be taken care of during the design phase.

\[
D_{\text{out}}[n] = (D_{\text{meas}}[n] + (D_{\text{meas}}[n-1] - D_{\text{out}}[n-1])) + D_{\text{dist}}[n]
\]  
(3.2)
Assuming that there is a 10% mismatch between R2 and R3, the implication is that the coefficient of $D_{out}[n-1]$ is no longer at unity, but at $(1+k)$. The constant $k$ accounts for the mismatch and can be $+0.1$ or $-0.1$. Equation (3.3) can be obtained by substituting this change into (3.2).

$$D_{out}[n] = (D_{mod}[n] + (D_{mod}[n-1] - D_{out}[n-1] - kD_{out}[n-1])) + D_{dist}[n]$$

$$= (D_{mod}[n] + (-D_{dist}[n-1] - kD_{out}[n-1])) + D_{dist}[n]$$

Applying $Z$-transform to (3.3), the result is as shown in (3.4). Note that the new STF and NTF differ from (2.5) by a factor of $(1+kZ^{-1})^{-1}$ (3.5).

$$(1 + kZ^{-1})D_{out}(Z) = D_{mod}(Z) + (1 - Z^{-1})D_{dist}(Z)$$

$$\begin{align*}
STF &= \frac{1}{1+kZ^{-1}} \\
NTF &= \frac{1-Z^{-1}}{1+kZ^{-1}}
\end{align*}$$

Using MATLAB, the new STF and NTF are plotted in Figure 3.21. The graph shows that the newly introduced $(1+kZ^{-1})^{-1}$ term has minimum impacts on the frequency response of the STF and NTF in the audio band.

Figure 3.21 Frequency responses of the STF and NTF with $k=0$, $0.1$ and $-0.1$. 
Before making any conclusion, it is worthwhile to simulate the effects of $k$ in the system level. Referring to (3.6), $C(Z)$ remains unchanged from (2.5), whereas $H(Z)$ has an additional term $kZ^{-1}$. Figure 3.22 shows the simulation result when $k$ is $+0.1$. Comparing to the ideal case when $k=0$, the harmonic suppression remains unchanged, whereas the noise suppression is a bit less. Overall, the performance impact is minimal. Similarly, when $k$ is $-0.1$ (see Figure 3.23); the harmonic suppression is also not affected. A few odd number of harmonics start to emerge. Overall, the noise floor is still well below the output stage PWM without distortion suppression. It can be concluded that this design is robust against mismatch between resistor $R2$ and $R3$.

\[
\begin{align*}
H(Z) &= (1 + k)Z^{-1} \\
C(Z) &= \frac{1}{1-Z^{-1}}
\end{align*}
\]  

(3.6)

![Figure 3.22 Comparison of the PWM distortion suppression ($k=0$ and $k=0.1$).](image)

Figure 3.22 Comparison of the PWM distortion suppression ($k=0$ and $k=0.1$).
3.7 SYSTEM SIMULATION

The analog feedback block is simulated with digital inputs generated from the digital simulation results. Parasitic extraction is also performed after layout in order to obtain more realistic simulation results (Figure 3.24 and 3.25). When analyzing the simulation results, PWM pulse width may be used instead of the duty ratio because they only differ by a constant. In Figure 3.24, after the integrator reset, the reference PWM (rising edge) has a pulse width of 0.874 and the output stage PWM (rising edge) has a width of 0.849 in cycle 0. There is a difference of 0.025, which is proportional to \(-D_{\text{dist}}[0]\). This difference is stored and added to the system output PWM \(D_{\text{sys}}[1]\) such that it is increased by 0.02 from \(D_{\text{sys}}[0]\). Note that the correction is not exactly 0.025, which is due to parasitic and non-idealities introduced.

A similar simulation is also performed on the falling edge PWMs, and the result
is shown in Figure 3.25. Simulations with process corners (fast, slow and typical) as well as temperature corners (25 °C to 100 °C) are also performed to guarantee the circuit's functionally with process variation and temperature variation.

3.8 **SILICON IMPLEMENTATION**

The class-D modulator and distortion suppression circuit were implemented using a 0.35μm CMOS process. The micrograph of the fabricated chip is shown in Figure 3.26. The total layout area is 1.8 mm x 0.6 mm.

![Post layout simulation result of the analog feedback block (rising edge).](image)
Figure 3.25 Post layout simulation result of the analog feedback block (falling edge).

Figure 3.26 Micrograph of the modulator chip with distortion suppression circuit.
The IC implementation of the distortion suppression circuit has been presented in this chapter. An integrated output stage chip and an output stage built from discrete components are presented in the next chapter.
CHAPTER 4

Output Stage Design

4.1 OVERVIEW

Two class D audio amplifier output stage prototypes are designed. One is implemented using the Power Integrated Circuits (PIC) technology, whereas the other one is realized using discrete components. This chapter presents the details on both output stages.

4.2 LOW-PASS FILTER

As described in Chapter 2, the low pass filter of the output stage has critical impacts on the class-D amplifier performance. Inductors and capacitors should be as linear as possible with respect to voltage and current across the device. The DC resistance of the inductor should be as low as possible, while the saturation current should be higher than the current of normal operating conditions. Panasonic ETQ-A series inductors with ferrite core are good candidates for the low pass filter because of their good linearity and low dc resistance. The capacitor should be of poly film type. Ceramic capacitors are highly non-linear and result in peaking in the frequency response.
4.3 INTEGRATED OUTPUT STAGE DESIGN

The integrated output stage, to be presented in IEEE ISPSD 09 [23], is implemented using a 40V, 0.35µm HV-CMOS technology [24]. This technology was developed based on a 0.35µm CMOS process with only 5 additional masking layers, and provides a simpler platform to implement PICs. The floating source n-channel EDMOS exhibits both low on-resistance and high blocking voltage, while the characteristics of the standard CMOS remain unchanged. There are four layers of metal in this technology.

The output stage employs n-channel floating source EDMOS transistors in an H-Bridge configuration. The high side gate driver is supplied by a bootstrap circuit (see Figure 4.1) [23]. The load is connected in a mono Bridge-Tied Load (BTL) configuration. The external LC filter and bootstrap capacitors are also shown in Figure 4.1.

Figure 4.1 Output stage PIC block diagram and the H-bridge components [23].
The integrated output stage design is based on a previous implementation in our research group [18], with modification in the over current protection circuit.

The power MOSFET is laid out as an array of unit cells (see Figure 4.2) [23]. Each power MOSFET is built from 256 (row) × 31 (column) unit transistors. The columns are grouped into sets of 11, 10, and 10 to make room for two columns of poly gate contacts. The source and drain are each connected by three layers of metal to reduce resistance.

The output stage is also designed to be robust against excess heat built-up or short circuit conditions. The Over Temperature (O.T.) protection circuit compares a bandgap reference voltage with a Proportional To Absolute Temperature (PTAT) voltage to detect high temperature conditions. The Over Current (O.C.) protection circuit uses SenseFET technique [25] on both high-side and low-side gate drivers to detect over current conditions.

![Figure 4.2 MOSFET layout arrangement and isolation structure [23].](image)

Figure 4.2 MOSFET layout arrangement and isolation structure [23].
The micrograph of the output stage is shown in Figure 4.3 [23]. The die area is 2.8mm × 3.4mm. Bonding wires are directly connected to pads embedded in power MOSFETs. The bootstrap diodes are also integrated on chip to reduce external component count. The PIC die is housed in a Power SOP3 package for better heat dissipation.

A prototype PCB layout for the output stage is shown in Figure 4.4, whereas the photo is shown in Figure 4.5 [23]. The LC filter consists of Panasonic ETQ-A15B330 high linearity inductors and poly film capacitors.
Figure 4.4 Integrated output stage PCB layout.

Figure 4.5 Photo of the integrated output stage PCB [23].
4.4 **DISCRETE OUTPUT STAGE DESIGN**

The block diagram of the discrete class D amplifier output stage is as shown in Figure 4.6.

The Zetex ZXM64N035GTA n-channel power MOSFET is selected because of its low on-resistance \((R_{on} = 50 \, \text{mΩ})\) and fast switching speed. The maximum drain to source voltage is 35V, whereas the maximum continuous drain current is 6.7A. Its specification is suitable for implementing a 50W class D amplifier output stage.

The TI gate driver UCC27201D is selected because of its ability to independently drive two n-channel MOSFETs in High-side/Low-side configuration. The delay between high-side and low-side is matched to only 1ns. Without a dead time generator, this gate driver provides more flexibility to the class D modulator in dead time control.

![Figure 4.6 Output stage built from discrete components.](image)

Figure 4.7 shows the PCB layout, and Table 4.1 summarizes all the discrete components used for the output stage design.
The output stage designs have been discussed in this chapter. In Chapter 5, the experimental results are presented.
CHAPTER 5

Experimental Results

5.1 TEST SETUP

In order to accurately test the performance of audio amplifiers, specially designed high-precision equipments must be utilized. The core equipment in the test setup is the Audio Precision SYS-2722 audio analyzer, which is a spectrum analyzer with very low residual noise and THD+N. The audio analyzer is controlled using a PC through an APIB cable (see Figure 5.1). Signal under test is transmitted by the XLR cable for proper noise shielding.

Figure 5.1 Class D audio power amplifier test setup.
Audio analyzers typically have broad bandwidth, broader than the audio band in order to characterize high frequency components. Class D amplifiers or any type of switching amplifiers generate high frequency carrier signals or other forms of intermodulated signals. The high frequency, high energy carrier signals present challenges for audio analyzers to accurately characterize audio signals. Therefore, it is necessary to add a low pass filter to attenuate the carrier signal. Audio Precision AUX-0025 switching amplifier measurement filter is a custom designed low pass filter for switching amplifiers. It has 0dB attenuation for audio signals and 55dB or higher attenuation for 400 kHz signal and beyond. Its frequency response can be found in [26].

The AUX-0025 filter is effective in suppressing the carrier signal, however, it lacks a sharp bandwidth limit characteristic near 20 kHz. It is recommended by the Audio Engineering Society that a very sharp bandwidth-limiting filter to be used when testing switch mode amplifiers [26]. Hence, the AES17 filter option is installed on the audio analyzer, and is turned on for all measurements. Its frequency response can be found in [27].

The audio analyzer generates very low distortion signals, and has three output options — analog, digital (parallel), and optical. The DUT, however, only accepts digital signals in I2S format (serial). An Audio Precision PSIA-2722 programmable serial interface adapter is employed to convert the digital output originated from the audio analyzer to I2S format, and to provide the master clock signal (MCLK).
The DUT consists of a digital class D amplifier modulator with integrated distortion suppression circuit and an integrated output stage or discrete output stage. They are mounted on printed circuit boards, with peripheral components. Table 5.1 summarizes the usage of each board. The layout of the PCBs and their interconnection are shown in Figure 5.2. A photograph of the modulator PCB is as shown in Figure 5.3.

The power supplies used are standard laboratory DC supplies, except for the NF BP4610, which is capable of superimposing a noise voltage on top of a DC voltage. NF BP4610 is used for Power Supply Rejection Ratio (PSRR) measurements.

### Table 5.4 Printed circuit boards for the DUT.

<table>
<thead>
<tr>
<th>PCB</th>
<th>Functions</th>
<th>Components</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Test Board</td>
<td>To provide analog/digital power supply, reference voltages and control signals for the modulator chip</td>
<td>LDOs, potentiometers, low pass filters, switches, pull-up resistors</td>
</tr>
<tr>
<td>2. Modulator Board</td>
<td>To provide I/O connections for the modulator chip</td>
<td>Modulator chip, low pass filters, attenuation resistor network, BNC connectors</td>
</tr>
<tr>
<td>3. Output Stage Board</td>
<td>To provide I/O connections for the output stage chip and flag O.T./O.C. warning signals</td>
<td>Output stage chip, band-gap reference chip, AND gate chip, Schottky diode pair, decoupling capacitors, XLR connector</td>
</tr>
</tbody>
</table>

### 5.2 TEST METHODOLOGY

The performance of the DUT is measured under both 20ns and 0ns dead time conditions. It is expected that the distortion is lower in 0ns dead time condition, while the output stage is more robust under 20ns dead time condition, especially at high
output power levels. The THD+N is plotted against output power and input frequency.

FFT plots are also generated to compare harmonic tones in both open loop and closed loop configuration.

The distortion suppression circuit is compatible with any type of output stages in H-bridge configuration. Therefore, it is also tested with an output stage built from discrete components in both open loop and closed loop configuration. The PCB layout and interconnections are as shown in Figure 5.4.
Figure 5.3 Photo of the modulator PCB.

Figure 5.4 DUT PCB layout and interconnections (discrete output stage).
The distortion suppression circuit relies on external resistors to sense the H-bridge switching waveforms. External resistors have different tolerance levels. It should be determined how much tolerance is allowed before performance starts to degrade. Resistance variation is modeled using potentiometer and sensitivity tests are conducted using the discrete output stage.

Finally, a noise voltage is superimposed on top of the output stage supply voltage to test the PSRR. The FFT of the output signal is plotted for both open and closed loop configurations.

5.3 TEST RESULTS

5.3.1 Power efficiency measurements

The power consumption of the DUT is summarized in Table 5.2. In stand-by mode (RESET is high), all digital circuits are not switching and all analog circuits are idle. In Quiet mode (RESET is low), the modulator input is set to silence, which makes the modulator produce a constant 50% duty cycle PWM waveform.

<table>
<thead>
<tr>
<th>Test Conditions</th>
<th>Class D Modulator</th>
<th>Integrated Output Stage</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Modulator (VDD=5V)</td>
<td>Suppression Circuit (VDD=5V)</td>
</tr>
<tr>
<td>R_{Load}=8 Ω</td>
<td>20mW</td>
<td>18.5mW</td>
</tr>
<tr>
<td>Stand-by mode</td>
<td>285mW</td>
<td>26mW</td>
</tr>
<tr>
<td>Quiet mode</td>
<td>315mW</td>
<td>42.5mW</td>
</tr>
<tr>
<td>1K sine wave</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 5.2 DUT power consumption.
Output stage efficiency is calculated using (5.1). $V_{\text{rms}}$ is obtained from the audio analyzer. The input voltage and current are obtained from the digital multi-meter.

$$\eta = \frac{\text{Output Power}}{\text{Input Power}} = \frac{V_{\text{rms}}^2 / R}{\text{Input Voltage} \times \text{Input Current}}$$  \hspace{1cm} (5.1)

Figure 5.5 shows the output stage power efficiency plots under different load conditions. The maximum power tested is 38.25W. Note that the power consumption of the output stage protection circuit, class-D modulator, and the suppression loop is not included in the efficiency calculations.

![Output stage efficiency vs. output power](image)

Figure 5.5 Output stage power efficiency vs. output power.

5.3.2 Protection circuits

The Over Current (O.C.) protection circuit is tested by generating a short circuit condition at the load. The response time is found to be 50ns (see Figure 5.6) [23]. The IC package is exposed to an external heat source during Over Temperature (O.T.) testing. The O.T. protection circuit is found to be triggered at a case
temperature of 100 °C and deactivated itself at 90 °C due to built-in hysteresis control (also see Figure 5.6) [23]. The O.T. protection circuit still has calibration issues as the reference voltage used is 0.8V instead of 1.23V. Both of the protection circuits only generate warning signals and do not shut down the output stage when active. Other parameters of the integrated output stage are summarized in Table 5.3 [23].

![Figure 5.6](image)

Figure 5.6 Scope capture of over current/over temperature protection signal.

Table 5.3 Integrated output stage performance summary [23].

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Typical Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power switch on-resistance</td>
<td>280 mΩ</td>
</tr>
<tr>
<td>Power stage supply voltage</td>
<td>25 V</td>
</tr>
<tr>
<td>Max power (4Ω load)</td>
<td>38 W</td>
</tr>
<tr>
<td>Over current response time</td>
<td>50 ns</td>
</tr>
<tr>
<td>Over temperature</td>
<td>100 °C</td>
</tr>
<tr>
<td>System efficiency</td>
<td>88 %</td>
</tr>
<tr>
<td>Power stage prop. Delay</td>
<td>28 ns</td>
</tr>
<tr>
<td>Power stage rise/fall time</td>
<td>26 ns</td>
</tr>
<tr>
<td>Quiescent current</td>
<td>29 mA</td>
</tr>
<tr>
<td>Chip size</td>
<td>9.71 mm²</td>
</tr>
<tr>
<td>Package</td>
<td>Power SOP3</td>
</tr>
</tbody>
</table>
5.3.3 Test results with 20ns dead time condition

Under 20ns dead time condition, the closed loop configuration performs better than open loop configuration at all output power levels and frequency range (see Figure 5.7 and 5.8). Distortion suppression is more evident at low frequencies and less evident at higher frequencies. This is expected because the NTF has 20dB/decade slope within audio band. High frequency noise is attenuated less than low frequency noise. Note that, in the frequency response, the THD+N values are valid only until 6.7 kHz. After 6.7 kHz, the third harmonic tone falls out of the audio band, and the THD+N value essentially becomes SNR. FFT result shows that, comparing to open loop, the closed loop side lobe at 2 kHz is reduced by 30dB and the 3rd harmonic tone is reduced by 25dB at 9.3 W output levels (see Figure 5.9).

Figure 5.7 THD+N versus output power for 20ns dead time condition.
5.3.4 Test results with 0 ns dead time condition

Under 0ns dead time condition, the closed loop configuration performs better than open loop configuration at medium to high output power levels (see Figure 5.10).
Theoretically, the closed loop configuration should have better performance for all output levels and frequencies. The degradation in performance is due to input offsets in the analog feedback block. Input offsets, especially if comparator and integrator have different offset values, can cause the PWM duty ratio to fluctuate around optimum values, resulting in THD+N degradation. It is more severe at lower output levels because the PWM duty ratio has less deviation from 50% at low output levels. The $W/L$ ratio of the input pair in this design is small. At the time of design, the fabrication process was still under development and no statistical model for simulating the input offset voltages was available. At 9.3W output level, the closed loop THD+N is better than open loop THD+N by a factor of 2 (see Figure 5.11).

Comparing to open loop, the closed loop side lobe at 2 kHz is reduced by 20dB and the 3rd harmonic tone is reduced by 25dB at 9.3W output levels (see Figure 5.12).

![THD+N vs. output power](image)

Figure 5.10 THD+N versus output power for 0ns dead time condition.
Figure 5.11 THD+N versus frequency for 0ns dead time condition.

Figure 5.12 FFT of the output signal for 1 KHz sine input and 9.3W output.
5.3.5 Test results with discrete output stage and 0 ns dead time

With discrete output stage and 0ns dead time, the closed loop configuration performs better than open loop configuration at a wide range of output power levels and frequency range (see Figure 5.13 and 5.14). Distortion suppression is more evident at low frequencies and less evident at higher frequencies. Degradation at low output levels is also due to input offsets in the analog feedback block. The suppression in side lobe and harmonic tones is very evident (see Figure 5.15).

![THD+N vs. output power graph](image)

Figure 5.13 THD+N versus output power for discrete power stage.

5.3.6 Sensitivity tests (with discrete output stage)

Sensitivity tests are conducted by varying the resistance values of the attenuation resistors. The nominal values are 1K and 9K for a 25V H-bridge supply voltage. System performance is tested with ±5% deviation from nominal values, and the performance impacts are minimum (see Figure 5.16 and 5.17). It can be
concluded that 5% variation of the resistance value can be tolerated. Further variation, such as ±10%, will result in severe degradation in performance and should be avoided.

Figure 5.14 THD+N versus frequency for discrete power stage.

Figure 5.15 FFT of the output signal for 1 KHz sine input and 18 W output.
Figure 5.16 THD+N versus output power for different R values.

Figure 5.17 THD+N versus frequency for different R values.
5.3.7 PSRR measurements

The previous tests are conducted using well regulated power supply for the output stage. In practice, however, class-D amplifiers do not have a clean laboratory power supply due to cost and space limitations. The power supply used is simple unregulated rectifying circuits that can be very noisy in the audio band. Hence, it is crucial for the system to have high PSRR.

The input to the DUT is set to be 1 kHz sine wave, while a 50Hz 1Vp-p sine wave is superimposed on top of the DC supply voltage for the output stage. FFT is generated from the DUT output, as shown in Figure 5.18. In closed loop configuration, the side lobes are reduced by 40dB, and the PSRR is 15dB better than open loop (see Figure 5.19), making the supply noise almost invisible to the system. It can be concluded that the closed loop configuration is very effective in suppressing power supply noise, and it will outperform open loop configuration for all test conditions if supply noise is present.

5.4 PERFORMANCE COMPARISON

With the help of distortion suppression circuit, the minimum THD+N of the digital class D audio amplifier is reduced to 0.03% with the discrete output stage. Figure 5.20 compares this work with the discrete implementation of the distortion suppression circuit by G. Wei [18]. In the previous implementation, low offset instrumentation op-amps and comparators were used. In addition, trimming resistors were used to fine tune the distortion suppression circuit. As a result, better
performance at low output power was observed. Figure 5.21 compares the performance with other published class-D amplifiers, both analog and digital. It can be concluded that the performance of this work is among the state of the art class D audio amplifiers.

Figure 5.18 PSRR measurements for both open loop and closed loop.

Figure 5.19 Zoomed in plot of Figure 5.18.
Figure 5.20 Performance comparison with the discrete implementation.

Figure 5.21 Performance comparison with other class D amplifiers.
CHAPTER 6

Conclusion

An IC implementation of a distortion suppression circuit for digital class D audio amplifiers has been presented. Using the concept of equalizing the effective duty ratio of the modulator PWM and the output stage PWM, the output stage noise is essentially shaped by a first order noise transfer function with 20dB per decade frequency response.

This design gives a lot of flexibility to the output stage design. The modulator is able to drive any output stage in H-bridge configuration. Depending on the application, it is expected to work with output stages of both low power levels and high power levels. This design is also proven to be robust with typical resistor mismatches.

The output stage design is critical to the system performance. In particular, the selection of dead time and LC filter components are crucial considerations.

Based on experimental results, the output stage signal distortion is greatly suppressed. The closed loop PSRR is also improved by 15dB. The THD+N value is reduced by a factor of 2 to 30, depending on the output power level and dead time condition. The minimum THD+N is 0.03%, which is among the state-of-art class D amplifiers.

The low power performance of this design can be improved by using larger
input transistors for the op-amps and comparators in order to minimize offset. Higher order distortion suppression circuit can be also explored. In addition, pop noise suppression is another beneficial feature to have.
REFERENCES


