W-BAND PASSIVE AND ACTIVE CIRCUITS IN 65-NM BULK CMOS FOR PASSIVE IMAGING APPLICATIONS

by

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A thesis submitted in conformity with the requirements for the degree of Master of Applied Science
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Abstract

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The design and implementation of mm-wave switches, variable attenuators, and a passive imaging system in 65-nm CMOS are presented. The design and analysis of shunt switches is presented with a demonstration circuit showing record performance for a single-pole single-throw switch with 1.6dB loss and 30dB isolation at 94GHz. Single-pole double-throw (SPDT) switches are shown, with 4dB insertion loss in the W-band (75-110GHz), and the only reported SPDT switch operating in the D-band (110-170GHz). A novel technique for implementing digitally controlled variable attenuation is presented, resulting in variable attenuation between 4 and 30dB in the W-band. Finally, a W-band radiometer is described integrating a record-high gain CMOS LNA, SPDT switch, and peak detector. This is the highest-frequency imaging system in CMOS with this level of integration, offering a responsivity over 90kV/W, and a noise-equivalent power less than 0.2pW/√Hz.
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1.1. Motivation

While the first applications of radio-frequency technology were dominated by the demand for wireless communication, higher and higher frequencies were soon being explored, driven mainly by alternative applications like radar systems and imaging. For these applications, higher frequency signals offer the benefit of improved angular and spatial resolution, as well as improved transmission or reflection profiles for object detection and imaging.

The range of the electromagnetic spectrum between 30 and 300 GHz is known as the millimeter-wave band due to the free-space wavelength of these signals being millimeters in length. Imaging systems that operate in the millimeter-wave band of the electromagnetic spectrum are particularly attractive because they offer a good balance between the high-spatial and temperature resolution provided by very short wavelength carrier frequencies, as well as good penetrative capabilities for various materials. There is fairly significant atmospheric absorption in the mm-wave band, as shown in Fig. 1.1 [1], especially when compared with the relative transparency of the atmosphere to RF signals occupying the typical range of frequencies used for wireless communication applications below a few GHz.

Integrated imaging systems operating in the mm-wave band [4,5] have typically been implemented using III/V technologies, such as indium phosphide (InP) and indium gallium arsenide (InGaAs). In such systems, multiple dies are typically required, with each die implemented in a different technology as appropriate for the specific circuit. Large system implementations often integrate a large number of parallel imaging channels to improve spacial and temperature resolution, and the complexity of each individual channels becomes a dominant factor.
1.2 Objectives

The objective of this thesis is to explore the application of CMOS technologies to mm-wave imaging applications typically reserved for III/V or SiGe technologies. Mm-wave passive switches and attenuators, key components of imaging systems, will be realized to compete with III/V technologies based solutions. Finally, the feasibility and in system cost and performance. With each channel requiring numerous individual components, complex and expensive modules become required in order to assemble the system. Integrating as many parts of the system as possible onto a single chip would solve many of these issues, driving down costs and complexity.

CMOS adoption has largely been driven by its ability to continually integrate larger parts of systems onto a single-die, thus by applying these same principles to mm-wave imaging systems we could potentially realize similar cost and performance benefits. CMOS performance and high frequencies has traditionally lagged behind III/V based solutions to a degree that made integrating CMOS systems at these frequencies unrealistic. In the past decade, the continued scaling of CMOS technologies has pushed the range of frequencies attainable using standard CMOS processes into the millimeter [6–8] and even sub-millimeter [9] wave frequency bands. Realizing the major components of an imaging system in a CMOS process with competitive performance could lead to higher levels of integration and lower cost than those possible with III/V materials.

**Fig. 1.1:** Electromagnetic absorption of Earth’s atmosphere [1].
performance of a CMOS based W-band (75-110 GHz) imager will be examined through the realization of a fully integrated passive imaging system implemented in a bulk version of a standard 65-nm CMOS process.

1.3. Outline

This thesis will be organized as follows. First, the background and theory will be presented for mm-wave passive imaging systems in Chapter 2. Key formulas and system considerations will be presented, and the fundamentals of passive switch technologies will be described. Chapter 3 will present the design and implementation of both single-pole, single-throw (SPST) and single-pole, double-throw (SPDT) switches, as well as digitally controlled variable attenuators. Emphasis is placed on designing these circuits for operation within the W-band and beyond. Finally, Chapter 4 will present the full implementation and characterization of a W-band passive imaging system realized in a 65-nm bulk CMOS process.
2.1. Passive Imaging Systems

Passive imaging or radiometer systems are remote sensing systems specifically designed to measure the radiation intensity, in the form of random noise, emitted by black body radiation sources in the micro- or millimeter-wave spectrum [10]. All objects emit thermal noise either as the result of their own internal temperature, via Planck’s law of black-body radiation, or from reflections of surrounding objects [2]. Planck’s law describes the spectral radiance of electromagnetic radiation, over all wavelengths, emitted from a black-body at a specific temperature. A plot of the theoretically predicted radiation intensity is shown in Fig. 2.1 indicating that there is a specific spectral intensity of noise radiation expected based on the wavelength (or frequency) of observation and the temperature of the black body emitting the signal. A sensitive receiver designed to measure noise power can thus determine the temperature of an observed object and then infer information regarding the object or scene.

Active imaging systems also exist that differ from passive systems by the use of a signal source that illuminates a target and then measures either a reflected or transmitted signal. By using an active source for radiation, the detected radiation levels by the receiver can be orders of magnitude higher than those produced passively by normal thermal generation. The use of these systems is limited to situations in which the illumination signal can be produced and transmitted with sufficient power and directionality to have the signal reflected or transmitted to the receiver. Often these conditions can only be met with the implementation of circuits that result in significant or even excessive power consumption beyond those consumed with passive imaging systems. Specifically the realization of mm-wave voltage-controlled oscillators and power amplifiers require particularly high amounts of
2.1 Passive Imaging Systems

Fig. 2.1: Black body radiation produced as a function of wavelength and temperature according to Planck's law of black body radiation [2].

power. The circuits described in this work, while focused on passive imaging techniques, are not necessarily precluded from being used in active imaging systems.

Imaging systems have seen extensive investments in recent years due to the recent interest in security and safety related research. Security screening, hidden-weapon detection, and video enhancement of low-visibility scenes are all examples of where imaging research, and specifically mm-wave imagers, show compelling potential for the future. Security check-point screening is a particularly significant market for mm-wave imaging systems, as systems operating at these frequency are already being installed in airports within the United States and other countries in order to screen passengers for restricted objects hidden on their person without resorting to invasive manual searching techniques. Imaging systems are also being pursued for use in aviation applications, where mm-wave systems have the ability to penetrate most fog and weather-based visual obscurants that contribute to delays and dangerous flying conditions.

The frequencies at which imaging systems can be realized is limited by the capabilities of solid-state electronics. As frequencies are increased, the gain available from transistors decreases, and the noise-figure increases,
limiting the overall performance of an imaging system. Technology scaling has permitted higher frequencies to be pursued as new generations of process technologies have been introduced. The current state of the art solid-state technology has led to the targeting of the W-band (75-110 GHz) as a compromise between the technology limitations of current transistors, and the attractive features of mm-waves in this frequency range, particularly spatial resolution, material penetration, and atmospheric absorption for these applications [11].

Commercial imaging systems operating in the W-band typically employ zero-bias Schottky diodes [12, 13] or planar doped barrier diodes as detectors [14]. Pre-amplification is often provided by one or several high-gain, low-noise InP HEMT amplifiers [15]. These systems offer excellent performance but require complex modules that integrate 2-4 separate chips. Each component is realized in a different technology, often incompatible with each other. For instance, zero-bias Schottky diodes and LNAs require two different incompatible technologies, and thus must be implemented on separate dies. Achieving competitive performance with these systems using CMOS may not be immediately possible, but being able to integrated most or all of the components on a single die may provide sufficient benefits to overcome some performance deficit.

More recently, a SiGe HBT LNA and detector, and silicon MOSFET switches, have been used in a 130-nm SiGe BiCMOS process to integrate a W-band imaging receiver on a single chip [16]. This type of work is the most directly competitive with realizing an entire system in CMOS technology. SiGe BiCMOS offers the benefits of CMOS technology for the implementation low-loss RF switches and any base-band digital electronics, while also offering high-performance low-noise SiGe HBT transistors for use in the LNA and detector. The cost of a SiGe BiCMOS technology along with its limited availability and use of 8-inch wafers for manufacturing may leave a role for nanoscale CMOS to further leverage the economies of scale and the potential for large-scale wafer-level integration. A modern CMOS process utilizes 300-mm wafers, benefits from lower switch loss, and can potentially permit the integration of thousands of imaging elements on a single wafer.

2.1.1. Total Power Radiometers

Direct-detection passive imagers are typically implemented as total power radiometers, with or without RF-path pre-amplification, as shown in Fig. 2.2 (a) and (b) respectively. The systems consist of a square-law detector, optionally preceded by a low-noise amplifier, and followed by a post-detector, low-frequency amplifier and integrator. This unit detector represents a single "pixel” element, in the form of an output voltage level that is
2.1 Passive Imaging Systems

Fig. 2.2: Passive imager based on total power radiometer architectures without, (a), and with (b) RF-path pre-amplification.

proportional to the incident noise-power. Full 2-dimensional images can be formed either by mechanically scanning an antenna in the X- and Y-directions, by implementing a 2-D imager array, or by some combination of these two solutions.

For thermal imaging systems, the sensitivity is established by the minimum input noise signal power that results in a post-detector SNR of unity [17]. A standard detector figure-of-merit, called the Noise-Equivalent Power (NEP), is defined as:

$$NEP = \frac{v_n}{\mathcal{R}} = \frac{v_n}{V_{outDC}/P_{inRF}}$$  (2.1)

Where $v_n$ is the detector output noise voltage, and $\mathcal{R}$ is the system responsivity. The latter is a constant of proportionality between the average absorbed input signal power and the resultant output voltage. The responsivity is dependent on the input signal frequency, but should be independent of the input power level, up to some saturated level.

It is often more convenient to express the sensitivity of a system with respect to the minimum detectable temperature change. The noise equivalent temperature difference (NETD) describes the change in temperature required to produce a given noise equivalent power:

$$NETD = \frac{NEP}{dP_{IN}/dT}$$  (2.2)

And can also be described as [18]:

$$NETD = T_S \sqrt{\frac{1}{B \tau} + \left(\frac{\Delta G}{G}\right)^2}$$  (2.3)

where $T_S$ is the system noise temperature equal to $T_A + T_R$, i.e. the antenna plus receiver noise temperature, $B$ is the RF front-end bandwidth, $\tau$, is the integration time of the integrator, and $\Delta G$ is the fluctuation of the
overall gain, \( G \), of the RF path of the radiometer. This equation indicates that, in order to improve the temperature resolution, the system noise temperature must be reduced and the integration time and bandwidth must be increased.

In order to achieve an NETD of less than 1 K, the temperature resolution typically required for most imaging applications [15], the system noise temperature must be sufficiently small and, to accomplish this, it is often necessary to include additional RF-path gain in order to overcome the noise contribution of the detector. A low-noise amplifier ensures that sufficient gain is provided while contributing minimal noise to the system. In the presence of such a low-noise pre-amplifier, the NETD of the radiometer can now be expressed by [15]:

\[
\text{NETD} = \frac{1}{\alpha} \sqrt{\left[ 2(\alpha T_A + (F_{LNA} - \alpha) T_o) \right]^2 + \left( \frac{v_n}{k_B R G_{LNA}} \right)^2 \frac{1}{B} B_{IF} \frac{B}{B}}
\]

Where \( \alpha \) is a pre-LNA attenuation factor, \( T_A \) is the equivalent noise temperature collected by the antenna, \( F_{LNA} \) is the LNA noise factor, \( T_o \) is the reference noise temperature of 290 K, \( B_{IF} \) is the IF bandwidth, and \( G_{LNA} \) is the power gain of the LNA. The benefit of a high-gain, low-noise LNA is immediately obvious, but a wide RF bandwidth, \( B \), is still important.

Finally, the NETD can be related to the NEP using [16]:

\[
\text{NETD} = \frac{\text{NEP}}{k B \sqrt{2T}}
\]

Where \( k \) is the Boltzman constant.
2.1.2. Dicke-Type Radiometers

The final term in Equation 2.3 describes the contribution of the low-frequency variation in the radiometer system gain to NETD. It lumps together a number of noise sources responsible for degrading receiver sensitivity and limiting the minimum temperature step that can be resolved. These noise sources principally consist of the 1/f noise of the detector and low-frequency fluctuations of the LNA gain.

The impact of LNA gain variation becomes apparent if we use the example [19] of a W-band radiometer with 10-GHz RF bandwidth, an LNA gain of 30 dB, a system temperature of 400 K, and an integration time of 20 mS. Using Equation 2.3, but excluding gain variation, an NETD of 0.028 K can be achieved. However, if an LNA gain variation of only 0.05 dB is assumed, the NETD increases dramatically to 4.62 K, corresponding to a sensitivity degradation of over 20 dB, far beyond the 1 K necessary for most imaging applications [15].

The impact of the 1/f noise and low-frequency gain variations can be eliminated, or at least greatly reduced, by periodically calibrating the radiometer using a Dicke-type radiometer architecture [20], which is shown in Fig. 2.3. The input of the receiver is switched between the antenna and a reference load with a repetition frequency $f_m$, typically much higher than the 1/f corner frequency of the radiometer [18]. A multiplier switch placed after the detector switches the detector output in synchronism with the antenna switch in opposite phase to the integrator, such that the detector output voltage corresponding to the reference temperature is subtracted [19]. Thus, the noise-power corresponding to the actual signal received at the antenna is modulated at frequency $f_m$ and enters the detector only during the switching half-period. This results in a reduction by a factor of 2 of the apparent incident power on the radiometer, corresponding to a doubling of the NETD:

$$\text{NETD} = (2)T_S \sqrt{\frac{1}{B \tau} + \left(\frac{\Delta G}{G}\right)^2}$$

(2.6)

This 3-dB degradation in sensitivity is more than compensated for by the elimination of the gain variation term (whose impact is larger than 20 dB) if $f_m$ is chosen to be significantly higher than the cut-off frequency of the low-frequency gain fluctuations.
2.2. RF Switches

The realization of an integrated Dicke-switching radiometer [20] requires the implementation of low-loss passive RF switches. RF switches are important elsewhere in many wireless applications, being used throughout the system to provide access to shared resources, such as antenna ports, and may be used for routing signals selectively within a system for the purpose of calibration or self-testing.

The main requirement for switches are that they provide two states: a low insertion-loss in the ON-state, and high isolation in the OFF-state, ideally approaching perfect shorts and opens respectively. These requirements typically translate into two distinct operating conditions at the device level: a very low ON-resistance, $R_{ON}$ when in a conducting mode, and a very low capacitance, $C_{OFF}$, when in an off state. This has led to an accepted figure of merit for the cut-off frequency of a switch given by:

$$f_c = \frac{1}{2\pi \cdot R_{ON} C_{OFF}}$$

(2.7)

Where $C_{OFF}$ and $R_{ON}$ scale proportionally and inversely respectively with regards to device width, making the RC product a constant for a given technology or configuration. This cut-off frequency is said to be roughly 10 times the useable frequency range of a given switch [21].

Switches can be implemented either as discrete board-level components or integrated on-chip, with initial or early implementations favouring discrete components and then transitioning towards integration as the system matures. PIN diodes, GaAs MESFETs, and MEMS devices are all potential options for board-level solutions, but they are also limited in their possibility for system integration. Specifically, MEMS devices face serious reliability and integration challenges that hamper efforts to further integrate these devices [22].

MESFETs can be realized in a variety of materials, including GaAs and InP, and provide excellent performance for moderate to high power levels. Specifically when implemented using GaAs, these switches can provide very low insertion loss at high frequencies [23], while also handling quite high powers due to their large band gaps and corresponding high break down voltages. Additionally, realizing low-loss passives with these materials, which is very important for mm-wave switch design, is helped by the semi-insulating nature of the substrate. The power-
consumption of MESFET switches is also essentially zero as they contain insulating gates that do not consume any DC power.

PIN diodes can similarly be realized in numerous materials, just as MESFETs, in addition to silicon, and they are particularly apt for high power applications. The ON-state for the diode can provide a very low on-resistance, but this comes with the cost of a non-negligible DC current consumption on the order of several milliamps. The OFF-state can have low capacitance making them appropriate for high-frequency applications [24]. While low-or zero-bias PIN diodes have been realized [25], the prospect for integrating these structures are slim.

Generally, due to their non-zero DC power consumption and their minimal performance advantage, GaAs MESFETs are typically preferred over PIN diodes for most MMIC implementations, but neither of these solutions are compatible with silicon technologies.

The silicon MOSFET is the cheapest and most widely available switch structures, and traditionally has been decidedly inferior to either MESFET or PIN diode solutions. Besides the very modest band-gap and consequently low break-down voltage of silicon technologies, the main weakness of the silicon MOSFET has always been the relatively high on-resistance of the silicon channel due to the poor electron-mobilities of n-type silicon semiconductors (or hole-mobilities of p-type silicon). However, one of the strengths of CMOS scaling has been the aggressive reduction of the gate length, leading to ever improving on-resistance values for CMOS technologies. As well, significant efforts have been expended improving carrier mobilities in silicon technologies using a variety of materials engineering approaches uniformly described as strain-enhancement engineering [26]. This has led to additional improvements for the silicon MOSFET technology on-resistance for a given $C_{OFF}$. This makes deeply scaled nanometer CMOS technology an interesting prospect for switch applications.
3.1. Introduction

Numerous publications have explored switch topologies for both single-pole, single-throw (SPST) [23,27–30] and single-pole, double-throw (SPDT) [30–33] FET switches, and have shown that they can be readily extended into the mm-wave frequency range and even as far as the W-band (75-110GHz). These works have converged on to a switch design that implements multiple shunt-transistor switches called a traveling-wave switch. Switches generally utilize the high ON-state conductance and low OFF-state capacitance of what are typically III/V, but more recently CMOS, transistors to produce two distinct operating states with low insertion loss and high isolation, respectively. This chapter describes the design, fabrication, and testing of a range of SPST and SPDT switches as well as digitally-controlled variable attenuators realized in a 65-nm bulk CMOS process.

3.2. Traveling-Wave SPST Switch Design

3.2.1. Simplified Switch Model

The building block of the traveling-wave switch is shown in Fig. 3.1 (a), consisting of two shunt transistor switch devices separated by a complex impedance. The conventional approach for the design and simulation of traveling-wave shunt switches was first shown for III/V switches in [30], and models the OFF-state transistors as capacitors and ON-state transistors as conductances. Each of these shunt elements then form π-networks with transmission lines or lumped inductors, as seen in Fig 3.1 (b), and (c). These unit segments can then be potentially cascaded depending on the design requirements.
3.2 Traveling-Wave SPST Switch Design

![Traveling-wave SPST Switch Design Diagram](image)

Fig. 3.1: a) Traveling-wave circuit block, and the simplified b) on-state and c) off-state equivalent circuits.

![Classical Definition of L and C Components](image)

Fig. 3.2: Classical definition of the L and C components for a $\pi$-section

With all transistors off, and the shunt transistors modeled as capacitors, the structures resemble an LC low-pass $\pi$-section filter, providing a broadband frequency response up to a cut-off frequency. Using the component definitions [10] shown in Fig. 3.2, the $\pi$-segments cutoff frequency, $\omega_c$, is defined by:

$$\omega_c = \frac{2}{\sqrt{LC}} \quad (3.1)$$

and the nominal characteristic impedance, $R_o$, by:

$$R_o = \sqrt{\frac{L}{C}} \quad (3.2)$$

The major parasitic elements of the transistor are shown in Fig. 3.3a, where the transistor itself acts as a
Fig. 3.3: (a) Important parasitic capacitance elements for switch modeling (b) 'ON' and 'OFF' equivalent models for shunt transistors.
variable channel resistance controlled by the gate voltage. For switch applications, the gate is typically biased through a high-value resistor (on the order of several kΩ), and the intrinsic gate resistance, denoted as $R_G$, is negligible compared to this added resistance. This large discrete resistance helps ensure that the gate acts as an AC-floating node, thus minimizing signal loss through parasitic gate coupling. A similar technique can be applied to the substrate/body node of the transistor, but requires the additional use of a triple-well process so that the p-type body of the transistor can be isolated from the p-type substrate by the reverse biased junctions of an isolation n-well.

Biasing the gate through a large resistor can also help improve the linearity of the switch. For large input powers, the corresponding large voltage swings result in channel conductivity modulation due to fluctuating gate-source ($V_{GS}$) and drain-source ($V_{DS}$) voltages. Biasing the gate through a large resistor ensures that the gate node remains floating at RF, thus bootstrapping the gate voltage to the source/drain voltages and keeping the $V_{GS}$ approximately constant. Linearity is also impacted by the parasitic drain and source junction diodes. These diodes can become forward biased under large negative voltage swings (for NFET transistors), clipping the signal to approximately 0.7V below ground. This source of non-linearity can be improved, just as with the gate node, using the floating-body technique previously described.

In the ON-state (with $V_G$=1.2 V applied to the gate), the channel resistance is (ideally) very small and this impedance will dominate over the parallel parasitic capacitances. The channel conductance per unit gate width (including the impact of source and drain resistance) for a transistor in a given technology can be determined from simulation or measurement of device S-parameters and extracting the $\Re(Y_{22})$ for low $V_{DS}$ ($\approx$0.1 V) and large $V_{GS}$ (1.2 V) at low frequency. An example for this is shown in Fig. 3.4 for an NFET SVT (standard threshold voltage) 80x1µmx60nm transistor in a 65-nm GP (general purpose) CMOS technology from STMicro. These measurement were performed on a high-frequency test-structure with the input and output parasitics (pad and interconnect) de-embedded using the T-line procedure described in [34]. These measurements show an ON-state conductance, $g_{DS}$, of approximately 2.5-2.7 mS/µm or equivalently $(370\Omega \cdot \mu m)^{-1}$. The net effective conductance for the device will scale with the total gate width.

In the OFF-state (with 0V applied to the gate), the channel resistance is high and can be considered an open-circuit. In this state, the gate capacitances ($C_{GD}$ and $C_{GS}$) appear in series due to the high impedance of the
Fig. 3.4: Experimental measurement results of the channel conductance per unit gate width, $g'_{DS}$, including the impact of source and drain resistance, for an NMOS transistor test structure (NFET SVT 80x1$\mu$mx60nm).

gate resistor. A similar statement can be made regarding the bulk capacitances only if a large impedance has been placed between the bulk node of the transistor and the substrate node. This can only be accomplished if an isolation n-well has been implemented, thus creating a very large effective $R_{SUB}$, essentially placing the two bulk capacitances in series with each other.

For the case in which the n-well has not been implemented, the $R_{SUB}$ will have typically been minimized through the careful placement of multiple P-TAP substrate contacts in close proximity to the source and drain regions. In the case of a shunted transistor with the source node grounded, $C_{SB}$ can be ignored and only $C_{DB}$ included. The total OFF-state capacitance, $C_{OFF}$, is given by:

$$C_{OFF} = \frac{C_{GS} \cdot C_{GD}}{C_{GS} + C_{GD}} + C_{DS} + C_{DB} \quad (3.3)$$

The unit values for the various parasitics elements can be determined, as with the channel conductance, from either simulations or measurements of a device test structure. An example of this is shown for $C_{GD}$ in Fig. 3.5 for
3.2 Traveling-Wave SPST Switch Design

Fig. 3.5: Experimental measurement results of the MOSFET gate-drain capacitance ($C_{GD}$) for an NMOS transistor test structure (NFET SVT 80x1µm x 60nm).

an NFET SVT 80x1µm x 60nm in the same technology as previously described. $C_{GD}$ is extracted using:

$$C_{GD} = \frac{\Im(-Y_{12})}{\omega}$$  \hspace{1cm} (3.4)

From Fig. 3.5, the OFF-state $C_{GD}$ can be seen to be approximately 0.4 fF/µm. The rest of the extracted values for an NFET SVT 80x1µm x 60nm device manufactured in the STMicro 65-nm technology is shown in Table 3.1. The total off-state capacitance is approximately 1.05 fF/µm.

These model parameters can now be used to assemble single-$\pi$ equivalent circuits for the ON- and OFF-state switch transistors. The classical form for a single-$\pi$ circuit is shown in Fig. 3.6, where $Y_1$ and $Y_2$ are equal to

Table 3.1: Transistor parasitic capacitance values from an NFET SVT 80x1µm x 60nm device.

<table>
<thead>
<tr>
<th>Param</th>
<th>Value (fF/µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{GD}$</td>
<td>0.40</td>
</tr>
<tr>
<td>$C_{GS}$</td>
<td>0.55</td>
</tr>
<tr>
<td>$C_{DS}$</td>
<td>0.38</td>
</tr>
<tr>
<td>$C_{DB}$</td>
<td>0.44</td>
</tr>
<tr>
<td>$C_{OFF}$</td>
<td>1.05</td>
</tr>
</tbody>
</table>
either the ON-state channel conductance or the OFF-state capacitance, and $Y_3$ is equal to the impedance of the transmission line or lumped inductor. ABCD-matrix parameters can be determined from the $\pi$ circuit using the standard relationships [10]:

\[
\begin{align*}
A &= 1 + \frac{Y_2}{Y_3} \\
B &= \frac{1}{Y_3} \\
C &= Y_1 + Y_2 + \frac{Y_1 Y_2}{Y_3} \\
D &= 1 + \frac{Y_1}{Y_3}
\end{align*}
\]

This ABCD matrix can now be used on its own or as a cascade of stages as appropriate. One of the conveniences of ABCD parameters is that multiple matrices can be cascaded simply by using straight-forward matrix multiplication. With the desired final ABCD matrix (after cascading stages as desired), the S-parameters for the system can then be determined from standard network parameter relationships [10].

The various extracted model parameters can be used to perform simulations using the shunt capacitances or conductances along with a series inductance to assess switch performance and to gauge the impact of various design parameters. The value of these custom models extend beyond just an initial assessment, as foundry-provided MOSFET models lack accuracy in the mm-wave regime due to the limited frequency range over which model extraction is performed. Model extraction is not performed at these high frequencies being considered and the behaviour of such models under these conditions is thus dependent on the methodologies employed by the foundry MOSFET model development team to fit or approximate the various model parameters.
An additional problem with foundry models exists because the majority of foundry-provided MOSFET models, including BSIM3 and BSIM4, utilize a forced source/drain symmetry that results in discontinuities or singularities in the charge and current expressions when transitioning from the forward \( V_{DS} \geq 0 \) to reverse \( V_{DS} \leq 0 \) operating regions [35]. Transistors operating within this region, such as switches, experience issues in the simulation of the higher-order non-linearities, preventing the modeling of terms such as the third-order intermodulation [36].

### 3.2.2. Design Parameter Optimization and Example

In evaluating the switch performance, several metrics must be examined, particularly at the frequency points of interest, including:

1. **Insertion loss** - From the magnitude response of \( S_{21} \) in the OFF-state for the transistor.

2. **Isolation** - From the magnitude response of \( S_{21} \) in the ON-state for the transistor.

3. **\( S_{11} \) and \( S_{22} \)** - The return loss in both the ON- and OFF-states.

Generally speaking, there is a trade-off between the two primary system metrics: insertion loss and isolation. In dealing specifically with shunt switches, increasing the switch transistor width, \( W \), will allow a higher achievable isolation through higher shunt conductances. However, a larger \( W \) will also increase the OFF-state parasitic capacitance, \( C_{OFF} \), negatively impacting the insertion loss, particularly at high frequencies. Series switches will have different design considerations.

A starting point for device sizing can be found by using some given performance requirement for switch isolation. Regardless of the frequency for which this particular switch isolation is required, initial device sizes can be found through a calculation of the DC or low-frequency isolation. This value is determined by the shunt conductance of the devices, and consequently, because the unit conductance is determined by the technology and device characteristics, the device width. At low-frequency, the two shunt MOSFETs of a \( \pi \)-section can be considered one device of width \( 2 \cdot W \), and the combined effective ON-resistance of the two shunt MOSFETs, \( R_{SHUNT} \), can be described as:

\[
R_{SHUNT} = \frac{1}{2 \cdot g'_{DS} \cdot W} \quad (3.5)
\]
3.2 Traveling-Wave SPST Switch Design

Fig. 3.7: The total device width ($2 \cdot W$) required to produce a given DC isolation

where $g_{DS}',$ as before, is the transistor conductance per unit gate width.

Fig. 3.8: Parameters for a shunt two-port circuit.

The isolation (in dB) at DC or low-frequency can be calculated for a given system characteristic impedance, $Z_o,$ from the basic two port circuit shown in Fig. 3.8, where the ABCD matrix is given by [10]:

\[
A = 1
\]
\[
B = 0
\]
\[
C = Y = \frac{1}{R_{SHUNT}}
\]
\[
D = 1.
\]
From this matrix, the isolation can be calculated as the power transfer or $S_{21}$ giving:

$$S_{21} = \frac{2}{A + B/Z_0 + C/Z_0 + D} = \frac{2R_{SHUNT}}{2R_{SHUNT} + Z_0} \quad (3.6)$$

And the isolation is then given by [37]:

$$ISO = -20\log\left(\frac{2R_{SHUNT}}{2R_{SHUNT} + Z_0}\right) \quad (3.7)$$

By substituting in the equation for $R_{SHUNT}$, the combined transistor width required (for two shunt transistors) in order to achieve a given DC isolation becomes:

$$W = \frac{2 - 2 \cdot 10^{-\frac{ISO}{20}}}{2 \cdot g'_{DS} \cdot R_o \cdot 10^{-\frac{ISO}{20}}} \quad (3.8)$$

This result is plotted in Fig. 3.7, with the the total device width ($2 \cdot W$) plotted as a function of the required DC isolation. This result is produced using a transistor conductance per unit width of 2.7 mS/µm. To achieve an isolation of 20 dB, it can be seen that a total device width of 128 µm is required, or 64 µm per device. It can be seen that achieving higher DC isolation requires a significant increase in total device width, with a 6-dB improvement in isolation imposing a doubling of the devices widths. Increasing from 20 dB to 30 dB isolation leads to an almost 4-fold increase in device size, which may negatively impact the high-frequency performance of the switch, as will be later demonstrated. Applications requiring these types of isolation are likely better served with a different switch configuration that implement series transistors.

Additionally, the isolation at higher frequencies will increase compared to at DC due to the low-pass response of the R-L-R $\pi$-network formed by the ON-state shunt transistors and the series inductor. Later examples will show that this low-pass response can provide an additional 10+ dB of attenuation at mm-wave frequencies. For this example, a DC isolation of 16 dB is used, and a device size of 42 µm is selected and operation into the W-band (75-110 GHz) will be expected.

With an initial width of 42 µm per device selected, providing 44 fF of parasitic capacitance, the frequency response of the switch is now determined by the inductor design. Determining the inductor value directly from
the classical expressions for the $\omega_c$ or $R_o$ of a $\pi$-segment can lead to divergent results that do not give clear design guidance. Using equation 3.1 for the cutoff frequency, $f_c$, and substituting $C = 2 \cdot 44 \text{ fF} = 88 \text{ fF}$ and $f_c = 100 \text{ GHz}$, we get an inductance value of:

$$\omega_c = \frac{2}{\sqrt{LC}} \Rightarrow L = \frac{1}{(\pi f_c)^2 C} = 27.4 \text{ pH}$$  \hspace{0.5cm} (3.9)$$

Which results in a nominal characteristic impedance, from equation 3.2, of $R_o = 17.2 \Omega$. This impedance mismatch, assuming a system impedance of 50-\Omega will result in additional signal loss. Alternatively, using equation 3.2 for the characteristic impedance and the same values as above, we get an inductance value of:

$$R_o = \sqrt{\frac{L}{C}} \Rightarrow L = R_o^2 C = 231 \text{ pH}$$  \hspace{0.5cm} (3.10)$$

Which results in a cutoff frequency, from equation 3.1, of $f_c = 69 \text{ GHz}$, which is lower than the required operating frequency range of the W-band. The ideal value for the inductor therefore lies somewhere between these two inductor values.

Using the $\pi$-model and S-parameters for the circuit, it is possible to sweep the inductor value, and look at the high-frequency performance as a function of the inductance. Consistent with applications in the W-band, results are extracted at 100 GHz, and an inductor quality factor of 10 (@ 100 GHz) is assumed, neglecting other high-frequency effects such as the skin-effect [38]. Shown in Fig. 3.9, it can be seen that optimal insertion loss occurs simultaneously with good return loss matching. In this case, the optimal inductor sizing is around 70-80 pH. With this configuration, the OFF-state switch return loss is better than 15 dB, the insertion loss is around -1 dB, and the isolation is 28-30 dB. The ON-state return loss, an important parameter when the SPST switch is being used in a larger switch configuration, such as in a SPDT switch, is slightly less than 3 dB.

Fixing the inductor value at 75 pH allows us to go back and attempt to verify the device width that was previously selected. The simulation results are plotted in Fig. 3.10 for a fixed 75 pH inductor with a quality factor of 10 and at a frequency of 100 GHz. Looking at the full results in the figure, the trade-off between large and small devices is apparent: the smaller devices may not provide the isolation or ON-state return loss required by the system specifications, but larger devices will potentially produce excessive OFF-state insertion loss. Looking
Fig. 3.9: Simulated SPST switch S-parameters extracted at 100 GHz as a function of inductor value using two 42 \( \mu \)m shunt transistors.

Fig. 3.10: Simulated SPST switch S-parameters extracted at 100 GHz as a function of gate width (per shunt device) using a 75pH inductor.
at the results only at 42 $\mu$m, insertion loss and isolation results of 1.1 and 29 dB can be seen. OFF- and ON-state return losses are 18 and 2.6 dB respectively.

Regardless of the device width ultimately used, it remains important to ensure that the return loss of the SPST switch is optimized not only to reduce the insertion loss, but also to provide the appropriate impedance to any adjacent circuits. The load impedance of the switch was previously given by equation 3.2, and can be revised to give:

$$R_L = \sqrt{\frac{L}{2(C_{PAR} + C_{OFF})}}$$ (3.11)

where the capacitance term $C_{PAR}$ is the parasitic capacitance elements of the inductor, which can initially be taken to be small such that the total capacitance is dominated by the transistor Off-state device parasitics. The inductor value that produces a $R_L$ that matches the system impedance ($Z_o$, typically 50-$\Omega$), will also help determine the frequency response ripple in the pass-band. The group delay is also impacted by the inductor sizing, so care must be taken in this case to ensure that the gain flatness and phase response are appropriate for the application. Fig. 3.11 shows the insertion loss and group delay for three different inductor sizes. There is visible insertion loss ripple for the 80 and 40 pH examples, but the full ripple magnitude is dampened by the finite Q of the inductor. With a 160 pH inductor, the ripple has visibly declined and the frequency response approaches that of a maximally flat low-pass filter.

The group-delay of the switches can be seen in Fig. 3.11 to be well behaved for frequency ranges that cover all potential broadband circuit applications up to and including 100-GB Ethernet (which require at most 60-70 GHz of bandwidth), with less than 1 ps group-delay variation up to 60 GHz for all of the shown switch configurations. For the 80 pH switch, there is less than 1 ps group-delay variation beyond 90 GHz. Narrow-band applications, even up to 150 GHz will have no group-delay related issues. For applications that call for the absolute minimum group-delay variation, it is possible to optimize the switch to have a maximally-flat time delay low-pass filter response, as described in traditional LC-filter design textbooks for the Insertion Loss Method [10].

With these conclusions, final design parameters for an SPST switch operating up to the W-band can be established. As previously described, 42 $\mu$m wide devices and a 75 pH inductor will be used. The preliminary schematic of the SPST switch is shown in Fig. 3.12 and the initial simulated performance results are shown in Fig. 3.13. The switch insertion loss has a 1-, 2-, and 3-dB bandwidth of 52, 120, and 130 GHz respectively. The
3.2 Traveling-Wave SPST Switch Design

Fig. 3.11: Switch insertion loss and group-delay as a function of inductor value for fixed device sizes (42x1µm).

Fig. 3.12: The final SPST switch schematic showing inductor and device sizing.
OFF-state return loss of the switch is better than 10 dB up to 115 GHz, and the ON-state return loss is 2.6 dB at 110 GHz. Low-frequency isolation of the switch is 17.5 dB, and is approximately 30 dB at 110 GHz. There is a maximum of 1 ps group-delay variation up to a frequency of 93 GHz.

### 3.2.3. Digitally Controlled Variable Attenuation MOSFET Switches

The use of multi-fingered FETs in the switch devices permits an additional feature: the selective control of individual gates. This allows for the gradual increase of the net shunt-conductance, and consequently the effective attenuation, via the application of discrete bias voltages to individual gates. Typically, variable attenuators are implemented using analog control techniques that can be complex and PVT dependent [39, 40]. Attenuation control via selective gate biasing can eliminate much of this complexity, providing digitally-controlled variable attenuation in discrete steps, ideally with a monotonic response. While theoretically perfect, the monotonicity of the response is in reality a function of the specific implementation, and is thus subject to several layout-related non-idealities.

We can use the previous model to simulate the impact of this approach by keeping the total number of OFF-state fingers constant, and simply adding shunt transistors as appropriate. Fig. 3.14 shows the simulation results for such a structure with 3-bit gate control implemented on a SPST switch with 42 \( \mu \)m devices, as previously
3.2 Traveling-Wave SPST Switch Design

Fig. 3.14: Switch attenuation and return loss for 3-bit control settings.

Fig. 3.15: Switch return loss as a function of attenuation for all 3-bit control settings.
described. As the attenuation setting increases, the return loss degrades, but for a frequency range within the W-band, the return loss remains acceptable for the first 3 control-words. Plotting the return loss as a function of the given attenuation, as in Fig. 3.15, we can see that with approximately 14 dB attenuation, there is a return loss of about 8 dB.

For these simulations, the transistor conductance per unit gate width has been 2.7 mS/µm or equivalently \((370\Omega \cdot \mu m)^{-1}\). Thus the effective total shunt conductance as a function of the corresponding digital control words can be calculated as:

\[
g_{\text{SHUNT}} = \left(\frac{2 \cdot 6\mu m}{370\Omega \cdot \mu m}\right) \left(b_0 \cdot 2^0 + b_1 \cdot 2^1 + b_2 \cdot 2^2\right)
\]

where \(b_i = 0, 1\).

Only 3 control bits were used for simplicity’s sake, but the number of control bits can be increased such that the least-significant bit corresponds to a single MOSFET gate finger. This would allow the attenuation to be digitally controlled with high resolution.

### 3.3. SPDT Switch Design

SPDT switches are used to selectively couple a signal between two different paths, ideally with simultaneous high isolation to the inactive path, and low insertion-loss for the active path. The application of an SPDT as a transmit/receive switch is shown in Fig. 3.16, with the switch selecting between a transmit path with a PA, and a receive path through an LNA. The SPDT is constructed from two unit SPST switches, as shown in Fig. 3.17.

![Fig. 3.16: SPDT utilization as a transmit/receive switch in a transceiver.](image)
with the activated SPST switch providing low-insertion loss, and good return loss, with a 50-Ω input impedance. The inactive switch should provide high-isolation and a high input impedance, ideally presenting a perfect open circuit.

The traveling wave SPST switch operates appropriately when in pass-mode, with low-insertion loss and good return loss, but unfortunately, presents a very low input impedance when operated in isolation mode. Fig. 3.18 shows the SPST switch input impedance operating in both pass and isolation mode. The switch acts as a low impedance to ground, which is closer to a short than an ideal open.

3.3.1. Quarter Wavelength Transmission Lines

The issue of transforming a short-circuit into an open-circuit can be addressed by using quarter wavelength transmission lines. The mathematics and derivations of quarter wavelength transmission line transformers are addressed in numerous sources [10, 41], but a brief description will be provided here. Inserting transmission line segments with the same characteristic impedance as the source impedance, \( Z_o \), has no impact on the magnitude of the network parameters, but will rather produce a rotation of the complex phase of the same parameters. The size of this phase-shift is equal to the electrical length (normalized to the wavelength, \( \lambda \), of a signal at a given frequency, \( f_o \)), for transmission parameters (\( S_{21} \) and \( S_{12} \)), and twice the electrical length for reflection parameters (\( S_{11} \) and \( S_{22} \)). Focusing on the reflection parameters, adding precisely a quarter wavelength, \( \lambda/4 \), or 90°, will result in a 180° phase shift, effectively producing the complex conjugate of the initial value. This has the result of transforming an ideal short into an ideal open-circuit.

When dealing with a non-ideal short, as with an SPST switch in shunt-mode with some nominal ON-state resistance, the transformed open-circuit will also be non-ideal, with some non-infinite input impedance. Placing an ideal \( \lambda/4 \) transmission line at the input to an SPST switch, the real component of the input resistance is shown
Fig. 3.18: Traveling-wave SPST switch input impedance in pass and isolation mode.

Fig. 3.19: Quarter wavelength input impedance as a function of shunt resistance.
in Fig. 3.19 as a function of the SPST switch shunt resistance, and it is clear that in order to produce an input impedance at least 10x the nominal system impedance, $Z_o=50\,\Omega$, the shunt resistance must be $5\,\Omega$ or below.

### 3.3.2. SPDT Switch Implementation Using $\lambda/4$ Matching Segments

Using $\lambda/4$ transmission line segments to provide proper matching permits the use of traveling-wave SPST switches in an SPDT switch as shown in Fig. 3.20(a). A pair of $\lambda/4$ matching segments are required, one for each SPST switch. The two SPST switches are controlled by complementary control signals, with only one switch activated at once. Applying the proper control voltages, as in Fig. 3.20(b), the SPST switch on port 3, in its ON-state, can be replaced with its equivalent circuit, with two small shunt resistances to ground. This small shunt-resistance is transformed by the transmission line to produce a high input impedance looking into the branch towards port 3.

Taking the input impedance to be sufficiently large, we can simplify the circuit, as in Fig. 3.20(c), and replace the branch towards port 3 with an open circuit. The SPST on port 2 is replaced with its OFF-state equivalent circuit, producing a nominal 50-\Omega characteristic impedance and low-pass behavior, ideally allowing the signal to pass with minimal insertion loss.

As previously described, due to the non-zero shunt resistance of the ON-state SPST switch at port 3, the actual transformed input impedance of branch 3 will be something less than an open circuit. Instead of the signal reaching port 2 with only the insertion loss of the SPST switch, there is an additional signal degradation due to leakage into the inactive branch 3. The additional signal insertion loss in an SPDT configuration beyond the nominal insertion loss of the stand-alone SPST switch can be calculated as a function of the stand-alone SPST $S_{11}$, as in Fig. 3.21. These results demonstrate that with an SPST $S_{11}$ of -1 dB, a very difficult result to achieve, there is an additional 0.25 dB loss. A more reasonable -4 dB $S_{11}$ value results in an additional loss of 1 dB. An $S_{11}$ of -10 dB results in 2 dB additional loss. The additional SPDT loss approaches 3 dB as the SPST input match improves, indicating an even power split between port 2 and port 3. Note that all of these calculations assume ideal, lossless transmission line segments.

### 3.3.3. Lumped-Element Quarter-Wave Transmission Line Equivalent Circuit

The cost of implementing quarter wavelength transmission line segments on silicon can be costly due to the required dimensions. Although less of an issue in the mm-wave spectrum compared to lower frequency ranges,
Fig. 3.20: SPDT configuration using traveling wave unit SPST switches.
the wavelength of a 100-GHz signal is still not insignificant. The wavelength, $\lambda$, is given by:

$$\lambda = \frac{c}{f \cdot \sqrt{\varepsilon_R}}$$  \hspace{1cm} (3.13)

Where $c$ is the speed of light in a vacuum, $f$ is the frequency, and $\varepsilon_R$ is the relative permittivity of silicon dioxide, or approximately 3.9. Evaluating this at 100 GHz produces a wavelength of 1.5 mm, or 375 $\mu$m for a quarter wavelength. For this reason, it is often preferable to use lumped-element equivalent networks in place of the silicon area-intensive transmission lines.

Fig. 3.21: SPDT switch insertion loss degradation as a function of SPST $S_{11}$.

Fig. 3.22: Quarter wavelength transmission line segment and its $\pi$-equivalent circuit.
The lumped-element $\pi$ equivalent circuit for a $\lambda/4$ transmission line section is shown in Fig. 3.22 [42], with the component values determined by:

$$C_P = \frac{1}{2\pi f_o Z_o}$$
$$L_S = \frac{Z_o}{2\pi f_o}.$$

This relationship is valid only for quarter-wave (as well as $3\lambda/4$) lines at a center frequency $f_o$ and with a characteristic impedance $Z_o$. While the given relationship is only valid at $f_o$, the approximation is valid with a reasonable bandwidth around this center frequency of approximately $\pm 10\%$. Within this band, the $\pi$ network can theoretically provide performance (with regards to insertion loss, return loss, etc) similar to that of the fully distributed transmission line segment.

### 3.4. Fabrication and Measurements

All designs were implemented in a general purpose (GP) 65-nm CMOS digital process with a 7-metal back-end from STMicroelectronics. The process additionally offered some analog/RF options, such as high sheet-resistance poly resistors and high-density MiM capacitors with 5 fF/$\mu$m$^2$. The GP version of this technology offers core-oxide (13 Å) transistors with 60-nm drawn gate lengths, and 45-nm physical gate lengths.

All measurements were carried out on-wafer. Two s-parameter measurement setups were used: from DC to 94 GHz, measurements were carried out using a 94-GHz Wiltron 360B VNA, 110-GHz Cascade Infinity probes, and Cascade W-Band calibration substrates. For D-band measurements from 110-170 GHz, a second s-parameter setup was used that consisted of two OML (Oleson Labs) 110-170 GHz transmit/receive VNA extension heads used in conjunction with an HP 8510 network analyzer. Cascade Infinity 110-170 GHz D-band waveguide probes were used in conjunction with GGB Industries CS-5 calibration substrates. Note that the measurement results produced with the Wiltron 360B measurement system are noisy over a frequency range of approximately 40-58 GHz due to some un-resolved equipment problems.

Where appropriate (or possible), pad capacitance, as well as input/output line-loss, were de-embedded using the transmission line based procedure described in [34].
3.4 Fabrication and Measurements

3.4.1. Traveling-Wave SPST Switch

The traveling-wave SPST switch was designed and implemented exactly as described in Section 3.2. The design was realized with selective gate-control, as described in Section 3.2.3, using 3 control bits that bias binary-weighted low threshold voltage (LVT) MOSFETs with 1 \( \mu \text{m} \) finger width, with 6, 12, and 24 fingers. Simulation results now include skin-effect modeling for the inductor, as apposed to simple Q-factor modeling as previously used. A photograph of the manufactured die is shown in Fig 3.24 with a total area of 0.52x0.29 mm\(^2\) and the core switch occupying only 65x35 \( \mu \text{m}^2 \).

The measured s-parameters for the switch are shown in Fig. 3.25 with symbols representing measured results, and simulation result shown as solid lines. These results have had the input/output pad capacitance and transmission line interconnects de-embedded. Excellent matching can be seen between simulation and measurement up to about 80 GHz, where the results begin to diverge slightly, with approximately 0.5 dB error at 94 GHz. The measured insertion loss at 94 GHz is only 1.6 dB. The measured return loss is within 5dB of the simulated values, with the measured results being consistently 4-5 dB better than the simulated values. The isolation measurements are within 2 dB of the simulated values, with better than 30 dB isolation measured at 94 GHz. The measured isolation values are consistently slightly better than the simulated values.

Fig 3.26 compares the measured and simulated insertion loss, from 1 GHz to 94 GHz for the 8 digital control words. Measured results are shown as symbols, and simulation results are shown as solid lines. Each curve corresponds to one of the 8 digital control words. Simulated data shows good agreement with the measured results, with the discrepancy increasing with increasing attenuation. All digital states can be seen to be monotonic.

![Schematic of the manufactured traveling-wave SPST switch](image)

**Fig. 3.23:** Schematic of the manufactured traveling-wave SPST switch
3.4 Fabrication and Measurements

Fig. 3.24: Manufactured SPST switch photograph. The total area is 0.52x0.29 mm$^2$, with the actual circuit occupying 65x35 µm$^2$.

Fig. 3.25: Measured s-parameters of SPST switch operated as typical switch. Measured results are indicated by closed symbols and simulation results by solid lines.
Fig. 3.26: Measured SPST switch attenuation versus frequency for the 8 digital states, increasing from top to bottom. Measured results are indicated by closed symbols and simulation results by solid lines.

Fig. 3.27: Measured effective isolation curves at 1, 24, 60, and 94 GHz of the attenuator test structure.
3.4 Fabrication and Measurements

Due to the non-flat frequency response of the switch, the attenuation is not constant over frequency, with increased attenuation provided at higher frequencies for a given digital control word. Fig. 3.27 compiles the measured switch attenuation as a function of the digital control word for several frequencies. This problem is most severe at high attenuation settings where the attenuation variation from low to high frequency is just over 10 dB, with a worst case isolation of 19 dB at 1 GHz, and a maximum of 30.2 dB at 94 GHz. The minimum measured insertion loss is 0.14, 0.46, 1.2, and 1.6 dB at 1, 24, 60, and 94 GHz respectively.

The measured return-loss is plotted in Fig 3.28, with the curves representing increasing attenuation settings from bottom to top. The switch becomes reflective in nature as the attenuation setting is increased, with increased reflection as the transistor shunt conductance increases. While the minimum insertion loss setting provides a return-loss better than -12 dB from DC to 94 GHz, the other digital settings rapidly degrade the input match. Plotting the return loss as a function of a given attenuation at 90 GHz, it can be seen that an attenuation of approximately 10 dB can be achieved while maintaining a return loss better than 10 dB.

One of the attractive features of passive switches and attenuators are their linearity and power dissipation when compared with active alternatives to these circuits. For this SPST switch, it was not possible to measure the linearity of the switch within the W-band due to a lack of large-power signal sources that can provide sufficient RF power to drive the system non-linearly. The best mm-wave source available was an Agilent E8257D signal source that can produce almost +10 dBm of power at the measurement probe-tip at frequencies up to the 67 GHz, after input losses due to cables, connectors, etc. The output power was measured using an Agilent V8486A V-band (50-75 GHz) power sensor. All setup losses and power-levels are manually de-embedded, so measurement are not vector-calibrated as they would be when done using a network analyzer, likely introducing measurement uncertainty on the order of 1-2 dB.

The measured linearity of the SPST switch is shown Fig. 3.30 for both ON- and OFF-states at 60 GHz. No compression is observed up to the equipment-limited maximum power of +9 dBm, indicating a $P_{1\text{dB}}$ for the switch greater than +9 dBm.

A performance comparison with other reported mm-wave SPST switches is presented in Table 3.2, indicating that this design offers similar or better performance to those implemented in III/V technologies. Previously published CMOS mm-wave switches [31, 33] do not report the performance for SPST switches, and have been
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Fig. 3.28: Measured return-loss over frequency for the 8 digital states. From bottom to top, the curves represent increased isolation settings.

Fig. 3.29: Measured return-loss as a function of attenuation at 90 GHz.
Fig. 3.30: Measured P1dB of the switch in pass mode and isolation mode.

Table 3.2: SPST Switch Performance Comparison.

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Technology</th>
<th>Operating Frequency</th>
<th>Insertion Loss (dB)</th>
<th>Isolation (dB)</th>
<th>Area (mm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[27]</td>
<td>GaAs HJFET</td>
<td>DC-60 GHz</td>
<td>1.64</td>
<td>20.6</td>
<td>0.52x0.63</td>
</tr>
<tr>
<td>[28]</td>
<td>GaAs HJFET</td>
<td>DC-60 GHz</td>
<td>1.37</td>
<td>23.1-39.6</td>
<td>0.4x0.07</td>
</tr>
<tr>
<td>[29]</td>
<td>GaAs HJFET</td>
<td>DC-110 GHz</td>
<td>2.55</td>
<td>22.2</td>
<td>0.85x0.45</td>
</tr>
<tr>
<td>[23]</td>
<td>GaAs pHEMT</td>
<td>75-110 GHz</td>
<td>1.6</td>
<td>22.5</td>
<td>-</td>
</tr>
<tr>
<td>[24]</td>
<td>GaAs PIN</td>
<td>55-85 GHz</td>
<td>0.6</td>
<td>20</td>
<td>-</td>
</tr>
<tr>
<td>[30]</td>
<td>GaAs pHEMT</td>
<td>DC-80 GHz</td>
<td>3</td>
<td>24.5</td>
<td>1.0x0.75</td>
</tr>
<tr>
<td>This Work</td>
<td>65nm CMOS</td>
<td>DC-94 GHz</td>
<td>1.6</td>
<td>19-30.2</td>
<td>0.52x0.29</td>
</tr>
</tbody>
</table>
3.4 Fabrication and Measurements

therefore left out. However, as SPDT switches, they too show competitive performance with those fabricated in III/V technologies.

3.4.2. 6-bit Digitally Controlled Variable Attenuator

An additional test structures was created for a variable attenuator in a similar 65-nm technology from Fujitsu Limited, and is shown in Fig. 3.31. This structure was designed to be used strictly as variable attenuator, thus reducing the nominal insertion loss requirements. In order to improve the linearity of a receive chain, the signal level must be controlled at various stages at which circuit linearity can become limiting. A critical point for which a variable attenuator can be used to improve linearity is within the RF-path (before down-conversion) but after the low-noise amplifier. By placing the attenuator after the low-noise amplifier, the nominal and successive degradation of noise-figure due to the variable attenuator is reduced according to Friis’ formula [10]. Input compression and 2\textsuperscript{nd}- and 3\textsuperscript{rd}-order inter-modulation products are all critical specifications that can be improved by controlling the signal level at the input to an RF-mixer.

This attenuator implements high-resolution control of the attenuation level (compared to 3-bits previously described) by using 6-bits of binary-weighted digital control. The circuit topology was implemented as before with two shunt transistors, but the total device size was increased slightly to accommodate 63 fingers, each 1.0 \( \mu \text{m} \) wide. The transistor fingers were lumped together and selectively controlled using binary weighting.

The measured s-parameters for the attenuator are shown in Fig. 3.32 for the two extreme configurations, corresponding to operation as an SPST switch. These results have not had the input/output pad capacitance and transmission line interconnects de-embedded. The measured insertion loss at 94 GHz is less than 4 dB, with only 2.6 dB at 60GHz. The measured return loss is better than -10 dB across the measurement band. The isolation is from 20 dB at low frequency to about 30 dB at 94 GHz.

![Fig. 3.31: Schematic of the manufactured 6-bit variable attenuator](image-url)
Fig. 3.32: Measured s-parameters of attenuator operated as typical SPST switch. Measured results are indicated by closed symbols and simulation results by solid lines.

Fig. 3.33: Measured insertion loss of the attenuator as a function of frequency for all control states.
The insertion loss, $S_{21}$, is plotted in Fig. 3.33 for all 64 digital control words, with the results at specific frequencies shown in Fig. 3.34. The high-resolution of the digital control is apparent, but there are clear monotonicity issues with the 3 MSBs. The monotonicity issue is exasperated at higher frequencies, with the results at 90 GHz much more apparent than at 1 GHz. Layout asymmetries coming from the binary-weighted implementation, combined with the more distributed nature of the switch as the frequency increases, results in these non-monotonicities. At DC or low-frequency, the switch structure appears lumped, resulting in the more linear behaviour.

The dynamic range of the variable attenuator, as defined as the range between the minimum attenuation state and the maximum attenuation state, has been plotted in Fig. 3.35, showing excellent dynamic range into the W-band.

The return loss is plotted over all frequencies and control-words in Fig. 3.36, and as a function of attenuation at 60 and 90 GHz in Fig. 3.37. The return loss of the attenuator is better at higher frequencies over all control words, and this can be seen explicitly in the second figure, where the return loss is seen to be better than -10 dB up to an attenuation of 10 dB when extracted at 60 GHz, but when measured at 90 GHz, all the way up to an attenuation of
3.4 Fabrication and Measurements

Fig. 3.35: Measured dynamic range of the variable attenuator

Fig. 3.36: Measured return loss of the attenuator as a function of frequency for all control states.
3.4 Fabrication and Measurements

Fig. 3.37: Measured return loss as a function of the attenuation setting. Results at 60 and 90 GHz shown.

-23 dB. This structure can be seen to have excellent performance as a well-matched digitally-controlled variable attenuator within the W-band region.

3.4.3. W-Band SPDT Switch

A W-band SPDT switch, shown in Fig. 3.38, was designed and implemented in the same 65-nm technology to be used in conjunction with a 90-GHz passive imaging receiver, to be presented in Chapter 4. The unit SPST switch is a slightly modified version of the switch previously presented, with the MOSFET layout modified to use wider finger widths. The previous design used a 1 µm gate width with 42 fingers. This updated design uses a 3 µm gate width with 14 fingers, providing the same 42 µm total gate width. This change was made in order to reduce the device parasitic capacitance by reducing the amount of metalization required to connect all device fingers. To match the reduced device parasitics, the inductor has also been reduced.

The λ/4 transmission lines have been replaced with lumped equivalents according to the previously described methodology. The values were optimized using the design kit simulator with extracted device parasitics and modeled inductor losses. A small amount of additional capacitance was required adjacent to each MOSFET in order to complete the π equivalent circuit. These small capacitors were implemented using design kit metal-oxide-
metal (MoM) capacitors because the small value is not realizable using the design kit MiM capacitors. The two capacitors (to complete the two matched networks) present at the common node at port 1 were merged into a single capacitor, and implemented as part of the required pad-capacitance. No compensation for the pad-capacitance on ports 2 or 3 was performed.

The layout for the test structure is shown in Fig. 3.39. On port 1, the signal pad can be seen to be enlarged compared with ports 2 and 3, in order to accommodate the larger capacitance required at this common node compared to the 20 fF pad capacitance of the standard high-speed signal pad. The output lines on port 2 and 3 were implemented in a 50-Ω transmission line, and the digital control circuitry (to produce complementary control voltages) was integrated on-chip. The layout of the high-speed test structure was implemented in perfect symmetry in order to ensure port-to-port matching.

The measurement results for the W-band SPDT are shown in Fig. 3.40, with results shown from 1-170 GHz. Measurement results for the 94-110 GHz range are not available due to equipment limitation. Measurement results are shown as symbols, and simulation results are shown in the associated lines. The measured insertion loss is approximately -4 dB centered in between 94 and 110 GHz (where there are no measurement results). The insertion loss is better than -5 dB from 42 to 134 GHz. Simulation results can be seen to distinctly under-estimate the insertion loss of the structure, with a fairly constant offset between the measurement and simulation results over the band of interest. A zoomed in version of the insertion loss is presented in Fig. 3.41, and a discrepancy of approximately 1.5 dB can be seen. The source of this discrepancy is uncertain, but can likely be attributed to
3.4 Fabrication and Measurements

Fig. 3.39: Layout of the W-band SPDT switch test structure.

Fig. 3.40: Measured (symbols) and simulated (lines) s-parameters of the W-band SPDT switch.
3.4 Fabrication and Measurements

Fig. 3.41: Measured (symbols) and simulated (lines) insertion loss and isolation of the W-band SPDT switch, zoomed into the frequency of interest.

an optimistic modeling of several loss vectors in the structure, including capacitor and inductor Q, and substrate losses for any transmission lines.

The return loss of the two ports is well behaved over the frequency of interest with $S_{11}$ better than -10 dB from approximately 32 to 148 GHz and $S_{22}$ better than -10 dB from 83-142 GHz. The isolation is well matched with simulation results and is between 25 and 30 dB in the W-band.

3.4.4. D-Band SPDT Switch

A D-band SPDT switch, shown in Fig. 3.38, was also designed and implemented, but not used in any associated circuit. The unit SPST switch is again modified from the previous switch, with the inductor decreased in order to extend the bandwidth of the SPST switch. Because this is a tuned circuit, any additional ripple in the pass-band in the lower-frequency ranges are not an issue. For this higher-frequency range, no additional capacitance was required at any of the nodes to properly match the circuit. The inherent capacitance of the high-speed signal pad, approximately 20 fF in this technology, is appropriate for the tuning requirements. Additionally, a series inductor of 40 pH was added at the two output ports to resonate with the pad capacitance and increase the bandwidth.

Due to equipment restrictions or limitations when measuring using waveguide components in the D-band,
there are no differential probes or matched loads, so the second output port of the circuit was terminated on-chip using discrete resistors. On-chip resistors have quite large variation, so these resistors may limit the input matching on port 1 when measurements are being performed in isolation mode.

Fig. 3.43 shows an image of the test structure. It is just like the W-band SPDT switch structure, with the elimination of one of the test-pads and the addition of on-chip termination for port 3. Again, all on-chip connections are made using 50-Ω transmission lines. The only asymmetry in this structure is due to the use of on-chip termination, and the pad-capacitance missing from the path with termination.

The measurement results for the D-band SPDT are shown in Fig. 3.44, with results shown from 40-170 GHz as before. Measurement results are shown as symbols, and simulation results are shown in the associated lines. The measured insertion loss is better than -4 dB between 130 and 140 GHz. The insertion loss is very flat, with a -0.1-dB bandwidth of 122-146 GHz, and a -1-dB bandwidth covering the entire D-band frequency range from 110-170 GHz. The simulation results are once again optimistic over much of the measurement range, with about 1.5 dB additional loss measured compared to simulation up to 140 GHz, and less than 2 dB up to 170 GHz. Once again, a zoomed in version of the insertion loss and isolation is presented in Fig. 3.45 from 110 to 170 GHz. The source of this discrepancy can likely be attributed to the same high-frequency modeling issues discussed for the W-band SPDT switch.

The return loss of the two ports is excellent in the frequency band of interest with $S_{11}$ better than -10 dB from approximately 48 to 170 GHz and $S_{22}$ better than -10 dB from 110-170 GHz. There is a fairly significant
3.4 Fabrication and Measurements

Fig. 3.43: Layout of the D-band SPDT switch test structure.

Fig. 3.44: Measured (symbols) and simulated (lines) s-parameters of the D-band SPDT switch.
3.4 Fabrication and Measurements

![Graph showing insertion loss and isolation vs frequency]

**Fig. 3.45:** Measured (symbols) and simulated (lines) insertion loss and isolation of the D-band SPDT switch, zoomed into the frequency of interest.

The discrepancy with simulation results at higher frequency, which is likely explained by issues in the inductor or transmission line modeling with regards to high-frequency losses through the skin-effect or the lossy substrate. The isolation is well matched with simulation results and is between 27 and 32 dB across the D-band.

Finally, the return losses and the input impedance from port 1 are shown in Fig. 3.46 for the isolation-mode measurement where the signal is being directed toward port 3 and into the on-chip termination. The $S_{11}$ is degraded compared to the pass-mode measurement which may be due to the lack of pad-capacitance on port 3, or due to mismatch from the on-chip resistors. The return loss from port 2, which is equal to the $S_{22}$ of the SPST switch itself is fairly poor, between -5 and -6 dB, which means that the poor shunt-isolation could contribute 1.1 to 1.3 dB of additional loss for the SPDT switch. The real part of the input impedance (from port 1) can be seen to cross through 50 Ω right at the center frequency of 140 GHz, but the matching is degraded by a non-zero imaginary component of the input impedance, which is fairly flat at between 22 and 28 Ω across the band.

### 3.4.5. SPDT Switch Comparison

A performance comparison with other reported mm-wave SPDT switches is presented in Table 3.3, indicating that these designs offers similar or better performance to those implemented in III/V technologies. The trade-off
3.4 Fabrication and Measurements

**Table 3.3:** SPDT Switch Performance Comparison for W-band and Above.

<table>
<thead>
<tr>
<th>Ref, year</th>
<th>Technology</th>
<th>Operating Frequency</th>
<th>Insertion Loss (dB)</th>
<th>Isolation (dB)</th>
<th>Area (mm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[16], 2009</td>
<td>0.12-µm (Bi)CMOS</td>
<td>85-105 GHz</td>
<td>2.3</td>
<td>21</td>
<td>0.18</td>
</tr>
<tr>
<td>[31], 2007</td>
<td>90-nm CMOS</td>
<td>50-94 GHz</td>
<td>2.7</td>
<td>29</td>
<td>0.24</td>
</tr>
<tr>
<td>[43], 2009</td>
<td>90-nm CMOS</td>
<td>50-70 GHz</td>
<td>2.0</td>
<td>25</td>
<td>0.275</td>
</tr>
<tr>
<td>[44], 2006</td>
<td>0.15-µm GaAs HEMT</td>
<td>60-135 GHz</td>
<td>5.5</td>
<td>42</td>
<td>0.68</td>
</tr>
<tr>
<td>[45], 2003</td>
<td>0.18-µm GaAs HEMT</td>
<td>30-85 GHz</td>
<td>2.5</td>
<td>33</td>
<td>1.45</td>
</tr>
<tr>
<td>[46], 2008</td>
<td>0.10-µm InAlGaAs</td>
<td>70-120 GHz</td>
<td>1.5</td>
<td>20</td>
<td>0.7</td>
</tr>
<tr>
<td>This Work (W-band), 2009</td>
<td>65-nm CMOS</td>
<td>42-134 GHz</td>
<td>3.9</td>
<td>26</td>
<td>0.06</td>
</tr>
<tr>
<td>This Work (D-band), 2009</td>
<td>65-nm CMOS</td>
<td>110-170 GHz</td>
<td>3.9</td>
<td>28</td>
<td>0.06</td>
</tr>
</tbody>
</table>

**Fig. 3.46:** Measured return losses in isolation mode, and the input impedance from port 1.
between insertion loss, isolation, and operating frequency range is clear from these various works. In comparing with results that use CMOS switches, [16] has a low 2.3 dB insertion loss, but also a relatively low 21 dB isolation, and uses an RF back-end with extra-thick metal layers that helps reduce losses in the transmission lines and passives. [31] has excellent performance with good insertion loss and isolation, but also uses a non-standard RF back-end with ultra-thick top metal layers (3.4 µm thick) compared to the standard digital back-end used for this work (0.9 µm thick top metal). [43] has excellent insertion loss and isolation, but is centered too low in frequency and again, uses an ultra-thick metal RF back-end. As well, all of the 3 works using CMOS switches also use distributed matching networks rather than lumped, as in this work, which may contribute to lower loss, but also results in a significantly larger area. At this time, we are aware of no other reported switches in any technology that operate up to the edge of the D-band (170-GHz) as in this work.
4.1. Introduction

W-band imagers are attractive due to their potential for high resolution operation and their ability to penetrate various materials. Typical imagers at these frequencies have been realized using III/V technologies, with InP HEMT LNAs in conjunction with planar doped barrier [12,14] or Schottky detectors [12,13]. Recent publications have investigated the use of zero-bias backward tunnel diodes [12], and even SiGe HBTs [16]. This chapter describes the implementation and testing of a W-band passive imaging chip manufactured in a 65-nm bulk CMOS process [47]. The principles of operation for such a systems are described in Section 2.1.

4.2. System Description

The proposed Dicke-switching radiometer receiver is shown in Fig. 4.1, with the area enclosed in a box integrated on-chip. The full system integrates an LNA centered around 90 GHz with greater than 27 dB gain and less than 7 dB noise figure, a square-law detector that utilizes a differential topology to suppress system and power-supply

![Fig. 4.1: Passive detector system schematic.](image-url)
noise, an on-chip SPDT switch with 4 dB insertion loss centered at 90 GHz and a reference 50-Ohm resistor for calibration. Additionally, a total-power radiometer, which excludes the input SPDT switch, was also implemented.

### 4.2.1. Low-Noise Amplifier

Just as in coherent receivers where LNAs are used to minimize the noise contribution of the frequency conversion mixer, passive receivers rely on RF pre-amplification by a low-noise amplifier to minimize the noise contribution of the detector circuit. In fact, this is a more significant problem for passive receivers as the detector circuits will typically contribute significantly more noise than active or passive mixer circuits.

For this receiver, a very high-gain, low-noise amplifier was required. Power consumption was to be kept minimal in order to maintain the power budget benefit when compared to a coherent imaging system. Fortunately, passive imaging systems have low linearity requirements, assuming in-band blocking signals are not present in the environment, which is a reasonable assumption for W-band imaging systems. This low linearity requirement means that high RF gain is achievable without excessive device scaling, and consequently with low power consumption.

The schematic for the implemented LNA is shown in Fig. 4.2. It consists of 5 telescopic cascode stages that are cascaded using lumped inductors for tuning and series MiM capacitors for inter-stage matching. Each stage is biased for minimum noise using the constant current biasing technique described in [48]. The input stage is simultaneously noise and impedance matched to 50-Ω using the transformer feedback technique described in [49], from which the initial LNA design was derived.

One of the many benefits of this type of matching network (described fully in [49]), is the minimization of the number of components used to achieve the match. The single 2:1 transformer replaces what is typically 2 or 3 other components, specifically a transistor source inductor, a gate inductor, and potentially some series or shunt capacitor. For example the MiM cap, which is still used for inter-stage matching and AC-coupling, is a rather lossy device when used at these mm-wave frequencies. Fig. 4.3 shows the measured Q and equivalent series resistance (ESR) for a 105 fF MiM capacitor test structure that was manufactured in the same CMOS technology. Qs of approximately 3 and an ESR of approximately 4 Ω around 90 GHz can be observed.

The transistors for the various stages were designed similarly. As a compromise between the optimization for high-gain and low-noise, a 1 μm gate finger width was selected with gate contacts placed on both sides of the
4.2 System Description

Fig. 4.2: Low-noise amplifier schematic.

Fig. 4.3: Measured 105fF MiM capacitor Q and ESR as a function of frequency.
device fingers (double-sided gate contacts). This selection was made based on an analysis described in [3] that examined transistor MAG and $\text{NF}_{\text{min}}$ at 94GHz as a function of gate finger width for both single- and double-sided gate contacts, the results of which are shown in Fig. 4.4.

Finally, the output stage of the LNA has a transformer which simultaneously acts as the load for the stage as well as converting the signal from single-ended to differential in order to drive the following stage (the detector circuit). The center-tap on the secondary-coil of the transformer provides an easy access point to bias the following circuit.

The layout of the LNA was optimized to reduce the height of the structure, as shown in Fig. 4.5, potentially permitting the convenient integration in an array configuration with multiple receiver elements. From 1.2V, the LNA consumes only 30mA and has over 27dB gain with a 3-dB bandwidth exceeding 10 GHz.

### 4.2.2. Square-Law Detector

The schematic of the square-law detector is shown in Fig. 4.6, and utilizes a differential topology similar to that in [50]. An input transformer, which also acts as the output load of the LNA, performs a single-ended to
4.2 System Description

Fig. 4.5: Layout of the W-band LNA.

Fig. 4.6: Square-law detector schematic.
differential conversion. The detector is matched at the input to 50-Ω using a shunt-series matching network in addition to a tuning capacitor placed across the secondary coil of the transformer. The common-mode signal at the source of the input transistors, which is proportional to the signal amplitude, is amplified by the common-gate amplifier formed by transistor M5 and the output load resistor.

Before the output voltage of the detector can be integrated and measured, the signal must be amplified using an external (off-chip) low-noise amplifier. The base-band frequencies over which these detectors operate (< 1MHz) are subject to numerous interferers that can contribute significant noise into the band of interest. These signals will all couple into the system at the detector stage or later in the signal path through numerous vectors, including power-supply noise and noise-coupling with the off-chip interconnect cables. In order to reduce the noise introduced by these various sources and the resulting negative impact on the system sensitivity, it is important to utilize a differential detector architecture. For this detector, this was accomplished by introducing a duplicate input pair and CG amplifier on-chip, in perfect layout symmetry. The second detector (with no input signal) provides an output voltage that can be used as a reference voltage for differential signal amplification by the external LNA.

### 4.2.3. W-Band SPDT Switch

The Dicke switch in the receiver is implemented as a SPDT switch realized with standard MOSFET devices. It is also possible to use a single-pole single-throw (SPST) switch [51]. The SPDT switch provides 50-Ω matching to the input of the LNA in both states, by connecting either the antenna or an on-chip reference resistor to the LNA. The latter is needed for low-frequency noise-chopping. A full description of the switch design is included in Section 3, and implemented switch is the same, but a brief summary will be included here.

The SPDT switch, shown in Fig. 4.7, features two SPST unit-cells based on shunt-connected MOSFETs with relatively large, 3-μm wide, gate fingers to reduce the impact of parasitic metallization and fringing capacitance compared to the smaller finger widths employed in the LNA. A relatively large resistance of a few KΩ is added in series with the gate to reduce switch capacitance and, therefore, insertion loss. In this design, the λ/4 transmission lines used to match both ports of the SPDT switch have been replaced with lumped inductors to reduce the layout footprint and may be responsible for the higher loss of this switch compared to some other recent results such as [43].
4.3 Fabrication and Measurement Results

The full receiver, Fig. 4.8, and a stand-alone detector breakout, Fig. 4.9, were fabricated and occupy 865x470µm² and 420x495µm² respectively. Additionally, a radiometer version (which is not shown) without the input antenna switch was manufactured and characterized in order to independently determine the impact of the SPDT switch on receiver sensitivity. The circuits were fabricated in the GP (general-purpose) variant of a 65nm bulk CMOS process with a standard digital back-end and MiM capacitors. The n-MOSFETs with a minimum effective gate-length of 45 nm have an fT and fMAX of 180 GHz and 250 GHz, respectively, the latter depending strongly on layout geometry.

4.3.1. Low-Noise Amplifier Measurements

The LNA was measured using a Wiltron 360B network analyzer up to 94GHz, and using an Agilent NFA (noise figure analyzer) with a single side-band down-converter between 75-88.5GHz. Shown in Fig. 4.10, the measurements of the gain obtained with the VNA are in good agreement with those from the noise-figure setup.

NFA measurements are typically less accurate than the corresponding VNA measurements due to the lack of vector-calibrated de-embedding up to the measurement probe-tips, which the VNA has. The NFA measurements require scalar de-embedding of losses on the input signal measurement path, which are prone to reflections from discontinuities and mismatches. These measurements show a 1-2dB higher gain result for the NFA measurements which can be attributed to a saturation at the input of the LNA due to the larger signal signal strength of the
4.3 Fabrication and Measurement Results

**Fig. 4.8:** Die photo of the full receiver. The circuit occupies $865 \times 470 \mu \text{m}^2$ including all pads.

**Fig. 4.9:** Die photo of the stand alone detector. The circuit occupies $420 \times 495 \mu \text{m}^2$ including all pads.
VNA measurement system. Discrete attenuation was required at the input to the amplifier in order to increase the linearity but the dynamic range of the system set an upper limit on the amount of attenuation that could be added before corrupting results due to inaccuracies during the vector calibration process.

Overall, the peak gain of the LNA is over 27 dB at 88 GHz, coinciding with the minimum noise figure of 6.8 dB. This marks the highest reported gain for a W-band CMOS amplifier. The return loss is better than 10 dB from below 70 GHz to over 94 GHz.

Fig. 4.11 reproduces the LNA gain and noise-figure measured with the NFA as a function of the MOSFET drain current density. The gain remains within 1 dB of its peak value for current densities ranging from under 0.2 mA/m to over 0.3 mA/m. Similarly, the noise-figure remains between 6.8 and 7 dB from 0.15 mA/m to over 0.3 mA/m. As a compromise between gain, noise figure, and the associated power consumption, the nominal bias of the LNA was set at 0.2 mA/m, corresponding to a total current consumption of 28 mA.

4.3.2. SPDT Switch Measurements

The W-band SPDT switch measurements were originally presented in Chapter 3, but are briefly repeated here. Fig. 4.12 compares the measured (symbols) and simulated (lines) S-parameters of the SPDT switch breakout from
4.3 Fabrication and Measurement Results

![Graph of Gain and Noise Figure vs. Current Density](image1)

**Fig. 4.11:** Measured noise and gain vs. bias current density of the LNA.

![Graph of S-Parameters vs. Frequency](image2)

**Fig. 4.12:** Measured (symbols) and simulated (lines) s-parameters of the SPDT switch.
1 to 94 GHz and from 110 to 170 GHz. The minimum insertion loss is approximately -4 dB, centered between 94 and 110 GHz, and is better than -5 dB from 42 to 134 GHz. The return loss of all ports is well behaved over the frequency of interest, with S11 lower than -10 dB from 32 to 148 GHz and S22 better than -10 dB from 83 and 142 GHz. The isolation hovers between 25 and 30 dB over the W-band.

A zoomed version of the insertion loss and isolation for the SPDT switch are shown in Fig. 4.13 over only the frequency of interest. The insertion loss is better than -5 dB over the whole W-band, and the minimum measured insertion loss is -4.2 dB at 94 GHz. Isolation is flat at approximately -25 dB.

4.3.3. Receiver Measurements

4.3.3.1. Experimental Setup

The measurement setup for testing the receiver is shown in Fig. 4.14, with the portion of the diagram enclosed in a checkered box integrated on-chip. The W-band signal was produced using a 6x signal multiplier, driven by a 50GHz HP source in the 12-18GHz range. The output signal power was controlled using a discrete wave-guide attenuator, before transitioning from W-10 wave-guide to W1 1mm coaxial connectors using an Agilent wave-guide to coax transition. The on-wafer circuit was measured using GGB 110GHz probes and a discrete 110GHz W1 coaxial decoupling cap.

An off-chip, low-noise differential post-amplifier with high input impedance was used at the detector output to further boost the signal and to drive the 50-Ω test equipment. The differential post-amplifier was configured with 34 dB gain (into 50-Ω) and a 3-dB bandwidth of 200 kHz. It has an input-referred noise of 11 nV/√Hz at 1 kHz. The gain of the post-amplifier has been removed from the responsivity measurement results but its noise contribution has not been de-embedded. The limited bandwidth of the post-amplifier has restricted the range of frequencies over which measurements could be carried out.

4.3.3.2. Stand-Alone Detector

The low-frequency noise voltage at the output of the detector is shown in Fig. 4.15, and was obtained by sweeping the detector reference current and measuring the noise voltage at various baseband frequencies. The results demonstrate that the output noise voltage decreases with increasing frequency and is thus still within the 1/f noise range of the MOSFET technology. The bandwidth of the low-noise post-amplifier limits the maximum
measurement frequency to about 400 kHz. It is expected that measurements at higher frequencies will produce lower noise results.

At low bias current densities, the various noise voltage curves converge to a noise-floor value of approximately 10 nV/$\sqrt{\text{Hz}}$, which corresponds to the manufacturer provided noise-floor for the external pre-amplifier. While the measured noise begins to rise above this value, especially the results for the 400-kHz measurements at current densities up to 10 $\mu$A/$\mu$m are still quite close to this noise-floor, and it is an indication that a superior amplifier with lower noise would contribute to improved measurement results with smaller uncertainty.

As the bias current density decreases, the dominant 1/f noise contribution from the detector also decreases. At low current densities, the thermal noise of the load resistor and of the MOSFET channel ultimately limit the lowest noise that can be achieved. Unfortunately, the benefits of biasing at very low current densities are mitigated by a simultaneous drop in receiver responsivity. This trade-off becomes apparent by plotting the system noise-equivalent power (NEP), given by Equation 2.1.

Fig. 4.16 shows the measured NEP and responsivity as a function of bias current density, providing insight into the optimal bias regime for this type of detector. The low output noise voltage obtained at very low current densities is completely negated by the significant decrease in responsivity, which results in an overall increase in
4.3 Fabrication and Measurement Results

The measurements discussed next are all taken at a bias current density of 10 $\mu$A/\(\mu\)m and a baseband frequency of 400 kHz. The responsivity and NEP characteristics versus frequency are plotted in Fig. 4.17, with a peak responsivity of over 200 V/W and the best NEP of 150 pW/$\sqrt{\text{Hz}}$, both centered at 80 GHz. The 3-dB bandwidth, corresponding to a 50% drop in responsivity, extends from 70 to 95 GHz. The measured return loss of the detector is shown in Fig. 4.18 overlayed with the responsivity, showing good matching from 78 GHz to at least 94 GHz.

Fig. 4.19 reproduces the measured transfer characteristics and linearity of the stand-alone detector. The responsivity and NEP start to degrade for input powers beyond -10 dBm, with a 3-dB compression point of approximately -6 dBm. The responsivity of the stand-alone detector versus frequency is shown in Fig. 4.20 for temperatures ranging from 25 $^\circ$C to 125 $^\circ$C.

Fig. 4.21 illustrates the stand-alone detector performance as a function of the power-supply voltage while maintaining constant current density. Responsivity can be seen to be relatively unchanged from a nominal result around 160 V/W, with performance leveling out at 1.5 V or above. The system NEP demonstrates a local-minimum value around approximately 1.2 V, likely due to the optimal noise bias current density changing as a result of the voltage. Optimal current densities would have to be found for each power supply voltage.
4.3 Fabrication and Measurement Results

Fig. 4.15: Measurement results of the output noise voltage as a function of the detector current density for several frequency points.

Fig. 4.16: The measured detector responsivity (at 88 GHz) and NEP over detector current densities and output frequencies.
4.3 Fabrication and Measurement Results

**Fig. 4.17:** Measured detector responsivity and NEP over frequency.

**Fig. 4.18:** Measured detector return loss overlayed with the detector responsivity.
**Fig. 4.19:** Measured responsivity and NEP at 88GHz as a function of input power. Measured without the SPDT switch.

**Fig. 4.20:** Measured responsivity and NEP at 88GHz as a function of input power. Measured without the SPDT switch.
4.3 Fabrication and Measurement Results

![Graph showing detector responsivity and NEP vs. power supply voltage at 88GHz]

**Fig. 4.21:** Measured detector responsivity and NEP at 88GHz as a function of detector power-supply voltage at constant current density

### 4.3.3.3. Total Power Radiometer

A total power radiometer, which does not include an input SPDT switch, was also fabricated and characterized. As before, the detector and the LNA were biased at 10 µA/µm, and 0.2 mA/µm, respectively. Fig. 4.22 shows that the responsivity peaks at over 220 kV/W and that the best NEP is below 0.1 pW/√Hz, both at 86 GHz. The 3-dB bandwidth, defined based on a 50% drop in either responsivity or NEP, extends from 81 to 93 GHz.

The saturation of the detector is shown in Fig. 4.23. As a function on input power, the responsivity and NEP can be seen to degrade beyond input powers of around -45 dBm, with a -3-dB compression point of approximately -35 dBm. This saturation, coming as a result of either LNA and/or detector saturation, should not present any issues for a passive thermal imaging system, as signal strengths for the desired signals lie close to the thermal noise floor which is located well below these signal levels.

The improvement in system responsivity as a result of adding the LNA to the stand-alone detector is shown in Fig. ?? as a function of frequency. For the sake of comparison, the frequency response of the stand-alone LNA is also including, demonstrating that the observed system improvement exceeds that expected from the LNA measurements alone by several dB around the center frequency of 80-90 GHz, and by almost 10 dB at lower
4.3 Fabrication and Measurement Results

Fig. 4.22: Measured total power radiometer responsivity and NEP over frequency.

Fig. 4.23: Measured total power radiometer responsivity and NEP at 88GHz as a function of input power.
4.3 Fabrication and Measurement Results

Fig. 4.24: The measured receiver responsivity improvement due to the addition of the LNA compared with the stand-alone detector. The measured gain results of the discrete LNA test structure, from both VNA and NFA measurements, are also shown.

Frequency. This can be attributed to improved inter-stage matching between the LNA and the detector, as well as to reduced insertion loss for the transformer performing single-ended to differential conversion.

4.3.3.4 Dicke Radiometer

The Dicke radiometer places an SPDT switch at the input to the receiver that will introduce a signal degradation equal to the insertion loss of the stand-alone SPDT switch, previously shown in Fig. 4.13. The signal loss will degrade the system responsivity and consequently the NEP. This degradation in system sensitivity acceptable due to the elimination of low-frequency noise as a result of the SPDT switch’s ability to perform noise chopping to mitigate the contribution of 1/f noise at the receiver output. Fig. 4.25 shows the receiver responsivity and NEP, with a peak responsivity of approximately 90 kV/W, and an NEP of 0.2 pW/√Hz. The 3dB bandwidth is unchanged at 81-93 GHz.

The responsivity is approximately 40% that of the receiver without SPDT, as shown in Fig. 4.26, which corresponds to an approximate 4dB drop. The receiver responsivity drop due to the inclusion of the SPDT switch
Fig. 4.25: Measured responsivity and NEP over frequency of the receiver with SPDT switch.

Fig. 4.26: Comparison of receive performance with and without the input SPDT switch.
versus frequency is compared with the measured SPDT losses in Fig. 4.26. The Dicke receiver measurements were also carried out with the SPDT switch in isolation mode, providing approximately 28 dB isolation.

Finally, Fig. 4.28 shows the measured performance of the Dicke radiometer as a function of the LNA power supply voltage (top curve) and temperature (bottom curve). Variation of the LNA power-supply voltage results in significant system gain variation when compared to changes in gain due to the detector power-supply (not shown here). The latter remain below 1 dB over the same power-supply range. When the LNA is biased from 1.4 V instead of 1.2 V, the receiver responsivity increases by 3 dB. At 2 V, the improvement is 9 dB. Degradation due to temperature variation impacts all blocks, with SPDT switch losses increasing, and the LNA gain and detector responsivity decreasing at high temperature. There is a fairly linear (in dB) decrease in system responsivity as a result of increased temperature, with a 3.4-dB decrease at 50 °C, and a 13-dB drop-off at 125 °C.
4.4. Performance Summary and Comparison

This chapter has presented the design and integration of W-band total power and Dicke-switched radiometers in a bulk 65-nm CMOS process. The Dicke radiometer chip, occupying only 0.41 mm\(^2\) and consuming less than 33 mA from 1.2 V, is the first W-band passive imager reported in CMOS. It consists of the highest reported gain CMOS LNA in the W-band with over 27 dB gain and 13 GHz bandwidth, a differential square-law detector, and a W-band SPDT switch with 4 dB loss. The peak responsivity is greater than 90 kV/W and the NEP is less than 0.2

<table>
<thead>
<tr>
<th></th>
<th>Total Power Radiometer</th>
<th>Dicke-switched Radiometer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Responsivity</td>
<td>220 kV/W</td>
<td>90 kV/W</td>
</tr>
<tr>
<td>Output Noise (@ 400 kHz)</td>
<td>24 nV/√Hz</td>
<td>24 nV/√Hz</td>
</tr>
<tr>
<td>NEP</td>
<td>&lt; 0.1 pW/√Hz</td>
<td>&lt; 0.2 pW/√Hz</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>81-93 GHz</td>
<td>81-93 GHz</td>
</tr>
<tr>
<td>NETD (τ = 30 mS)</td>
<td>4.4</td>
<td>9.86</td>
</tr>
<tr>
<td>Power (@ 1.2V)</td>
<td>38.4 mW (32 mA)</td>
<td>38.4 mW (32 mA)</td>
</tr>
<tr>
<td>Size</td>
<td>0.665x0.47 = 0.31 mm(^2)</td>
<td>0.865x0.47 = 0.41 mm(^2)</td>
</tr>
</tbody>
</table>
Table 4.2: W-Band Radiometer Comparison.

<table>
<thead>
<tr>
<th>Ref, year</th>
<th>NETD [K]</th>
<th>Frequency [GHz]</th>
<th>Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>This work</td>
<td>4.4</td>
<td>81-93 GHz</td>
<td>65-nm CMOS LNA+detector</td>
</tr>
<tr>
<td>This work</td>
<td>9.86</td>
<td>81-93 GHz</td>
<td>65-nm CMOS SPDT+LNA+detector</td>
</tr>
<tr>
<td>[16], 2009</td>
<td>0.69</td>
<td>83-103 GHz</td>
<td>0.12 μm SiGe BiCMOS LNA+detector</td>
</tr>
<tr>
<td>[16], 2009</td>
<td>0.83</td>
<td>84-99 GHz</td>
<td>0.12 μm SiGe BiCMOS SPDT+LNA+detector</td>
</tr>
<tr>
<td>[11], 2007</td>
<td>0.32</td>
<td>91-97 GHz</td>
<td>InAlGaAs LNA+Mixer MMIC</td>
</tr>
<tr>
<td>[15], 2007</td>
<td>0.8</td>
<td>80-100 GHz</td>
<td>InP LNA, AlSb-heterostruct diode</td>
</tr>
</tbody>
</table>

pW/√Hz around the center frequency of 86 GHz. When tested without the added losses of the SPDT switch, as a total power radiometer, the receiver shows a responsivity above 200 kV/W and an NEP below 0.1 pW/√Hz. The performance of the radiometers is summarized in Table 4.1. The NETD results, calculated using equation 2.5, include a factor of 2 increase from (external) mechanical noise-chopping for the case of the total power radiometer and from electronic noise-chopping for the Dicke-switched radiometer. An integration time of 30 mS is used as a typical value corresponding to video imaging systems (30 frames per second).

A comparison of this work with other published W-band radiometers is presented in Table 4.2. This table demonstrates that the current state-of-the-art CMOS results are 5-10x behind the cutting-edge of SiGe or III/V results, and the desired 1 K temperature resolution. It is worth noting that the works shown in [11, 15] are multi-chip solutions realized in highly specialized technologies that may have difficulties reaching the yield and reliability expected from commercial products. There is significant cost associated with using these technologies and requiring separate dies for each sub-circuit. The source of the performance advantage shown by [15] is dominated by the highly responsive and low-noise diode that they implement. The InP LNA in that system achieves similar gain to the CMOS LNA in this work, while maintaining a lower noise-figure, but the relatively low responsivity and high-noise of the CMOS detector limits the achievable performance in comparison.

The high performance results shown in [16] are similarly due to the performance of the SiGe HBT detector circuit compared with the CMOS detector. The other system components offer comparable performance, with their SPDT switch having slightly lower loss, while their LNA has lower gain and higher noise figure than the CMOS LNA from this work.

The gap between this work in CMOS and the results in other technologies should be readily closed through optimization of the RF-path, either from a reduction of SPDT losses, or an increase in LNA gain. The responsivity
improvement presented in Fig. 4.28 due to an increase of the LNA operating voltage would lead to a factor of 8 reduction in NETD, providing sub 1 K from the total power radiometer, and a 1-2 K NETD for the Dicke-switching radiometer.

The integration of mm-wave passive imagers in CMOS technologies is a natural progression from the discrete and III/V MMIC imagers that are currently in use. The yield, economies of scale, and potential for large wafer-scale integration, all make CMOS a viable alternative. To date, the limited gain and large noise figure of W-band CMOS circuits have limited their attractiveness for imaging applications. However, these results demonstrate that CMOS technology has reached a stage of maturity and competitiveness that opens entirely new opportunities.
Conclusion

The focus of this thesis has been the design and implementation of CMOS mm-wave switches, attenuators, and circuits for application in mm-wave imagers and transceivers. While the use of switches at these frequencies is relatively common-place in III/V technologies, their use in CMOS systems is relatively new, and represents an attractive option for highly-integrated imagers and transceivers. Designs for SPST, SPDT, and digitally-controlled variable attenuators are presented. Finally, a fully-integrated W-band imager in a 65-nm bulk CMOS process is presented. Deeply scaled nm-CMOS, such as 65-nm CMOS, represents an excellent candidate for integrating low-loss, high-isolation passive switches, along with high-performance, low-noise circuits, all operating in the mm-wave regime.

5.1. Contributions

This thesis makes several contributions to the field of CMOS mm-wave design, including:

- The design and fabrication of mm-wave traveling-wave SPST switches. Transistor parameters are extracted for a given process technology and are used to provide simple predictive models to guide switch design. An SPST switch is implemented and characterized showing excellent performance beyond the W-band, with 1.6 dB loss and 30 dB isolation, comparing favourably with competing switches implemented in III/V technologies.

- The novel implementation of digitally-controlled mm-wave variable attenuators using binary-weighted selective gate biasing is presented. A wide dynamic-range, well-matched, wide-band variable attenuator is presented operating in the W-band with an attenuation range of 4 to 30 dB in 63 digital control steps.
• SPDT switch design using traveling-wave SPST switches is described. Two SPDT switches operating in the W- and D- band respectively were implemented, showing excellent performance up to 170GHz with less than 4dB loss at their center frequency. These switches represent the highest frequency switches demonstrated in any silicon technology.

• A high-performance W-band passive imager was implemented. The system represents the highest frequency of operation and highest level of integration passive imager reported in CMOS. The system integrates a W-band SPDT switch, a square-wave W-band detector, and a high-gain, low-noise amplifier. The integrated LNA has the highest reported gain for any W-band amplifier in CMOS.

5.2. Future Work

The integration of the on-chip SPDT switch is critical for over-coming any performance issues related to low-frequency $1/f$ noise in the receiver. Unfortunately, the loss of such a switch not only decreases the responsivity of the system, but also directly degrades the noise-figure of the RF-path. Research is warranted to investigate techniques for mitigating this issue, including:

• Reducing the amount that the SPDT switch loss contributes to noise degradation by placing the SPDT switch after a few RF-gain stages.

• Examine the possibility of using active switching as a means to avoid the loss of passive SPDT switches.

This type of improvement, particularly the second option, would be a significant enhancement for this type of system. The implementation of noise-chopping in passive imagers is often done externally using off-chip mechanical chopping because it does not degrade nominal performance, but this can significantly complicate the system design and increase system costs and power consumption. Alternatively, chopping is eliminated altogether [52] to avoid the larger system-level impacts, but this adds significant noise and stability requirements to the RF pre-amplifiers and the detectors themselves. Implementing the second option described above may be able to completely eliminate any performance degradation from electronic noise chopping, thus allowing the feature to be potentially included for "free".
Even without significant changes to the current W-band passive receiver topology, immediate system improvements could be made by optimizing the switch design to improve insertion loss. Recent publications of CMOS mm-wave SPDT switches [43] have shown topologies that may offer the possibility for performance improvement, specifically in the achievable insertion loss.

Additionally, the overall system performance could benefit from increasing the performance of the LNA. Recent publications, such as [53, 54], examine the prospect of operating telescopic cascode stages from powersupplies above the nominal core transistor voltage. This is done using deep n-well isolation structures, and the usual concerns regarding oxide or junction reliability issues are being examined with some promising results. In these deeply-scaled CMOS technologies, the reduced transistor $V_{DS}$ from stacked topologies seriously degrade the gain and NF of an amplifier, and increasing the power-supply would drastically improve system performance. Operating the current amplifier from 1.4V (instead of 1.2V) provides a 3-4dB improvement in gain, and just less than 0.5dB improvement in noise figure. At the very least, the addition of a few extra gain stages could provide 5-10dB more gain, drastically improving system performance.

Finally, the pursuit of larger system integration is important. For the benefits of using CMOS or silicon technologies to be realized, large system integration is required in order to minimize the number of off-chip components, and reduce system-level power consumption. This option could be pursued through the integration of multiple channels, performing either RF-path signal control using RF phase-shifters, or base-band signal combining using digital analysis and calibration.

### 5.3. Selected Publications


3. *(Submitted for publication with invitation)*


[33] M.-C. Yeh, Z.-M. Tsai, and H. Wang, “A miniature DC-to-50 GHz CMOS SPDT distributed switch,” in

technique for de-embedding noise parameters,” in Proceedings of IEEE Int. Conference on Microelectronic
Test Structures, Mar. 2007.


Models: Gateway to Modern CMOS Design,” in Proceedings of the 2004 IEEE Internation Conference on

[37] D. Kelly, “CMOS RF switch design and applications,” in CSICS, Short Course: ‘RF and High Speed CMOS’,
Nov. 2006.

[38] T. Dickson, M.-A. LaCroix, S. Boret, D. Gloria, R. Beerkens, and S. Voinigescu, “30-100 GHz Inductors
123–133, 2005.


