Coaxial Cable Equalization Techniques at 50-110 Gbps

By

Andreea Balteanu

A thesis submitted in conformity with the requirements for the degree of Master of Applied Science
Graduate Department of Electrical and Computer Engineering
University of Toronto

© Andreea Balteanu, 2010
Coaxial Cable Equalization Techniques at 50-110 Gbps

Andreea Balteanu

Master of Applied Science, 2010
Graduate Department of Electrical and Computer Engineering
University of Toronto

Abstract

Next generation communication systems are reaching 110Gbps rates. At these frequencies, the skin effect and dielectric loss of copper cables cause inter-symbol interference (ISI) and frequency dependent loss, severely limiting the channel bandwidth. In this thesis, different methods for alleviating ISI are explored. The design of the critical blocks of an adaptive channel equalizer with up to two times oversampling are presented.

The circuits were fabricated in a 0.13μm SiGe BiCMOS technology. The linear, adaptive equalizer operates up to 70Gbps and its measured S-parameters exhibit a single-ended peak gain of 12.2dB at 52GHz, allowing for 31dB of peaking between DC and 52GHz. Equalization is demonstrated experimentally at 59Gbps for a cable loss of 17.9dB. These results make it the fastest receive equalizer published to date. A retiming flip-flop operating between 72 and 118 GHz, the highest reported in silicon, is also designed and characterized, showing less than 500-fs jitter.
Acknowledgements

Foremost, I would like to thank Professor Sorin Voinigescu for his guidance and supervision. His knowledge, dedication and hands-on approach to research have taught me a great deal throughout these past two years.

I would like to thank all my colleagues and friends in BA4182 who made things bearable during the all nighters: Ricardo Aroca, Adam Hart, Mehdi Khanpour, Ekaterina Laskin, Sean Nicolson, Ioannis Sarkas, Shahriar Shahramian, Alexander Tomkins and Kenneth Yau. I would especially like to thank Ricardo and Ken for helping me measure and Ioannis for moral support.

I would also like to thank Prf. Johns, Prf. Hatzinakos, and Prf. Sheikholeslami for serving on the supervising committee for this thesis. This work would not have been possible without the generous support of the National Science and Engineering Research Council (NSERC), STMicroelectronics and Gennum Corporation. I also thank Canadian Microelectronics Corporation (CMC) for providing the CAD tools and Jaro Pristupa for his impeccable support.

Most of all, I would like to thank my fabulous parents, Liliana and Florinel for their love and support.
Contents

Abstract ........................................................................................................................................... ii
Acknowledgements ........................................................................................................................ iii
List of Tables .................................................................................................................................. vi
List of Figures ............................................................................................................................... vii
1 Introduction .......................................................................................................................... 1
  1.1 Motivation .................................................................................................................... 1
  1.2 Cable Characteristics ................................................................................................. 1
  1.3 Equalizer Topologies ................................................................................................. 5
  1.4 Technology Overview .............................................................................................. 9
  1.5 Outline ......................................................................................................................... 9
2 Equalizer Design ................................................................................................................ 10
  2.1 Equalizer Stage ........................................................................................................... 11
  2.2 Equalizer Input Buffers .............................................................................................. 14
  2.3 Equalizer Input Matching ........................................................................................... 16
  2.4 Equalizer Output Buffers ............................................................................................ 17
  2.5 Control Stage .............................................................................................................. 19
  2.6 Equalizer Simulation Results ...................................................................................... 20
3 Retimer Design ................................................................................................................ 22
  3.1 Background ................................................................................................................ 22
  3.2 Retimer Block Diagram .............................................................................................. 23
  3.3 Retimer Latch Design ................................................................................................. 24
  3.4 Retimer Output Buffers .............................................................................................. 31
  3.5 Simulation Results ...................................................................................................... 33
  3.6 Test Chip ...................................................................................................................... 37
4 Equalizer Fabrication and Experimental Results ............................................................... 39
  4.1 Test Chip ..................................................................................................................... 39
  4.2 S Parameter Measurements ........................................................................................ 40
  4.3 Time Domain Measurements ...................................................................................... 44
  4.4 Performance Comparisons .......................................................................................... 55
5 Retimer Fabrication and Experimental Results ................................................................. 59
  5.1 Measurement Setup .................................................................................................... 61
  5.2 Measurement Results .................................................................................................. 63
  5.3 Performance Comparisons .......................................................................................... 67
6 Conclusions ........................................................................................................................ 69
  6.1 Contributions .............................................................................................................. 70
  6.2 Future Work ................................................................................................................ 70
References ..................................................................................................................................... 71
 Appendix ....................................................................................................................................... 76
List of Tables

Table 4-1: Comparison of equalizer with previously published work ........................................ 55
Table 5-1: Pad description for the retimer test circuit ................................................................. 59
Table 5-2: Retimer performance comparison with previously published work. ....................... 67
List of Figures

Figure 1.1: A NRZ signal after (a) an infinite bandwidth channel and (b) a finite-bandwidth channel. ........................................................................................................................................... 2
Figure 1.2: Measurements of the cables used in the equalization experiments. ......................... 3
Figure 1.3: Measured group delay for cables used in equalization experiment.............................. 4
Figure 1.4: An equalizer system consisting of a three tap FFE and a two tap DFE. ...................... 6
Figure 1.5: Examples of Bode equalizers in which (a) low frequency gain is adjusted, (b) a flat response path is summed with a peaking path, and (c) high frequency gain is adjusted to achieve the desired response. ........................................................................................................................................... 8
Figure 1.6: Proposed equalizer with a one tap DFE. ...................................................................... 9
Figure 2.1: Equalizer response to varying cable lengths. ............................................................. 10
Figure 2.2: Equalizer stage schematic. .......................................................................................... 11
Figure 2.3: Equalizer block diagram............................................................................................. 13
Figure 2.4: Circuit schematic of the equalizer input buffers. ......................................................... 14
Figure 2.5: Input buffers AC response.......................................................................................... 15
Figure 2.6: Input 50 Ω matching.................................................................................................... 16
Figure 2.7: 50-Ω output driver....................................................................................................... 17
Figure 2.8: Output buffer AC response.......................................................................................... 18
Figure 2.9: Control circuit schematic........................................................................................... 19
Figure 2.10: Control circuit simulation........................................................................................ 19
Figure 2.11: Simulated S₂₁ of the equalizer ................................................................................ 20
Figure 2.12: Simulated output eye using a 40-Gbps PRBS input sequence................................. 21
Figure 2.13: Simulated output eye using an 80-Gbps PRBS input sequence............................... 21
Figure 3.1: Retimer block diagram consisting of the Master – Slave D Flip – Flop and output buffers................................................................................................................................. 23
Figure 3.2: Latch topologies in BiCMOS technology................................................................. 24
Figure 3.3: Half circuit for the BiCMOS latch topologies............................................................ 25
Figure 3.4: Simulated 80-Gbps eye diagrams for the (a) HBT-HBT (b) BiCMOS (c) HBT-MOS and (d) MOS-MOS latch topologies. ........................................................................................................... 28
Figure 3.5: Fabricated latch using the HBT-HBT topology ......................................................... 29
Figure 3.6: Retimer output buffers: (a) first buffer and (b) final 50-Ω buffer ........................................... 31
Figure 3.7: Emitter followers used to (a) cascade output buffers and (b) provide proper DC levels for latch clock inputs .................................................................................................................... 32
Figure 3.8: A 125-Gbps signal at the output of the retimer when retimed at 125GHz ............................... 33
Figure 3.9: A 125-Gbps signal after the 50-Ω output buffer when retimed at 125GHz .............................. 33
Figure 3.10: A 62.5-Gbps signal at the output of the retimer when retimed at 125GHz ............................ 34
Figure 3.11: A 62.5-Gbps signal after the 50-Ω output buffer when retimed at 125GHz ......................... 34
Figure 3.12: Retimer simulations with 100-Gbps input data and 100-GHz retimer clock ............................ 35
Figure 3.13: Retimer simulations with 50-Gbps input data and 100-GHz retimer clock ......................... 36
Figure 3.14: The retimer test chip block diagram ....................................................................................... 37
Figure 4.1: Photomicrograph of the equalizer ............................................................................................ 39
Figure 4.2: Test setup for S-parameter measurements ............................................................................... 40
Figure 4.3: Measured and simulated S21 of the equalizer ......................................................................... 41
Figure 4.4: Measured and simulated S11 and S22 of the equalizer ............................................................ 42
Figure 4.5: Test setup for S parameter measurements using the cables and equalizer ............................ 42
Figure 4.6: S21 measurements using the V cable ..................................................................................... 43
Figure 4.7: S21 measurements using the SMA cable ................................................................................ 43
Figure 4.8: S21 measurements using the Belden cable ............................................................................. 44
Figure 4.9: Schematic of the test setup for time domain measurements ..................................................... 45
Figure 4.10: Picture of the test setup for time domain measurements ...................................................... 45
Figure 4.11: The measured signal at 59.2 Gbps before (top) and after the 1.8-m cable (bottom) .......... 46
Figure 4.12: Measured 59.2-Gbps data at the output of the equalizer after 17.9 dB of channel loss ........ 46
Figure 4.13: Output of the equalizer at 50.6 Gbps when equalizing a 1-m long V cable ......................... 47
Figure 4.14: Output of the equalizer at 60 Gbps when equalizing a 1-m long V cable ......................... 47
Figure 4.15: Equalizer output at 70 Gbps after a 1-m long V cable ......................................................... 48
Figure 4.16: The differential input to the equalizer after a 1-m V cable ................................................... 49
Figure 4.17: Test setup for time domain measurements using the driver ................................................ 50
Figure 4.18: Picture of the test setup for time domain measurements using the driver ........................... 50
Figure 4.19: A 30-Gbps signal after a 10 m cable. The channel loss at 15 GHz is -15.8 dB .......... 51
Figure 4.20: The 30-Gbps signal after the equalizer ................................................................................. 51
Figure 4.21: A 34.6-Gbps signal after a 10-m cable with channel loss of 26.4 dB at 17 GHz..... 52
Figure 4.22: A 34.6-Gbps signal after the equalizer for a channel loss 26.4 dB of at 17 GHz. ... 52
Figure 4.23: Equalizer output at 38.3 Gbps when all stages are set to non-peaking mode. ....... 53
Figure 4.24: Equalizer output at 38.3 Gbps when three stages are set to non-peaking mode. ..... 53
Figure 4.25: Equalizer output at 38.3 Gbps when two stages are set to non-peaking mode. ...... 53
Figure 4.26: Equalizer output at 38.3 Gbps when two stages are set to non-peaking mode. ..... 54
Figure 4.27: Data rate versus channel loss for the equalizers described in Table 4-1.......... 57
Figure 4.28: Figure of merit for different for the equalizers described in Table 4-1........... 58
Figure 5.1: Photomicrograph of the retimer test chip. .......................................................... 60
Figure 5.2: Retimer Test Setup Diagram. ........................................................................... 61
Figure 5.3: Picture of the retimer Measurement Setup. ......................................................... 62
Figure 5.4: Improvement in jitter performance due to retiming. ......................................... 63
Figure 5.5: Eye diagrams for a 39-Gbps signal when measured with 67-GHz and 110-GHz
probes. ........................................................................................................................................... 64
Figure 5.6: Full spectrum of the 59-Gbps signal retimed at 118 Gbps................................. 65
Figure 5.7: Zoomed in spectrum of the 59-Gbps signal retimed at 118 Gbps..................... 66
Figure 5.8: Measured versus ideal 2^7-1 PRBS signal. ......................................................... 66
Figure 5.9: The clock speed as a function of technology f_T for the retimers described in Table
5-2. ................................................................................................................................................ 68
1 Introduction

1.1 Motivation

Consumer demands have fuelled the growth in high speed communications while scaling of semiconductor technologies have allowed for rapid improvement in computing and data transmission capabilities. One of the bottlenecks now is the limitations of the channel bandwidth. Future generations of the High Definition Television (HDTV) standard at 6 Gbps and beyond have triggered the need to transmit increasingly higher data rates over existing coaxial cable connections originally designed for 1.5 Gbps operation. When several 6-Gbps HDTV signals are multiplexed, the aggregate serial data rate can quickly rise up to 50 Gbps. Many physical effects such as skin effect, dielectric loss and reflections associated with impedance mismatches severely limit the ability of the channel to function in the gigahertz range. Although optical links can be used to increase communication speeds, it is more cost effective to improve the operation of the currently installed coaxial cable infrastructure.

It has been shown that equalizers can be used to improve transmission rates over bandwidth limited channels when placed in the transmitter [2, 26], receiver [4, 15, 18, 11], or in both the transmitter and receiver [5]. Since the exact channel characteristics are not known, using an adaptive equalizer in the receiver is desirable in order to compensate for actual channel characteristics.

1.2 Cable Characteristics

The finite bandwidth of the transmission mediums such as copper interconnects gives rise to a phenomenon called intersymbol interference (ISI) in which the signal level of the current bit is affected by the values of the previously transmitted bits (postcursor ISI) and the values of the succeeding bits (precursor ISI). A transmission system typically has a latency of many bits, hence precursor ISI does not violate causality. A graphical depiction of a non-return to zero (NRZ) signal transmitted over an infinite and a finite bandwidth channel can be seen in
Figure 1.1. The ISI degrades the eye at the receiver and, depending on the severity, the eye can even be closed making data recovery impossible.

It is not known beforehand what cable length or quality the user will employ, therefore several cables must be characterized. For the purpose of this experiment, three cables of different qualities and lengths were measured: a 10-m Belden cable with two BNC-to-K transitions and two K-to-V transitions, a 1.8-m SMA cable consisting of two cascaded 90-cm SMA cables with K-to-V transitions on each side and one K-to-K connector, and a 1-m long V cable. The cable frequency response can be seen in Figure 1.2. As expected, the cable exhibits a linear loss with frequency.
The cable loss characteristics can be modeled as a function of frequency [44]:

\[ C(f) = e^{-k_s l(1+j) \sqrt{f}} - k_d f \]  

(1.1)

where \( k_s \) is the skin effect constant, \( k_d \) is the dielectric constant, \( f \) is frequency and \( l \) is the cable length.

While the cable bandwidth causes vertical distortion in the eye diagram, horizontal distortion in the form of data-dependent jitter occurs when the cable does not have a linear phase response. Phase linearity is the variation in group delay with frequency given by [40]:

\[ \tau(\omega) = -\frac{d\Phi}{d\omega} \]  

(1.2)

Where \( \tau(\omega) \) is the frequency dependent group delay, \( \Phi \) is the phase in radians and \( \omega \) is the radian frequency. For a given cable length, the delay can be approximated using [36]:

\[ Delay \approx \frac{l \times \sqrt{\varepsilon_r}}{c} \]  

(1.3)
where \( l \) is the cable length, \( c \) is the speed of light and \( \varepsilon_r \) is the relative permittivity of the dielectric. For the 1-m V cable, the dielectric is low density polytetrafluoroethylene (PTFF), therefore \( \varepsilon_r = 1.5 \) [30] corresponding to a delay of 4.1 ns. The 1.8-m cable has a dielectric filled with Teflon, hence \( \varepsilon_r = 2.08 \) [36] corresponding to a delay of 8.7 ns. The 10-m cable uses polyethylene as the dielectric corresponding to a permittivity of 2.25 [36] resulting in a group delay of 50 ns. The group delay for the cables was calculated using the S parameter data which were taken at 4 MHz intervals from 1 GHz to 50 GHz. The \( S_{21} \) phase was unwrapped and then the derivative with respect to frequency was taken. The measured cable delay is plotted in Figure 1.3. At low frequencies, the group delay for the 1-m V cable is roughly 4.1 ns and the group delay for the 1.8-m SMA cable is 7.85 ns. These measurements vary slightly from the hand calculations because the dielectric is not constant throughout the entire cable and hence the relative permittivity varies. Above 25 GHz, the group delay measurements for the 1.8-m SMA cable are no longer accurate due to the high loss of the cable, and the sensitivity of the equipment. In addition, as the frequency and cable length increase, measurements have to be taken at much finer frequency steps for the group delay to be accurate. For this reason, the delay of the 10-m cable could not be measured.

Figure 1.3: Measured group delay for cables used in equalization experiment.
In order to limit the data dependent jitter, a group delay variation of less than 10% of the bit period (UI) over the desired bandwidth is needed [40]. The group delay variation ($\Delta \tau$) for the 1-m V cable is 435 ps (which corresponds to 230 GHz when using the 10% rule) up to 50 GHz hence there is no need for phase equalization at data rates below 50 GHz. The 1.8-m SMA cable has a $\Delta \tau$ of 600 ps up to 25 GHz, allowing operation up to 167 GHz using the 10% rule.

1.3 Equalizer Topologies

Unlike noise, which is unpredictable, ISI depends on the data as well as the transmission medium, making it deterministic and hence reversible. An equalizer can be used to mitigate the ISI and improve the effective bandwidth for a channel. It is well established that the highest theoretical performance can be achieved using maximum likelihood sequence estimation (MLSE) [14, 29, 40]. The continuous time approach requires an analog to digital converter (ADC) at the receiver after which a digital signal processor (DSP) is used. Although ADCs functioning at above 40 GSamples/s [8] exist and such a system has been proven to work at 10 Gbps [25], designing the high speed ADCs is complex and requires a large chip area making this approach not suitable for high speed communication. In the alternate, discrete time approach, the signal is sampled using a track and hold amplifier after which the data is processed using analog techniques. High speed track and hold amplifiers have been proven to work at above 40 GSamples/s [42], however their power and size requirements also make this approach undesirable.

A more common approach is the use of a filter before the decision circuit. The filter must be adaptive in order to be able to function without prior knowledge of the channel. A common implementation is a feed-forward equalizer (FFE), also known as a transversal filter or finite impulse response (FIR) filter. In this implementation, the input is feed into a series of delay lines the output of which is multiplied by a pre-determined coefficient after which all the outputs are summed together and passed to the decision circuit. The coefficients are determined based on the transmission channel. When the delay lines are equivalent to one bit period, the system is known as a synchronous equalizer. A fractional equalizer is when the delays are less than one bit period, the advantage being that it improves the horizontal eye opening, not just the vertical eye opening as is the case with the synchronous equalizer [40]. The FFE can be used to mitigate precursor ISI
while a decision-feedback equalizer (DFE) can be used to mitigate postcursor ISI without amplifying noise. A system consisting of a three tap FFE and a two tap DFE can be seen in Figure 1.4 where $\alpha_{1,5}$ are amplification terms. The DFE consists of a feedback path from the output of the decision circuit back to the summation node. If the previous bit was a one, the amplitude of the bit currently under consideration is reduced by $\alpha_4$ and if the previous bit was a zero, the amplitude is increased by $\alpha_4$. Non-linear effects associated with impedance mismatches due to chip packages and connectors can be corrected using the DFE. The combination of a FFE and DFE can address both precursor and postcursor ISI. The weighting coefficients for the FFE and DFE can be controlled using algorithms such as Least-Mean-Square and Recursive Least Square [20]. The adaptive equalizer approximates the inverse characteristic of the channel, restoring the high frequency signal and reducing ISI.

![Figure 1.4: An equalizer system consisting of a three tap FFE and a two tap DFE.](image)

The FFE can be implemented using either a digital or an analog architecture. The digital implementation however suffers from the same downsfalls as the MLSE architecture, namely the difficulty in creating a high speed ADC or track and hold amplifier. For high speed applications, the FFE is commonly implemented using a continuous time analog architecture. In [29], a continuous time approach consisting of an automatic gain control (AGC) stage followed by a FFE and a DFE is employed to achieve 10 Gbps data rates. The most challenging part in designing an analog FFE is creating wide-bandwidth delay structures. Often, and as is the case in [2, 18, 29], the delays are implemented using microstrip transmission lines. When compared to
transistor based implementations, the microstrip delay elements have higher bandwidth, zero power dissipation, less group delay variation, however they occupy a large area. In order to minimize area, the lines are often bent making them harder and less accurate to model. In addition, they introduce frequency dependent loss. Nevertheless a transversal filter operating at 49 Gbps was reported in [18] using a 0.18-µm SiGe BiCMOS technology.

One impediment to high speed operation for the DFE is the feedback propagation time. In [17] a look-ahead architecture is proposed which relaxes the timing constraints. The architecture makes a tentative decision assuming the previous bit was “zero” and another decision assuming that the previous bit was a “one”. The correct result is then selected using a shorter feedback look. This architecture however employs three flip flops in order to make the correct decision. At high frequencies, this becomes quite taxing on the clock distribution network. In [15] two of the flip flops are replaced with a cascade of three ECL buffers that act as slicers thus reducing the complexity of the clock path. Data rates of up to 40 Gbps were achieved using this architecture.

In order to alleviate the large area requirements due to the microstrip delay lines in the FFE, a frequency domain adaptive equalizer is proposed, also known as a Bode equalizer. The equalizer functions by providing the inverse of the channel response, namely by providing peaking at high frequencies in order to alleviate the channel losses. Several such equalizers have been published. In [32] a Cherry Hopper topology was employed to realize the adjustable equalizer. The high frequency peaking was constant while the low frequency gain can be adjusted in order to generate the required inverse channel response as seen in Figure 1.5.a. Another approach used in [49] is to have a flat response amplifier in parallel with a tuned amplifier as seen in Figure 1.5.b. The difficulty in such an approach is to match the delay between the flat response path and the tuned path. Mismatches in these delays further reduced the eye horizontal opening and thus decrease the maximum achievable bandwidth. A better approach is to combine the flat response path and the tuned path into one stage [4, 9, 19, 34, 44] as seen in Figure 1.5.c. This approach is further developed in Chapter 2.
Figure 1.5: Examples of Bode equalizers in which (a) low frequency gain is adjusted, (b) a flat response path is summed with a peaking path, and (c) high frequency gain is adjusted to achieve the desired response.

As is the case with many equalizers, the output eye exhibits significant jitter (time variation in the signal edge) and therefore a retimer should be used at the output of the equalizer to reduce jitter. The retimer can also be used in a feedback configuration in order to implement a one tap DFE as seen in Figure 1.6. This decreases the bandwidth due to the feedback path and the addition of the summation node at the input of the retimer. A look-ahead topology as proposed in [15] can be used to further increase the bandwidth. The DFE provides further equalization without amplifying the noise while the retiming reduces the jitter of the signal. If the clock signal is recovered from the transmitted signal using a clock and data recovery system (CDR), the jitter is further reduced by ensuring that the retimer is triggered at the center of the eye, regardless of drift in the transmitter frequency. In order to measure the effect of the Bode equalizer and the maximum operating frequency of the retimer, the two circuits were fabricated separately.
1.4 Technology Overview

The circuits discussed in this thesis were designed in STMicroelectronics’ 0.13-μm SiGe BiCMOS9MW technology. The process is dedicated to millimetre-wave applications and has a thick copper back end intended for low-loss transmission lines and inductors. High quality factor metal-insulator-metal (MIM) capacitors are also provided. The HBT transistors have unity gain frequency ($f_T$) of 240 GHz and a maximum frequency of oscillation ($f_{MAX}$) of 270 GHz when biased at their peak $f_T$ current density ($I_{peak\ f_T}$) of 2 mA per micron of emitter length [3]. Measurements show a current gain ($\beta$) of 282 and a base-emitter voltage $V_{BE}$ of 0.91 V when the HBT is biased at its peak $f_T$ current density [3]. The n-MOSFET devices have an $f_T$ of 90 GHz when biased at 0.3 mA per micron of gate width [13].

1.5 Outline

The thesis concentrates on the design and measurement of a receive equalizer and retimer which were fabricated as separate chips for testing purposes. In Chapter 2, the equalizer architecture is presented followed by the retimer design in Chapter 3. Equalizer and retimer measurement results are presented in Chapter 4 and 5 respectively. Conclusions are offered in Chapter 6. Additional measurement results can be seen in Appendix A.
2 Equalizer Design

Equalization can be achieved by implementing a circuit whose frequency response is the inverse of the cable response seen in (1.1). This can be achieved by superposition of two functions, one that has constant gain over frequency and one whose gain increases with frequency:

\[ H(s) = G_{DC} + G_{HF} \frac{(s+\alpha_1)(s+\alpha_2)\cdots(s+\alpha_n)}{(s+\gamma_1)(s+\gamma_2)\cdots(s+\gamma_n)(s+\gamma_{n+1})} \]  

(2.1)

where \(G_{DC}\) is the DC gain, \(G_{HF}\) is a scaling constant for the frequency dependent gain term, and \(\alpha_n\) and \(\gamma_n\) are the zeros and poles of the frequency dependent term, chosen to best match the inverse of the cable response. A graphical depiction of the equalizer response is shown in Figure 2.1.

The equalizer bandwidth must be made sufficiently wide so that it does not further distort the signal, however too large a bandwidth results in too much noise getting passed to the decision circuit reducing the signal-to-noise ratio (SNR) of the system. The optimum 3-dB bandwidth is between 60% and 70% of the bit rate [40] meaning that an equalizer with 50-GHz bandwidth can be used for up to 70 Gbps data rates. By adding 30 dB of adjustable peaking at roughly 50 GHz, the 3-dB bandwidth can be extended to above 40 GHz for the 1-m cable and above 30 GHz for the 1.8-cm cable.
2.1 Equalizer Stage

A gain of 30 dB cannot be obtained from a single stage, however the effort can be broken over multiple equalization stages. The equalization function was realized physically with the circuit illustrated in Figure 2.2 where all transistors have 0.13-µm emitter width and Q1-4 have 2 µm emitter lengths. The equalizer stage consists of two differential transconductor stages and two Gilbert cells which act as a weighted current adder. The circuit was adapted from [44] by scaling the maximum gain frequency from 2 GHz to 50 GHz and adding inductive peaking to improve the bandwidth.

![Equalizer stage schematic](image)

Figure 2.2: Equalizer stage schematic.

The current per side at the output of the first transconductor (Q1, Q4) is given by:
while the current at the output of the second transconductor (Q2, Q3) is described by:

\[ i_2 = \frac{g_m}{(Z_{CS} \parallel \frac{Z_E}{Z})g_m + 1}v_i \]  

(2.3)

where \( g_m \) is the transconductance of Q1-4, \( Z_{CS} \) is the impedance of the current source (ideally much larger than \( R_E \) and \( Z_E \)), \( R_E \) is the emitter degeneration resistance in the first transconductor and \( Z_E \) is the frequency dependent emitter degeneration impedance in the second transconductor.

It must be noted that, in this implementation:

\[ Z_E \rightarrow R_4 \text{ as } f \rightarrow 0 \text{ Hz} \]  

(2.4)

As the frequency increases, \( Z_E \) decreases thus producing peaking at high frequencies which compensates for the cable loss. \( R_4 \) is equal to \( R_E \) (200 \( \Omega \)) to ensure that the gains of the two paths are equal at DC, regardless of the equalizer settings. In order to maximize the bandwidth, the capacitors are set to 27 fF, the smallest value allowed by the technology for MIM capacitors. The resistors \( R_1, R_2 \) and \( R_3 \) are chosen to be 100 \( \Omega \), 1 k\( \Omega \), and 10 k\( \Omega \), respectively in order to match the inverse channel response. First, the 100 \( \Omega \) resistor was chosen in order to provide the 400 mV linearity. The remaining resistors were scaled by a factor of ten in order to match the inverse channel response.

The voltage at the output of the equalizer stage can now be expressed as:

\[ v_o = -[\gamma i_1 + (1 - \gamma)i_2]Z_L \]  

(2.5)

where \( \gamma \), which varies between 0 and 1, is controlled by the differential voltage applied at the bases of the Gilbert cells and \( Z_L \) is the load impedance per side at the output of the equalizer stage. The DC gain obtained from (6) by setting \( \gamma \) to 1 is approximately:

\[ Gain_{DC} = -\frac{2R_{Lr}r_{eg_m}}{2r_e + R_E} \times Gain_{EF} = 0.86 \text{ V/V} \]  

(2.6)
where $g_m = \frac{I_C}{V_T}$. \(\text{Gain}_{\text{EF}}\) is the gain of the emitter follower stage, equal to one at DC, and \(r_e\) is the emitter resistance of the transistor. For a 0.13 \(\mu\)m \(\times\) 2 \(\mu\)m device, this is about 12 \(\Omega\). The simulated gain at DC is -0.71 (-3 dB). The maximum peaking gain is obtained when \(\gamma\) is zero and reaches its maximum value when \(Z_E\) is at its minimum. The measured transistor MAG at 52 GHz is 12 dB leading to a maximum theoretical gain of 4 in the absence of emitter degeneration. However, at 52 GHz, the gain of the emitter follower stage is simulated to be 0.9. The non-zero emitter degeneration impedance \(Z_E\), further reduces the gain at 52 GHz to be:

$$\text{Gain}_{52GHz} = - \frac{2R_Lr_{eg_m}}{2r_e + Z_E} \times \text{Gain}_{\text{EF}52GHz} \approx -1.37 \frac{V}{V}$$

The simulated gain at 52 GHz is -1.4 (3 dB) which results in a total gain peaking from DC to 52 GHz of 6 dB.

The linear peak-to-peak input voltage swing per side is given by \(I_E \times R_E\) and is equal to 400 mV\(_{pp}\) in this design. All differential pair transistors are biased at 8 mA/\(\mu\)m\(^2\). The minimum bias current is limited by the minimum transistor size, the parasitic capacitance of the current source and the required bandwidth. The latter consideration is dominant in this case and imposes the minimum usable bias current of 2 mA and transistor emitter length of 2 \(\mu\)m.

Since 30 dB of peaking is needed and each stage provides 6 dB of peaking, 5 equalizer stages must be cascaded to obtain the desired frequency response. The block diagram of the equalizer is shown in Figure 2.3 and consists of five identical equalizer stages with adjustable peaking control and 50-\(\Omega\) input and output buffers.

![Equalizer block diagram](image-url)
2.2 Equalizer Input Buffers

The circuit schematic of the input buffers can be seen in Figure 2.4. Two cascaded differential stages are used to provide adequate common-mode rejection at high frequency, needed to restore a single ended input to a differential signal.

![Circuit schematic of the equalizer input buffers.](image)

Figure 2.4: Circuit schematic of the equalizer input buffers.

In order to increase the input impedance of the HBTs and reduce the signal distortion, an emitter degeneration resistance is introduced. This increases the linear voltage range to 360 mV however the trade off is gain. The gain for a differential pair with emitter degeneration is given by:

$$A_v = \frac{-R_L}{2V_T + R_E}$$  \hspace{1cm} (2.8)

where $R_L$ is the load resistance, $R_E$ is the emitter degeneration, $V_T$ is the thermal voltage and $I$ is the tail current. The buffers were designed to have unity gain. The cascaded gain for the two buffers is calculated to be 1.17 V/V which is slightly higher than unity in order to combat the
loss introduced by the emitter followers that separate them. The emitter followers are introduce in order to produce the proper input DC level for the second buffers as well as increase the bandwidth of the first buffer.

A simulation of the buffers AC response can be seen in Figure 2.5. Extraction tools are not available in this design kit, hence slight peaking is introduced at 40 GHz in order to account for layout parasitic capacitances and interconnects.

![Figure 2.5: Input buffers AC response.](image-url)
2.3 Equalizer Input Matching

The channel to be equalized, as well as the measurement equipment, has a characteristic impedance of 50 Ω, hence the input to the equalizer is matched to 50 Ω using a resistive divider and an inductor as seen in Figure 2.6.

![Figure 2.6: Input 50 Ω matching.](image)

At low frequencies, the characteristic input impedance of this system is given by:

\[
R_{\text{in}} = R_1 \parallel R_2 \parallel R_{\text{inv}} \approx R_1 \parallel R_2 \approx \frac{R_1 R_2}{R_1 + R_2}
\]  

(2.9)

where \( R_1 \) and \( R_2 \) are labelled in Figure 2.6, \( R_{\text{in}} \) is the equalizer input resistance, and \( R_{\text{inv}} \) is the input resistance to the inverter in the following stage given by:

\[
R_{\text{inv}} \approx (\beta + 1)(r_\text{e} + R_E)
\]

(2.10)

where \( \beta \) is the HBT current gain, \( r_\text{e} \) is the HBT intrinsic emitter resistance and \( R_E \) is the emitter degeneration resistance seen in Figure 2.4. The emitter degeneration resistance for the buffer is 150 Ω and \( \beta \) is around 282 [3] therefore \( R_{\text{inv}} \) is much larger than either \( R_1 \) or \( R_2 \) thus \( R_{\text{in}} \) can be simplified to \( R_1 \parallel R_2 \) as seen in (2.9). The input to the equalizer is AC coupled, hence this resistive divider also serves to set the input DC level, \( V_{\text{in}} \), for the input buffer. \( V_{\text{in}} \) is given by:

\[
V_{\text{in}} = \frac{R_2}{R_1 + R_2} V_{\text{DD}}
\]

(2.11)

Rearranging the equations as seen in (2.9) and (2.11) and setting \( R_{\text{in}} \) to 50 Ω and \( V_{\text{in}} \) to be the necessary 2.2 V results in a \( R_1 \) of 75 Ω and \( R_2 \) of 150 Ω.
\[
R_1 = \frac{R_{in}}{V_{in}} V_{DD} = \frac{50 \, \Omega}{2.2 \, V} (3.3 \, V) = 75 \, \Omega 
\]

\[
R_2 = \frac{R_1 R_{in}}{R_1 - R_{in}} = \frac{(75 \, \Omega)(50 \, \Omega)}{(75 \, \Omega) - (50 \, \Omega)} = 150 \, \Omega
\]

(2.12) 

(2.13)

At high frequencies, the buffer input impedance \( Z_{inv} \) decreases due to base-emitter and base collector capacitances reducing the overall input impedance. The 150 pH inductor, \( L \), is introduced to mitigate this term and extend the frequency range in which the input is matched to 50 \( \Omega \).

2.4 Equalizer Output Buffers

The first consideration when designing the output stage is that the output must be matched to 50 \( \Omega \) over the entire operating frequency range. The simplest way to achieve this is to use a CML inverter with a 50-\( \Omega \) load as seen in Figure 2.7.

![Figure 2.7: 50-\( \Omega \) output driver.](image)

The effective load for the buffer is 25 \( \Omega \) due to the 50-\( \Omega \) load resistor being in parallel with the 50-\( \Omega \) impedance presented by the measurement equipment. In order to achieve a 200 mV output
swing a tail current of 8 mA was chosen for the buffer. The previous equalizer stages attenuate the DC component of the signal; therefore the input to the buffer is not large enough to fully switch the HBTs. For this reason, they are biased so that the current density flowing thorough each is \( J_{\text{peak}} f_T = \frac{2 \text{mA}}{\mu \text{m}} \) when \( \text{Inp} \) and \( \text{Inn} \) are equal. The small input signal to the buffer also relaxes the linearity requirement and lowers the value required for the degeneration resistor. A 22-\( \Omega \) was chosen, however in retrospect this is too large. Assuming that the input signal to the equalizer was 400 mV, after 15 dB of attenuation through 5 stages of equalization, the signal amplitude becomes 71 mV. For an 8-mA tail current, a 10-\( \Omega \) resistor would be more than sufficient to meet linearity requirements. Peaking inductors were used order to maximize the bandwidth. The emitter followers were used in order to provide the proper common mode voltage for the buffer. The 100-\( \Omega \) resistor was introduced in order to reduce the capacitance seen at the emitter as well as to match the current tail \( V_{\text{CE}} \) to that of the current mirror and provide better matching.

![Figure 2.8: Output buffer AC response.](image)

Figure 2.8: Output buffer AC response.
2.5 Control Stage

The peaking and main signals shown in Figure 2.2 to control the equalizer stages are provided using the differential buffer seen in Figure 2.9. The buffer is controlled off chip using $V_{\text{ctrl}}$ and provides the differential signal needed to switch the equalizer from the main path to the peaking path. The large degeneration resistance is used in order to provide a linear response shown in Figure 2.9.

![Control circuit schematic](image)

Figure 2.9: Control circuit schematic.

![Control circuit simulation](image)

Figure 2.10: Control circuit simulation.
2.6 Equalizer Simulation Results

The simulated gain of the equalizer when switching all the gain from the main path to the peaking path for no stages, one stage, two stages, three stages, four stages and finally five stages, is shown in Figure 2.11. A peak gain of 12.8 dB is observed at 49 GHz for a total of 30 dB of adjustable gain.

Figure 2.11: Simulated $S_{21}$ of the equalizer.

In the case of a good quality cable, all the equalizer stages will be turned to the main path in order to not disturb the signal. Such a situation was simulated using an ideal 500 mV$_{p-p}$ single ended PRBS signal at 40 Gbps in Figure 2.12 and 80 Gbps Figure 2.13.
Figure 2.12: Simulated output eye using a 40-Gbps PRBS input sequence.

Figure 2.13: Simulated output eye using an 80-Gbps PRBS input sequence.
3 Retimer Design

3.1 Background

The rapid and continual grown in multimedia services has created an ever increasing demand for high data rate communication systems. Flip-flops are one of the most critical digital blocks and have several uses in today’s communication systems. They can be used as retimers in transmitters, as phase detectors in clock and data recovery circuits (CDR), and as decision circuits when placed at the front of a receiver. In a full-rate transceiver, the flip-flop must operate at a clock frequency equal to the data rate making it one of the highest frequency block in the system. Their maximum operating frequency can limit the system operating frequency hence the flip flop performance is critical for high speed data communication.

Several variations of the classical CML latch have been proposed in literature in order to extend the bandwidth. Double emitter followers (E²F) are used in order to extend the operating frequency to 51 GHz in [39]; this however requires the use of a higher supply voltage of -5.2 V. In [12] MOSFETs replace the clock transistors and only one set of source followers are used instead of E²F in order to reduce the supply voltage to 2.5 V, the trade off being an operating frequency of 48 GHz.

Many low voltage latch topologies have been proposed in literature. In [37], a triple-tail cell is proposed in which the differential data pair is controlled using clamp transistors whose base is connected to the clock signal and its emitter is connected to the emitters of the differential pair. When a high voltage is applied to the clamping clock transistor, it starves the current flowing through the corresponding differential pair. Unfortunately large clock signals are required in order to properly turn off the differential pair. In [22], the clock differential pair is replaced by current mirror controlled logic in order to lower the supply voltage. The increased delay on the clock path due the current mirror makes it not suitable for high frequency operation. Low voltage topologies were implemented in CMOS by removing the tail current source [6]. This however is not an option when using an HBT implementation due to the fact that the current through the HBT varies exponentially with $V_{BE}$. Small variations in the base-emitter voltage due to process variations and ground resistance lead the transistors to no longer be biased at $I_{peak} f_r$ thus
diminishing performance. Another method for lowering the supply voltage is to use a transformer to couple the signal between clock differential pair and the data transistors. This however leads to a limited operating range due to the tuned nature of the transformer.

3.2 Retimer Block Diagram

The retimer consists of two latches arranged in a master slave configuration that form a CML flip-flop. When the retimer is intended as part of the transmitter, it is placed as the last element in the chain so that the system transmits with the lowest possible jitter. However, the system must be matched to the cable impedance. Although the latch can be designed to be matched to 50 Ω, or 75 Ω as the case may be, this reduces the maximum operating frequency because a larger resistive load must be used. In order to achieve the fastest latch possible, it should be designed without matching consideration after which a series of buffers can be added to achieve the necessary output matching. This project was targeting the highest achievable operating frequency hence the output buffers were added at the expense of extra power consumption, added jitter and increased area. The retimer block diagram can be seen Figure 3.1. A cascade of two buffers is used following the retimer in order to achieve an output matching of 50 Ω. The emitter followers (EF) are necessary in order to provide the required DC operating level for the subsequent stage. The transistor level description for each block is detailed in Chapters 3.3 and 3.4. The full chip used to test the retimer is discussed in Chapter 3.6.

Figure 3.1: Retimer block diagram consisting of the Master – Slave D Flip – Flop and output buffers.
3.3 Retimer Latch Design

Due to the availability of both MOSFET and Bipolar transistors, BiCMOS technologies allow for numerous latch topologies several of which were discussed in Chapter 3.1. The topologies most suited for high speed operation, and the ones analyzed here are seen in Figure 3.2. These topologies were adapted from [12] by adding the emitter follower stage in order to increase the bandwidth.

Figure 3.2: Latch topologies in BiCMOS technology.

In order to simplify the analysis, the load resistance ($R_L$) and tail current ($I_T$) are kept constant for each design while the MOSFETs and HBTs, with the exception of the emitter followers, are
sized so that they function at their respective peak $f_T$ current density ($I_{\text{peak}f_T}$). The emitter followers are primarily used as signal buffers for the preceding stage due to their high input impedance and low output impedance. In the feedback path, they also allow for a higher $V_{DS}$ (or $V_{CE}$) for the data path MOSFETs (or HBTs) thus maximizing their $f_T$. The main obstacle to lowering the power dissipation of the latch is due to the $V_{BE}$ of the SiGe HBT which exceeds 0.9 V when the device is biased at $I_{\text{peak}f_T}$. Emitter followers in the feedback path further increase the supply voltage, hence only one set of emitter followers will be used in order to maintain the supply voltage at 3.3 V and reduce power consumption.

In Figure 3.3, the half circuit schematic of the BiCMOS latch is shown. The maximum operating speed of each topology can be compared by examining the open-circuit time constants of each of the latches. The process used to examine cascode inverters outlined in [12] can then be applied to analyze the time constant of the latches.

Figure 3.3: Half circuit for the BiCMOS latch topologies.
It can be noted that each latch is loaded by the same emitter follower stage; hence it is sufficient to compare the time constants at the input of the emitter followers to be able to compare the relative speeds of the different topologies. For this analysis, $\Delta V_{\text{MOS}}$ ($\Delta V_{\text{HBT}}$) is the voltage swing needed to switch the MOSFET (HBT) clock pairs. The time constants at the input of each emitter follower are given by:

$$
\tau_{\text{HBT-HBT}} = \frac{\Delta V_{\text{HBT}}}{I_T} \left\{ 2C_{be} + 3\left( 1 + g_{m,\text{HBT}} R_l \right) C_{bc} + C_{bc,\text{EF}} + C_{be,\text{EF}} \right\} \\
+ \frac{\Delta V_{\text{HBT}}}{I_T} \frac{R_b}{R_L} \left( \frac{C_{bc} + C_{be,\text{EF}} + C_{be,\text{EF}}}{g_{m,\text{HBT}}} \right)
$$

(3.1)

$$
\tau_{\text{BICMOS}} = \frac{\Delta V_{\text{MOS}}}{I_T} \left\{ 2C_{be} + 3\left( 1 + g_{m,\text{HBT}} R_l \right) C_{bc} + C_{bc,\text{EF}} + C_{be,\text{EF}} \right\} \\
+ \frac{\Delta V_{\text{MOS}}}{I_T} \frac{R_g}{R_L} \left( \frac{C_{gs} + (1 + g_{m,\text{MOS}} R_l) C_{gd}}{g_{m,\text{HBT}}} \right) \\
+ \frac{2C_{be} + C_{db} + C_{gd}}{g_{m,\text{HBT}}}
$$

(3.2)

$$
\tau_{\text{HBT-MOS}} = \frac{\Delta V_{\text{HBT}}}{I_T} \left\{ 2C_{gs} + 3\left( 1 + g_{m,\text{MOS}} R_l \right) C_{gd} + C_{bc,\text{EF}} + C_{be,\text{EF}} \right\} \\
+ \frac{\Delta V_{\text{HBT}}}{I_T} \frac{R_b}{R_L} \left( \frac{C_{be} + (1 + g_{m,\text{MOS}} R_l) C_{bc}}{g_{m,\text{HBT}}} \right) \\
+ \frac{2C_{gs} + C_{cs} + C_{bc}}{g_{m,\text{MOS}}}
$$

(3.3)

$$
\tau_{\text{MOS-MOS}} = \frac{\Delta V_{\text{MOS}}}{I_T} \left\{ 2C_{gs} + 3\left( 1 + g_{m,\text{MOS}} R_l \right) C_{gd} + C_{bc,\text{EF}} + C_{be,\text{EF}} \right\} \\
+ \frac{\Delta V_{\text{MOS}}}{I_T} \frac{R_g}{R_L} \left( \frac{C_{gs} + (1 + 2) C_{gd}}{g_{m,\text{MOS}}} \right) \\
+ \frac{2C_{gs} + C_{db} + C_{sb} + C_{gd}}{g_{m,\text{MOS}}}
$$

(3.4)

Each equation is of the form:

$$
\tau = \tau_{\text{OUT}} + \tau_{\text{IN}} + \tau_{\text{MID}}
$$

(3.5)

The first term of the equation, $\tau_{\text{OUT}}$, represents the time constant at the output of the cascode pair and input of the emitter follower stage. The second term $\tau_{\text{IN}}$ represents the time constant at the
input of the clock transistors while $\tau_{MID}$ represents the time constant seen at the drain (or collector) of the clock transistor.

When carrying the same current, and sized so that they are each biased at their respective $J_{peak} f_T$, the parasitic capacitances are much higher for the MOSFET than for the HBT, while the $g_m$ of an HBT is much higher than that of the MOSFET.

The intrinsic and extrinsic components of the base resistance for the SiGe HBT can be reduced by using multiple emitter stripes. This however increase the base-to-collector capacitance making $R_b C_{bc}$ approximately constant for a given technology node [47]. The gate resistance for MOSFETs however can be reduced through layout minimization while the gate-drain overall area is kept constant thus $C_{gd}$ remains constant. For these reasons and the equations (3.1) through (3.4), it is expected that the HBT-HBT topology has the lowest $\tau_{MID}$ followed by the BiCMOS, HBT-MOS and then the MOS-MOS topology.

For 0.13-µm MOSFETs, the required swing $\Delta V_{MOS}$ is roughly 400 mV and reduces by a factor of $\sqrt{2}$ for each technology node [12]. For HBT gates, the required voltage swing $\Delta V_{HBT}$ is slightly lower at 300 mV [12] regardless of technology node. It is therefore expected that the HBT-HBT topology has the best $\tau_{OUT}$ while the MOS-MOS topology has the slowest $\tau_{OUT}$. The $\tau_{IN}$ term depends on the relative speeds of the HBT and MOS device which for the HBT is given by:

$$f_{T,HBT} = \frac{1}{2\pi} \frac{g_{m,HBT}}{C_{BE} + C_{BC}}$$

(3.6)

while for a MOS is given by

$$f_{T,MOS} = \frac{1}{2\pi} \frac{g_{m,MOS}}{C_{GS} + C_{GD}}$$

(3.7)

where $f_{T,HBT}$ is the unity gain frequency of the HBT while $f_{T,MOS}$ is the unity gain frequency of the MOS device.

Setting the tail current to 8 mA results in a load resistance, $R_L$, of 50 Ω in the case of MOSFET data pairs and 37.5 Ω in the case of HBT data pairs. In order to be biased at $J_{peak} f_T$, the HBTs are sized to 2 µm emitter lengths while the MOSFETs are realized using 14 fingers each of 1µm. The tail current is set using a MOSFET current mirror with gate width of 32 µm. The HBTs in
the emitter pairs are sized at $0.5 \times f_{\text{peak}} f_T$. Simulation results for the four different topologies using an 80-GHz clock frequency are shown in Figure 3.4.

![Simulated 80-Gbps eye diagrams for the (a) HBT-HBT (b) BiCMOS (c) HBT-MOS and (d) MOS-MOS latch topologies.](image)

Figure 3.4: Simulated 80-Gbps eye diagrams for the (a) HBT-HBT (b) BiCMOS (c) HBT-MOS and (d) MOS-MOS latch topologies.

A similar performance is observed for the HBT-HBT topology and the BiCMOS technology. This contradicts the findings in [27, 12] where the BiCMOS topology slightly outperformed the HBT-HBT topology. This is due to the fact that they used a 0.13-µm SiGe BiCMOS topology which had slower HBTs with $f_T$ of 150 GHz compared to the 240 GHz for this technology [3].
while the MOSFETs remained the same. The 60% increase in HBT performance was enough to make the HBT-HBT comparable in performance with the BiCMOS topology.

The HBT-HBT topology requires the smallest voltage swing to be applied on the clock pair, lowering the strain on the clock buffers, which is a major consideration when operating with above 100-GHz signals. As well, after extraction, a larger degradation in performance is expected in the BiCMOS implementation as oppose to the HBT-HBT implementation due to extra parasitic capacitances in the MOSFET. Unfortunately, extraction capabilities are not available in the design. Taking the hand calculations and simulation results into account, the HBT-HBT topology was chosen for fabrication. The transistor level schematic of the manufactured latch is shown in Figure 3.5.

![Figure 3.5: Fabricated latch using the HBT-HBT topology.](image)

The first design step is choosing the tail current, which is 8 mA in this case. From this, it follows that the load resistance should be 37.5 Ω in order to allow for a 300 mV swing. In order to
account for contact and metal resistances in the inductor, the load resistor was slightly reduced to 35 \( \Omega \). A 15\%-variation in the resistor size corresponds to a 45-mV difference in the \( \Delta V_{HBT} \) still leaving enough margin to switch the HBTs.

In order to be biased at \( J_{peak \, f_T} \) of 2 mA/\( \mu m \) [6] when balanced, 2 \( \mu m \) emitter lengths are chosen. The emitter followers are sized at 0.5 \( \times J_{peak \, f_T} \). The tail currents are implemented using MOSFET current mirrors and a 220-\( \Omega \) resistor is inserted in the emitter follower in order to reduce the MOSFET \( V_{DS} \) to approximately 300 mV and provide better \( V_{DS} \) matching with the bias distribution as well as lower the capacitance seen at the emitter of the HBT.

The latch bandwidth can be improved by up to 60\% by using inductive peaking [28] and sizing the inductor using:

\[
L = \frac{R_L^2 C_L}{3.1}
\]  

(3.8)

From the above equation it becomes obvious that a small load resistor is desirable in order to reduce the inductor size and save area. Decreasing the resistor however increases the power consumption since the tail current must be increased in order to maintain the same voltage swing. The increase in tail current also entails an increase in device size so that the HBTs are still biased at \( J_{peak \, f_T} \) thus leading to larger parasitic capacitance and hence larger load capacitance \( C_L \).

\[
C_L \approx 2C_{bc} + 2C_{cs} + C_{bc,EF} + C_{be,EF} \approx 126 \, fF
\]  

(3.9)

Using equation (3.8), this leads to a peaking inductor if roughly 50 pH. This extends the -3 dB bandwidth \( BW_{3dB} \) [9] to:

\[
BW_{3dB} \approx 1.6 \times \frac{1}{2 \pi R_L C_L} \approx 57.7 \, GHz
\]  

(3.10)

which is sufficient for 110 Gbps operation. The inductor is implemented as a spiral inductor employing the copper Metal 5 and Metal 6 layers of the millimetre-wave back end. The Q factor of this inductor is not highly important since its resistance can be absorbed by \( R_L \).
3.4 Retimer Output Buffers

In order to match to the 50-Ω system output load, two buffers are cascaded after the retimer as depicted in Figure 3.1. The cascode buffer schematics can be seen in Figure 3.6.

![Figure 3.6: Retimer output buffers: (a) first buffer and (b) final 50-Ω buffer.](image)

The input HBTs are biased at $I_{\text{peak}}f_T$ while the common base HBTs are biased at slightly higher current density. The role of the 2-mA current tail is to prevent the common base transistors from fully switching off and hence enhance the maximum operating frequency. It also serves to provide the proper common mode level for the following stage. One approach would have been to keep the same bias current but increase the load resistance; this however would have deteriorated the frequency response of the cascode. Another approach is to increase the tail
current, however this would have required bigger HBTs in order to maintain $J_{peak f_T}$ biasing. Introducing the 2-mA current source produces the same effect for the same power consumption, without the need for bigger devices at the input. In addition, the common base transistors are never current starved hence are faster when switching from the “off” state to the “on” state. The resistor sizes are chosen so that the voltage swing is 300 mV. The 12-mA output buffer is AC coupled to a 50-$\Omega$ load making the effective load 25-$\Omega$. The output buffer has an additional 25-pH inductor in order to account for parasitic in the pads.

In order to provide the proper DC biasing between the stages, the buffers are separated by an 8-mA per side emitter follower seen in Figure 3.7 (a). The emitter follower has the benefit of extending the bandwidth of the 8-mA buffer without the need for peaking inductors which occupy a large area. Two other 4-mA emitter followers seen in Figure 3.7 (b) are used to provide the proper DC levels for the latch clock inputs. The preceding clock buffers are biased from 2.5 V, therefore, in order to save power, and due to the availability of the power supply, the emitter follower stage was also biased from 2.5 V. The HBTs in the emitter followers are biased at $J_{peak f_T}$ while the role of the resistor is to set the MOSFET $V_{DS}$ for proper current mirror matching as well as decreasing the capacitance seen at the emitter and thus increasing stability.

Figure 3.7: Emitter followers used to (a) cascade output buffers and (b) provide proper DC levels for latch clock inputs.
3.5 Simulation Results

The retimer was first simulated using an ideal 300-mVpp, 125-Gbps differential input signal. The output eye after the retimer and after the final output buffers can be seen in Figure 3.8 and Figure 3.9 respectively. Parasitic extraction was not available in this design kit, hence these are schematic simulations. It can be seen that the output buffers deteriorated jitter seen after the retimer.

![Figure 3.8: A 125-Gbps signal at the output of the retimer when retimed at 125GHz.](image)

![Figure 3.9: A 125-Gbps signal after the 50-Ω output buffer when retimed at 125GHz.](image)
The retimer can also be used to retime half rate data. An ideal 62.5-Gbps input data stream retimer at 125 GHz can be seen at the output of the retimer in Figure 3.10 and after the 50-Ω output buffer in Figure 3.11.

Figure 3.10: A 62.5-Gbps signal at the output of the retimer when retimed at 125 GHz.

Figure 3.11: A 62.5-Gbps signal after the 50-Ω output buffer when retimed at 125 GHz.
The output of the retimer and of the output buffer when retiming the on chip generate $2^7-1$ PRBS data using an 100-GHz clock is shown in Figure 3.12 and Figure 3.13.

Figure 3.12: Retimer simulations with 100-Gbps input data and 100-GHz retimer clock.
Figure 3.13: Retimer simulations with 50-Gbps input data and 100-GHz retimer clock.
3.6 Test Chip

In order to test the retimer, a test circuit was fabricated that has an on-chip PRBS generator. A diagram of the retimer test circuit can be seen Figure 3.14. The work discussed in this thesis, the retimer and output buffers, is highlighted in the diagram while the other blocks were designed by other students.

![Figure 3.14: The retimer test chip block diagram.](image)

In order to eliminate the need for an on-chip VCO and thus reduce space, the retimer clock signal (R_CLK) is provided by an external source as a single ended input. In order to generate the differential signal needed by the retimer, a transformer balun followed by two tuned buffers are used. The transformer, previously designed by Ioannis Sarkas, has primary and secondary inductances of 100 pH and a coupling factor of 0.8. The two clock buffers, designed by Shahriar Shahramian, each consist of an HBT cascode with emitter followers. The clock buffers are tuned at 110 GHz using 40-pH inductive loading. Each buffer consumes 20 mA from a 2.5-V supply for a total power consumption of 100 mW for the pair. A chain of these buffers could have been used to transform the single ended clock input into a differential signal; however their high
power consumption along with their low common mode rejection at 110 GHz made the use of the transformer balun at the input the preferred choice.

The PRBS generator was originally designed by Tod Dickson and published as an 86 Gbps $2^7 - 1$ PRBS Generator in [12]. It produced an eye amplitude of 300 mVpp per side and RMS jitter of 582 fF. A re-spin of the circuit for this tapeout was made by Katya Laskin and Ricardo Aroca. A separate clock is used for the PRBS generator in order to be able to align the PRBS data provided at the input of the retimer with the retimer clock. Two external clock signals allows for a phase shift to be introduced between the two.
4 Equalizer Fabrication and Experimental Results

This chapter describes the experiments carried out in order to measure the performance of the equalizer as well as providing the measurement results. A photomicrograph of the chip is shown in section 4.1. Sections 4.2 and 4.3 detail the test setup and results for S-parameter measurements and time domain measurements respectively. A performance comparison is given in Chapter 4.4.

4.1 Test Chip

The test chip was designed in STMicroelectronics’ 0.13-µm SiGe BiCMOS9MW technology. A photomicrograph of the fabricated test chip can be seen in Figure 4.1. The pad limited area of the chip is 990-µm x 895-µm while the equalizer circuit occupies 680-µm x 170-µm.

Figure 4.1: Photomicrograph of the equalizer.
The circuit has five control pads (Cntr1...5), which are labelled in Figure 4.1. The biasing for the input stages is provided using Bias1. The bias for the first three equalizer stages is provided using Bias2, while the bias current for the final two stages of the equalizer is provided using Bias3. Bias4 is used to control the bias current for the output buffer. The circuit consumes 336.6 mW and three DC pads (V3p3) are used to provide the power. The unlabeled pads are connected to ground. All measurements were conducted on wafer using 67-GHz GGB probes for input and output.

4.2 S Parameter Measurements

The S-parameter measurements were performed up to 65 GHz using a Wiltron 360B Vector Network Analyzer (VNA). A diagram and picture of the test setup can be seen in Figure 4.2.

Figure 4.2: Test setup for S-parameter measurements.
A comparison of the measured and simulated single-ended gain ($S_{21}$) is shown in Figure 4.3. With the control voltage in all stages set for maximum peaking, a gain of 12.2 dB (18.2 dB differentially) is observed at 52 GHz, 0.4 dB lower than the simulated value. The DC “gain” is -19 dB, giving a total of 31 dB of adjustable peaking between DC and 52 GHz. For differential gain, 6 dB should be added to the measured values.

The simulated and measured input ($S_{11}$) and output ($S_{22}$) return loss are plotted in Figure 4.4. $S_{11}$ is less than -16.1 dB and the $S_{22}$ is below -9.3 dB up to 65 GHz. At low frequency, $S_{11}$ and $S_{22}$ are both better than -29 dB indicating less than 3% deviation of the 50-$\Omega$ input and output resistors from the nominal value.
In order to measure the equalization capabilities, the three cables whose frequency responses are shown in Figure 1.2 are inserted at the input of the equalizer. The new test setups are illustrated in Figure 4.5.

Figure 4.4: Measured and simulated $S_{11}$ and $S_{22}$ of the equalizer.

Figure 4.5: Test setup for S parameter measurements using the cables and equalizer.
The equalizer is capable of improving the 3-dB bandwidth from 16 GHz to 43 GHz for the 1-mV cable as shown in Figure 4.6. The non equalized cable measurements were previously shown in Figure 1.2.

![Figure 4.6: S_{21} measurements using the V cable.](image)

The 3-dB bandwidth for the SMA cable is improved from 11 GHz to 30 GHz as seen in Figure 4.7, while the 3-dB bandwidth for the 10-m Belden cable is improved and from 3 GHz to 7 GHz. This is illustrated in Figure 4.8.

![Figure 4.7: S_{21} measurements using the SMA cable.](image)
When measuring the performance of the equalizer alone, the calibration of the equipment was performed using Line Reflect Match (LRM). This allows the effect of the probes to be extracted from the performance results. The same calibration was performed when measuring the ensemble formed by the cable and the equalizer, however, following the calibration, the cable to be equalized was inserted between Port 1 of the VNA and the probe attached to the input of the equalizer. This created a less accurate calibration. This reason along with the high attenuation results in an increasingly non-smooth $S_{21}$ measurement at high frequencies.

4.3 Time Domain Measurements

Large signal equalization experiments were performed on the three cables. All measurements were conducted on wafer using 67-GHz GGB probes. Each probe has a loss of up to 1.1 dB [16] hence the channel loss consists of the channel loss plus up to 2.2 dB of probe loss. The test setup for the time domain measurements is shown in Figure 4.9 and Figure 4.10. The input signal is provided by an 80-Gbps $2^7$-1 PRBS Generator described in [12] which produces an eye amplitude of 300 mV$_{pp}$ per side.
Figure 4.9: Schematic of the test setup for time domain measurements.

Figure 4.10: Picture of the test setup for time domain measurements.
Equalization of the 1.8-m SMA cable at 59.2 Gbps is shown in Figure 4.11 and Figure 4.12. The eye diagrams are shown for the signal at the output of the transmitter, after the cable and after the equalizer. The channel loss at 30 GHz for the probes and cables is 17.9 dB. Maximum gain settings were applied to the equalizer in order to achieve the cleanest eye diagram; this however introduces excessive peaking which is visible in Figure 4.12. The equalizer improves the -3-dB bandwidth of the cable from 11 GHz to 30 GHz as shown in Figure 4.7.

Figure 4.11: The measured signal at 59.2 Gbps before (top) and after the 1.8-m cable (bottom).

Figure 4.12: Measured 59.2-Gbps data at the output of the equalizer after 17.9 dB of channel loss.
Equalization of the 1-m V cable at 50.6 Gbps is shown in Figure 4.13. In this case, only two of the equalizer stages need to be turned on in order to equalize -3.6 dB of channel loss at 25 GHz. The channel loss at 30 GHz is 1 dB higher, which requires all stages to be turned on in order to equalize the 60-Gbps data seen in Figure 4.14.

Figure 4.13: Output of the equalizer at 50.6 Gbps when equalizing a 1-m long V cable.

Figure 4.14: Output of the equalizer at 60 Gbps when equalizing a 1-m long V cable.
The output of the equalizer for a 70 Gbps data is seen in Figure 4.15. The channel loss at 35 GHz is 7.2 dB causing a significant deterioration in the eye diagrams. All stages needed to be turned on in order to achieve an open eye, however excessive peaking is introduced as a result. Another problem is the miss-alignment of the differential signals at the input of the equalizer as can be seen in Figure 4.16 which is attributed to the slight length difference of the two V cables. It can be concluded that due to the high quality of the cable and the difficulty in matching between the two cables, the equalizer should not be used to equalize the 1-m V cable.

Figure 4.15: Equalizer output at 70 Gbps after a 1-m long V cable.
The high loss of the 10-m Belden cable causes the signal to be too small for the input of the equalizer. A 40-Gbps driver described in [2] capable of producing a signal with adjustable amplitude from $1-V_{pp}$ to $3.6-V_{pp}$ was used in order to generate a large enough input for the equalizer. The $2^{31}-1$ PRBS input pattern was generated by an external Centelax board. The new measurement setup can be seen in Figure 4.17 and Figure 4.18. It should be noted that, in this situation, the input to the equalizer was single ended and that the 10-m Belden cable and driver have a 75-$\Omega$ impedance while the equalizer has a 50-$\Omega$ input impedance causing reflection and power loss at the input of the equalizer.
Figure 4.17: Test setup for time domain measurements using the driver.

Figure 4.18: Picture of the test setup for time domain measurements using the driver.
A 30-Gbps signal after the 10-m cable and after equalization is shown in Figure 4.19 and Figure 4.20 respectively. A clear improvement in the eye opening when compared to the signal amplitude can be observed. The signal jitter can be further improved by using the retimer described in Chapter 3 at the output of the equalizer.

Figure 4.19: A 30-Gbps signal after a 10 m cable. The channel loss at 15 GHz is -15.8 dB.

Figure 4.20: The 30-Gbps signal after the equalizer.
At 34.6 Gbps, the channel loss of 26.4 dB causes the eyes to be fully closed after 10 m as seen in Figure 4.21, however, after the equalizer the eyes are now open again as seen in Figure 4.22.

Figure 4.21: A 34.6-Gbps signal after a 10-m cable with channel loss of 26.4 dB at 17 GHz.

Figure 4.22: A 34.6-Gbps signal after the equalizer for a channel loss 26.4 dB at 17 GHz.
The cable was replaced with the 1-m V cable and the same experiment was performed. The effect of turning different stages of the equalizer was observed at 38.3 Gbps when the channel loss is 5.9 dB at 19 GHz. An improvement in eye opening is observed in Figures 3.22 thru 3.25 as the equalizer stages are gradually turned from non-peaking mode to peaking mode.

Figure 4.23: Equalizer output at 38.3 Gbps when all stages are set to non-peaking mode.

Figure 4.24: Equalizer output at 38.3 Gbps when three stages are set to non-peaking mode.
Figure 4.25: Equalizer output at 38.3 Gbps when two stages are set to non-peaking mode.

Figure 4.26: Equalizer output at 38.3 Gbps when two stages are set to non-peaking mode.
4.4 Performance Comparisons

The equalizer is capable of providing a peak gain of 12.2 dB at 52 GHz with 31 dB of adjustable gain peaking from DC to 52 GHz. Operation up to 70 Gbps was shown making this the fastest receive equalizer published to date. A comparison of this work with previously published channel equalizers is given in Table 4-1.

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Technology Node</th>
<th>Power Consumption</th>
<th>Description and Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>This work</td>
<td>0.13-µm SiGe BiCMOS $f_T, \text{SiGe HBT} = 240 \text{ GHz}$</td>
<td>336.6 mW from a 3.3-V supply.</td>
<td>Receive equalizer with 31 dB of adjustable peaking at 52 GHz. Equalization is shown at 59.3 Gbps while combating 17.9 dB of channel loss, and at 34.6 Gbps while combating 26.4 dB of channel loss. Equalizer operation at 70 Gbps is also shown.</td>
</tr>
<tr>
<td>[26]</td>
<td>SiGe8HP $f_T, \text{SiGe HBT} = 210 \text{GHz}$</td>
<td>1.55 W from a 3.3-V supply.</td>
<td>A 2:1 MUX with 1-tap FFE. Equalization shown at 90 Gbps for 12 dB of channel loss and at 80 Gbps for 14 dB of channel loss.</td>
</tr>
<tr>
<td>[2]</td>
<td>0.18-µm SiGe BiCMOS $f_T, \text{SiGe HBT} = 160 \text{GHz}$</td>
<td>3.6 W from 4-, 6-, and 8-V supplies.</td>
<td>Driver with adjustable pre-emphasis. Equalization is shown at 38 GHz for 22 dB of channel loss.</td>
</tr>
<tr>
<td>[18]</td>
<td>0.18-µm SiGe BiCMOS $f_T, \text{SiGe HBT} = 160 \text{GHz}$</td>
<td>750 mW from a 5-V supply.</td>
<td>7-Tap transversal filter. Equalization shown at 49 Gbps for 15 dB of channel loss.</td>
</tr>
<tr>
<td>[15]</td>
<td>0.18-µm SiGe BiCMOS $f_T, \text{SiGe HBT} = 160 \text{GHz}$</td>
<td>759 mW from a 3.3-V supply.</td>
<td>One tap look ahead DFE. Equalization shown at 39.5 Gbps for 17 dB of channel loss.</td>
</tr>
<tr>
<td>[19]</td>
<td>0.25-µm SiGe BiCMOS $f_T, \text{SiGe HBT} = 50 \text{GHz}$</td>
<td>260 mW from a 2.5-V supply, excluding output buffer.</td>
<td>NRZ receiver with a 4-stage FFE and CDR. FFE provides 17 dB of adjustable peaking between 5-7 GHz and data recovery is shown at 10 Gbps.</td>
</tr>
<tr>
<td>[49]</td>
<td>0.18-µm SiGe BiCMOS $f_T, \text{SiGe HBT} = 120 \text{GHz}$</td>
<td>350 mW from a 3.3-V supply.</td>
<td>Analog equalize with feedback control loop. Equalization is shown at 10 Gbps when combating 22 dB of channel loss.</td>
</tr>
<tr>
<td>Ref.</td>
<td>Technology Node</td>
<td>Power Consumption per Latch</td>
<td>Performance</td>
</tr>
<tr>
<td>------</td>
<td>----------------</td>
<td>----------------------------</td>
<td>-------------</td>
</tr>
<tr>
<td>[5]</td>
<td>90-nm CMOS</td>
<td>300 mW from 1.2 V for the transmitter, receiver and PLL.</td>
<td>A 4-tap DFE in the receiver and a 4-tap FFE in the transmitter. Equalization of 30 dB of channel loss is shown at 10 Gbps.</td>
</tr>
<tr>
<td>[35]</td>
<td>90-nm CMOS</td>
<td>138 mW from a 1.3-V supply.</td>
<td>Analog peaking equalizer capable of compensating 7.5 dB of loss at 20 Gbps.</td>
</tr>
<tr>
<td>[46]</td>
<td>0.11-µm CMOS</td>
<td>13.2 mW from a 1.2-V supply.</td>
<td>A Cherry-Hopper amplifier is used to equalize up to 20 dB of channel loss at 10 Gbps.</td>
</tr>
<tr>
<td>[33]</td>
<td>0.13-µm CMOS</td>
<td>30 mW from a 1.2 V supply.</td>
<td>A transversal 2-tap FFE capable of equalizing 14.3 dB of channel loss at 38 Gbps.</td>
</tr>
<tr>
<td>[7]</td>
<td>0.13-µm CMOS</td>
<td>1578 mW from a 1.8-V supply.</td>
<td>A dual-mode pulsedwidth modulation pre-emphasis transmitter capable of compensating 30 dB of loss when operating at 16 Gsymbols/s.</td>
</tr>
<tr>
<td>[41]</td>
<td>0.18-µm CMOS</td>
<td>70 mW from a 1.8 V supply.</td>
<td>A 3-tap FIR filter with a distributed 3-tap amplifier is used to equalize 17 dB of channel loss when operating at 40 Gbps.</td>
</tr>
<tr>
<td>[31]</td>
<td>0.1-µm InP/InGaAs f_t = 150 GHz</td>
<td>1.3 W from a 4.5-V supply.</td>
<td>A 1-tap FFE and a 1-tap DFE capable of compensating 20-ps differential group delay for 40 Gbps operation.</td>
</tr>
<tr>
<td>[34]</td>
<td>1-µm GaAs HBT</td>
<td>83 mW from a 5.2-V supply.</td>
<td>A two stage amplifier with high frequency peaking is used to equalize 24 dB of channel attenuation at 10 Gbps.</td>
</tr>
</tbody>
</table>
In order to compare the equalizers in Table 4-1, the data rate versus channel loss for each equalizer is plotted in Figure 4.27 showing this work to be the fastest receive equalizer.

![Figure 4.27: Data rate versus channel loss for the equalizers described in Table 4-1.](image)

A figure of merit (FoM) was also developed to compare the equalizers this being:

\[
\text{FoM} = \frac{\text{Channel Loss} \times \text{Data Rate}}{\text{Power}}
\]  

A higher FoM is the desired outcome. Figure 4.28 shows that the work presented in this thesis has similar FoM when compared to other published BiCMOS equalizers. The CMOS implementations show a better FoM due to their lower power consumption, however they do not achieve as high data rates as the BiCMOS examples.
Figure 4.28: Figure of merit for different equalizers described in Table 4-1.
5 Retimer Fabrication and Experimental Results

The retimer test chip was designed using the same technology that was used for the equalizer, this being STMicroelectronics’ 0.13-µm SiGe BiCMOS9MW technology. A photomicrograph of the fabricated test chip can be seen in Figure 4.1. The pad limited area of the chip is 1055 µm x 1290 µm. A description of each pad is given in Table 5-1. The unlabelled pads are connected to ground.

Table 5-1: Pad description for the retimer test circuit

<table>
<thead>
<tr>
<th>Pad Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_CLK</td>
<td>High speed clock input.</td>
</tr>
<tr>
<td>Out-</td>
<td>High speed differential retime output.</td>
</tr>
<tr>
<td>Out+</td>
<td>High speed differential retime output.</td>
</tr>
<tr>
<td>I_Retimer</td>
<td>Retimer bias current with nominal value of 2 mA.</td>
</tr>
<tr>
<td>V3p3</td>
<td>Retimer Vdd with nominal value of 3.3 V.</td>
</tr>
<tr>
<td>D_CLK</td>
<td>High speed data input clock.</td>
</tr>
<tr>
<td>Trigger</td>
<td>Output signal used to trigger the oscilloscope pattern capture function.</td>
</tr>
<tr>
<td>I_MUX</td>
<td>Mux bias current with nominal value of 1.2 mA.</td>
</tr>
<tr>
<td>Reset</td>
<td>PRBS data reset function.</td>
</tr>
<tr>
<td>M_CLK_Bias</td>
<td>Bias current for the MUX clock buffers with nominal value of 1.2 mA.</td>
</tr>
<tr>
<td>V2p5</td>
<td>Data Generator Vdd with nominal value of 2.5 V.</td>
</tr>
<tr>
<td>I_PRBS</td>
<td>Bias current for the PRBS with nominal value of 2 mA.</td>
</tr>
<tr>
<td>R_CLK_Bias</td>
<td>Bias current for the retime clock buffers with nominal value of 2 mA.</td>
</tr>
</tbody>
</table>
The circuit consumes 457 mA (1143 mW) from a 2.5-V supply hence three DC pads (V2p5) were used to provide this power. An additional 94 mA (310 mW) is consumed from a 3.3-V supply which is provided using only one DC pad. The 94-mA supplies the retimer, output buffers and the required bias circuitry.

Figure 5.1: Photomicrograph of the retime test chip.
5.1 Measurement Setup

All measurements were conducted on wafer and diagram of the test setup can be seen in Figure 5.2. The DC power supplies and sources are not shown in the diagram. A single ended 110-GHz GGB probe was used for the high speed retimer clock input. A low speed clock signal was provided by the Agilent E8257D PSG Analog Signal Generator and then feed to a Militech 236 multiplier. This produces a signal equivalent to 6 times the input signal frequency that can be used as the high speed R_CLK. The data clock was generated by Hewlet Packard 83650B Series Swept Signal Generator. In order to prevent phase drift, these two signal sources were synchronized using a 10-MHz signal produced by the Agilent source. In order to trigger the scope, the Agilent signal is split using an Anritsu V240 Power Divider, one signal is used to feed the multiplier while the other is for triggering the scope.

Figure 5.2: Diagram of the retimer test setup.
The design required that the output be measured using a differential 110-GHz probe in order to provide symmetrical loading for the output buffer. When the measurements were performed however, it was discovered that there was not enough space for the differential 110-GHz output probe due to the proximity of the composite probe. Two different experiments were therefore performed, first a differential 67-GHz probe was used, and then a single ended 110-GHz probe was used. The data was captured using an Agilent Infinium DCA-J 86100C Digital Communication Analyzer with an Agilent 86107A Precision Timebase Module. When using the differential probe, the second output was terminated using a capacitor and 50-Ω load. In the case of the single ended probe, the second output was left floating. A picture of the measurement setup can be seen in Figure 5.3.

Figure 5.3: Picture of the retimer measurement setup.
5.2 Measurement Results

When the chip was fabricated, it was discovered that the PRBS generator only functioned up to 72 Gbps. The clock path to the retimer, however, is tuned at 110 GHz and therefore cannot generate a strong enough signal at 72 GHz to retime the 72-Gbps data. The retimer functionality can still be tested by retiming half rate data. For example, a 50-Gbps signal can be retimed using a 100-GHz clock. In order to test the retimer performance, the system was first measured with the retimer clock off to get a base jitter measurement. In this situation, the retimer lets input data thru without actually retiming it. The retimer clock was then turned on by turning on the power to the external multiplier. The improvement in jitter was measured and plotted in Figure 5.4. The captured eye diagrams used to generate this data are attached in Appendix A. Measurements were performed up to 118 GHz after which the Militech multiplier was no longer able to prove a strong enough clock for the retimer. When using the 110-GHz probes, the measured phase margin at 72 GHz was 48° (1.85 ps), at 90 GHz it was 38° (1.17 ps), and at 105 GHz it was 25° (0.66 ps). The phase margin was measured by phase shifting the retimer clock and noting the range in which the retimed jitter is not affected.

![Figure 5.4: Improvement in jitter performance due to retiming.](image-url)
Clearly an improvement in jitter can be observed when the retimer clock signal is turned on. The lower quality 67-GHz probes also produce a much sharper signal then the 110-GHz probe. This is due to the fact that the 67-GHz probes are differential and provide a symmetrical load to the circuit while the 110-GHz is single ended and one output is left floating. This phenomenon is clearly observed in the eye diagrams for a 39-Gbps signal retimed using a 78-GHz clock in Figure 5.5. The measurements performed using the 110-GHz single ended probe show a degradation in RMS jitter in both the retimed and not retimed case when compared to the measurements performed using a differential 67-GHz probe.

Figure 5.5: Eye diagrams for a 39-Gbps signal when measured with 67-GHz and 110-GHz probes.
A Bit Error Rate Tester (BERT) capable at operating at over 20-Gbps was not available; however, PRBS operation can be verified by observing the spectrum of the output signal. The tone spacing is given by [27]:

\[
\text{Tone Spacing} = \frac{\text{Data Rate}}{\text{Pattern Length}}
\]  

(5.1)

For a 59-Gbps signal with \(2^7-1\) PRBS pattern, tone spacing is 456 MHz. The full spectrum can be observed in Figure 5.6 while the zoomed in spectrum can be observed in Figure 5.7.

![Figure 5.6: Full spectrum of the 59-Gbps signal retimed at 118 Gbps.](image)
Figure 5.7: Zoomed in spectrum of the 59-Gbps signal retimed at 118 Gbps.

The spectrum does not guarantee that every bit is correct, solely that the pattern is 127 bits long. In order to verify that each bit is correct, the oscilloscope was locked to a 127-bit long pattern and each bit was checked against the ideal measurement. The measured versus ideal pattern are plotted in Figure 5.8.

Figure 5.8: Measured versus ideal $2^7-1$ PRBS signal.
5.3 Performance Comparisons

The retimer described in this chapter has the faster operating clock frequency when compared with previously published work, as seen in Table 5-2. When compared with an InP HEMT technology with similar $f_T$ [45], an almost 50% improvement in clock frequency is observed while the supply voltage is significantly lower. An improvement from 45 GHz [10] to 118 GHz in clock frequency is observed over the previous 0.13-µm SiGe BiCMOS technology node. Although part of the frequency increase can be attributed to the improvement in $f_T$ from 150 GHz [10] to 240 GHz [3]. The use of HBTs for the clock transistors, emitter followers on the feedback path and increased supply from 2.5 V to 3.3 V all contributed to more than double the clock frequency.

<table>
<thead>
<tr>
<th>Technology</th>
<th>Ref.</th>
<th>Technology Node</th>
<th>Power Consumption per Latch</th>
<th>Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>BiCMOS</td>
<td>This work</td>
<td>0.13µm SiGe BiCMOS $f_T$, SiGe HBT = 240 GHz</td>
<td>52.8 mW, 16mA per latch from 3.3V</td>
<td>59 Gbps data with 118 GHz clock, 25° phase margin at 105 GHz</td>
</tr>
<tr>
<td></td>
<td>[39]</td>
<td>0.18µm SiGe BiCMOS $f_T$, SiGe HBT = 120GHz</td>
<td>156 mW; 30 mA per latch from -5.2 V</td>
<td>40 Gbps, 152° phase margin; 25.5 Gbps data with 51 GHz clock</td>
</tr>
<tr>
<td></td>
<td>[24]</td>
<td>0.18µm SiGe BiCMOS $f_T$, SiGe HBT = 120GHz</td>
<td>2.5 V, current not given</td>
<td>45.6 Gbps</td>
</tr>
<tr>
<td></td>
<td>[10]</td>
<td>0.13µm SiGe BiCMOS $f_T$, SiGe HBT = 150 GHz</td>
<td>27.5 mW; 11 mA per latch from 2.5 V</td>
<td>45 Gbps</td>
</tr>
<tr>
<td>CMOS</td>
<td>[43]</td>
<td>65 nm CMOS $f_T$ = 170 GHz</td>
<td>9.6 mW; 8 mA per latch from 1.2 V</td>
<td>81 Gbps</td>
</tr>
<tr>
<td></td>
<td>[6]</td>
<td>90 nm CMOS $f_T$ = 125 GHz</td>
<td>10.8 mW; 9 mA per latch from 1.2 V</td>
<td>40 Gbps, 163° phase margin</td>
</tr>
<tr>
<td>Technology</td>
<td>Ref.</td>
<td>Technology Node</td>
<td>Power Consumption per Latch</td>
<td>Performance</td>
</tr>
<tr>
<td>------------</td>
<td>------</td>
<td>--------------------------</td>
<td>----------------------------</td>
<td>-------------</td>
</tr>
<tr>
<td>InP</td>
<td>[45]</td>
<td>0.1µm InP HEMT (f_T = 245) GHz</td>
<td>-5.7 V, current not given</td>
<td>80 Gbps</td>
</tr>
<tr>
<td></td>
<td>[1]</td>
<td>InP HBT (f_T = 150) GHz</td>
<td>20 mW, 13 mA per latch from 1.5V</td>
<td>50 Gbps</td>
</tr>
<tr>
<td></td>
<td>[32]</td>
<td>0.13µm InP HEMT (f_T = 150) GHz</td>
<td>-5.2 V, current not given</td>
<td>50 Gbps, 70° phase margin</td>
</tr>
<tr>
<td></td>
<td>[23]</td>
<td>InP DHBT (f_T = 150) GHz</td>
<td>-4.2 V, current not given</td>
<td>43.2 Gbps, 190° phase margin</td>
</tr>
</tbody>
</table>

It can be argued that the increase in retimer clock frequency is mostly due to improvements in the technology. However, Figure 5.9 shows that this retimer achieves the highest ratio of clock speed to technology \(f_T\) when compared to previously published work.

Figure 5.9: The clock speed as a function of technology \(f_T\) for the retimers described in Table 5-2.
6 Conclusions

ISI caused by frequency dependent loss in the copper cable can be severely detrimental to the eye opening of high speed signals as shown in Figure 4.11. An equalizer, however, can be used to combat the channel characteristics and improve the BER at the receiver. The fabricated channel equalizer is based on a Gilbert cell topology and provides 31 dB of adjustable peaking at 52 GHz while consuming 336.6 mW from a 3.3-V supply. The S parameter measurements show an improvement of over 200% in the 3-dB bandwidth of the cable and equalizer system when compared to the cable alone. Equalization is shown at 59.3 Gbps while combating 17.9 dB of channel loss and at 34.6 Gbps while combating 26.4 dB of channel loss. Operation at 70 Gbps while combating 7.2 dB of channel loss is also shown; however no improvement over the received eye is demonstrated.

Due to the low amplitude of the equalizer output signal and the high jitter, a retimer is necessary at the output. The retimer can also function in a feedback configuration as shown in Figure 1.6 and serve as a one-tap DFE. The retimer test circuit has an on chip $2^7$-1 PRBS generator and is shown to function with a clock frequency between 72 GHz and 118 GHz while retiming half rate data. The retimer and output buffers portion of the circuit consume 94 mA from a 3.3-V supply.

Although this equalizer was tailored for data travelling over long coaxial cables, the same principles can be extended for other copper media used in backplanes and twisted pair cables as well as for fiber optic cables all of which suffer from frequency dependent signal degradation.
6.1 Contributions

The objective of this work was to investigate techniques and circuits to extend the serial data rates for wireline communications beyond 50 Gbps, specifically when operating over coaxial cables. Two record-breaking circuits, a 70-Gbps linear adaptive equalizer block and a 118 GHz retimer, were designed, fabricated and tested in the lab. The main results of this research were presented at the 2009 IEEE Bipolar/BiCMOS Circuits and Technology Meeting:


6.2 Future Work

The retimer circuit must be integrated with the equalizer signal in order to overcome the low amplitude, high jitter signal seen at the output of the equalizer. A CDR system can further be used to reduce the receiver jitter by ensuring that the retimer is triggered at the center of the eye regardless of the drift in the transmitter frequency.

The equalizer can be further expanded to work with cables of various qualities and lengths by replacing the MIM capacitors in the tuning path with varactors which will allow the system to vary the frequency at which the peak occurs. An on-chip eye monitor and algorithm for controlling the main and tune path weightings must also be implemented in order to for equalizer to be able to adapt to various cable lengths.
References


Appendix

Appendix Table of Figures

Figure A-1: 36-Gbps data, retimer clock off, 67-GHz probes. .................................................... 78
Figure A-2: 36-Gbps data, retimer clock on at 72-GHz, 67-GHz probes. ........................................ 78
Figure A-3: 36-Gbps data, retimer clock off, 110-GHz probes. ................................................... 79
Figure A-4: 36-Gbps data, retimer clock on at 72-GHz, 110-GHz probes. ........................................ 79
Figure A-5: 37.5-Gbps data, retimer clock off, 110-GHz probes. ................................................... 80
Figure A-6: 37.5-Gbps data, retimer clock on at 75-GHz, 110-GHz probes. ...................................... 80
Figure A-7: 39-Gbps data, retimer clock off, 67-GHz probes. .................................................... 81
Figure A-8: 39-Gbps data, retimer clock on at 78-GHz, 67-GHz probes. ........................................ 81
Figure A-9: 39-Gbps data, retimer clock off, 110-GHz probes. ................................................... 82
Figure A-10: 39-Gbps data, retimer clock on at 78-GHz, 110-GHz probes. ...................................... 82
Figure A-11: 40.5-Gbps data, retimer clock off, 110-GHz probes. ................................................ 83
Figure A-12: 40.5-Gbps data, retimer clock on at 81-GHz, 110-GHz probes. ..................................... 83
Figure A-13: 42-Gbps data, retimer clock off, 67-GHz probes. ................................................... 84
Figure A-14: 42-Gbps data, retimer clock on at 84-GHz, 67-GHz probes. ....................................... 84
Figure A-15: 42-Gbps data, retimer clock off, 110-GHz probes. ................................................... 85
Figure A-16: 42-Gbps data, retimer clock on at 84-GHz, 110-GHz probes. ..................................... 85
Figure A-17: 43.5-Gbps data, retimer clock off, 110-GHz probes. ................................................ 86
Figure A-18: 43.5-Gbps data, retimer clock on at 87-GHz, 110-GHz probes. ................................... 86
Figure A-19: 45-Gbps data, retimer clock off, 67-GHz probes. ................................................... 87
Figure A-20: 45-Gbps data, retimer clock on at 90-GHz, 67-GHz probes. ...................................... 87
Figure A-21: 45-Gbps data, retimer clock off, 110-GHz probes. ................................................... 88
Figure A-22: 45-Gbps data, retimer clock on at 90-GHz, 110-GHz probes. ...................................... 88
Figure A-23: 46.5-Gbps data, retimer clock off, 110-GHz probes. ................................................ 89
Figure A-24: 46.5-Gbps data, retimer clock on at 93-GHz, 110-GHz probes. ................................... 89
Figure A-25: 48-Gbps data, retimer clock off, 110-GHz probes. ................................................... 90
Figure A-26: 48-Gbps data, retimer clock on at 96-GHz, 110-GHz probes. ................................... 90
Figure A-27: 49.5-Gbps data, retimer clock off, 110-GHz probes. ................................................ 91
Figure A-28: 49.5-Gbps data, retimer clock on at 99-GHz, 110-GHz probes ......................... 91
Figure A-29: 51-Gbps data, retimer clock off, 110-GHz probes ........................................ 92
Figure A-30: 51-Gbps data, retimer clock on at 102-GHz, 110-GHz probes ....................... 92
Figure A-31: 52.5-Gbps data, retimer clock off, 110-GHz probes ..................................... 93
Figure A-32: 52.5-Gbps data, retimer clock on at 105-GHz, 110-GHz probes .................... 93
Figure A-33: 54-Gbps data, retimer clock off, 67-GHz probes .......................................... 94
Figure A-34: 54-Gbps data, retimer clock on at 108-GHz, 67-GHz probes ......................... 94
Figure A-35: 54-Gbps data, retimer clock off, 110-GHz probes ....................................... 95
Figure A-36: 54-Gbps data, retimer clock on at 108, 110-GHz probes .............................. 95
Figure A-37: 55.5-Gbps data, retimer clock off, 110-GHz probes ..................................... 96
Figure A-38: 55.5-Gbps data, retimer clock on at 111GHz, 110-GHz probes .................... 96
Figure A-39: 57-Gbps data, retimer clock off, 110-GHz probes ........................................ 97
Figure A-40: 57-Gbps data, retimer clock on at 114-GHz, 110-GHz probes ....................... 97
Figure A-41: 58.5-Gbps data, retimer clock off, 110-GHz probes ..................................... 98
Figure A-42: 58.5-Gbps data, retimer clock on at 117-GHz, 110-GHz probes .................... 98
Figure A-43: 60-Gbps data, retimer clock off, 110-GHz probes ....................................... 99
Figure A-44: 60-Gbps data, retimer clock on at 120-GHz, 110-GHz probes ....................... 99
Figure A-1: 36-Gbps data, retimer clock off, 67-GHz probes.

Figure A-2: 36-Gbps data, retimer clock on at 72-GHz, 67-GHz probes.
Figure A-3: 36-Gbps data, retimer clock off, 110-GHz probes.

Figure A-4: 36-Gbps data, retimer clock on at 72-GHz, 110-GHz probes.
Figure A-5: 37.5-Gbps data, retimer clock off, 110-GHz probes.

Figure A-6: 37.5-Gbps data, retimer clock on at 75-GHz, 110-GHz probes.
Figure A-7: 39-Gbps data, retimer clock off, 67-GHz probes.

Figure A-8: 39-Gbps data, retimer clock on at 78-GHz, 67-GHz probes.
Figure A-9: 39-Gbps data, retimer clock off, 110-GHz probes.

Figure A-10: 39-Gbps data, retimer clock on at 78-GHz, 110-GHz probes.
Figure A-11: 40.5-Gbps data, retimer clock off, 110-GHz probes.

Figure A-12: 40.5-Gbps data, retimer clock on at 81-GHz, 110-GHz probes.
Figure A-13: 42-Gbps data, retimer clock off, 67-GHz probes.

Figure A-14: 42-Gbps data, retimer clock on at 84-GHz, 67-GHz probes.
Figure A-15: 42-Gbps data, retimer clock off, 110-GHz probes.

Figure A-16: 42-Gbps data, retimer clock on at 84-GHz, 110-GHz probes.
Figure A-17: 43.5-Gbps data, retimer clock off, 110-GHz probes.

Figure A-18: 43.5-Gbps data, retimer clock on at 87-GHz, 110-GHz probes.
Figure A-19: 45-Gbps data, retimer clock off, 67-GHz probes.

Figure A-20: 45-Gbps data, retimer clock on at 90-GHz, 67-GHz probes.
Figure A-21: 45-Gbps data, retimer clock off, 110-GHz probes.

Figure A-22: 45-Gbps data, retimer clock on at 90-GHz, 110-GHz probes.
Figure A-23: 46.5-Gbps data, retimer clock off, 110-GHz probes.

Figure A-24: 46.5-Gbps data, retimer clock on at 93-GHz, 110-GHz probes.
Figure A-25: 48-Gbps data, retimer clock off, 110-GHz probes.

Figure A-26: 48-Gbps data, retimer clock on at 96-GHz, 110-GHz probes.
Figure A-27: 49.5-Gbps data, retimer clock off, 110-GHz probes.

Figure A-28: 49.5-Gbps data, retimer clock on at 99-GHz, 110-GHz probes.
Figure A-29: 51-Gbps data, retimer clock off, 110-GHz probes.

Figure A-30: 51-Gbps data, retimer clock on at 102-GHz, 110-GHz probes.
Figure A-31: 52.5-Gbps data, retimer clock off, 110-GHz probes.

Figure A-32: 52.5-Gbps data, retimer clock on at 105-GHz, 110-GHz probes.
Figure A-33: 54-Gbps data, retimer clock off, 67-GHz probes.

Figure A-34: 54-Gbps data, retimer clock on at 108-GHz, 67-GHz probes.
Appendix

Figure A-35: 54-Gbps data, retimer clock off, 110-GHz probes.

Figure A-36: 54-Gbps data, retimer clock on at 108, 110-GHz probes.
Figure A-37: 55.5-Gbps data, retimer clock off, 110-GHz probes.

Figure A-38: 55.5-Gbps data, retimer clock on at 111GHz, 110-GHz probes.
Figure A-39: 57-Gbps data, retimer clock off, 110-GHz probes.

Figure A-40: 57-Gbps data, retimer clock on at 114-GHz, 110-GHz probes.
Figure A-41: 58.5-Gbps data, retimer clock off, 110-GHz probes.

Figure A-42: 58.5-Gbps data, retimer clock on at 117-GHz, 110-GHz probes.
Figure A-43: 60-Gbps data, retimer clock off, 110-GHz probes.

Figure A-44: 60-Gbps data, retimer clock on at 120-GHz, 110-GHz probes.