Study of a Semiconductor Nanowire under a Scanning Probe Tip Gate

by

Jacky Kai-Tak Lau

A thesis submitted in conformity with the requirements for the degree of Master of Applied Science

Electrical and Computer Engineering
University of Toronto

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Abstract

Nanowires are sensitive to external influences such as surface charges or external electric fields. An Atomic Force Microscope (AFM) is modified to perform back gating and tip gating measurements in order to understand the interaction between an external field, and surface charge and nanowire conductance.

A 2D finite element method (FEM) model is developed to simulate the measured conductance. The model shows that surface states play a critical role in determining nanowire conductance. A 3D FEM model is developed to examine the influence of the AFM tip on the lateral resolution of the AFM tip in the electrostatic measurement. The radius of the AFM tip determines the lateral resolution of the tip. However, carrier concentration in the nanowire establishes a lower limit on the lateral resolution, for small tip radii. These results enable one to optimize Scanning Probe Microscopy experiments as well as inform sample preparation for nanowire characterization.
Acknowledgements

I would like to thank all members of the Electronic and Photonic Materials group in my journey to obtaining a Master degree. In particular, I thank Professor Harry E. Ruda for his guidance, supervision and support – there are a few moments that I was quite lost in my research path but a discussion with him always brought light to my research. I thank Joseph Salfi for fabricating my samples and sharing his knowledge of nanowires, and more. I thank Dr. Igor Saveliev, Dr. Marina Blumin and Dr. Usha Philiopose for growing the nanowire needed for the experiments and contributing their time to discuss the properties of their nanowires with me. I would also like to thank Dr. Christian de Souza and Dr. Selvakumar Nair for their assistance in the modeling of nanowires. I thank Dr. Bin Bin Li for her encouragement and assistance in my experiment.

Lastly I would like to thank my parents, sisters and Iris for their unending support – I’ll be a sounding brass without your love and encouragement during my research process.
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## List of Symbols and Abbreviations

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\varepsilon_0$</td>
<td>Vacuum permittivity, $8.854 \times 10^{-12} \text{F/m}$</td>
</tr>
<tr>
<td>$\varepsilon_{NW}$</td>
<td>Relative static dielectric constant of nanowire</td>
</tr>
<tr>
<td>$\varepsilon_{oxide}$</td>
<td>Relative static dielectric constant of SiO$_2$, 4.5</td>
</tr>
<tr>
<td>$\mu_{FE}$</td>
<td>Field-effect mobility (cm$^2$/Vs)</td>
</tr>
<tr>
<td>$\mu_n$</td>
<td>Electron mobility (cm$^2$/Vs)</td>
</tr>
<tr>
<td>$A$</td>
<td>Cross-sectional area of a nanowire</td>
</tr>
<tr>
<td>CPD</td>
<td>Contact Potential Difference</td>
</tr>
<tr>
<td>$D_{gs}$</td>
<td>Density of interface states</td>
</tr>
<tr>
<td>$D_{it, acceptor}$</td>
<td>Density of acceptor-like interface states</td>
</tr>
<tr>
<td>$D_{it, donor}$</td>
<td>Density of donor-like interface states</td>
</tr>
<tr>
<td>$\vec{E}$</td>
<td>Electric field</td>
</tr>
<tr>
<td>$E_c$</td>
<td>Energy of conduction band minimum</td>
</tr>
<tr>
<td>$E_f$</td>
<td>Fermi Energy</td>
</tr>
<tr>
<td>$E_{gap}$</td>
<td>Energy of band-gap; Difference between conduction band maximum and valence band minimum</td>
</tr>
<tr>
<td>$E_{it}$</td>
<td>Energy of maximum $D_{gs}$</td>
</tr>
<tr>
<td>$E_{mid-gap}$</td>
<td>Energy at the middle of the bandgap, $E_{mid-gap} = (E_c-E_v)/2$</td>
</tr>
<tr>
<td>$E_v$</td>
<td>Energy of valence band maximum</td>
</tr>
<tr>
<td>$F_{\omega}$</td>
<td>The force at frequency $\omega$, experienced by a scanning probe tip when subject to an external voltage $V(\omega)$</td>
</tr>
</tbody>
</table>
The force at frequency \(2\omega\), experienced by a scanning probe tip when subject to an external voltage \(V(\omega)\)

The static force \((\omega=0)\), experienced by a scanning probe tip when subject to an external voltage \(V(\omega)\)

The probability of occupation of acceptor states as a function of electron energy

The probability of occupation of donor states as a function of electron energy

The probability of bulk states being occupied as a function of electron energy

The probability of bulk states not being occupied as a function of electron energy

The probability of occupation of surface states as a function of electron energy

Drain-source current (A)

Current density of electron (A/cm²)

Boltzmann constant, \(1.381\times10^{-23}\) J/K

Length of gate; in the current study, the length of the nanowire between source and drain contact

Electron concentration

Average electron concentration in cases where there is a spatial distribution in electron concentration

Concentration of ionized acceptors

Effective density of states for the conduction band

Concentration of ionized donors

Bulk donor doping concentration in nanowire

Concentration of occupied donor-like interface state as a function of energy
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>$N_{\text{surf}}$, $N_{\text{SS}}$</td>
<td>Surface state distribution on nanowire surface</td>
</tr>
<tr>
<td>$N_v$</td>
<td>Effective density of states for the valence band</td>
</tr>
<tr>
<td>$p$</td>
<td>Hole concentration</td>
</tr>
<tr>
<td>$q$</td>
<td>Elementary electron charge, $1.603 \times 10^{-19} \text{C}$</td>
</tr>
<tr>
<td>$Q_{\text{bulk}}$</td>
<td>Bulk charge inside the nanowire</td>
</tr>
<tr>
<td>$Q_{\text{doping}}$</td>
<td>Doping charge inside a nanowire</td>
</tr>
<tr>
<td>$Q_{\text{fix}}$</td>
<td>Fixed charge inside a nanowire</td>
</tr>
<tr>
<td>$Q_{\text{it}}$</td>
<td>Interface charge inside a nanowire</td>
</tr>
<tr>
<td>$Q_{\text{sc}}$</td>
<td>Space layer charge inside a nanowire</td>
</tr>
<tr>
<td>$Q_{\text{surf}}$</td>
<td>Surface charge on a nanowire</td>
</tr>
<tr>
<td>$T$</td>
<td>Temperature</td>
</tr>
<tr>
<td>$U_{\text{AC}}$</td>
<td>AC voltage applied to a scanning probe tip at frequency $\omega$</td>
</tr>
<tr>
<td>$U_{\text{DC}}$</td>
<td>DC voltage applied to a scanning probe tip</td>
</tr>
<tr>
<td>$V_{\text{ds}}$</td>
<td>Drain-source voltage</td>
</tr>
<tr>
<td>$V_{\text{gs}}$</td>
<td>Gate-source voltage</td>
</tr>
<tr>
<td>AFM</td>
<td>Atomic Force Microscopy</td>
</tr>
<tr>
<td>CAN</td>
<td>Center for Advanced Nanotechnology</td>
</tr>
<tr>
<td>CVD</td>
<td>Chemical Vapour Deposition</td>
</tr>
<tr>
<td>FEM</td>
<td>Finite Element Method</td>
</tr>
<tr>
<td>MBE</td>
<td>Molecular Beam Epitaxy</td>
</tr>
<tr>
<td>NW</td>
<td>Nanowire</td>
</tr>
</tbody>
</table>

AFM: Atomic Force Microscopy  
CAN: Center for Advanced Nanotechnology  
CVD: Chemical Vapour Deposition  
FEM: Finite Element Method  
MBE: Molecular Beam Epitaxy  
NW: Nanowire
<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FET</td>
<td>Field Effect Transistor; NWFET refers to nanowire FET</td>
</tr>
<tr>
<td>PMMA</td>
<td>Polymethyl-methacrylate, resist for e-beam lithography</td>
</tr>
<tr>
<td>SCM</td>
<td>Scanning Capacitance Microscopy</td>
</tr>
<tr>
<td>SEM</td>
<td>Scanning Electron Microscopy</td>
</tr>
<tr>
<td>SKPM</td>
<td>Scanning Kelvin Probe Microscopy</td>
</tr>
<tr>
<td>STM</td>
<td>Scanning Tunnelling Microscopy</td>
</tr>
<tr>
<td>STS</td>
<td>Scanning Tunnelling Spectroscopy</td>
</tr>
<tr>
<td>TEM</td>
<td>Transmission Electron Microscopy</td>
</tr>
</tbody>
</table>
1 Introduction to Semiconductor nanowires and Scanning Probe Techniques

1.1 Overview: The Role of electric field on nanowire conductance

Dimensions of electronic devices have been decreasing at an exponential rate since the development of the bipolar transistor in 1947 [1]. New growth techniques and new fabrication technologies have allowed the creation of many new structures. In particular, semiconductor nanowires have drawn the attention of researchers over the past decades for their novel geometry and its compositional flexibility.

A nanowire, given its small size, is sensitive to external influences. For example, Figure 1.1 below, shows the factors that affect the conductance of a nanowire device.

![Figure 1.1: Electric fields and charges exist around a semiconductor nanowire device.](image)
It is difficult to eliminate the effect of charges arising from interface states or oxide on the nanowire surface. A model of how these parameters will affect the nanowire conductance is essential to an interpretation of the electrical properties of nanowires. Table 1.1 lists some of the pertinent parameters that influence nanowire conductance.

**Table 1.1: Parameters that affect conductance of a nanowire.**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Origin</th>
<th>Effect</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric constant</td>
<td>Material polarization</td>
<td>Affects the coupling between the gating source and the nanowire. Modern electronic devices often use high-k material for scaling purpose [2].</td>
</tr>
<tr>
<td>Interface/surface charges</td>
<td>discontinuity of bulk wave functions</td>
<td>Interface states introduce either donor-like states or acceptor-like states at the interfaces, changing the conductance of the nanowire [3].</td>
</tr>
<tr>
<td>Charges in/on oxide layer</td>
<td>Contamination of the surface, native oxide on the nanowire, imperfections in the oxide layer</td>
<td>There are a variety of ions, deformation of crystal, imperfection in the crystal lattice that introduce charges around the nanowire.</td>
</tr>
<tr>
<td>Back gate potential</td>
<td>Electrically connected substrate</td>
<td>Back gating is a popular method for nanowire characterization because of its simple setup.</td>
</tr>
<tr>
<td>Tip gate potential</td>
<td>Introduction of probe in scanning probe microscopy</td>
<td>Scanning probe microscopy often requires placing a metallic tip extremely close to the surface of a device.</td>
</tr>
<tr>
<td>Contact potential difference</td>
<td>Interfaces between two different materials</td>
<td>An Ohmic or a Schottky contact will form depending on the band line up of the metal and the semiconductor.</td>
</tr>
</tbody>
</table>

The next three sections provide a review of semiconductor nanowires, surface and interfaces states and scanning probe microscopy.

### 1.2 Semiconductor nanowires

Semiconductor nanowires are single crystals grown in a rod shape using methods such as Chemical Vapour Deposition (CVD) or Molecular Beam Epitaxy (MBE) [4]. They have a large surface area to volume ratio and can be grown using a variety of materials. These two factors
make nanowires a popular choice for photonic applications. There are many publications on nanowire growth with wide-gap materials such as ZnO [5] for blue/UV device or narrow-gap materials such as InAs [6] as an infrared sensor, or composition of materials such as nanowire LED with embedded quantum dot [7]. Other applications include nanowire logic blocks comprised of n-Si nanowires and p-GaN nanowires [8]. However, the electrical properties of semiconductor nanowires are typically poorer than their bulk counterparts. For example, the electron mobility in bulk InAs is 22,600 cm$^2$/Vs, whereas the electron mobility of InAs nanowires are typically between 1,000 and 10,000 cm$^2$/Vs [9]. The lower mobility is typically attributed to nanowire’s sensitivity towards surface effects such as surface roughness and ionized interface state scattering.

The current-voltage measurements of nanowire field-effect transistors (NWFET) have become a standard method of characterizing nanowires. A schematic of a NWFET is shown in Figure 1.2. NWFET measurements can be used to extract the field-effect carrier mobility and average carrier concentration of the semiconductor sample. Equation 1.1 extracts the field-effect mobility of the nanowire and represents the lower bound of the real electron mobility of the sample. Equation 1.2 extracts the electron concentration assuming the current is dominated by drift component. [10].

$$\mu_{FE} = \frac{dI}{dV_g} \frac{L_G^2}{CV_{ds}}$$  \hspace{1cm} \text{Eq. 1.1}

$$n_{avg} = \frac{I_{ds}L_G}{q\mu_{FE}V_{ds}A}$$  \hspace{1cm} \text{Eq. 1.2}
Figure 1.2: A typical setup for NWFET measurement. The n+ silicon substrate act as a back gate for modulating nanowire carries.

Current-voltage measurements provide the overall electrical characteristic of the nanowire. However, in order to observe local variation of parameters, or the condition of the surface along a nanowire, researchers need a localized experimental method.

1.3 Surface and interface states

The periodic arrangement of the potential gives rise to a band gap, where electronic states are forbidden. When the periodic structure is broken at an interface or a surface, then electronic states can exist within the band gap, as surface or interface states. Solution of the Schrödinger’s Equation in 1D shows that the wave functions are localized at the interface and their energy eigenvalues are located within the band gap [3]. The distribution of interface state is approximately,

\[ D_{gs}(E) \approx \frac{1}{2\pi \sqrt{E_{gap}^2 - (E - E_{mid-gap})^2}} \]

Eq. 1.3
Equation 1.3 shows that the calculated interface state density for an ideal interface is highest near the band edges. In reality, the distribution of interface states depends heavily on the surface condition, such as lattice orientation, surface reconstruction and interface materials. Dangling bonds, surface defects and oxidation layer all affect how interface states are distributed. Figure 1.4a and 1.4b shows an interface state profile for a Silicon (111) surface under different reconstructions [11].

Similar to impurities in bulk semiconductors, interface states can donate or accept an electron from the conduction band or valence band, respectively. When the valence band (conduction
band) wave function contributes more to the interface state, it will have a donor-like (acceptor-like) behaviour. Expressions for the occupation probability of the interface states are the same as for impurities in a bulk semiconductor:

\[
f_{\text{donor}}(E) = \frac{1}{1 + 2 \exp \left( \frac{E_f - E}{kT} \right)} \quad \text{Eq. 1.4}
\]

\[
f_{\text{acceptor}}(E) = \frac{1}{1 + 4 \exp \left( \frac{E - E_f}{kT} \right)} \quad \text{Eq. 1.5}
\]

When an interface state becomes ionized, it must give up or receive an electron from the bulk levels. The condition of charge neutrality is stated in Equation 1.6:

\[
Q_{it} + Q_{sc} = 0 \quad \text{Eq. 1.6}
\]

\[
Q_{it} = q \left( \int D_{it,donor}(E) * (1 - f_{\text{donor}}(E)) dE - \int D_{it,acceptor}(E) * f_{\text{acceptor}}(E) dE \right) \quad \text{Eq. 1.7}
\]

\[Q_{it}\] is the interface charge, and \[Q_{sc}\] is the space charge within the bulk semiconductor. The space charge \[Q_{sc}\] can be obtained by solving Poisson’s equation and the carrier distribution function together:

\[
\nabla^2 V = Q_{sc} = q \left( N_d^+ - N_a^- - n + p \right) \quad \text{Eq. 1.8}
\]

By solving equations 1.6-1.8, the nature of space charge layer can be modeled, and classified as belonging to one of 4 types of behaviours, according to the voltage profile and bulk doping (see Table 1.2):
Table 1.2 Behaviour of space charge layer under different surface state condition [3]

<table>
<thead>
<tr>
<th></th>
<th>n-type semiconductor</th>
<th>p-type semiconductor</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Acceptor-like</strong></td>
<td>Depletion (or Inversion)</td>
<td>Accumulation</td>
</tr>
<tr>
<td>interface states</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td><img src="image1" alt="Diagram" /></td>
<td><img src="image2" alt="Diagram" /></td>
</tr>
<tr>
<td><strong>Donor-like</strong></td>
<td>Accumulation</td>
<td>Depletion (or Inversion)</td>
</tr>
<tr>
<td>interface states</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td><img src="image3" alt="Diagram" /></td>
<td><img src="image4" alt="Diagram" /></td>
</tr>
</tbody>
</table>

The case of an accumulation layer has been observed in n-type InAs surface, under cleaved surface[12], oxidated surface [13, 14] or metal covered surface [15]. The origin of interface states in each of the case is different, but an electron accumulation layer (or inversion layer for p-type InAs) formed in all three cases. The formation of an accumulation layer at the surface of InAs will have a significant effect on the electrical properties of nano-scale structures.

1.4 Scanning probe techniques

Atomic Force Microscopy (AFM) is a localized characterization method that is mainly used for topology scans with a resolution on the nanometer scale [10]. Figure 1.5 shows the basic setup of an AFM.
Two types of AFM operational mode will be discussed here. In the contact mode, an AFM cantilever is pushed against the sample. As the tip on the cantilever touches the sample, the sample pushes back against the cantilever and bends it. A laser is used to record the deflection of the cantilever. The height of the cantilever is then controlled by maintaining a constant deflection. In the non-contact mode, there is an excitation of the piezoelectric tube, causing the tube to vibrate the AFM cantilever at its resonance frequency. The AFM controller then places the cantilever at a close proximity to the sample. A laser is pointed at the cantilever and a photo-detector is used to record its vibration. The cantilever will approach the sample until the tip of the cantilever reaches within a few nanometers from the surface of the sample. The sample will then exert a van-der-Waals force on the cantilever via the tip. This force will cause a shift in the resonance frequency of the cantilever. The AFM controller will shift the height of the cantilever to maintain a constant frequency shift for the cantilever. By maintaining a fixed frequency throughout the scan, an image of topology can be recorded.

Both AFM modes operate by maintaining a fixed force either through physical contact in contact mode or a fixed resonance frequency shift in non-contact mode. The force sensing
mechanism of AFM can be modified into a large family of scanning probe techniques. Figure 1.6 illustrates some of the widely used scanning probe methods derived from AFM.

![Figure 1.6: Scanning probe techniques derived from Atomic Force Microscopy.](image)

Scanning Capacitance Microscopy (SCM) is a technique that can extract doping concentrations by measuring the capacitance across the sample. There are a few ways to implement this technique but all of them require an AC bias for high sensitivity measurements. In one implementation, an AC bias is applied to the sample and the tip held to ground. A sensor is attached to the tip to measure the capacitance. As the AFM tip scans across the sample’s surface, capacitance will vary based on the geometry and charge distribution. With proper modeling, carrier density and therefore doping concentration can be extracted from the capacitance data [18]. SCM has been used for carrier concentration profiling on multi-quantum well lasers [19], and measuring screening in InAs nanowire devices [20].

Scanning Kelvin Probe Microscopy (SKPM) is a non-invasive method for surface potential profiling. In SKPM, an AC voltage $U_{AC}$ with a DC bias ($U_{DC}$) is applied to the AFM tip. When the AFM tip is biased by an AC voltage with a frequency of $\omega$, electrostatic force will vary at the
same frequency. The electrostatic force between the tip and the sample, and the voltage bias can be related using Equation 1.9-1.11 [21]

\[
F_{DC} = \frac{dC}{dz}\left(\frac{1}{2} (U_{DC} - CPD)^2 + \frac{U_{AC}^2}{4}\right) \quad \text{Eq. 1.9}
\]

\[
F_{\omega} = \frac{dC}{dz} (U_{DC} - CPD)U_{AC} \quad \text{Eq. 1.10}
\]

\[
F_{2\omega} = \frac{dC}{dz} \frac{U_{AC}^2}{4} \quad \text{Eq. 1.11}
\]

The \(F_{\omega}\) signal in Eq. 1.10 can be nulled by controlling \(U_{DC}\) to the tip to be exactly the same as the contact potential difference (CPD). A controller can be used to minimize the \(F_{\omega}\) signal while the AFM tip is scanning across the sample. Surface potential profiling has been performed on a ZnO nanowire transistor for contact barrier observation [22], and on InP/InAsP heterojunction for depletion region observation [5].

Scanning Gate Microscopy (SGM) differs from the previous two techniques as the tip is not used as a sensor. The tip of AFM acts as a metal gate that changes the carrier concentration in the sample. As the tip scans across the sample, the current passing through the sample is measured. Using the current measured and a proper modeling of the sample, the capacitance and carrier concentration profile can be analyzed. [16] At low temperatures, Coulomb-blockade has been observed in a InAs quantum dot embedded in an InAs/InP nanowire. As the tip scans across the surface of the nanowire, the modulation voltage on the quantum dot inside the nanowire changes with tip distance [23].
1.5 Thesis Outline

Correct interpretation of an image from a Scanning Probe Microscope requires a good physical model of the sample surface. This is especially important for nanowires because of their sensitivity to external interference. A better understanding of the nanowire and its interactions with the AFM system would improve the design of nanowire experiments in the future.

The objective of this thesis is to first develop a model that incorporates the effects of charges on the nanowire conductance, and that can be used to explain the experimental results of backgating measurements of on a InAs nanowire. Secondly, the nanowire model will be used to simulate tip gating experiments. The result will be used to outline the requirements for an AFM experiment on nanowires.

In chapter two, the experimental setup for the current-voltage measurement will be discussed. In chapter three, the current-voltage measurement and nanowire model will be analyzed with finite element method modeling. In chapter four, improvements and potential AFM applications based upon the nanowire model will be discussed.
2 Experimental Setup for nanowire measurements

2.1 Nanowire sample preparation

InAs nanowires are grown using MBE in the Center for Advanced Nanotechnology (CAN) on GaAs-(100) surfaces, seeded by gold droplets. The diameters of the nanowires vary from 20nm to 80nm. Diffraction patterns obtained using transmission electron microscopy (TEM) shows that the InAs nanowires have a Wurtzite crystal structure. The nanowires are transferred onto a degenerately p-doped silicon substrate with 100nm of thermally grown oxide. E-beam lithography is used to pattern metal contacts on the nanowires. Polymethyl-methacrylate (PMMA) is used as a resist for patterning the contacts. A Ni/Au layer is chosen as the metal contact, since this form an Ohmic contact with the InAs. Figure 2.1 shows an InAs nanowire sample imaged using non-contact mode AFM.

Figure 2.1: AFM image of InAs nanowire fabricated in CAN. This InAs nanowire has a diameter of 48nm.
2.2 AFM Modification for nanowire measurements

The AFM used at CAN is a variable temperature dual AFM-STM system purchased from Omicron. This AFM’s major feature is the combination of three probing techniques (contact mode AFM, non-contact mode AFM and Scanning Tunnelling Microscopy, STM) in a single probe station. The AFM is designed to perform topology measurement on nano-scale features. Therefore, the probe station does not include any setup for current measurements and electrical isolation is needed for nano-device measurements. The probe station comes with a resistive heating connection that can be modified into an electrical contact to the sample. However, only two terminals can be created using the resistive heating connection. NWFET measurement requires three electrical isolated terminals as shown in Figure 1.2 ($V_{ds}$, $V_{gs}$ and ground). This can be done by modifying the Omicron sample holder, that is, electrically isolating both heating terminals and using the shielding plate as a ground contact. Figure 2.2 shows the modified sample holder:

![AFM sample holder with terminals labelled.](image)
The drain and back gate contact in Figure 2.2 are the original heating contact used for resistive heating measurements. Both contacts are electrically isolated from the ground plates with ceramic washers that hold the contact plates. The back gate of the sample is isolated from the ground plates by a quartz stud. Quartz is an excellent insulator (resistivity greater than 1GΩ*m) and provides excellent isolation for the back gate. However, quartz is a poor thermal conductor with thermal conductivity of 1.3W/(m.K) [24]. If low temperature measurements are implemented, the quartz stud should be replaced by a thermally conductive but electrically insulating ceramic such as sapphire (thermal conductivity of > 18W/(m.K)) [24]. Ultra-high vacuum varnish is used to glue the sample onto the quartz stud.

The sample holder and the sample are connected manually. In order to fit the modified sample holder into the AFM probe station, the sample must be smaller than 10mm by 7mm. A piece of indium is used to press a gold wire against the patterned gold contact on the sample. This ensures a good electrical connection between the sample holder and the sample. During the process of setting up the AFM sample holder, one hand must be connected to the ground through a metal wire, and anti-static mat must be used on both the lab table and on the ground to avoid electrostatic build up.

InAs nanowires can be easily damaged because of their small diameter. Electric current passes through the nanowire only, unlike bulk samples which have a large volume for current to pass through. For example, a current of 10µA passing through a nanowire with a diameter of 40nm will result in a current density of 7.9x10^5 A/cm^2. In addition, there are limited numbers of paths for heat to dissipate from a nanowire – the sample is placed under UHV conditions. Heat can
only dissipate through the metal contacts, thermal oxide, or through radiation. These two factors combine to make nanowire extremely fragile and many samples were burned either before measurement due to electrostatic discharge or during the measurement due to the high current used. In order to work around this problem, a low voltage bias is used during experiments and a protection circuit is implemented.

The sample holder's drain contact is connected to the external circuitry such as voltmeter or electrometer. Any external noise or electrostatic discharge will pass directly through the nanowire. Such noise or discharge can damage or destroy the nanowire. A grounding circuit is used to protect the nanowire from these noise sources. The schematic of the grounding circuit is shown in Figure 2.3. The grounding circuit holds the nanowire at ground at all times, until the electrical equipment is ready for current-voltage measurements. 10MΩ resistors are used to prevent any large current from passing through the nanowire accidentally. Voltage pulses in the order of millivolts will generate a current in the range of picoamps when the grounding circuit is switched on.

![Grounding circuit schematic](image.png)

**Figure 2.3:** Grounding circuit for nanowire measurements.
2.3 Experimental setup of back-gating/tip-gating nanowire

InAs is a relatively conductive semiconductor with intrinsic carrier concentration of $1 \times 10^{15}/cm^3$.

NWFET measurements made on InAs nanowire require a low voltage bias and a sensitive current meter. Electrometers are commonly used for high sensitivity measurements at low-current. Figure 2.3 shows the setup of a NWFET measurement. An Agilent E363A voltage source is connected to a voltage divider in order to obtain a low resistance and low noise voltage source, in the millivolt range. The output of the millivolt bias is then fed to the inner shield of the Keithley 617 electrometer’s tri-axial cable. In the low-current mode, the inner shield is at the same potential as the current carrying wire, hence minimizing the leakage current between the two conductors. A differential amplifier is used to extract the current from the electrometer.

Figure 2.4: AFM system setup for low voltage-low current NWFET measurement. a) Photo of the tip-sample system. b) Heating contact port modified for electrical contacts. The four switches on the port panel are the grounding switches shown in Figure 2.2.
Both the back gate voltage and the drain voltage are connected to the AFM system through the modified heating contact port shown in Figure 2.3b. The tip voltage can be directly controlled by either the AFM system software, or by connecting to a voltage source externally. The voltage control is not programmable using the system software, and therefore, a function generator is used as an external voltage input to the AFM tip. The function generator is also used for the back gate voltage. The leakage current passing through the tip gate and back gate are both negligible.

The Omicron AFM comes with two external input ports for data collection. One port is reserved for recording the current value from the electrometer. The other port is used to record either the tip gate voltage or the back gate voltage. The AFM tip scans across the nanowire and can be stopped at any point along the nanowire. AFM software is used to control the height of the tip from the sample. Gating measurements can be made while holding the AFM tip at a fixed distance from the nanowire.
3 Result and Discussion

3.1 Modeling of nanowire using back gating data

3.1.1 Parameter extraction from simplified NWFET model

An InAs nanowire is characterized using the NWFET setup discussed in chapter 2. An AFM scan shows that the diameter of the nanowire is 40nm. The distance between two contacts (source and drain) of the nanowire is 500nm. The oxide thickness is 100nm. A DC voltage of 2.5mV is applied across the nanowire. The main reason for using such a low drain voltage is to avoid damaging or destroying the nanowire during measurement, which can take up to half an hour to complete. A voltage of -5V to 5V is applied to the back gate of the sample. The purpose of the back gate measurement is to extract the basic parameters of the nanowire, such as mobility and carrier concentration. Figure 3.1 shows the back gating measurement of the InAs nanowire taken by the AFM system.

![Figure 3.1: Back gating measurement of InAs nanowire biased at 2.5mV.](image)
The nanowire is n-type, as the drain current increases with increasing back gate voltage. This observation is consistent with reported behaviour [6]; that is, as-grown InAs nanowires are invariably n-type.

In this AFM, all V-I characteristics are measured using two terminals. This method will include the contact resistance between the nanowire and the metal. A simplified model below shows a typical way to remove contact contribution from the nanowire resistance [25, 26]. In order to obtain an accurate contact resistance of the nanowire, a four point contacts V-I measurement must be made. It can be done by performing such a measurement before putting the sample into the AFM, or modify the AFM sample chamber with two additional electrical contacts.

![Simplified model of NWFET setup.](image)

Base on estimations of the contact resistance from other samples measured with four point contacts method, the contact resistance of the nanowire should be in the range of thousands of kilohms. The calculated transconductance taken at 0V bias without contact resistance is 4.33nA/V.

The oxide capacitance between a back gate and a nanowire can be approximated using the following equation [27]:

\[ C = \frac{Q}{V} \]
\[
\frac{C}{L_G} = \frac{2\pi \varepsilon_0 \varepsilon_{\text{oxide}}}{\cosh^{-1}(t/R)}
\]

Eq. 3.1

L is the length of the nanowire; t is the distance between the center of the nanowire and the back gate; R is the radius of the nanowire; \( \varepsilon_{\text{oxide}} \) is the effective dielectric constant of the oxide adjusted for a non-embedded NWFET. The oxide capacitance is calculated to be \( 24.7 \times 10^{-18} \text{F} \).

The electron mobility is calculated as \( 175 \text{cm}^2/\text{Vs} \) using equation 1.1. Electron concentration is calculated using equation 1.2. The concentration under zero bias is \( 1.2 \times 10^{18} / \text{cm}^3 \).

This mobility is very low, even compared with other InAs nanowire mobility reported in the literature. The bulk value of mobility of electron in InAs is in the range of \( 10^4 \text{ cm}^2/\text{Vs} \) [10]. Firstly, field-effect mobility is an underestimation of the actual mobility. Secondly, equation 3.1 only includes the oxide capacitance between the back gate and the nanowire. This capacitance calculation assumes a metal-like surface for the nanowire and also that the nanowire is free of surface states. Lastly, given the high electron concentration and implied high concentration of ionized donors, ionized impurity scattering is likely to be the dominate scattering mechanism controlling electron mobility. In such sample, with high levels of compensation, a low \( \mu \) values can be expected. The simplified model cannot provide an understanding of how surface states interact with the nanowire and how the back gate depletes the nanowire of its carriers.

### 3.1.2 Modeling of nanowire system using the finite element method

The simplified model in section 3.1.1 cannot reveal how surface charges interact with the nanowire. In order to model the distribution of electrons inside a nanowire, a 2D model is developed for the cross-section of the nanowire. COMSOL Multiphysics is used for the finite
element calculations. The goal of the 2D model is to calculate the electron distribution in a nanowire under the effect of surface states and a back gate voltage, and understand the role of surface states on the conductance of the nanowire.

Figure 3.3 shows the geometric setup of the simulations. The software generates mesh according to geometry complexity. The mesh density increases with decreasing feature size, such as in the region of the nanowire. The foundation of the model is Poisson’s equation (Eq. 1.8). The voltage is defined as the energy difference between the conduction band and the Fermi level. Table 3.1 summarize all functions used in the 2D model.

![Diagram of 2D finite elements simulation of nanowire electron distribution. The three domains are the oxide and vacuum with no charge and the semiconductor nanowire with free carriers. The circle below the nanowire label is where the surface charges are located.](image)

**Figure 3.3:** 2D finite elements simulation of nanowire electron distribution. The three domains are the oxide and vacuum with no charge and the semiconductor nanowire with free carriers. The circle below the nanowire label is where the surface charges are located.
Table 3.1: Parameters involved in 2D finite elements simulation for nanowire electron distribution [1, 28].

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Equations</th>
</tr>
</thead>
<tbody>
<tr>
<td>2D Potential profile – Poisson’s equation</td>
<td>Eq. 3.2 ( \nabla^2 V = \frac{q}{\varepsilon_0 \varepsilon_r} * (N) )</td>
</tr>
<tr>
<td>Total charges</td>
<td>Eq. 3.3 ( N = Q_{\text{bulk}} + Q_{\text{surf}} + Q_{\text{doping}} + Q_{\text{fix}} )</td>
</tr>
<tr>
<td>Bulk carriers</td>
<td>Eq. 3.4 ( Q_{\text{bulk}} = N_v \cdot f_{\text{hole}} - N_e \cdot f_{\text{electron}} )</td>
</tr>
<tr>
<td></td>
<td>Eq. 3.5 ( f_{\text{electron}} = \frac{2}{\sqrt{\pi}} \int_0^\infty \frac{\sqrt{x}}{1 + \exp \left( x - \frac{qV}{kT} \right)} , dx )</td>
</tr>
<tr>
<td></td>
<td>Eq. 3.6 ( f_{\text{hole}} = \frac{2}{\sqrt{\pi}} \int_0^\infty \frac{\sqrt{x}}{1 + \exp \left( x + \frac{(qV + E_g)}{kT} \right)} , dx )</td>
</tr>
<tr>
<td>Surface states</td>
<td>Eq. 3.7 ( Q_{\text{surf}} = N_{\text{surf}} * f_{\text{surf}} )</td>
</tr>
<tr>
<td></td>
<td>Eq. 3.8 ( f_{\text{surf}} = \int_{-\infty}^{\infty} N_{\text{surf}}(E) \cdot (1 - f_{\text{donor}}(E)) , dE )</td>
</tr>
<tr>
<td>Doping impurities</td>
<td>Eq. 3.9 ( Q_{\text{donor}} = N_{\text{donor}} * f_{\text{donor}} )</td>
</tr>
<tr>
<td></td>
<td>Eq. 3.10 ( f_{\text{donor}} = \frac{1}{1 + 2 \exp \left( \frac{qV + E_d}{kT} \right)} )</td>
</tr>
<tr>
<td>Fixed charges</td>
<td>( Q_{\text{fix}} )</td>
</tr>
</tbody>
</table>

As discussed in section 1.1, there are various charges around the nanowire which will affect its conductance and its gating behaviour. There are four types of charges to be examined in the nanowire simulation: bulk free carriers, surface state donors, doping impurities, and fixed charges inside the nanowire. Bulk free carriers are modeled with the 3D density of states with electrons obeying Fermi-Dirac statistics. Surface state donors are modeled using a surface state distribution function.
There are several assumptions made to simplify the 2D model:

1) The simulation is done in two dimensions for back gating, to take advantage of the axial symmetry of the nanowire-backgate system (this symmetry will be broken for the tip gating simulations in section 3.2). 2D finite element simulations greatly reduce the number of elements involved and reduce the simulation time. There is strong support in the literature that Ohmic contacts exist for metal/InAs interfaces and therefore, the influence of the contacts is minimal.

2) The model assumes electron conductance from either surface donors or bulk donors and ignores the possibility of acceptors on the surface of the nanowires. While acceptor-like surface states can be incorporated, there is no indication of a significant hole contribution in any of the current measurements.

3) The carrier concentration calculated is based on the drift current assumption (from Eq. 1.2). In a semiconductor, both drift and diffusion currents exist to form the total current as shown in equation 3.11 below:

\[ J_n = q \cdot \left( n \mu_n \frac{E}{d} + \mu_n \frac{kT}{q} \frac{dn}{dx} \right) \]

Eq. 3.11

However, single crystal nanowires are homogenous devices and differences in carrier concentration between the two contacts are negligible. Also, the carrier concentration (n) of the wire is sufficiently high compared with the gradient of concentration (dn/dx). In the present case, it is safe to assume that conduction is mainly through drift, rather than diffusion.

4) The classical 3D density of states is used for the bulk carrier concentration calculations. Although the nanowire has a diameter of 40nm, the 1D quantized states is not used in the
simulations. The sample is characterized at room temperature and has a very high electron density. The electrons are distributed across a few quantized states in the nanowire’s conduction band. A Poisson-Schrodinger’s self-consistent equation is difficult to solve when many quantized states must be included. It is still possible to approximate the density with the classical 3D bulk density of states at room temperature and when many quantized state are filled (or partially filled). A more detailed calculation is given in the appendix.

The simulated carrier concentration is plotted against the carrier concentration extracted from the experimental measurements using Eq. 1.2 in Figure 3.4. Figure 3.5a-f shows the electron concentration across the InAs nanowire.

Figure 3.4: Simulation of InAs nanowire carrier concentration under back gate bias. The light gray plot is the extracted carrier concentration from the experimental data in Figure 3.1.
Figure 3.5 a-f: Electron concentration of InAs nanowire at different back gate voltage from top left to bottom right 3V, 1V, 0V, -1V, -3V -5V. Electrons are pinned at the surface.

The parameters used in the simulations are as follows: 1.3x10^{12}/cm^2 for surface state density and the state energy is centered at 0.3eV above the conduction band at the surface. The
surface state density is assumed to have a Gaussian profile with a standard derivation of 1kT (around 25mV for room temperature). The actual surface state density distribution can be measured with a different experiment. The difficulty of measuring the surface state density will be addressed in the future work section. This simulation assumes no fixed intentional doping and no fixed oxide charges around the nanowire. The bandgap of InAs is 0.5eV, for the Wurtzite crystal structure [29]. The temperature used in the simulations is 300K. The effective mass for electrons in InAs is 0.023m₀. The simulations are performed from 3V to -5V with 0.5V steps.

The simulations clearly show that the electron concentration is highest around the surface of the nanowire due to the existence of surface state donors. This is in agreement with observation for bulk like InAs surface, where an accumulation layer exists on the InAs oxide interface. As the back gate voltage increases, electrons at the surface are being depleted at the bottom of the nanowire. In Figure 3.4, the simulation agrees quite well with the experimentally extracted electron concentration except near the depletion region. In the depletion region, the extracted electron concentration is lower than the simulated value in general and has a more logarithmic characteristic. The derivation can be attributed to how the surface state density is modelled. The surface state density might not be a perfect Gaussian and therefore will have a different screening behaviour. The accurate modeling of surface state density will be further discussed in section 4.2.

Figure 3.6 shows the voltage profile (difference between Fermi level and the conductance band minimum) from the top of the nanowire to the bottom of the nanowire. The back gate voltage changes from 0V to -5V back gate bias. At 0V bias, the Fermi level of the nanowire remains
above the conduction band minimum. As the back gate voltage decreases, the top of the nanowire remained strongly pinned while the bottom of the nanowire is pulled down. This corresponds to electron depletion, as shown in Figure 3.5. The back gate voltage is screened non-uniformly across the nanowire.

![Fermi level calculated relative to conduction band minimum](image)

**Figure 3.6**: Fermi level of nanowire measured vertically from the top of the nanowire (0nm) to the bottom of the nanowire (40nm).

Figure 3.7 shows the voltage profile for the nanowire with no back gate bias and approximating of the profile using a cosh function and an exponential function. The hyperbolic cosine profile is a sum of two exponential functions, each profile decays exponentially from the surface of the nanowire. In a typical bulk samples, the electric field can be screened completely for a sufficiently large depth. The nanowire has a limited depth, and electrons inside the nanowire
experience the external field from all around the nanowire. This different makes screening much weaker in nanowires than their bulk counterpart.

3.1.3 Parameteric analysis of the nanowire system

In the previous section, the nanowire model was used to investigate surface state density and the gating behaviour of the nanowire. One can also use the nanowire model to examine the effect of different charges has on the nanowire. Table 3.2 listed the parameters that will be studied for their influence on nanowire conductance.

Figure 3.7: Fermi level profile approximated by exponential functions.
Table 3.2: Parameters investigated using 2D finite elements model of nanowire.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Range</th>
<th>Reason</th>
</tr>
</thead>
<tbody>
<tr>
<td>Nanowire doping concentration</td>
<td>1x10^{15} to 1x10^{17} (cm^{-3})</td>
<td>Relationship between intentional doping and surface states</td>
</tr>
<tr>
<td>Surface donor concentration</td>
<td>1.25x10^{12} to 1.28x10^{10} (cm^{-2})</td>
<td>Determine the concentration for lower electrical conductance</td>
</tr>
<tr>
<td>Nanowire radius</td>
<td>R = 20nm to 60nm</td>
<td>Effect of surface state on different nanowire size</td>
</tr>
<tr>
<td>Surface donor energy level (E_D - E_C)</td>
<td>0.3eV to -0.3eV</td>
<td>Effect of different surface state distribution</td>
</tr>
</tbody>
</table>

The first parameter to be examined is the doping concentration in the nanowire. It is a common practice to dope a semiconductor in order to change its electrical properties. However, doping of nanowires is not as straightforward since the bulk doping can be compensated by the surface donor states. Figure 3.9 shows how the electron concentration changes as doping varies.

Figure 3.8: Electron concentration of nanowire under different doping assumption. The value Nd represent n-doping concentration, Na represent p-doping concentration. Energy level of donors are assume to be 0.001eV below/above the conduction/valence band (shallow donors/acceptors), respectively.
The simulated data shows that with a surface donor level of $1.25 \times 10^{12} / \text{cm}^2$, there is virtually no change in electron concentration until the nanowire is highly doped with acceptors. This is not surprising given the large surface area to volume ratio for a nanowire. The number of states inside the nanowire must be sufficiently high such that they can compensate the number of surface states around the nanowire. This indicates that when any device is to be made using a nanowire, one must reduce the concentration of surface states so that the properties of the nanowire will not be dominated by the surface.

The second parameter to investigate is surface donor concentration. Surface donors directly control the concentration of free carriers in the nanowire. The main focus is on the gating behaviour of the nanowire and how surface donors influence the conductance of the nanowire. The measured gating curve in Figure 3.4 indicates a change in electron concentration from $10^{18} / \text{cm}^3$ to $10^{17} / \text{cm}^3$ for a surface donor concentration of $1.3 \times 10^{12} / \text{cm}^2$.

![Figure 3.9: Electron concentration of nanowire under back gate bias with different surface donor concentration.](image)
At a surface donor concentration of $1.25 \times 10^{12}/\text{cm}^2$, there is little change in electron concentration over -5V of back gate voltage. When the surface donor concentration is reduced by a factor of five (i.e., to $5.0 \times 10^{11}/\text{cm}^2$) the threshold voltage is increases to -2V~-3V range. Depletion of the nanowire can occur at -1V by further reduction in the surface donor concentration below $2.5 \times 10^{11}/\text{cm}^2$ (cases of $2.0 \times 10^{11}/\text{cm}^2$ to $1.28 \times 10^{10}/\text{cm}^2$ is shown). By reducing the carrier concentration, the bulk properties of the nanowire will be more apparent.

The next parameter to examine is the nanowire radius. Figure 3.10 shows the voltage profile for nanowires with radius from 20nm to 60nm - the typical of the range of nanowire radius for MBE growth.

**Figure 3.10:** Fermi level of nanowire from top to bottom relative to the conduction band minimum.
Figure 3.11 shows how the carrier concentration increases with decreasing concentration.

Figure 3.11: Relationship between radius of nanowire and electron concentration under a surface donor density ($N_{\text{surf}}$) of $1.25 \times 10^{12}$ cm$^{-2}$.

As the radius of the nanowire decreases, the effect of surface donor increases accordingly. The Fermi level increases on the nanowire periphery as the nanowire shrinks in diameter. The electrons are being squeezed into a smaller volume. However, one should note the approximation to neglect quantum confinement with nanowires having lower electron concentration and smaller radius.

The last parameter to be analyzed is the surface donor energy level. In the analysis so far, the surface donor energy level is centered at 0.3eV above the conduction band minimum. Figure
3.12 below shows the simulation with a fix surface donor concentration with donor energy level changing from above to below the conduction band minimum.

![Graph showing surface state energy level's effect on gating and concentration](image)

**Figure 3.12:** $V_{gs}$-$I_{ds}$ simulation with surface donor energy level changing from 0.3eV above the conduction band to -0.3eV below the conduction band.

As the surface donor energy is lowered to below the conduction band minimum, the concentration of ionized surface donors decreases. There will be very few ionized surface donors when the surface donor energy approaches the mid-gap of the semiconductor. When the surface donor energy level is located at 0.2eV to 0.3eV below the conduction band minimum, most of the surface donors are not ionized and the electron concentration is about the same as for an intrinsic InAs sample ($10^{15}$/cm$^3$). Figure 3.12 shows the backgate voltage needed to ionize surface donors. When the donor state energy is centered above the conduction band minimum,
most of the donors are ionized and the screening is provided by mobile electrons inside the nanowire. When the donor state energy is below the conduction band minimum, most donors are not ionized. Therefore, the donor states will screen out the electric field from the back gate when the donor state energy is centered at the mid-gap. The sharp transconductance observed near zero bias for simulations with surface donor energy near mid-gap is caused by the lack of screening by either surface states or free carriers.

The analysis so far assumes that the dominant source of mobile electrons comes from the surface donors. However, it is possible to simulate the nanowire current characteristics by assuming mobile carriers originate from the bulk instead, whatever the source of the bulk charge is. From table 3.1, we replace the contribution from surface donors by setting the fixed charges equal to $1.3 \times 10^{18}/\text{cm}^3$. All electrons that are originally created by ionized surface donors are now generated by positive fixed charges inside the nanowire. Figure 3.13 shows a comparison of electron concentration versus back gate voltage between the surface donor model and the fixed charge model.
Figure 3.13: Comparison of gating characteristics for fix charges model and surface donor model.

There is not a significant difference between surface donor model and fixed charge model, other than the small derivation for the positive back gate bias. This identical behaviour can be attributed to the fact that screening in both models are caused by mobile electrons. In the surface donor model, most of the donors are already ionized and do not contribute to screening. The situation is similar to the fixed charge model, in which the fixed charges inside the nanowire do not contribute to screening. The deviation at positive bias voltages can be attributed to electrons filling up ionized surface donor states as the positive back gate voltage attracts electrons.

Although the relationship between back gate voltage and electron concentration is nearly identical for both models, the 2D finite element model reveals an important difference between the two models by plotting electron concentration across the surface. Figure 3.14 shows the electron concentration across the nanowire under back gate voltages of 3V to -5V.
Figure 3.14a-f: Electron concentration of InAs nanowire using fixed charges model at different back gate voltage from top left to bottom right: 3V, 1V, 0V, -1V, -3V, -5V. The white area represents high electron concentration. Note that the electrons are no longer pinned at the surface.

A major difference between electron concentration in Figure 3.14 and Figure 3.5 is the electron’s location under negative voltage bias. For the surface donor model, electrons
accumulate at the surface of the nanowire. For the fixed charge model, the electrons are concentrated at the center of the nanowire. The Fermi level at the nanowire surface is not pinned in the fixed charge model. In order to differentiate which models are more appropriate in describing the electrostatics of the nanowire, a different technique other than back gating must be used.

3.1.4 Summary

Section 3.1.1 described the experimental results for an InAs nanowire back gating measurement and extracted the basic parameters of the nanowire. An electrostatic model is developed in section 3.1.2 to describe the conductance of the nanowire using 2D finite elements method running in COMSOL Multiphysics. Section 3.1.3 investigates the properties of the nanowire by using a parametric analysis. The four parameters explored are bulk doping concentration, surface donor concentration, nanowire radius and donor energy level. A comparison between the surface donor model and the fixed charge model is also made.
3.2 Tip gating of a InAs nanowire

3.2.1 Modeling of tip-nanowire system and the effect of surface charges

With the knowledge of nanowire surface modeling in section 3.1, a three dimensional finite element model can be developed to analyze the interaction between an AFM tip and the nanowire. Figure 3.15 shows the 3D model of the nanowire-tip system simulated in COMSOL Multiphysics.

The AFM tip is a non-contact mode tip covered with tungsten purchased from ND-MDT. The tip radius is set to 35nm and a tip angle of $22^\circ$ as specified by the manufacturer. The tip is placed 20nm above the nanowire (a standard distance for electrostatic measurement). All parameters of the nanowire are identical to the 2D model. The contacts are assumed to be Ohmic and are pinned above the conduction band minimum as reported in the literature. The 3D model first
calculates the charge distribution of the nanowire under a fixed tip voltage and back gate voltage. The program then divides the nanowire into 2.5nm pieces and calculates the conductance of each piece individually. The total conductance of the nanowire is then calculated by combining all the conductances of the nanowire.

Using the 3D tip-nanowire model, one can compare the effect of different tip radius has on tip gating nanowire. The simulation is performed for four different tip radii: 2nm, 35nm, 50nm and 100nm. The 2nm tip radius corresponded to a super-sharp tip AFM tip. Table 3.3 lists the dimensions and properties of normal AFM tips and a super sharp tip. The simulation first determines what happens if the tip is damaged and has a larger radius when performing tip gating, and second by how a super-sharp tip will help to improve the resolution of field effect probing techniques such as tip gating.

### Table 3.3: Specification of a normal AFM tip from ND-MDT and a super sharp tip from Nanosensor.

<table>
<thead>
<tr>
<th>Name</th>
<th>Tip radius</th>
<th>Cone angle of the tip</th>
<th>Tip aspect ratio</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>NSG01 (ND-MDT) Conductive tip</td>
<td>35nm</td>
<td>22°</td>
<td>From 3:1 to 7:1</td>
<td>Tungsten Carbide (WC) Coated</td>
</tr>
<tr>
<td>Non-contact mode</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SSS-NCL (Nanosensor) Super</td>
<td>2nm</td>
<td>10°</td>
<td>4:1</td>
<td>Highly doped silicon</td>
</tr>
<tr>
<td>sharp tip</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Non-contact mode</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Although the manufacturer’s specification of the AFM tip is 35nm, it is always possible to damage the AFM tip during the process of image scanning. During an AFM nanowire scan, it usually takes a few hours to days in order to search for the exact location of the nanowire.

During this process, numerous scans are made in order to locate the nanowire. Tip damage will cause an increase in tip radius. The damage can manifest itself in two ways: convolution of the
nanowire topology scan and increase of transconductance during tip gating. De-convoluting the topology image of the AFM scan shows that the radius of the AFM tip is approximately 150nm. Actual tip radius can be obtained by measuring the radius directly under a Scanning Electron Microscopy (SEM). Figure 3.16 shows the simulated conductance of nanowire under tip voltage bias change from 0V to -5V under five different conditions.

Table 3.4: The six different conditions examined in Figure 3.16.

<table>
<thead>
<tr>
<th>Case</th>
<th>Tip radius used</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>2nm</td>
<td>Super-sharp tip is modeled</td>
</tr>
<tr>
<td>B</td>
<td>35nm</td>
<td>Conductive non-contact tip</td>
</tr>
<tr>
<td>C</td>
<td>50nm</td>
<td>Damaged conductive non-contact tip</td>
</tr>
<tr>
<td>D</td>
<td>100nm</td>
<td>Damaged conductive non-contact tip</td>
</tr>
<tr>
<td>E</td>
<td>150nm</td>
<td>Damaged conductive non-contact tip</td>
</tr>
<tr>
<td>F</td>
<td>150nm</td>
<td>Damaged conductive non-contact tip with a surface fix charge density of one electron per 30nm by 30nm.</td>
</tr>
</tbody>
</table>

Figure 3.16: Six cases with simulation of 3D models against experiments data. Tip radius of A (top most): 2nm, B: 35nm, C: 50nm, D: 100nm, E: 150nm, F: tip radius of 100nm and a oxide charge density of $1e_0/(900\text{nm}^2)$. 
The transconductance of the nanowire increases as the tip radius increases as shown from case A to case D. However, in order to approximate the measurement of the tip gating data, sheet negative charges of $1e_0/(900\text{nm}^2)$ are added to the interface between the vacuum and the oxide domain (shown in Figure 3.15) in case E. These charges can occur after a back gating experiment because the oxide layer contains many charges that can response to the back gate potential. It has already been shown that oxide layer contains mobile charges that had been measured with frequency analysis in a NWFET measurement [25]. The approximation in case E agrees with the experimental measurement quite well but begin to deviate as negative tip gate bias increases beyond -2V. Similar deviation is observed in back gating measurement in Figure 3.4. Two assumptions are probably causing this inaccuracy, namely, the assumption of drift current and the assumption of bulk density of states. Under a large tip gating voltage, the charge density along the nanowire is no longer uniform, unlike the case of back gating measurement. The electron transport deviates from being drift current dominated. However, the effect of diffusion current will still be minor if the tip is creating a symmetric profile on both half of the nanowire – as assumed in the 3D model. Another effect not considered in the 3D model is confinement quantization. The density of states will deviate from the bulk density of states to a 1D density of states. The more detailed calculation is given in the appendix.

3.2.2 Voltage profile analysis of the surface potential of a tip-nanowire system

Figure 3.17 shows the electron concentration of a nanowire biased at 3V, 0V, -3V and -5V using tip gating in case E. The distribution is essentially the same as a back gated nanowire except that the depleted area in a tip gated nanowire is smaller than in the back gated nanowire.
Figure 3.17: Electron concentration of InAs nanowire using fixed charges model at different back gate voltage from top left to bottom right 3V, 0V, -3V -5V. The white area represents high electron concentration.
Figure 3.18 to Figure 3.21 shows the surface potential of the nanowire from contact to contact with tip gate bias of 0V, -3V and -5V. The angle $0^\circ$ and $360^\circ$ represent the bottom of the nanowire, and $180^\circ$ represent the top side of the nanowire facing the tip. The spread of surface potential is examined in the following figures.

Figure 3.18 a-c: Case A, simulation of tip gating with tip radius of 2nm, tip gate bias at 0V (left), -3V (center), -5V (right).

Figure 3.19 a-c: Case B, simulation of tip gating with tip radius of 35nm, tip gate bias at 0V (left), -3V (center), -5V (right).
As shown in Figure 18 and Figure 19, the use of a super sharp tip can indeed reduce the surface band bending from the AFM tip. This property is important for scanning techniques such as Scanning Kelvin Probe Microscopy where minimal surface band bending is often assumed.

Surface potential only decreased by 0.05V under the tip even a -5V bias is used. However, one should note that the lateral resolution of a super sharp tip is similar to that of a normal AFM tip.

Figure 3.20 a-c: Case C, simulation of tip gating with tip radius of 50nm, tip gate bias at 0V (left), -3V (center), -5V (right).

Figure 3.21 a-c: Case D, simulation of tip gating with tip radius of 100nm, tip gate bias at 0V (left), -3V (center), -5V (right).
Figure 3.20 and 3.21 shows the surface potential of a nanowire under tip gating with tip radius of 50nm and 100nm, respectively. The increase of surface potential spread between a 35nm tip and 50nm is minimal, but the increase of surface potential spread between a 50nm tip and 100nm is significant. The increase in surface potential spread is also non-isotropic, for the field cannot penetrate around to the bottom of the nanowire but spread further along the nanowire.

The simulation of Case E is almost identical to the simulation of Case D because the only difference between the two cases is the addition of oxide charges. The gating behaviour is identical since the same tip is used to gate the nanowire.

![Figure 3.20 and 3.21: Surface potential of a nanowire under tip gating with tip radius of 50nm and 100nm, respectively.](image)

Figure 3.22 a-c: Case E, simulation of tip gating with tip radius of 100nm with oxide charges, tip gate bias at 0V (left), -3V (center), -5V (right).

The voltage profile spread on the surface of the nanowire can be used to approximate the resolution of an AFM tip for scanning probe techniques that employs electric potentials. The largest voltage profile spread occurs at the top portion of the nanowire in the longitudinal direction. The voltage profile of the line at the top of the nanowire is taken and a Gaussian approximation is made to quantify the resolution of the AFM tip. Eight approximations are
made for AFM tip with tip radius of 2nm, 4nm, 8nm, 16nm, 35nm, 50nm and 100nm. Figure 3.23 and 3.24 shows such calculations for case E and case A.

Figure 3.23: Gaussian approximation of voltage profile for nanowire under tip bias of -5V (tip radius = 100nm).

Figure 3.24: Gaussian approximation of voltage profile for nanowire under tip bias of -5V (tip radius = 2nm).
A Gaussian function is used to approximate the voltage profile for tip gating with a tip gate bias at -5V. The standard deviation is used to characterize the spread of the voltage profile. These results are combined and plot in Figure 3.25.

**Figure 3.25:** The effect of tip radius on lateral resolution characterized by voltage profile spread. The tip radiiuses used for simulation are 2nm, 4nm, 8nm, 16nm, 35nm, 50nm and 100nm.

Figure 3.25 shows that as the tip radius is the dominant factor that determines the voltage potential spread on a nanowire. The voltage profile spread increases significantly when the tip radius increases from 50nm to 100nm. As the tip radius reduces to less than 20nm, the potential spread saturates at about 17nm. The reason for this limit can be explained by the screening of the electric field in a nanowire. Screening of electric field is provided by mobile electrons inside a nanowire as mentioned in section 3.1.3. For a small tip radius, the nanowire can sufficiently screen out the electric field from the tip. However, once the tip depleted the electrons in the area under the tip, the screening must be provided by the electrons further out...
from the tip. This is similar to the situation shown in Figure 3.17 where although the bottom of the nanowire remains conductive, the top half of the nanowire is depleted of carriers. Once that happens, the tip geometry will become a dominating factor because the larger the tip, and larger the depleted area and screening must be provided the electrons further down the nanowire.

3.2.3 Summary

In this section, the effect of tip gating on nanowire is examined. A 3D finite element model is developed in order to simulate the experimental data collected by the AFM measurements. Different tip radii are used in simulations in order to find the best approximation to the experimental data. Surface voltage spread is examined using surface potential plot of the nanowire under different tip gating condition. The effect of screening by mobile electrons and the effect of tip geometry in tip gating are discussed.
4 Conclusions and Future Work

In this thesis, the role of electric field on nanowire conductance was examined from two perspectives: first to develop a model that will help provide understanding of how conductance relates to surface charges and an external applied field, such as a backgating; Second, to develop a model to include the effects of a metallic tip and outline the requirements for an AFM experiment. Here are the conclusions taken from the analysis:

- A surface state model can be used in nanowire modeling to predict the gating behaviour of the nanowire. An InAs nanowire was modeled by a surface donor concentration of 1.3x10^{12}/cm^2 using a Gaussian surface donor profile.

- The nanowire’s conductance will be dominated by surface states when the state density is sufficiently high and located close to or above the band edges. In the case of InAs, one must reduce the donor density to below 10^{11}/cm^2 in order for the bulk properties of the nanowire to dominate.

- The energy level of the surface states determines under what conditions the surface states will be ionized – When the states lie above the conduction band minimum, surface donors will contribute mobile electrons, forming an accumulation layer at the surface. When they lie below the conduction band minimum, the donors will contribute to screening of the external field.
• The use for super sharp tips can help reduce surface band bending as shown in Figure 3.18. However, the lateral resolution of the tip remains unchanged because the screening of the nanowire is dominated by mobile electrons for radii less than 20nm.

• For scanning probe techniques that employ a tip bias, any features smaller than 40nm will be heavily convoluted, even with a super sharp tip.

The AFM system that is modified to carry out conductivity measurement can be improved and expanded in many ways. The following are a few possible directions:

• Modify the sample holder to include temperature variation. The AFM system allows the sample station to be cooled down to 22K using helium cooling. However, the current setup of the sample holder must be modified also to improve thermal conductivity between the sample and the sample station. The advantage of implementing a low-temperature measurement is that quantum confirmation effect can be measured more precisely in low temperature than it is in room temperature [30].

• Combine AFM/STM measurement for surface state probing. The Omicron AFM system has a dual control system for AFM and STM. The two methods of measurement can be switched when employing a sufficiently sharp tip. While it is difficult to locate the nanowire with STM, it is possible to do so with AFM. One possible way to quantify the surface state density function is to use an STM scan on the nanowire.

• Passivate the surface of a nanowire (or at least, for InAs nanowires). It had been shown that passivation can reduce surface state density [31, 32]. It is clear that a high surface
donor density will cause such a high electron concentration in the nanowire. This can make many experimental observations impractical, such as full depletion of nanowires.

AFM is a scanning technique that provides many methods for investigating and measuring parameters of nanostructures. With a good sample preparation procedure, proper modeling and the correct experimental setup, AFM can be an extremely useful method and can be used extensively in nanotechnology research.
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Appendix – Quantization of energy states in nanowires

The radius of nanowire is small enough for quantum confinement to occur. One can identify the quantized energy level of a nanowire by solving the Schrödinger’s Equation in cylindrical coordinates. The Schrödinger’s Equation states that:

$$E\Psi(r) = \left(-\frac{\hbar^2 \nabla^2}{2m^*} + V(r)\right)\Psi(r)$$

Eq. 4.1

As an elementary analysis, the equation is simplified with the following assumptions:

1) Voltage is zero inside the nanowire and infinite everywhere else. This assumption place a zero boundary condition for the wave function at the edge of the nanowire.

2) All material parameters outside of the nanowire are omitted.

After solving Eq. 4.1 using separation of variables, one will arrive at the following equations:

$$\Psi(r) = Z(z)\Phi(\theta)R(r)$$

$$R(r) = J_l\left(\frac{2m^*E}{\hbar^2}r\right) Z(z) = \exp(\pm ik_z z) \quad \Phi(\theta) = \exp(\pm il\theta)$$

$J_l(r')$ is the Bessel function. The energy level $E$ can be found by applying the zero boundary condition of the wave function ($R(20\text{nm}) = 0$). The first 10 energy levels of the nanowire are listed in table 4.1.
Table 4.1: Calculated energy level of InAs nanowire with radius of 20nm.

<table>
<thead>
<tr>
<th>Quantum number (l, n)</th>
<th>Zeros of Bessel function</th>
<th>Energy level (eV) relative to conduction band minimum</th>
</tr>
</thead>
<tbody>
<tr>
<td>l=0, n=0</td>
<td>2.4048</td>
<td>0.024eV</td>
</tr>
<tr>
<td>l=1, n=0</td>
<td>3.832</td>
<td>0.061eV</td>
</tr>
<tr>
<td>l=2, n=0</td>
<td>5.1356</td>
<td>0.1096eV</td>
</tr>
<tr>
<td>l=0, n=1</td>
<td>5.5201</td>
<td>0.1266eV</td>
</tr>
<tr>
<td>l=3, n=0</td>
<td>6.3802</td>
<td>0.1691eV</td>
</tr>
<tr>
<td>l=1, n=1</td>
<td>7.0156</td>
<td>0.2045eV</td>
</tr>
<tr>
<td>l=4, n=0</td>
<td>7.5883</td>
<td>0.2392eV</td>
</tr>
<tr>
<td>l=2, n=1</td>
<td>8.4172</td>
<td>0.2943eV</td>
</tr>
<tr>
<td>l=0, n=2</td>
<td>8.6537</td>
<td>0.3111eV</td>
</tr>
<tr>
<td>l=5, n=0</td>
<td>8.7715</td>
<td>0.3196eV</td>
</tr>
</tbody>
</table>

The over-all 1D density of states can be calculated by adding contribution of states from each quantized energy level for a specific Fermi level. Figure 4.1 shows the 1D density of states of an InAs nanowire compared with the 3D density of states.

![Comparison of 1D density of states and bulk density of states](image)

**Figure 4.1: Density of state for a 3D system vs 1D system.**
It is clear that using 3D density of states calculation overestimated the electron concentration for a given Fermi level. The quantization of density is not evident especially at room temperature. For the nanowire measured experimentally (with electron concentration of $1 \times 10^{18}/\text{cm}^3$), multiple energy levels are being filled up. One must reduce the electron concentration and the temperature of the nanowire in order to observe quantum effect in a nanowire.

The previous analytical model cannot take into account the many parameters of the nanowire system, such as back gating electric field and oxide layer below the nanowire. The goal is to compare the effect of back gate potential with quantum confined stark effect in quantum wells. The energy levels of a quantum well will decrease through a second order correction to the energy level. The correction is proportional to the square of the applied field. A second model is constructed with the help of Dr. Selvakumar Nair that can include the effect of the back gate potential. It is a finite difference model that accepts an electrochemical profile of a system and solves the Schrödinger’s Equation for quantized energy states. Table 4.2 shows the calculated energy level of InAs nanowire under a back gate potential with a 100nm oxide layer in between. Figure 4.2 shows how the energy levels in a nanowire are shifted under a back gate bias.
Table 4.2: Energy levels of InAs nanowire under back gate bias. Energy levels are measured from the conduction band minimum in eV.

<table>
<thead>
<tr>
<th></th>
<th>0V</th>
<th>-1V</th>
<th>-2V</th>
<th>-3V</th>
<th>-4V</th>
<th>-5V</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.14454</td>
<td>0.12933</td>
<td>0.10679</td>
<td>0.06828</td>
<td>-0.00952</td>
<td>-0.15883</td>
</tr>
<tr>
<td>1</td>
<td>0.1901</td>
<td>0.1723</td>
<td>0.14877</td>
<td>0.11692</td>
<td>0.05738</td>
<td>-0.07945</td>
</tr>
<tr>
<td>2</td>
<td>0.19117</td>
<td>0.17597</td>
<td>0.15486</td>
<td>0.12215</td>
<td>0.06475</td>
<td>-0.04943</td>
</tr>
<tr>
<td>3</td>
<td>0.24379</td>
<td>0.22583</td>
<td>0.20193</td>
<td>0.17004</td>
<td>0.1197</td>
<td>0.00521</td>
</tr>
<tr>
<td>4</td>
<td>0.24427</td>
<td>0.22636</td>
<td>0.20347</td>
<td>0.17175</td>
<td>0.1198</td>
<td>0.01067</td>
</tr>
<tr>
<td>5</td>
<td>0.25328</td>
<td>0.23725</td>
<td>0.21657</td>
<td>0.18704</td>
<td>0.13386</td>
<td>0.03188</td>
</tr>
</tbody>
</table>

Figure 4.2: Energy levels in InAs nanowire under negative back gate bias. The thicken line indicates the ground state and the dotted line indicates its quadratic approximation. The conduction band is being shifted by the back gate potential into a triangular shape, just like the case in quantum well.

In the calculation, it is shown that the behaviour of energy level of nanowire is very similar to that of a quantum well under the influence of an external field. The energy level of the ground state is being shifted downward in an approximately quadratic relationship with the back gate voltage. The applied back gate voltage breaks the symmetry of the nanowire the originally
degenerate states are now spreading out. These behaviours are in agreement with the theory of quantum confined stark effect in quantum wells. Further research can be done on the potential of using back gate as a modulator for quantized energy level in a nanowire.