Laser Fired Aluminum Emitter for High Efficiency Silicon Photovoltaics Using Hydrogenated Amorphous Silicon and Silicon Oxide Dielectric Passivation

by

Anton Fischer

A thesis submitted in conformity with the requirements for the degree of Masters of Applied Science Graduate Department of The Edward S. Rogers Sr. Electrical and Computer Engineering, University of Toronto

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Abstract

This thesis proposes and demonstrates a hydrogenated amorphous silicon passivated, inverted photovoltaic device on $n$-type silicon, utilizing a Laser Fired Emitter on a rear $i$-$a$-Si:H/$SiO_x$ dielectric stack. This novel low-temperature-fabricated device architecture constitutes the first demonstration of an LFE on a dielectric passivation stack. The optimization of the device is explored through Sentaurus computational modeling, predicting a potential efficiency of >20%. Proof of concept devices are fabricated using the DC Saddle Field PECVD system for the deposition of hydrogenated amorphous silicon passivation layers. Laser parameters are explored highlighting pulse energy density as a key performance determining factor. Annealing of devices in nitrogen atmosphere shows performance improvements albeit that the maximum annealing temperature is limited by the thermal stability of the passivation. A proof of concept device efficiency of 11.1% is realized forming the basis for further device optimization.
Acknowledgments

It is with great appreciation that I thank Prof. Nazir Kherani for his guidance, encouragement and patience in the journey my thesis has been. To benefit from his altruistic support of the academic pursuits as his student, has been an education unto itself.

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Finally I would like to thank my mother, father, siblings and girlfriend Madeleine, who’s unending love, support and understanding gives me the strength to pursue and realize my goals.
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<th>Definition</th>
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<tr>
<td>Ag</td>
<td>Silver</td>
</tr>
<tr>
<td>Al</td>
<td>Aluminum</td>
</tr>
<tr>
<td>AOM</td>
<td>Acousto-Optic Modulator</td>
</tr>
<tr>
<td>AR</td>
<td>Anti-Reflective</td>
</tr>
<tr>
<td>a-Si:H</td>
<td>Hydrogenated Amorphous Silicon</td>
</tr>
<tr>
<td>BACH</td>
<td>Back Amorphous Crystalline Heterojunction</td>
</tr>
<tr>
<td>BSF</td>
<td>Back Surface Field</td>
</tr>
<tr>
<td>CCP</td>
<td>Capacitively Coupled Plasma</td>
</tr>
<tr>
<td>c-Si</td>
<td>Crystalline Silicon</td>
</tr>
<tr>
<td>CZ</td>
<td>Czochralski</td>
</tr>
<tr>
<td>DB</td>
<td>Dangling Bond</td>
</tr>
<tr>
<td>DC</td>
<td>Direct Current</td>
</tr>
<tr>
<td>EBIC</td>
<td>Electron Beam Induced Current</td>
</tr>
<tr>
<td>ECN</td>
<td>Energy research Center of the Netherlands</td>
</tr>
<tr>
<td>EDX</td>
<td>Energy Dispersive X-ray spectroscopy</td>
</tr>
<tr>
<td>EHP</td>
<td>Electron Hole Pair</td>
</tr>
<tr>
<td>FF</td>
<td>Fill Factor</td>
</tr>
<tr>
<td>FSF</td>
<td>Front Surface Field</td>
</tr>
<tr>
<td>FZ</td>
<td>Float Zone</td>
</tr>
<tr>
<td>HIT</td>
<td>Heterojunction with Intrinsic Thin-layer</td>
</tr>
<tr>
<td>i-a-Si:H</td>
<td>Intrinsic Hydrogenated Amorphous Silicon</td>
</tr>
<tr>
<td>ICP</td>
<td>Inductively Coupled Plasma</td>
</tr>
<tr>
<td>IR</td>
<td>Infra Red</td>
</tr>
<tr>
<td>ITO</td>
<td>Indium Tin Oxide</td>
</tr>
<tr>
<td>IV</td>
<td>Current-Voltage</td>
</tr>
<tr>
<td>J_{sc}</td>
<td>Short Circuit Current Density</td>
</tr>
<tr>
<td>LFC</td>
<td>Laser Fired Contact</td>
</tr>
<tr>
<td>LFE</td>
<td>Laser Fired Emitter</td>
</tr>
<tr>
<td>LIDZ</td>
<td>Laser-Induced Damage Zone</td>
</tr>
<tr>
<td>LIT</td>
<td>Lock-In Thermography</td>
</tr>
<tr>
<td>MC</td>
<td>Multicrystalline</td>
</tr>
<tr>
<td>(\eta)</td>
<td>Photoelectric Conversion Efficiency</td>
</tr>
<tr>
<td>n-a-Si:H</td>
<td>n-Type Hydrogenated Amorphous Silicon</td>
</tr>
<tr>
<td>Nd:YAG</td>
<td>Neodymium-doped Yttrium Aluminum Garnet</td>
</tr>
<tr>
<td>Nd:YVO_{4}</td>
<td>Neodymium –doped Yttrium Orthovanadate</td>
</tr>
<tr>
<td>ODR</td>
<td>Orthogonal Distance Regression</td>
</tr>
<tr>
<td>Pd</td>
<td>Palladium</td>
</tr>
<tr>
<td>PECVD</td>
<td>Plasma Enhanced Chemical Vapour Deposition</td>
</tr>
<tr>
<td>Acronym</td>
<td>Description</td>
</tr>
<tr>
<td>---------</td>
<td>-------------</td>
</tr>
<tr>
<td>PERL</td>
<td>Passivated Emitter, Rear Locally diffused</td>
</tr>
<tr>
<td>PV</td>
<td>Photovoltaic</td>
</tr>
<tr>
<td>Q-Switched</td>
<td>Quality Switched</td>
</tr>
<tr>
<td>rf</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>SCR</td>
<td>Space Charge Region</td>
</tr>
<tr>
<td>SE</td>
<td>Spectroscopic Ellipsometry</td>
</tr>
<tr>
<td>Si</td>
<td>Silicon</td>
</tr>
<tr>
<td>SIMS</td>
<td>Secondary Ion Mass Spectrometry</td>
</tr>
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<td>SiNx</td>
<td>Silicon Nitride</td>
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<td>SiOx</td>
<td>Silicon Oxide</td>
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<tr>
<td>SRH</td>
<td>Shockley-Read-Hall</td>
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<tr>
<td>SRV</td>
<td>Surface Recombination Velocity</td>
</tr>
<tr>
<td>TCO</td>
<td>Transparent Conductive Oxide</td>
</tr>
<tr>
<td>TEM</td>
<td>Transmission Electron Microscopy</td>
</tr>
<tr>
<td>Ti</td>
<td>Titanium</td>
</tr>
<tr>
<td>μPCD</td>
<td>Microwave Photoconductance Decay</td>
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<tr>
<td>XRD</td>
<td>X-ray Diffraction</td>
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List of Symbols

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<thead>
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<tbody>
<tr>
<td>B</td>
<td>radiative recombination coefficient</td>
</tr>
<tr>
<td>c</td>
<td>speed of light</td>
</tr>
<tr>
<td>c</td>
<td>specific heat capacity</td>
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<tr>
<td>C_n, C_p</td>
<td>Auger recombination coefficient</td>
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<tr>
<td>d_0</td>
<td>focal spot size</td>
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<tr>
<td>D_n, D_p</td>
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<td>I_Ph</td>
<td>photogenerated current</td>
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<td>J_{mpp}</td>
<td>current density at maximum power point</td>
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<td>short circuit current density</td>
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<td>electron and hole equilibrium carrier population</td>
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<tr>
<td>R_r</td>
<td>recombination rate</td>
</tr>
<tr>
<td>R_S</td>
<td>series resistance</td>
</tr>
<tr>
<td>R_{sh}</td>
<td>shunt resistance</td>
</tr>
<tr>
<td>T</td>
<td>temperature</td>
</tr>
<tr>
<td>V_{mpp}</td>
<td>voltage at maximum power point</td>
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</table>
$V_{OC}$ open circuit voltage
$v_{th}$ thermal voltage
$W$ wafer thickness
$w$ beam width
$w_w$ beam waist
$\alpha_\lambda$ absorption coefficient (wavelength dependent)
$\Delta n, \Delta p$ electron and hole excess carrier population
$\Delta n_0$ initial excess carrier density
$\eta$ photoelectric conversion efficiency
$\theta$ angle of incidence
$\theta_d$ divergence angle
$\lambda$ wavelength
$\rho$ material density
$\sigma_n, \sigma_p$ electron and hole capture cross section
$\tau$ carrier lifetime
$\tau_{Auger}$ Auger recombination carrier lifetime
$\tau_b$ bulk carrier lifetime
$\tau_{eff}$ effective carrier lifetime
$\tau_n, \tau_p$ electron and hole lifetimes
$\tau_{pl}$ laser pulse length
$\tau_{rad}$ radiative recombination carrier lifetime
$\tau_S$ surface recombination carrier lifetime
$\tau_{SRH}$ Shockley-Read-Hall recombination carrier lifetime
Chapter 1
Introduction

1.1 Motivation

The potential for photovoltaic (PV) solar cells to play a significant role in our future electricity supply mix is clear. An illustrative metric is that the entire global annual energy consumption is equivalent to a single hour of sunlight incident on the earth’s surface [1]. This abundance of solar energy coupled with the finite nature of fossil fuel energy sources positions solar electricity, and in particular PV solar electricity, to become an important contributor in the quest for a sustainable electricity future.

The adoption rate of solar cells has occurred at an average growth rate of greater than 40% per annum over the last decade and is projected to continue at this growth as illustrated in Figure 1-1. This high rate of growth is driven by both cost reduction as well as renewable energy enabling policies in the form of feed-in tariffs [2, 3]. These feed-in tariffs in addition to providing an incentives for solar PV adoption also promote further fundamental and applied research and development to ultimately bring about a marked reduction in the cost per watt. For photovoltaic technology to sustain itself as a commercially viable form of electricity generation, the generation cost of solar electricity must reach grid parity. That is, the net amortized cost for the production of solar electricity must be equal to the price of electricity generated by conventional sources available through the electricity distribution grid. The competitiveness of PV generated electricity is dependent on a wide range of input parameters, including among others local time-of-day electricity cost, local annual average irradiation, and initial PV system and installation cost. An accepted simplification of this complex scenario suggests that grid parity in some regions of the world will require solar cell costs to come down to the order of one dollar per watt ($/W). The realization of solar cell cost reduction as defined by the $/W indicator, is the focus of a substantial amount of fundamental and applied research.
The incumbent solar cell technology uses crystalline silicon (c-Si). Crystalline silicon, an abundant (>25%) element in the earth’s crust, is non-toxic and an optoelectronically well-behaved material with a near ideal single junction band gap, which today comprises 78% of industrially produced solar cells[4]. Crystalline silicon-based cell technologies such as the Passivated Emitter, Rear Locally diffused solar cell (PERL) have demonstrated excellent absolute efficiencies of up to 25% [5, 6]. Recently c-Si technologies have also reported solar cell manufacturing cost of $1.1/W [7], indicating that c-Si based technology possesses the fundamental properties to contribute to the electricity generation mix at grid parity. The reduction in the cost per watt of c-Si devices has been realized through a combination of increases in manufacturing scale and improved manufacturing methods, and through technological improvements resulting in increased device efficiency.

This reduction in cost per watt is approached through several technical avenues. A cost reduction can also be realized with both reduction of material usage and reduction in material quality. As c-Si comprises the single largest portion of the device cost, ~75% of the finished solar cell [7], and hence there is a trend toward lower base thickness and the use of lower quality materials such as multicrystalline Si. Both of these substrate traits result in challenges vis-à-vis
maintaining cell performance with high temperature processing. Cost reduction can also be achieved by replacing batch processes with in-line processes, thus achieving higher throughput. One of the most technically interesting approaches to the reduction of $/W is the implementation of high efficiency architectures using high throughput processes.

The PERL cell achieves record efficiency through device features that maximize carrier generation and minimize recombination. High carrier lifetimes are achieved through the passivation of the front and rear surfaces using high quality thermal oxide passivation and point contacting of the rear surface. The passivation is opened locally with photolithography for contacting, which precludes cost effective mass production. As does the thermal boron diffusions used to form the local $p^+$ back surface field (BSF) for the rear contact, requiring a 2h thermal soak at $> 900 \, ^\circ C$ [5]. This high temperature step can also have a detrimental effect on bulk carrier lifetime in lower quality silicon[8].

In the context of high throughput production vis-à-vis rapid deposition of nm thick films at relatively low temperatures, hydrogenated amorphous silicon (a-Si:H) on c-Si has been demonstrated to produce excellent surface passivation with device efficiencies of 23% in the Heterojunction with Intrinsic Thin-layer cell [9]. Additionally, various laser processes have been demonstrated, achieving localized device features which are amenable to attaining high device conversion efficiency as well as in-line production of solar cells. A novel laser processing technique demonstrated by Schneiderlochner facilitates the formation of a point rear contact through a dielectric passivation layer, emulating the performance features of high efficiency device concepts such as the PERL, but with an in-line amenable process referred to as the Laser Fired Contact (LFC) [10].

1.2 Laser Processed High Efficiency Photovoltaics

The use of lasers for doping silicon in the formation of $pn$ junctions was first demonstrated by the diffusion of phosphorus into Si using a pulsed ruby laser [11]. The first laser-induced diffusion of aluminum into silicon was demonstrated using a Q-switched Nd:YAG laser [12]. Laser doping has been investigated in the context of solar cells for both local and large area diffusion of solid phase and liquid phase dopants. Various dopant delivery methods have been
explored, including deposition of a thin metallic dopant layer with subsequent laser-induced diffusion into the Si base [13], as well as liquid phase dopant delivery for the realization of spatially varying dopant profiles such as selective emitters [14]. The laser-induced doping of Si with aluminum (Al) has been investigated in detail by Demireva, demonstrating an increase in solubility of Al in Si over that seen in isothermal diffusion [15].

The localized contact of the LFC device structure is formed by localized laser heating of the Al layer which is part of a pre-deposited Al/dielectric passivation stack on the rear surface of the c-Si absorber. The heat imparted by the laser drives a portion of the Al through the dielectric passivation and into the silicon base, thus effectively forming a laser-assisted, localized diffused electrical contact. This fabrication technique has realized excellent device performance of 22% while presenting a fabrication process that is amenable to mass production [16]. Inherent to the LFC device concept is the realization of excellent rear surface passivation through the utilization of localized rear point contacts and full area passivation [17].

The LFC, illustrated in Figure 1-2, shares the structural features of the high efficiency PERL device, but implements local rear diffusion with a laser rather than with photolithographic and thermal diffusion processes. It utilizes a conventional $p$-type base high efficiency front surface device architecture comprised of random pyramids, thermally diffused phosphorous emitter, thermal oxide passivation, and Ti/Pd/Ag evaporated front metallization. The rear surface is comprised of a full surface passivation, which in turn is covered by a full surface Al metallization, typically of 2 $\mu$m thickness. The rear metallization is driven through the passivating layer locally by laser heating. Typically a 1064nm laser is used to form contacts of 150 $\mu$m diameter, at spacing intervals of 1000 $\mu$m.

The excellent performance of LFC devices is not solely due to the full area rear passivation afforded by localized rear contacts. Transient laser alloying of Al with Si has been shown to result in Al diffusion to a concentration which is two orders of magnitude greater than that for thermal diffusion [15]. The resulting localized diffusion of Al in the Si base creates a localized $p^+$ region in the base and acts as an effective BSF, allowing excellent cell performance across four decades of base resistivity[18].
The formation of a $p^+$ region in the base enables the formation of a localized emitter on an $n$-type base. The Laser Fired Emitter (LFE) was first proposed by Glunz [18] and differs from previous localized, solid phase, laser-induced $pn$ junction formation by the introduction of a dielectric layer between the solid phase dopant and the bulk silicon. The formation of a localized emitter through a dielectric layer was first reported by Glunz [20, 21] and further studied by Granek with demonstrated efficiencies of 19.4% [22]. In this initial implementation, Al was fired through a rear passivation layer of thermal SiO$_2$ into a $n$-type crystalline silicon base. The laser fired emitter presents the novel possibility of a localized homojunction emitter on an $n$-type base, without subjecting the entire cell to the potential material degradation associated with the high temperature process of a conventional boron diffusion.

A feature of the laser fired contact is its performance independence of the surface passivation employed. As a result a range of rear surface passivation schemes have been explored in the context of the LFC. The standard passivation is a double sided thermal oxide passivation. A number of low temperature passivation materials have been explored in an effort to reduce the thermal budget of cell fabrication, as well as reduce wafer warping and material degradation associated with high temperature steps. Low temperature surface passivations have predominantly been prepared by Plasma Enhanced Chemical Vapour Deposition (PECVD) and
have utilized silicon nitride (SiNₓ), silicon oxide (SiOₓ) and intrinsic hydrogenated amorphous silicon (i-a-Si:H). Dielectric passivation schemes explored in the context of the LFC have included PEVCD SiNₓ/PEVCD SiOₓ [23], PECVD a-Si:H/SiNₓ[24] and PECVD a-Si:H/SiOₓ [19] passivation stacks. Excellent passivation results have been demonstrated, although predominantly with high temperature front architectures incorporating thermally diffused phosphorus emitters and thermal oxide front passivation. A completely low-temperature approach which provides excellent surface passivation requires the use of hydrogenated amorphous silicon on both surfaces[25].

1.3 Thesis Objective

In this research we propose and demonstrate a hydrogenated amorphous silicon passivated, inverted device on n-type silicon, utilizing a Laser Fired Emitter on a rear i-a-Si:H/SiOₓ dielectric stack. This constitutes the first demonstration of an LFE on a low temperature dielectric passivation stack. This proposed device architecture is implemented using the unique DC Saddle Field (DCSF) PECVD technique for a-Si:H passivation and a simple, all low temperature process, requiring no batch or wet chemical processing. This complete low temperature processing, coupled with the use of n-type c-Si and the excellent potential surface passivation of a-Si:H, makes the proposed device concept amenable to the realization of high efficiency devices on thin, low quality material, at high manufacturing throughput rates.

In this work we explore potential device performance and fabrication feasibility through device simulation and fabrication of proof of concept devices. The thesis is organized as follows: Chapter 2 provides a summary of solar cell device theory relevant to high efficiency silicon device concepts. Chapter 3 presents the device concept and explores the optimization of the device through Sentaurus computational modeling. Chapter 4 presents the fabrication processes developed for the realization of the device precursor. Chapter 5 presents the development of the laser-induced diffusion process through an initial exploration of the LFE laser parameter space. Chapter 6 investigates the effect of laser parameters in the context of full device structures, and presents a successful proof of concept result in support of the simulated device performance.
Chapter 2
Solar Cell Device Theory: An Overview

2.1 Introduction

Silicon photovoltaic devices have demonstrated efficiencies closely approaching the theoretical limit of 28.8%[26] The passivated emitter rear locally diffused device architecture proposed by Wang has demonstrated efficiencies of 25%[5]. A number of fundamentally distinct silicon device architectures have demonstrated efficiencies greater than 22% including the Heterojunction cell proposed by Tanaka[27] and back point contact cell proposed by Swanson[28].

While absolute device efficiency is certainly an interesting scientific pursuit, a central theme in current solar photovoltaic device research is cost reduction. The $/W of a solar cell is dictated by both the initial manufacturing cost and the long term efficiency of the device. Thus, the objective of many current research efforts is the development of low process cost implementation of high efficiency device concepts, while reducing materials costs by reducing material use and material quality requirements.

A clear path to reduced material cost is the reduction of base thickness, as the silicon wafer accounts for the greatest single cost in the overall production cost of a solar cell. Reduction of cell thickness alone does not ensure a reduced $/W as there is the potential for cell thickness reduction to detrimentally affect manufacturability and cell performance through a number of mechanisms; these include wafer warping, reduced optical absorption and increased carrier recombination at the device surfaces. These effects can be largely mitigated by device architecture. The aforementioned high efficiency device concepts have demonstrated excellent results on thin substrates [29] [21]. The device architecture components that facilitate the excellent thickness scaling of high efficiency device concepts are: optical confinement and surface passivation.
The following sections introduce the device elements, operation and electrical model of the crystalline silicon photovoltaic solar cell. Subsequently, theory pertaining to processes of particular importance to high efficiency devices with thin absorbers is presented.

2.2 Crystalline Silicon Solar Cell Operating Principles

The processes required of a photovoltaic device to facilitate photoelectric conversion can be broadly grouped into carrier generation and carrier extraction. To maximize the photoelectric conversion efficiency, carrier generation must be maximized and carrier recombination prior to extraction must be minimized.

The fundamental features required for photoelectric conversion in a semiconductor solar cell are the existence of an electronic band gap for energetic separation of electrons and holes, and an asymmetrical electronic element for the spatial separation of these carriers. The architecture of a high efficiency solar cell, the Passivated Emitter, Rear Locally diffused (PERL), solar cell is illustrated in Figure 2-1.

![Figure 2-1: Structure of a solar cell - PERL [5]](image)

For inorganic photovoltaics, the asymmetric junction is provided by a pn junction, formed at the boundary between p-type and n-type doped material. P-type silicon has a higher concentration of holes, created by doping the silicon with an acceptor impurity, while n-type has a higher concentration of electrons, created by doping with a donor impurity. This junction is formed at
the interface, also known as the metallurgical junction, between the base and emitter in a solar cell and the depleted region about the interface is referred to as the space charge region (SCR).

Silicon has an indirect band gap of 1.1 eV, thus a photon possessing energy greater than this threshold value can be absorbed, promoting an electron from the conduction band to the valence band, thereby; generating an electron-hole pair (EHP). Once created, carriers diffuse freely within the material before they either recombine, typically releasing their energy as heat, or they arrive at the \( pn \) junction. Here the electrons are swept towards the \( n \)-type material and the holes are swept to the \( p \)-type material, resulting in carrier separation. The constituent elements of a typical Si solar cell device are now described below.

**Front Metallization**

The ideal front metallization provides an ohmic contact to the emitter and a highly conductive pathway for charge extraction on the front-side of the cell. As the metallization is opaque, there is an inherent tradeoff between front contact resistance and front contact coverage or shadowing where the former leads to ohmic losses while the later results in current generation loss.

**Anti-Reflection Coating**

The anti-reflection (AR) coating is an optical coating on the front surface of the cell which reduces the reflection of incoming photons through destructive interference. The ideal AR coating is lossless over the spectral region absorbed by Si.

**Emitter**

In a conventional solar cell, the emitter is comprised of a thin, highly doped layer with a dopant impurity type which is opposite to that of the base. Accordingly, the emitter, in concert with the base, gives rise to the built-in field that provides the asymmetric electrical element which supports the photoelectric conversion. The ideal emitter is highly doped so as to realize a large built in voltage, and has low resistivity. In reality, inherent tradeoffs ensue, high doping density results in low carrier collection in the emitter as well as affecting the response in the blue part of the spectrum.
**Base**

The base or absorber comprises the majority of the device volume. The base is comprised of lowly doped crystalline silicon and is responsible for the majority of the optical absorption.

**Rear Metallization**

The ideal rear metallization provides an ohmic contact to the base and a highly conductive pathway on the rear of the cell.

**Surface Passivation**

The surface passivation is comprised of dielectric layers on the surfaces of the cell that reduce recombination at the surface through chemical or field passivation, or a combination of both. Field passivation layers are referred to as surface fields and can take the form of both Back Surface Field (BSF), or a Front Surface Field (FSF).

Depending on the device architecture a single layer may fulfill multiple functionalities.

**2.3 Electrical Models of the Solar Cell**

The electrical output of a solar cell is best modeled as a current source in parallel with two diodes and a shunt resistor, all of which is in series with a series resistor, as illustrated in Figure 2-2.

![Figure 2-2: Two diode electrical model of a solar cell](image)
Initially considering a simplified case, the current-voltage (IV) characteristic of the device can be related to the device properties through Eq. (2.1), which is simply the equation of an ideal diode superpositioned with a photogenerated current ($I_{\text{Ph}}$).

$$I(V) = I_0 \left[ \frac{qV}{e^{n_k T}} - 1 \right] + I_{\text{Ph}} \tag{2.1}$$

Here $q$ is the elementary charge, $n$ is the ideality factor, $k_B$ is the Boltzmann constant, $T$ is the device temperature in Kelvin, $V$ is the applied voltage and $I_0$ is the reverse saturation current density. The reverse saturation current relates the cell IV characteristic to the device parameters through Eq. (2.2):

$$I_0 = I_{0b} + I_{0e} = \frac{qD_n n_i^2}{L_n N_A} + \frac{qD_p n_i^2}{L_p N_D} \tag{2.2}$$

Here $D_n, L_n$ and $D_p, L_p$ are the diffusivities and diffusion lengths, respectively, of electrons and holes, respectively; $N_D, N_A$ are the dopant concentrations of donors and acceptors, respectively; and $n_i$ is the intrinsic carrier density. Thus, the open circuit voltage ($V_{\text{OC}}$) of the device can be related to the device parameters $D, L, N$ and $I_{\text{Ph}}$.

A more accurate model, accounting for non-ideal elements, is provided by the two diode model described by Eq. (2.3) and illustrated in Figure 2-2.

$$I(V) = I_{01} \left[ e^{\frac{V-I_R S}{V_{th}}} - 1 \right] + I_{02} \left[ e^{\frac{V-I_R S}{V_{th}}} - 1 \right] + \frac{V-I_R S}{R_p} - I_{\text{Ph}} \tag{2.3}$$

Here $I_{01}, I_{02}$ are generally accepted as the reverse saturation current densities of the diffusion based recombination in the base and the space charge region recombination, respectively. The diode ideality factors $n_1$ has a value of 1, while $n_2$ is between 1 and 2 but a value of 2 is typically set for the model [30]. Other recombination currents with ideality factors >2 can be active in devices with high defect densities at the emitter [30]. The parasitic resistances $R_S$ and $R_{Sh}$ are the series and shunt resistances, respectively [31].

The short circuit current ($I_{\text{SC}}$) is obtained from Eq. (2.3) by setting $V$ to zero. Except for devices with extreme values of $R_S$ or $R_{Sh}$, the short circuit current is equivalent to the photogenerated
current. The open circuit voltage \((V_{OC})\) is obtained from Eq. (2.3) by setting \(I\) to zero and solving for \(V\). The open circuit voltage is found to vary as the natural log of the photogenerated current, and vary strongly with the values of the reverse saturation current densities \(I_{01}\) and \(I_{02}\).

As the one and two diode models are implicit equations, a range of techniques have been explored to appropriately fit device data with these models. In this work we use a fitting routine utilizing orthogonal distance regression (ODR). The fitting program is available from the Energy research Center of the Netherlands (ECN) and demonstrates reduced fitting uncertainty related to the strongly varying slope in voltage near the maximum power point compared to that of a standard least squares fit[32].

### 2.4 Solar Cell Performance Parameters

The performance of individual devices are compared using the device performance parameters open circuit voltage \((V_{OC})\), short circuit current density \((J_{SC})\), fill factor \((FF)\) and photoelectric conversion efficiency \((\eta)\).

The fill factor describes the squareness of the IV curve and is defined by Eq. (2.4). The maximum achievable \(FF\) for a Si device is 0.85, however the non-ideal terms of Eq. (2.3) including \(n_2, R_S,\) and \(R_{Sh}\), serve to reduce the fill factor of the device.

\[
FF = \frac{V_{mpp}I_{mpp}}{V_{OC}J_{SC}}
\]  

(2.4)

Here \(V_{mpp}\) and \(J_{mpp}\) are the voltage and current density of the cell at the maximum power operating point.

The photoelectric conversion efficiency \((\eta)\) relates the total electrical power output to the incident optical power \((P_{ill})\), and can also be calculated as a function of \(V_{OC}, J_{SC}\) and \(FF\) using Eq. (2.5):

\[
\eta = \frac{P_{mpp}}{P_{ill}} = \frac{V_{mpp}I_{mpp}}{P_{ill}} = \frac{V_{OC}J_{SC}FF}{P_{ill}}
\]

(2.5)
Through the analysis of Eq. (2.3) at short circuit and open circuit conditions, the influence of device parameters on device performance can be inferred.

2.5 Optical Confinement and Carrier Generation

The maximum current flux of a photovoltaic device is determined by the total photon absorption in the device. The total photon flux and the photon energy distribution that is incident on the surface of a solar cell is dictated by solar irradiance and its spectral distribution. This varies with terrestrial conditions including location, time of year, angle of incidence, altitude and weather conditions.

![AM1.5G solar spectrum](image)

**Figure 2-3**: AM1.5G solar spectrum

Standard test conditions exist to facilitate the comparison of device results. The accepted test spectrum for non-concentrating solar cells is the AM1.5G spectrum defined by the ASTM G173 standard [33]. The total irradiance of AM1.5G is 1000W/cm², and the spectral distribution is representative of sunlight that has traveled through the atmosphere a length equivalent to 1.5 times the atmosphere depth, due to an off-normal angle of incidence and accounts for both direct and diffuse light (global). The spectral distribution of the AM1.5G spectrum is presented in Figure 2-3.
Absorption of light in a material can be described macroscopically by the drop in intensity $I_L(x)$ as a function of depth in the material, for a given photon energy. In a non-homogeneous material the variation of intensity with depth is described by Eq. (2.6)

$$I_L(x) = I_L(0)e^{-\int_0^x \alpha(E,x')dx'}$$

Here $\alpha$ is the extinction coefficient as a function of wavelength and $I_L(0)$ is the intensity impinging on the material at $x=0$. Silicon has a strongly varying absorption coefficient, which is presented in Figure 2-4 a). The absorption of blue photons near the front surface of the device is high, while infra-red (IR) photons, if absorbed, are absorbed near the rear surface of the device. The dependence of absorption depth on photon energy results in an asymmetrical net absorption profile and thereby an asymmetrical net carrier generation as illustrated in Figure 2-4 b). The carrier generation at the front surface of the cell is several orders of magnitude higher than at the rear of the cell. This absorption profile means that devices can be made as thin as 100 $\mu$m without significant losses in net carrier generation.

**Figure 2-4**: a) Absorption coefficient and absorption depth in Si as a function of wavelength [34], b) net carrier generation as a function of depth in Si [35]

Reflection plays an important role in photogeneration both at the front and rear surfaces of the device. Photon flux incident on the front surface of the cell must be transmitted in order to
produce a photocurrent. Polished silicon surfaces have a native reflectivity of approximately 40%[34]. The loss associated with front surface reflection can be addressed by two means: anti-reflection coatings and surface texture. A single layer AR coating acts to minimize the reflection for a specific portion of the spectrum. The AR coating is comprised of a transparent layer with an index of refraction between that of air and silicon, and a thickness that is an odd multiple of one quarter of the wavelength to be minimized. Reflection can be eliminated at the target wavelength if the AR coating has a refractive index that is equal to the square root of the refractive index of silicon, or \( n \sim 1.84 \). The minimized wavelength is tuned with the coating thickness with the resulting surface reflectivity described by Eq. (2.7).

\[
R = \frac{(n_0 n_S)^2 + (n_0 n_S/n_m - n_m)^2 \tan^2 \delta}{(n_0 n_S)^2 + (n_0 n_S/n_m + n_m)^2 \tan^2 \delta}, \quad \delta = 2\pi n_m d \cos \theta / \lambda
\]  

(2.7)

Here \( n_0, n_1, n_S \), are the refractive indices of air, the AR coating and Si respectively, \( d \) is the AR coating thickness, \( \theta \) is the angle of incidence of light with respect to the surface normal, and \( \lambda \) is the wavelength of the incident light.

Conversely, reflection at the back of the cell is desirable, particularly in thin cells where a significant portion of the IR irradiance might otherwise be lost if it were to exit the rear side. Here metallic back reflectors are frequently employed, as they serve a dual role of electrical contact and rear reflector, but the standard aluminum rear reflector has a reflectance of <80% [36]. Reflection provided by rear surface dielectric passivation layers has been shown to provide superior reflectivity in the IR to metallic mirrors as illustrated in Figure 2-5. Green shows a maximum in IR reflection for an SiO₂ layer of 105nm [26] and Hofmann shows the superior IR reflection performance with a-Si:H/SiOₓ dielectric stacks compared to all other two layer dielectric stacks tested[16]. Near perfect reflectivity is seen in the IR for a-Si:H/SiNₓ Bragg reflectors [36].
Figure 2-5: Dielectric rear surface passivation reflectivity as a function of wavelength, including an a-Si:H/SiNx Bragg reflector [36].

The absorption of photons with an energy $\frac{hc}{\lambda} > E_g$, leads to the transition of an electron from the valence band to the conduction band, which is referred to as generation. For silicon, with an in-direct band gap of 1.1eV, electron-hole pairs are generated for photons with a wavelength less than 1100nm. Assuming that all photons incident on an untextured device are absorbed to generate free carriers, the net generation as a function of depth is described by Eq. (2.8):

$$G(x) = \int (1 - R(E)) \alpha(E) I_L(E) e^{-\int_0^x \alpha(E,x') dx'} dx$$

where $R(E)$ and $I_L(E)$ are the surface reflectivity and normally incident light/photon flux density. Generation results in an equal injection of holes and electrons, resulting in instantaneous carrier population described by Eq. (2.9):

$$n = \Delta n + n_0, \quad p = \Delta p + p_0$$

Here $n$ and $p$ are the instantaneous carrier concentrations, $\Delta n$ and $\Delta p$ are the excess carrier concentrations, and $n_0$ and $p_0$ are the equilibrium carrier populations, of electrons and holes, respectively.
Chapter 1
Introduction

1.1 Motivation

The potential for photovoltaic (PV) solar cells to play a significant role in our future electricity supply mix is clear. An illustrative metric is that the entire global annual energy consumption is equivalent to a single hour of sunlight incident on the earth’s surface [1]. This abundance of solar energy coupled with the finite nature of fossil fuel energy sources positions solar electricity, and in particular PV solar electricity, to become an important contributor in the quest for a sustainable electricity future.

The adoption rate of solar cells has occurred at an average growth rate of greater than 40% per annum over the last decade and is projected to continue at this growth as illustrated in Figure 1-1. This high rate of growth is driven by both cost reduction as well as renewable energy enabling policies in the form of feed-in tariffs [2, 3]. These feed-in tariffs in addition to providing an incentives for solar PV adoption also promote further fundamental and applied research and development to ultimately bring about a marked reduction in the cost per watt. For photovoltaic technology to sustain itself as a commercially viable form of electricity generation, the generation cost of solar electricity must reach grid parity. That is, the net amortized cost for the production of solar electricity must be equal to the price of electricity generated by conventional sources available through the electricity distribution grid. The competitiveness of PV generated electricity is dependent on a wide range of input parameters, including among others local time-of-day electricity cost, local annual average irradiation, and initial PV system and installation cost. An accepted simplification of this complex scenario suggests that grid parity in some regions of the world will require solar cell costs to come down to the order of one dollar per watt ($/W). The realization of solar cell cost reduction as defined by the $/W indicator, is the focus of a substantial amount of fundamental and applied research.
Figure 1-1: Historical annual installed PV capacity and annual capacity increases forecasted by the European Photovoltaic Industry Association as a function of technology adoption enabling policy [4]

The incumbent solar cell technology uses crystalline silicon (c-Si). Crystalline silicon, an abundant (>25%) element in the earth’s crust, is non-toxic and an optoelectronically well behaved material with a near ideal single junction band gap, which today comprises 78% of industrially produced solar cells[4]. Crystalline silicon based cell technologies such as the Passivated Emitter, Rear Locally diffused solar cell (PERL) have demonstrated excellent absolute efficiencies of up to 25% [5, 6]. Recently c-Si technologies have also reported solar cell manufacturing cost of $1.1/W [7], indicating that c-Si based technology possesses the fundamental properties to contribute to the electricity generation mix at grid parity. The reduction in the cost per watt of c-Si devices has been realized through a combination of increases in manufacturing scale and improved manufacturing methods, and through technological improvements resulting in increased device efficiency.

This reduction in cost per watt is approached through several technical avenues. A cost reduction can also be realized with both reduction of material usage and reduction in material quality. As c-Si comprises the single largest portion of the device cost, ~75% of the finished solar cell [7], and hence there is a trend toward lower base thickness and the use of lower quality materials such as multicrystalline Si. Both of these substrate traits result in challenges vis-à-vis
maintaining cell performance with high temperature processing. Cost reduction can also be achieved by replacing batch processes with in-line processes, thus achieving higher throughput. One of the most technically interesting approaches to the reduction of $/W is the implementation of high efficiency architectures using high throughput processes.

The PERL cell achieves record efficiency through device features that maximize carrier generation and minimize recombination. High carrier lifetimes are achieved through the passivation of the front and rear surfaces using high quality thermal oxide passivation and point contacting of the rear surface. The passivation is opened locally with photolithography for contacting, which precludes cost effective mass production. As does the thermal boron diffusions used to form the local \( p^+ \) back surface field (BSF) for the rear contact, requiring a 2h thermal soak at > 900 °C [5]. This high temperature step can also have a detrimental effect on bulk carrier lifetime in lower quality silicon[8].

In the context of high throughput production \textit{vis-à-vis} rapid deposition of nm thick films at relatively low temperatures, hydrogenated amorphous silicon (a-Si:H) on c-Si has been demonstrated to produce excellent surface passivation with device efficiencies of 23% in the Heterojunction with Intrinsic Thin-layer cell [9]. Additionally, various laser processes have been demonstrated, achieving localized device features which are amenable to attaining high device conversion efficiency as well as in-line production of solar cells. A novel laser processing technique demonstrated by Schneiderlochner facilitates the formation of a point rear contact through a dielectric passivation layer, emulating the performance features of high efficiency device concepts such as the PERL, but with an in-line amenable process referred to as the Laser Fired Contact (LFC) [10].

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The localized contact of the LFC device structure is formed by localized laser heating of the Al layer which is part of a pre-deposited Al/dielectric passivation stack on the rear surface of the c-Si absorber. The heat imparted by the laser drives a portion of the Al through the dielectric passivation and into the silicon base, thus effectively forming a laser-assisted, localized diffused electrical contact. This fabrication technique has realized excellent device performance of 22% while presenting a fabrication process that is amenable to mass production [16]. Inherent to the LFC device concept is the realization of excellent rear surface passivation through the utilization of localized rear point contacts and full area passivation [17].

The LFC, illustrated in Figure 1-2, shares the structural features of the high efficiency PERL device, but implements local rear diffusion with a laser rather than with photolithographic and thermal diffusion processes. It utilizes a conventional $p$-type base high efficiency front surface device architecture comprised of random pyramids, thermally diffused phosphorous emitter, thermal oxide passivation, and Ti/Pd/Ag evaporated front metallization. The rear surface is comprised of a full surface passivation, which in turn is covered by a full surface Al metallization, typically of 2 $\mu$m thickness. The rear metallization is driven through the passivating layer locally by laser heating. Typically a 1064nm laser is used to form contacts of 150 $\mu$m diameter, at spacing intervals of 1000 $\mu$m.

The excellent performance of LFC devices is not solely due to the full area rear passivation afforded by localized rear contacts. Transient laser alloying of Al with Si has been shown to result in Al diffusion to a concentration which is two orders of magnitude greater than that for thermal diffusion [15]. The resulting localized diffusion of Al in the Si base creates a localized $p^+$ region in the base and acts as an effective BSF, allowing excellent cell performance across four decades of base resistivity[18].
The formation of a $p^+$ region in the base enables the formation of a localized emitter on an $n$-type base. The Laser Fired Emitter (LFE) was first proposed by Glunz [18] and differs from previous localized, solid phase, laser-induced $pn$ junction formation by the introduction of a dielectric layer between the solid phase dopant and the bulk silicon. The formation of a localized emitter through a dielectric layer was first reported by Glunz [20, 21] and further studied by Granek with demonstrated efficiencies of 19.4% [22]. In this initial implementation, Al was fired through a rear passivation layer of thermal SiO$_2$ into a $n$-type crystalline silicon base. The laser fired emitter presents the novel possibility of a localized homojunction emitter on an $n$-type base, without subjecting the entire cell to the potential material degradation associated with the high temperature process of a conventional boron diffusion.

A feature of the laser fired contact is its performance independence of the surface passivation employed. As a result a range of rear surface passivation schemes have been explored in the context of the LFC. The standard passivation is a double sided thermal oxide passivation. A number of low temperature passivation materials have been explored in an effort to reduce the thermal budget of cell fabrication, as well as reduce wafer warping and material degradation associated with high temperature steps. Low temperature surface passivations have predominantly been prepared by Plasma Enhanced Chemical Vapour Deposition (PECVD) and

**Figure 1-2:** Laser Fired Contact solar cell structure [19]
have utilized silicon nitride (SiNₓ), silicon oxide (SiOₓ) and intrinsic hydrogenated amorphous silicon (i-a-Si:H). Dielectric passivation schemes explored in the context of the LFC have included PEVCD SiNₓ/ PEVCD SiOₓ [23], PECVD a-Si:H/SiNₓ[24] and PECVD a-Si:H/SiOₓ [19] passivation stacks. Excellent passivation results have been demonstrated, although predominantly with high temperature front architectures incorporating thermally diffused phosphorus emitters and thermal oxide front passivation. A completely low-temperature approach which provides excellent surface passivation requires the use of hydrogenated amorphous silicon on both surfaces [25].

1.3 Thesis Objective

In this research we propose and demonstrate a hydrogenated amorphous silicon passivated, inverted device on n-type silicon, utilizing a Laser Fired Emitter on a rear i-a-Si:H/SiOₓ dielectric stack. This constitutes the first demonstration of an LFE on a low temperature dielectric passivation stack. This proposed device architecture is implemented using the unique DC Saddle Field (DCSF) PECVD technique for a-Si:H passivation and a simple, all low temperature process, requiring no batch or wet chemical processing. This complete low temperature processing, coupled with the use of n-type c-Si and the excellent potential surface passivation of a-Si:H, makes the proposed device concept amenable to the realization of high efficiency devices on thin, low quality material, at high manufacturing throughput rates.

In this work we explore potential device performance and fabrication feasibility through device simulation and fabrication of proof of concept devices. The thesis is organized as follows: Chapter 2 provides a summary of solar cell device theory relevant to high efficiency silicon device concepts. Chapter 3 presents the device concept and explores the optimization of the device through Sentaurus computational modeling. Chapter 4 presents the fabrication processes developed for the realization of the device precursor. Chapter 5 presents the development of the laser-induced diffusion process through an initial exploration of the LFE laser parameter space. Chapter 6 investigates the effect of laser parameters in the context of full device structures, and presents a successful proof of concept result in support of the simulated device performance.
Chapter 2
Solar Cell Device Theory: An Overview

2.1 Introduction

Silicon photovoltaic devices have demonstrated efficiencies closely approaching the theoretical limit of 28.8%[26] The passivated emitter rear locally diffused device architecture proposed by Wang has demonstrated efficiencies of 25%[5]. A number of fundamentally distinct silicon device architectures have demonstrated efficiencies greater than 22% including the Heterojunction cell proposed by Tanaka[27] and back point contact cell proposed by Swanson [28].

While absolute device efficiency is certainly an interesting scientific pursuit, a central theme in current solar photovoltaic device research is cost reduction. The $/W of a solar cell is dictated by both the initial manufacturing cost and the long term efficiency of the device. Thus, the objective of many current research efforts is the development of low process cost implementation of high efficiency device concepts, while reducing materials costs by reducing material use and material quality requirements.

A clear path to reduced material cost is the reduction of base thickness, as the silicon wafer accounts for the greatest single cost in the overall production cost of a solar cell. Reduction of cell thickness alone does not ensure a reduced $/W as there is the potential for cell thickness reduction to detrimentally affect manufacturability and cell performance through a number of mechanisms; these include wafer warping, reduced optical absorption and increased carrier recombination at the device surfaces. These effects can be largely mitigated by device architecture. The aforementioned high efficiency device concepts have demonstrated excellent results on thin substrates [29] [21]. The device architecture components that facilitate the excellent thickness scaling of high efficiency device concepts are: optical confinement and surface passivation.
The following sections introduce the device elements, operation and electrical model of the crystalline silicon photovoltaic solar cell. Subsequently, theory pertaining to processes of particular importance to high efficiency devices with thin absorbers is presented.

2.2 Crystalline Silicon Solar Cell Operating Principles

The processes required of a photovoltaic device to facilitate photoelectric conversion can be broadly grouped into carrier generation and carrier extraction. To maximize the photoelectric conversion efficiency, carrier generation must be maximized and carrier recombination prior to extraction must be minimized.

The fundamental features required for photoelectric conversion in a semiconductor solar cell are the existence of an electronic band gap for energetic separation of electrons and holes, and an asymmetrical electronic element for the spatial separation of these carriers. The architecture of a high efficiency solar cell, the Passivated Emitter, Rear Locally diffused (PERL), solar cell is illustrated in Figure 2-1.

![Figure 2-1: Structure of a solar cell - PERL [5]](image)

For inorganic photovoltaics, the asymmetric junction is provided by a $pn$ junction, formed at the boundary between $p$-type and $n$-type doped material. $P$-type silicon has a higher concentration of holes, created by doping the silicon with an acceptor impurity, while $n$-type has a higher concentration of electrons, created by doping with a donor impurity. This junction is formed at
the interface, also known as the metallurgical junction, between the base and emitter in a solar cell and the depleted region about the interface is referred to as the space charge region (SCR).

Silicon has an indirect band gap of 1.1 eV, thus a photon possessing energy greater than this threshold value can be absorbed, promoting an electron from the conduction band to the valence band, thereby; generating an electron-hole pair (EHP). Once created, carriers diffuse freely within the material before they either recombine, typically releasing their energy as heat, or they arrive at the \(pn\) junction. Here the electrons are swept towards the \(n\)-type material and the holes are swept to the \(p\)-type material, resulting in carrier separation. The constituent elements of a typical Si solar cell device are now described below.

**Front Metallization**

The ideal front metallization provides an ohmic contact to the emitter and a highly conductive pathway for charge extraction on the front-side of the cell. As the metallization is opaque, there is an inherent tradeoff between front contact resistance and front contact coverage or shadowing where the former leads to ohmic losses while the later results in current generation loss.

**Anti-Reflection Coating**

The anti-reflection (AR) coating is an optical coating on the front surface of the cell which reduces the reflection of incoming photons through destructive interference. The ideal AR coating is lossless over the spectral region absorbed by Si.

**Emitter**

In a conventional solar cell, the emitter is comprised of a thin, highly doped layer with a dopant impurity type which is opposite to that of the base. Accordingly, the emitter, in concert with the base, gives rise to the built-in field that provides the asymmetric electrical element which supports the photoelectric conversion. The ideal emitter is highly doped so as to realize a large built in voltage, and has low resistivity. In reality, inherent tradeoffs ensue, high doping density results in low carrier collection in the emitter as well as affecting the response in the blue part of the spectrum.
Base

The base or absorber comprises the majority of the device volume. The base is comprised of lowly doped crystalline silicon and is responsible for the majority of the optical absorption.

Rear Metallization

The ideal rear metallization provides an ohmic contact to the base and a highly conductive pathway on the rear of the cell.

Surface Passivation

The surface passivation is comprised of dielectric layers on the surfaces of the cell that reduce recombination at the surface through chemical or field passivation, or a combination of both. Field passivation layers are referred to as surface fields and can take the form of both Back Surface Field (BSF), or a Front Surface Field (FSF).

Depending on the device architecture a single layer may fulfill multiple functionalities.

2.3 Electrical Models of the Solar Cell

The electrical output of a solar cell is best modeled as a current source in parallel with two diodes and a shunt resistor, all of which is in series with a series resistor, as illustrated in Figure 2-2.

![Two diode electrical model of a solar cell](image)

**Figure 2-2:** Two diode electrical model of a solar cell
Initially considering a simplified case, the current-voltage (IV) characteristic of the device can be related to the device properties through Eq. (2.1), which is simply the equation of an ideal diode superpositioned with a photogenerated current ($I_{Ph}$).

$$I(V) = I_0 \left[ e^{\frac{qV}{n k_b T}} - 1 \right] + I_{Ph} \tag{2.1}$$

Here $q$ is the elementary charge, $n$ is the ideality factor, $k_B$ is the Boltzmann constant, $T$ is the device temperature in Kelvin, $V$ is the applied voltage and $I_0$ is the reverse saturation current density. The reverse saturation current relates the cell IV characteristic to the device parameters through Eq. (2.2):

$$I_0 = I_{0b} + I_{0e} = \frac{q D_n n_1^2}{L_n N_A} + \frac{q D_p n_2^2}{L_p N_D} \tag{2.2}$$

Here $D_n$, $L_n$ and $D_p$, $L_p$ are the diffusivities and diffusion lengths, respectively, of electrons and holes, respectively; $N_D$, $N_A$ are the dopant concentrations of donors and acceptors, respectively; and $n_i$ is the intrinsic carrier density. Thus, the open circuit voltage ($V_{OC}$) of the device can be related to the device parameters $D$, $L$, $N$ and $I_{Ph}$.

A more accurate model, accounting for non-ideal elements, is provided by the two diode model described by Eq. (2.3) and illustrated in Figure 2-2.

$$I(V) = I_{01} \left[ \frac{V - jR_S}{e^{n_1 V_{th}} - 1} \right] + I_{02} \left[ \frac{V - jR_S}{e^{n_2 V_{th}} - 1} \right] + \frac{V - jR_S}{R_p} - I_{Ph} \tag{2.3}$$

Here $I_{01}$, $I_{02}$ are generally accepted as the reverse saturation current densities of the diffusion based recombination in the base and the space charge region recombination, respectively. The diode ideality factors $n_1$ has a value of 1, while $n_2$ is between 1 and 2 but a value of 2 is typically set for the model [30]. Other recombination currents with ideality factors >2 can be active in devices with high defect densities at the emitter [30]. The parasitic resistances $R_S$ and $R_{Sh}$ are the series and shunt resistances, respectively [31].

The short circuit current ($I_{SC}$) is obtained from Eq. (2.3) by setting $V$ to zero. Except for devices with extreme values of $R_S$ or $R_{Sh}$, the short circuit current is equivalent to the photogenerated
current. The open circuit voltage ($V_{OC}$) is obtained from Eq. (2.3) by setting $I$ to zero and solving for $V$. The open circuit voltage is found to vary as the natural log of the photogenerated current, and vary strongly with the values of the reverse saturation current densities $I_{01}$ and $I_{02}$.

As the one and two diode models are implicit equations, a range of techniques have been explored to appropriately fit device data with these models. In this work we use a fitting routine utilizing orthogonal distance regression (ODR). The fitting program is available from the Energy research Center of the Netherlands (ECN) and demonstrates reduced fitting uncertainly related to the strongly varying slope in voltage near the maximum power point compared to that of a standard least squares fit[32].

2.4 Solar Cell Performance Parameters

The performance of individual devices are compared using the device performance parameters open circuit voltage ($V_{OC}$), short circuit current density ($J_{SC}$), fill factor ($FF$) and photoelectric conversion efficiency ($\eta$).

The fill factor describes the squareness of the IV curve and is defined by Eq. (2.4). The maximum achievable $FF$ for a Si device is 0.85, however the non-ideal terms of Eq. (2.3) including $n_2$, $R_S$, and $R_{Sh}$, serve to reduce the fill factor of the device.

$$FF = \frac{V_{mpp}J_{mpp}}{V_{OC}J_{SC}}$$

(2.4)

Here $V_{mpp}$ and $J_{mpp}$ are the voltage and current density of the cell at the maximum power operating point.

The photoelectric conversion efficiency ($\eta$) relates the total electrical power output to the incident optical power ($P_{ill}$), and can also be calculated as a function of $V_{OC}$, $J_{SC}$ and $FF$ using Eq. (2.5):

$$\eta = \frac{P_{mpp}}{P_{ill}} = \frac{V_{mpp}J_{mpp}}{P_{ill}} = \frac{V_{OC}J_{SC}FF}{P_{ill}}$$

(2.5)
Through the analysis of Eq. (2.3) at short circuit and open circuit conditions, the influence of device parameters on device performance can be inferred.

2.5 Optical Confinement and Carrier Generation

The maximum current flux of a photovoltaic device is determined by the total photon absorption in the device. The total photon flux and the photon energy distribution that is incident on the surface of a solar cell is dictated by solar irradiance and its spectral distribution. This varies with terrestrial conditions including location, time of year, angle of incidence, altitude and weather conditions.

![Figure 2-3: AM1.5G solar spectrum](image)

Standard test conditions exist to facilitate the comparison of device results. The accepted test spectrum for non-concentrating solar cells is the AM1.5G spectrum defined by the ASTM G173 standard [33]. The total irradiance of AM1.5G is 1000W/cm², and the spectral distribution is representative of sunlight that has traveled through the atmosphere a length equivalent to 1.5 times the atmosphere depth, due to an off-normal angle of incidence and accounts for both direct and diffuse light (global). The spectral distribution of the AM1.5G spectrum is presented in Figure 2-3.
Absorption of light in a material can be described macroscopically by the drop in intensity $I_L(x)$ as a function of depth in the material, for a given photon energy. In a non-homogeneous material the variation of intensity with depth is described by Eq. (2.6)

$$I_L(x) = I_L(0)e^{-\int_0^x \alpha(E,x')dx'}$$  \hspace{1cm} (2.6)

Here $\alpha$ is the extinction coefficient as a function of wavelength and $I_L(0)$ is the intensity impinging on the material at $x=0$. Silicon has a strongly varying absorption coefficient, which is presented in Figure 2-4 a). The absorption of blue photons near the front surface of the device is high, while infra-red (IR) photons, if absorbed, are absorbed near the rear surface of the device. The dependence of absorption depth on photon energy results in an asymmetrical net absorption profile and thereby an asymmetrical net carrier generation as illustrated in Figure 2-4 b). The carrier generation at the front surface of the cell is several orders of magnitude higher than at the rear of the cell. This absorption profile means that devices can be made as thin as 100 µm without significant losses in net carrier generation.

**Figure 2-4**: a) Absorption coefficient and absorption depth in Si as a function of wavelength [34], b) net carrier generation as a function of depth in Si [35]

Reflection plays an important role in photogeneration both at the front and rear surfaces of the device. Photon flux incident on the front surface of the cell must be transmitted in order to
produce a photocurrent. Polished silicon surfaces have a native reflectivity of approximately 40\%[34]. The loss associated with front surface reflection can be addressed by two means: anti-reflection coatings and surface texture. A single layer AR coating acts to minimize the reflection for a specific portion of the spectrum. The AR coating is comprised of a transparent layer with an index of refraction between that of air and silicon, and a thickness that is an odd multiple of one quarter of the wavelength to be minimized. Reflection can be eliminated at the target wavelength if the AR coating has a refractive index that is equal to the square root of the refractive index of silicon, or \( n \sim 1.84 \). The minimized wavelength is tuned with the coating thickness with the resulting surface reflectivity described by Eq. (2.7).

\[
R = \frac{(n_0n_S)^2+(n_0n_S/n_m-n_m)^2\tan^2\delta}{(n_0n_S)^2+(n_0n_S/n_m+n_m)^2\tan^2\delta}, \quad \delta = \frac{2\pi n_m d \cos\theta}{\lambda} \tag{2.7}
\]

Here \( n_0, n_1, n_S \), are the refractive indices of air, the AR coating and Si respectively, \( d \) is the AR coating thickness, \( \theta \) is the angle of incidence of light with respect to the surface normal, and \( \lambda \) is the wavelength of the incident light.

Conversely, reflection at the back of the cell is desirable, particularly in thin cells where a significant portion of the IR irradiance might otherwise be lost if it were to exit the rear side. Here metallic back reflectors are frequently employed, as they serve a dual role of electrical contact and rear reflector, but the standard aluminum rear reflector has a reflectance of <80\% [36]. Reflection provided by rear surface dielectric passivation layers has been shown to provide superior reflectivity in the IR to metallic mirrors as illustrated in Figure 2-5. Green shows a maximum in IR reflection for an SiO\(_2\) layer of 105nm [26] and Hofmann shows the superior IR reflection performance with a-Si:H/SiO\(_x\) dielectric stacks compared to all other two layer dielectric stacks tested[16]. Near perfect reflectivity is seen in the IR for a-Si:H/SiN\(_x\) Bragg reflectors [36].
The absorption of photons with an energy $\frac{hc}{\lambda} > E_g$, leads to the transition of an electron from the valence band to the conduction band, which is referred to as generation. For silicon, with an in-direct band gap of 1.1eV, electron-hole pairs are generated for photons with a wavelength less than 1100nm. Assuming that all photons incident on an untextured device are absorbed to generate free carriers, the net generation as a function of depth is described by Eq. (2.8):

$$G(x) = \int (1 - R(E)) \alpha(E) I_L(E) e^{-\int^x_0 \alpha(E,x') dx'} dE$$

(2.8)

where $R(E)$ and $I_L(E)$ are the surface reflectivity and normally incident light/photon flux density. Generation results in an equal injection of holes and electrons, resulting in instantaneous carrier population described by Eq. (2.9):

$$n = \Delta n + n_0, \quad p = \Delta p + p_0$$

(2.9)

Here $n$ and $p$ are the instantaneous carrier concentrations, $\Delta n$ and $\Delta p$ are the excess carrier concentrations, and $n_0$ and $p_0$ are the equilibrium carrier populations, of electrons and holes, respectively.
2.6 Carrier Recombination Processes

The opposite process to carrier generation is carrier recombination. Once carriers are generated, it is a matter of time before they recombine. The duration of their excited state is referred to as the excess carrier lifetime. While the generation of EHP’s in solar cells is dominated by photon absorption, there are several processes by which carriers recombine, thereby; redistributing the energy of their excited state in the form of light (photons) or heat (phonons). The recombination of carriers prior to collection and extraction is a dominate efficiency limiting mechanism in solar cells.

Carriers may recombine by band to band radiative recombination, band to band Auger recombination in multi-carrier interaction, or by way of trap states in the band gap, known as Shockley-Read-Hall (SRH) recombination. These processes can be subdivided into those intrinsic to the material properties, including radiative and Auger recombination, and those extrinsic to the material which are avoidable processes that are functions of material quality (for example, impurity type and concentration) and defects. In equilibrium, the excess carrier lifetime ($\tau$) for $n$-type material is given by Eq. (2.10) for a given excess carrier density ($\Delta n$) and a given recombination rate ($R_r$) and is dependent on the excess carrier injection level[37].

$$\tau = \frac{\Delta n}{R_r} \quad (2.10)$$

Here $\Delta n$ is the excess carrier densities of electrons and $\tau$ is the carrier lifetime and $R_r$ is the recombination rate.

The bulk recombination mechanisms are independent of each other, and as such can be combined together to give the bulk carrier lifetime ($\tau_b$) as described by Eq. (2.11) [38].

$$\frac{1}{\tau_b} = \frac{1}{\tau_{rad}} + \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{SRH}} \quad (2.11)$$

Here $\tau_{rad}$, $\tau_{Auger}$ and $\tau_{SRH}$, are the radiative, Auger and Shockley-Read-Hall carrier lifetimes respectively.

Radiative recombination lifetime is inversely proportional to carrier concentration as described by Eq. (2.12), as both an electron and hole must be present for the band to band transition to
occur. This is not a significant recombination mechanism in silicon solar cells, due to the indirect band gap of silicon which requires phonon interaction for momentum conservation.

\[ \tau_{rad} = \frac{1}{B(n_0 + p_0 + \Delta n)} \]  

(2.12)

Here \( B \) is the radiative recombination coefficient.

Auger recombination is a three carrier process whereby an electron and hole recombine imparting the energy to a like carrier. This energy is subsequently thermalized in the lattice. Auger recombination can occur between two electrons and a hole or between two holes and an electron. As this is a multi carrier recombination mechanism described by Eq. (2.13) the Auger lifetime is inverse to the square of the carrier concentration and becomes the dominate recombination mechanism in highly doped materials and at high injection[37].

\[ \tau_{Auger} = \frac{1}{C_p(p_0^2 + 2p_0\Delta n + \Delta n^2) + C_n(n_0^2 + 2n_0\Delta n + \Delta n^2)} \]  

(2.13)

Here \( C_n \) and \( C_p \) are the Auger recombination coefficients.

SRH recombination occurs through a trap state and thus is influenced by the concentration of trap states and energetic position of trap states in the band gap as described by Eq. (2.14). Trap states exist due to impurities and defects, and thus SRH recombination is an extrinsic effect dependent on material quality. The probability of an impurity capturing a carrier is described by the capture cross section of the trap \( \sigma \) [37].

\[ \tau_{SRH} = \frac{\sigma_p^{-1}(n_0 + n_1 + \Delta n) + \sigma_n^{-1}(p_0 + p_1 + \Delta n)}{N_T\nu_{th}(n_0 + \Delta n + p_0)} \]  

(2.14)

with \( n_1 = n_ie^{(E_T - E_i)/kT} \), \( p_1 = n_ie^{(E_T - E_i)/kT} \)

Here \( \sigma_n \) and \( \sigma_p \) are the capture cross section of impurities for electrons and holes respectively, \( N_T \) is the impurity concentration and \( E_T \) is the energy level of these impurities.

Recombination centers are prevalent at material surfaces. The interruption of the crystal lattice results in incomplete bonding of surface atoms and exposure of the lattice increases the potential
for contamination. The high density of unsatisfied bonds and impurities lead to a nearly
continuous distribution of states in the band gap. SRH recombination can be used to describe the
surface recombination, but as the defects are distributed in two dimensions, the unit of the
recombination rate is a velocity and is thus referred to as the surface recombination velocity
(SRV). For a constant interface trap density $N_{it}$, the surface recombination velocity is described
by Eq. (2.15) [37]:

$$SRV = \frac{S_n S_p (p_s + n_s + n_i^2)}{S_n (n_s + n_{i1}) + S_p (p_s + p_{1s})}$$ (2.15)

$$S_n = \sigma_{ns} v_{th} N_{it} \quad S_p = \sigma_{ps} v_{th} N_{it}$$

Here the “s” subscript refers to the surface. Recombination occurs at the surface can be reduced
through the combination of approaches: reducing the defect states at the surface through
appropriate cleaning to remove surface impurities, chemically satisfying the dangling bonds, and
reducing concentration of the limiting carrier at the surface. The surface is typically passivated
with a thin layer of dielectric that has the potential to reduce the interface defect density, as well
as the minority carrier concentration at the surface. SRV is used to describe the surface
passivation quality, where a lower SRV reflects a lower rate of recombination at the surface.

The effective carrier lifetime ($\tau_{eff}$) is a combination of both the bulk and surface lifetimes as
simply described by Eq. (2.16).

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \frac{1}{\tau_s}$$ (2.16)

Here the carrier lifetime associated with the surface recombination ($\tau_s$) is dependent on the
carrier diffusion constant ($D$) and the wafer thickness ($W$) as carriers must first reach the surface
before recombining. As such the effective carrier lifetime is described by Eq. (2.17):

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \left[ \frac{W}{2SRV} + \frac{1}{D} \left( \frac{W}{\pi} \right)^2 \right]^{-1}$$ (2.17)

The importance of effective passivation in high efficiency devices is increased as the base
thickness is reduced. At low injection, with the use of higher quality base material, such as float
zone silicon, surface recombination dominates the effective lifetime, dictating the performance of the device.

The carrier concentrations in intrinsic material are equal to \( n_i \) and the intrinsic population is dependent on the temperature of the material. With the introduction of dopant impurities in extrinsic material, at equilibrium the carrier concentrations are dictated by the dopant impurity concentration (\( N_{D,A} \)) such that in \( n \)-type material \( n_0 \approx N_D \). Carrier populations are described by \( n_0p_0 = n_i^2 \), thus at low injection, recombination processes, which require both carriers are limited by the population of the minority carrier. At high injection conditions, the concentration of generated carriers is greater than the dopant concentration, and recombination becomes dominated by the injected carrier concentrations as reflected in Table 2-1.

Table 2-1: Expressions for low level and high level injection regimes for each of the recombination mechanisms [37]

<table>
<thead>
<tr>
<th>Recombination Mechanism</th>
<th>Low Level Injection</th>
<th>High Level Injection</th>
</tr>
</thead>
<tbody>
<tr>
<td>Radiative</td>
<td>( \tau_{Rad} = \frac{1}{Bn_0} )</td>
<td>( \tau_{Rad} = \frac{1}{B\Delta n} )</td>
</tr>
<tr>
<td>Auger</td>
<td>( \tau_{Aug} = \frac{1}{Cn_p^2} )</td>
<td>( \tau_{Aug} = \frac{1}{(C_n + C_p)\Delta n^2} )</td>
</tr>
<tr>
<td>SRH</td>
<td>( \tau_{SRH} = \tau_n )</td>
<td>( \tau_{SRH} = \tau_n + \tau_p )</td>
</tr>
</tbody>
</table>

2.7 Minority Carrier Diffusion Length

The performance of a solar cell is limited by the collection efficiency of the minority carriers. A parameter strongly affecting the collection efficiency is the minority carrier diffusion length which is related to the minority carrier lifetime by Eq. (2.18).

\[
L_n = \sqrt{D_n \tau_n} \quad L_p = \sqrt{D_p \tau_p}
\]  

(2.18)
Here $L_n, L_p$, are the minority carrier diffusion lengths of electrons and holes, respectively. To ensure efficient carrier collection the minority carrier diffusion length should be two to three times the distance between the location of generation and the region where the minority carriers are extracted[39]. The minority carrier diffusion length as a function of lifetime for 20 Ω-cm $n$-type silicon is illustrated in Figure 2-6.

**Figure 2-6**: Minority carrier diffusion length as a function of effective lifetime for 20 Ω-cm $n$-type silicon
Chapter 3

Device Concept and Sentaurus Modeling

This chapter introduces the architecture of the proposed device, highlights the features and discusses process simplifications in relation to the fabrication of similar high efficiency devices. The potential device performance is then explored as a function of the device parameters, using a two dimensional computational model.

3.1 Device Concept

We propose a true low temperature device architecture amenable to thin silicon wafers. The cell concept illustrated in Figure 3-1, combines an n-type base, hydrogenated amorphous silicon passivation and a rear point contact emitter formed using the LFE process. This represents a high efficiency device concept with a simplified fabrication sequence.

![Figure 3-1: Schematic of the Laser Fired Aluminum Emitter on Silicon using Hydrogenated Amorphous Silicon and Silicon Dioxide Dielectric Passivation Device Concept.](image)

The base of the cell is comprised of high resistivity n-type silicon. The front surface is
passivated with a full area $n$-doped hydrogenated amorphous silicon ($n$-a-Si:H) layer which has the dual role of both a passivating layer and a front surface field. An indium tin oxide (ITO) layer on the $n$-a-Si:H serves both as a transparent conducting oxide (TCO) and as an antireflective coating (ARC). This, in concert with chromium/silver (Cr/Ag) front metallization, constitutes the front of the cell.

The rear surface of the cell is passivated with a full area $i$-a-Si:H layer. The $i$-a-Si:H layer is capped with low temperature PECVD SiO$_x$ which acts as an effective electrically insulating layer as well as a dielectric rear mirror. Full area Al rear metallization covers the SiO$_x$ layer. An array of localized rear emitters is then formed by the LFE process, electrically connecting the Al layer to the cell via a junction formed by local diffusion of Al into the $n$-type base. The fabrication of this structure is carried out with only low temperature processing, notwithstanding the localized laser process.

### 3.2 Features of the a-Si:H/SiO$_x$ Passivated LFE Device

The inherent features of hydrogenated amorphous silicon passivated LFE on $n$-type crystalline silicon device are discussed below.

The use of $p$-type base material is well established in silicon photovoltaics due to its higher mobility for electrons ($1400 \text{ cmV}^{-1}\text{s}^{-1}$) compared to that of holes ($460 \text{ cmV}^{-1}\text{s}^{-1}$) which promotes efficient collection of photogenerated carriers. The advent of higher quality material and better surface passivation techniques has led to higher effective minority carrier lifetimes and thus longer hole diffusion lengths. Excellent surface passivation and relatively high hole mobility in low doped $n$-type wafers leads to demonstrated minority carrier diffusion lengths of $>4.5 \text{ mm}$ [22]. This coupled with thinner bases has led to very high charge collection efficiencies with open circuit voltages as high as 736 mV for cell concepts based on $n$-type material [40]. As well, the use of an $n$-type base reduces the material quality constraints for high performance devices as $n$-type crystalline material demonstrates higher bulk minority carrier lifetimes in Czochralski (CZ) and multicrystalline (MC) material than equivalent $p$-type material [41]. In addition, the long term performance of $p$-type based cells is negatively affected by the formation of light
induced boron-oxygen complex and thus reduction in cell efficiency; in contrast, \( n \)-type material does not suffer from this degradation [42].

The LFE cell concept facilitates the formation of an emitter in a matter of seconds, making it amenable to in-line production while avoiding the relatively significant heating up time and associated thermal load with batch emitter diffusion processing. This is particularly true in the case of \( n \)-type substrates, which require a thermal boron diffusion process for conventional emitter formation. The diffusion of boron requires sustained temperatures of \( > 900 \, ^\circ C \) [8], which can be detrimental to even high quality substrates such as Float Zone material, not to mention the temperature sensitive, defective materials such as MC substrates [8]. Additionally, the LFE presents the possibility of the fabrication process now being fully at low temperatures for amorphous passivated devices while avoiding the use of \( p \)-a-Si:H material for the formation of an emitter. The passivation quality of boron doped \( p \)-a-Si is found to be inferior to \( n \)-a-Si:H and \( i \)-a-Si:H [43], as well as \( p \)-a-Si:H exhibiting a reduction in band gap with increased doping density [44]. This results in increased optical absorption in the emitter and thus a reduction in the collection of photo-generated carriers. As an alternative to a \( p \)-a-Si:H emitter, promising results have been reported for thermally diffused Al full area emitters in inverted cells, albeit a minimum temperature of 900 °C is required [45].

The LFE results in a point emitter, which due to reduced emitter coverage area leads to a decreased reverse saturation current, and reduced interruption of rear surface passivation. Both effects theoretically contribute to an increase in \( V_{OC} \). The formation of the LFE is, however, accompanied by the formation of a laser-induced damage zone (LIDZ) that envelops the Al diffusion in the c-Si base. This LIDZ has been described electronically by Glunz as a 5 \( \mu \)m thick region, with a minority carrier lifetime of 0.3 \( \mu s \) [21]. This damage zone increases recombination in the SCR thus increasing the reverse saturation current of the second diode in Eq. (2.3); thereby, competing with the aforementioned factors. It has been demonstrated that the detrimental effect of the LIDZ can be mitigated with a 425 °C thermal anneal [22]. The point contact nature of the LFE also makes it a promising candidate for the simplification of the fabrication process of back contact solar cells such the Back Amorphous-Crystalline silicon Heterojunction cell (BACH) proposed by our research group [46].
The majority of LFC and LFE device structures reported to date involve some high temperature processing, with the highest device efficiency reported with thermally grown silicon oxide on both the front and rear surfaces[16]. Typically, even in cell concepts that utilize low-temperature PECVD based passivation in place of a thermal oxide, these cell concepts still utilize phosphorous front diffusion that requires a drive in temperature of >800 °C [8]. The passivation of crystalline silicon with amorphous silicon is a low temperature process, providing both excellent chemical and field effect passivation capabilities; excellent minority carrier lifetimes in excess of 7 ms have been demonstrated [47]. The potential for the realization of high efficiency devices, utilizing a-Si:H passivation is highlighted by the success of the Heterojunction with Intrinsic Thin-Layer device which has obtained efficiencies of 23% [27]. In addition to excellent chemical passivation of c-Si surfaces, a-Si:H possesses the advantage of tunable field effect passivation through appropriate doping allowing the a-Si:H passivation layer to play a dual role of surface passivation and surface field [48]. The realization of high minority carrier lifetime through low temperature surface passivation presents a process amenable to low cost, high yield production of high efficiency devices on thin silicon substrates.

3.2.1 Role of a SiO\textsubscript{x} Dielectric Layer

A range of device structures have been reported for which aluminum is fired through various single and dual passivation layers as reviewed in section 1.2. A completely low-temperature approach which provides excellent surface passivation requires the use of hydrogenated amorphous silicon on both surfaces [25]. Recently, Munoz reported the first fully low-temperature passivated LFC and LFE devices [49] using double sided amorphous passivation. These devices possess only a-Si:H passivation layers on the rear surface of the cell, leading to (i) reduction in passivation due to the AlSi formation at the Al/a-Si:H interface; (ii) band-bending due to the doping of the a-Si:H by Al; and (iii) performance limiting shunting in the case of the a-Si:H passivated LFE device.

The introduction of a dielectric stack of a-Si:H/SiO\textsubscript{x} overcomes these issues as the SiO\textsubscript{x} layer acts as both an electrical and chemical isolation layer. This layer prevents the large area formation of AlSi now that the aluminum back metallization is not in direct contact with the a-
Si:H passivation layer. Additionally, aluminum is known to catalyze the crystallization of a-Si:H at low temperatures (as low as 180°C) [50], which would be disastrous for passivation quality of the applied a-Si:H layer. Thus, the absence of a chemical barrier between the Al rear metallization and a-Si:H precludes device annealing.

A rear electrical isolation layer is required to prevent the shunting of the rear sheet metallization to the base via the $i$-a-Si:H rear passivation layer. The requirement of this rear surface isolation is highlighted by the decrease of $V_{OC}$ values with increasing pitch, reported by Munoz [49]. It can be expected that a shunting effect through Al spiking will occur between the rear metallization and the base through the intrinsic layer, thus significantly reducing $V_{OC}$, as seen by the trend toward lower $V_{OC}$ with reduced LFE to $i$-a-Si:H passivated area [49]. In addition the a-Si/SiO$_x$ stack provides the highest reflection of IR wavelengths, thus increasing the device spectral response in the IR and hence device efficiency [51].

### 3.3 Fabrication Simplification

With the trend toward thinner wafers and lower cost material, the issues associated with high temperature process steps are exacerbated. The proposed cell concept offers the potential of excellent manufacturability as a result of the absence of (i) wet chemical steps; and (ii) high temperature, long duration batch processing.

High efficiency device structures frequently employ photolithography for the definition of localized device features, but with an associated cost and processing complexity. High temperature batch processing for the growth of thermal SiO$_2$, thermal diffusion of boron, and thermal diffusion of phosphorus are also typically present in the fabrication of high efficiency devices. The standard LFC/LFE process utilizes both thermal oxidation and diffusion processes. A comparison of device fabrication steps for the a-Si:H passivated LFE and thermal oxide passivated LFC is presented in Figure 3-2. The fabrication process of the standard LFE already represents a reduction of six photolithography and diffusion steps over the standard PERL fabrication for the implementation of a localized BSF. A description of the fabrication processes of our proposed device is presented in detail in section 4.1.
Figure 3-2: Fabrication process comparison of the proposed a-Si:H/SiOₓ LFE and standard LFC

3.4 Device Model

To explore the optimal device architecture, a two dimensional computational model was implemented in Sentaurus, a three dimensional capable silicon device simulation software [52]. The modeling was developed collaboratively with Z. Rahim [53], a PhD candidate in our research group.

The device was simplified, using geometric arguments to a two dimensional unit cell represented in Figure 3-3. The device structure simplification was made to reduce the computational requirements for initial simulations. The unit cell represents a slice of the device extending from the midpoint of the front-side grid/finger metallization, to the midpoint between two neighboring metallization fingers. The unit cell is comprised of a textured front surface, modeled with Lambertian reflection. The front stack is comprised of an \( n \)-a-Si:H FSF layer, capped with an ITO layer. Conduction losses in the front metallization are not considered in this 2D implementation.
Figure 3-3: Two dimensional unit cell modeled in Sentaurus

The rear surface is modeled with a series of point emitters, that result in line emitters in the 2D simplification. Each point emitter is represented by uniform Al diffusion. Uniform Al diffusion is used to reduce computational requirements. The Al diffusion is surrounded by a LIDZ as suggested by Glunz [18] and is represented through a reduction in carrier lifetime in the defined region. The rear passivation is modeled as a 105 nm SiO$_2$ layer. The $i$-$a$-Si:H passivation layer is not explicitly included in the model, but is accounted for instead by setting the rear SRV to a correspondingly low value. The unit cell is completed by an Al rear metallization. The default device parameters used when investigating the effect of specific parameters are presented in Table 3-1.

<table>
<thead>
<tr>
<th>Device Parameter</th>
<th>Default Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Front metallization coverage</td>
<td>5 %</td>
</tr>
<tr>
<td>$n$-$a$-$i$-Si:H thickness</td>
<td>10 nm</td>
</tr>
<tr>
<td>Front SRV</td>
<td>10 cm·s$^{-1}$</td>
</tr>
<tr>
<td>Rear SRV</td>
<td>10 cm·s$^{-1}$</td>
</tr>
<tr>
<td>Base resistivity</td>
<td>1 Ω-cm</td>
</tr>
<tr>
<td>Base Thickness</td>
<td>300 μm</td>
</tr>
<tr>
<td>LFE width</td>
<td>15 μm</td>
</tr>
<tr>
<td>LFE pitch</td>
<td>500 μm</td>
</tr>
<tr>
<td>LFE Al Concentration</td>
<td>3.4e16 cm$^{-3}$</td>
</tr>
<tr>
<td>LIDZ width</td>
<td>5 μm</td>
</tr>
<tr>
<td>LIDZ lifetime</td>
<td>0.3 μs</td>
</tr>
</tbody>
</table>
3.5 Device Simulation Results

A number of interesting optimization factors are presented by the proposed device structure. These optimization factors are discussed below in conjunction with the presentation of simulation results.

Front Metallization

The total coverage of front metallization affects performance in two respects due to fabrication constraints. As arbitrary height to width ratios of front metallization cannot be realized with practical fabrication methods an inherent trade-off exists. Increased metallization coverage results in increased shadowing losses, but is associated with a reduction in series resistance and thus increase in fill factor. The effect of increased shadowing loss is illustrated in Figure 3-4, but does not account for resistive losses. As a result of the 2D simplification in the model, the impact of current flow along a metal finger of finite dimensions and the associated ohmic losses are not considered. The simulation shows the expected reduction in performance with increased shadowing loss for an ideal, lossless front metallization, but not the reduction in $FF$ associated with a reduction in series resistance.

![Figure 3-4: Influence of shadowing loss on device performance parameters](image-url)
FSF $n$-a-Si:H Thickness

Hydrogenated amorphous silicon, while possessing excellent c-Si passivation properties, has a direct-like band gap of 1.7 eV. The result of this is high absorption for wavelengths < 700 nm. The low carrier mobility in $n$-a-Si:H on the order of 1 cm$^2$/V·s and high defect density of $10^{18}$ cm$^{-3}$ [44], in comparison to those of c-Si, imply that carriers generated in the amorphous layer are less likely to be separated and collected than those absorbed in the c-Si base. An absorption depth of 100 nm is found for 500 nm light [54], thus the thickness of the layer should be minimized. A logarithmic relationship was found experimentally between $n$-a-Si:H thickness and passivation quality, thus a tradeoff exists, where adequate passivation must be achieved with a minimal FSF thickness. The influence of increased absorption of the $n$-a-Si:H FSF with increased thickness is illustrated in Figure 3-5. The device performance is seen to peak for a FSF thickness between 7 and 15 nm as the increase in surface passivation associated with thicker $n$-a-Si:H has a stronger effect on efficiency than the associated reduction in photogeneration in the base. For FSF thicknesses >15 nm, we see a reduction in $J_{SC}$ and $FF$ due to increased absorption in the FSF and increased series resistance associate with increased thicker $n$-a-Si:H.

![Graph showing the influence of increased $n$-a-Si:H FSF thickness on device performance parameters.](image)

**Figure 3-5**: Influence of increased $n$-a-Si:H FSF thickness on device performance parameters.
**Base Resistivity**

While there is a reduction in series resistance associated with decreased base resistivity resulting from increased dopant density, LFE device performance has been demonstrated to increase with increasing base resistivity. An increase in minority carrier lifetime and thus minority carrier diffusion length is seen with decreased dopant density[18]. Granek suggests that this has a secondary effect on increased performance. He suggests reduced recombination in the LIDZ with increased base resistivity, arguing that decreased base dopant density results in a higher injected minority carrier density than majority carrier density. The device operates in the high injection regime as a result of low dopant concentration. As indicated in Table 2-1, at high injection SRH recombination is limited by the availability of both carriers, not just the minority carrier. Thus SRH recombination in the LIDZ is suppressed due to the low concentration of majority carriers in the region, resulting in increased device performance[22]. This trend is reflected in the simulation result for wafers ranging from 0.1 – 100 Ω-cm presented in Figure 3-6. Here all performance parameters are seen to improve as a result of the decreased recombination, with the exception of $FF$, which can be expected to decrease as a result of increased series resistance with higher base resistivity.

![Figure 3-6: Influence of increased base resistivity on device performance parameters](image)

**Figure 3-6:** Influence of increased base resistivity on device performance parameters
**Base Thickness**

Thinner, higher quality wafers in the context of rear emitters, increase the importance of surface passivation as recombination shifts predominantly from the bulk to the surfaces. Thinner wafers also result in a reduced IR absorption on the first pass and thus rear surface reflection plays an important role in the ability to maximize the absorption of IR light (>1000 nm) through multiple reflections. In the context of inverted cell topologies, thinner wafers, may result in higher collection efficiency, as the carriers generated predominantly at the front of the cell as illustrated in Figure 2-4 b), have to travel a shorter distance to the emitter. The optimization of $J_{SC}$ is dependent on minority carrier diffusion length and rear surface IR reflectivity. The diffusion length is maximized with ideal passivation, while IR reflectivity can be increased with the use of back surface mirror. The dielectric mirror presented by an a-Si:H/SiO$_x$ stack provides excellent IR reflection, suggesting the high efficiencies should be realized on thin wafers as well[16]. Our model assumes an equal SRV of both surfaces of 10 cm·s$^{-1}$ and 100% IR reflection at the rear surface. A variation of base thickness shows a performance maximum for 150 µm thick wafers, as illustrated in Figure 3-7, where the variation in cell performance is dominated by the variation in photogenerated current as expected.

![Figure 3-7: Influence of base thickness on device performance parameters](image)
LFE Pitch

Pitch refers to the distance separating the LFEs. The LFE’s are fired in a square array, with each LFE separated from all 4 neighboring LFEs by a distance equal to the pitch as illustrated in Figure 3-3. An increased pitch is expected to result in an increase in $V_{oc}$ for the following reasons:

- an increase in carrier lifetime due to a reduction in rear surface passivation interruption;
- a reduction in the integrated density of laser-induced defects [17]; and
- a reduction in total emitter area and thus a reduction in the reverse saturation current for the device.

These performance improvement factors compete with the effects of an increased collection volume for each LFE. As pitch increases, the collection volume of each LFE increases until the minority carrier diffusion length is insufficient for full carrier collection, beyond which point dead areas in the cell result. An increased collection volume also leads to increased current crowding and thus an increased series resistance. In Figure 3-8 the variations in device efficiency as a function of both pitch and LIDZ thickness are presented. Here, for an assumed SRV of both surfaces of 10 cm s$^{-1}$ we see a performance optimum at a pitch of 500 µm. This is larger than the reported experimental value of 300 µm, demonstrating the ideal nature of the model. While further refinements of the model are required a trend of reduced performance with increased laser damage zone is observed with a maximum performance of $> 20.5\%$, if the LIDZ could be eliminated completely. The model predicts an efficiency of 19.5% for a LIDZ of 5 µm, substantiating Glunz’s proposed 5 µm and $\tau = 0.3 \, \mu$s LIDZ model with a reported efficiency of 19.4% for an LFE device [22].
Figure 3-8: Influence of LFE pitch and LIDZ width on a) $V_{OC}$ and b) efficiency ($\eta$).

LFE Diameter.

Provided sufficient laser pulse energy and appropriate beam delivery are available, the diameter of the LFE can be varied, thus modifying the percentage coverage of the emitter independent of LFE pitch. A reduction in $V_{OC}$ with increasing LFE diameter is expected as a result of an increase in the fractional surface area of the LIDZ and an increase in the reverse saturation current with increasing emitter area. In Figure 3-9 we see the impact of LFE line width variation as a result of the 2D simplification. An increase in current is observed with increasing LFE width, leading to a maximum performance at 15 $\mu$m; for larger LFE widths the degradation in $V_{OC}$ and $FF$ results in decreased device efficiency.
Summary of Modeling Results

Using the presented 2D Sentaurus simulation results as a basis to address the optimization of the device structure, optimal performance should be achieved with the following device parameters:

- Minimized metallization shadowing
- 10 nm $n$-a-Si:H FSF
- 150 $\mu$m thick, 100 $\Omega$-cm $n$-type base
- 15 $\mu$m width, 500 $\mu$m pitch LFE, with minimized LIDZ (2.5 $\mu$m)
Chapter 4
Experimental Results – Device Precursor Fabrication

This chapter presents the experimental work undertaken to fabricate a device precursor for the proof of concept. The required fabrication sequence is first outlined, followed by a brief description of hydrogenated amorphous silicon, associated deposition techniques and the passivation characterization technique used. Sections following this described the synthesis and corresponding results of each constituent layer of the device precursor.

4.1 Fabrication Sequence

The realization of the precursor for the LFE device which is illustrated in Figure 3-1, is implemented through a series of simple, low temperature steps without any wet processing illustrated in Figure 4-1. First, the high resistivity $n$-type crystalline silicon wafer is cleaned using an RCA cleaning procedure in order to minimize surface contaminants. Next, a 5% HF oxide etch is carried out and immediately thereafter an intrinsic hydrogenated amorphous silicon rear surface passivation layer is deposited on the wafer using the Direct Current Saddle Field Plasma Enhanced Chemical Vapour Deposition (DCSF PECVD) system. Subsequently, a thin $n$-type hydrogenated amorphous silicon front surface field is deposited on the other side of the wafer, completing the passivation of the device precursor. The amorphous silicon passivated crystalline silicon wafer is annealed to increase the effective minority carrier lifetime through the further reduction of the surface recombination velocity.

A transparent conductive oxide layer of indium tin oxide is deposited directly on top of the $n$-type hydrogenated amorphous silicon layer by rf-sputtering. The deposition of ITO is followed by an annealing step to recover the surface passivation lost during the ITO deposition. Next a rf-PECVD layer of $\text{SiO}_x$ is deposited on the intrinsic amorphous silicon rear surface passivation layer, forming a dual layer rear surface dielectric passivation stack. The $\text{SiO}_x$ layer thus providing the necessary electrical isolation for a high efficiency LFE device.
4.2 Hydrogenated Amorphous Silicon on Crystalline Silicon

4.2.1 Amorphous Silicon

Fundamentally, Hydrogenated Amorphous Silicon is distinguished from crystalline silicon by the absence of long range order. a-Si:H is composed of a continuous random network of Si and H atoms, with Si ideally covalently bonded to its four neighbor atoms, in a tetrahedral configuration, at least one of which is another Si atom. In this way the amorphous material consists of a Si-Si network that is internally passivated by hydride bonds. This leads to local order, with deviations in bond length and bond angle of less than 10% from its crystalline
counterpart [44]. The existence of local order results in analogous electronic features to c-Si including the existence of a band gap. The lack of long range order leads to flexibility in the network, and electronic features not shared with c-Si. Perhaps the most prominent being a direct-like band gap owing to the relaxation of the momentum conservation rule, extended band tails that result from the disorder of the network, and defect states in the mid gap owing to a fraction of Si atoms with dangling bonds (DB) in the network[44]. The density of states of hydrogenated amorphous silicon is shown in Figure 4-2.

![Density of states of hydrogenated amorphous silicon as a function of energy](image)

**Figure 4-2:** Density of states of hydrogenated amorphous silicon as a function of energy [44].

The properties of a-Si:H can vary strongly with deposition technique and deposition conditions. Both the atomic structure and hydrogen content vary with deposition conditions, meaning that dangling bond densities vary with the growth conditions of the material and lie in the range of $10^{20}$ cm$^{-3}$ for pure a-Si [44] to $< 5 \times 10^{14}$ cm$^{-3}$ for state of the art a-Si:H material [55]. Atomic hydrogen present in the network provides passivation of material defects by terminating the dangling bonds of the silicon atoms, thus hydrogen plays an essential role in reducing the defect density of the material. A composition of 10% atomic hydrogen is typical, with hydrogen existing in SiH$_3$, SiH$_2$, SiH$_1$ and in clusters as illustrated in Figure 4-3. Increasing hydrogen content is also known to increase the band gap of the material [56].
Hydrogenated amorphous silicon can be doped substitutionally despite the flexibility of the network and the availability of hydrogen for passivation. Doping is however associated with an increase in defects, as well as a logarithmic relationship between dopant concentration and dopant activation. This results in increases in defects associated with higher doping in a-Si:H, but limited modifications to the Fermi level. $P$-type doping is known to cause a reduction of the band gap, thus it is not an ideal front layer for a solar cell [44].

The crystalline silicon surface passivating properties of a-Si:H is a topic of significant scientific and industrial interest. Excellent passivation and thus high minority carrier lifetimes have been demonstrated in test structures, with lifetimes in excess of 7 ms attained [47]. Amorphous silicon passivation possesses both excellent chemical and field effect passivation capabilities, while possessing the advantage of tunable field effect passivation through appropriate doping of the passivation layer [48]. Chemical surface passivation is maximized by a-Si:H deposition conditions that promote an abrupt crystalline/amorphous interface, and monohydride surface passivation[57].

The deposition of a-Si:H passivation is inherently a low temperature process, thus enabling a true low temperature device fabrication process while providing excellent surface passivation properties. The importance of the role of hydrogen in the excellent passivation properties places a limitation on the thermal stability of a-Si:H based passivation. While increased temperature increases hydrogen diffusion, promoting the redistribution of hydrogen and passivation of
dangling bonds, exposure to temperatures in excess of 400 °C results in hydrogen evolution [44]. Thus, the application of a-Si:H as a passivation material results in post a-Si:H deposition processing temperature limit.

4.2.2 Amorphous Silicon PECVD Deposition

Amorphous silicon has been deposited by a range techniques, including thermal decomposition [25], photo decomposition [58], Direct Current (DC) PECVD and non-DC PECVD. The most widely used and studied deposition method for a-Si:H is the Capacitively Coupled Plasma (CCP) PECVD, operated at 13.56 MHz [55]. A range of other technologies have also been explored including higher rf-frequencies [59] and inductively coupled plasmas (ICP) [60].

The Direct Current Saddle Field Plasma Enhanced Chemical Vapour Deposition system is a novel PECVD system unique to our research laboratory. The elegant simplicity of the DCSF PECVD system is illustrated in Figure 4-4.

Figure 4-4: Schematic of the Direct Current Saddle Field Plasma Enhanced Chemical Vapour Deposition System in possible electrode configurations; a) Pentode, b) Tetrode, and c) Triode.
The DCSF PECVD posses the simplicity of a DC glow discharge, while addressing the low pressure operation and ion energy control limitations of DC PECVD. The DCSF PECVD concept is a variation of the DC diode PECVD reactor, designed to extend the path length of electrons. A DC diode PEVCD is comprised of 2 parallel plates (anode and cathode) while the DCSF PECVD is comprised of a semi-transparent anode with parallel cathodes on either side. The semi-transparent anode serves to extend the path length of electrons by virtue of its symmetric electric field which promotes the oscillation of electrons. Extending the electron path length without increasing the length of the deposition chamber is akin to making the plasma denser while the physical size of the reactor is unchanged, and thus the advantages of low pressure PECVD are retained.

Growth of good quality a-Si:H requires optimal deposition conditions. A large parameter space is associated with the DCSF PECVD depositions, including grid configuration, chamber pressure, gas mixture, gas flow rate, substrate temperature and voltages applied to substrate, cathodes and anode. Three electrode configurations are presented in Figure 4-4. In this study the tetrode configuration was used, which provides high quality a-Si:H but at the lowest growth rate as the substrate is furthest removed from the plasma. The tetrode configuration is comprised of a semi-transparent cathode nearest to the substrate and an opaque cathode furthest from the substrate. This configuration creates a remote plasma region relative to the film growth surface. Ions and radicals created in the plasma region will drift and diffuse to the substrate; during this transit period the more reactive radicals such as SiH$_2$ and SiH will undergo a reduction in their concentration. A heater and an electrical contact in the substrate holder facilitate the control of substrate temperature and substrate bias.

Currently there are two generations of the DCSF PECVD system in our laboratory. The first, denoted Gen 1, is a simpler system which does not have a loadlock and hence the deposition chamber is exposed to atmosphere during loading and unloading of each sample. The electrodes of this system are vertically oriented. The electrodes and chamber lining are removed and cleaned in a heated KOH bath following each deposition. The second system, denoted Gen 2.1, is a larger and more complicated system which has both a loadlock attached to the deposition chamber and a nitrogen atmosphere glove box interfacing the loadlock entrance doorway. This
permits pre-deposition chemical wafer treatments to occur in a controlled atmosphere without the influence of atmospheric oxygen levels or particulate contamination.

4.2.3 Microwave Photoconductance Decay

The Microwave Photoconductance Decay (µPCD) measurement technique is a well accepted, spatially resolved, direct method for determining the effective minority carrier lifetime in silicon wafers. Microwave reflection is used to locally monitor the conductivity of the wafer, and thus the excess carrier concentration, the operation of which is illustrated in Figure 4-5. Initially excess carriers are generated in the sample using a 904 nm laser which illuminates a 100 µm diameter spot for a period on the order of 100 ns. Excess carriers are generated in a volume about 30 µm deep [61]. Following the generation of carriers, 10.377 GHz microwaves impinge on the sample and the reflected signal is collected by an antenna. The microwave reflectivity of the sample is proportional to the carrier concentration. The effective minority carrier lifetime can be determined by fitting the decay of the reflected power of the microwave signal as a function of time with Eq. (4.1) to determine the effective minority carrier lifetime ($\tau_{eff}$).

$$\Delta n(t) = \Delta n_0 e^{-t/\tau_{eff}}$$  \hspace{1cm} (0.1)

Here $\Delta n_0$ is the initial excess carrier density and $\Delta n(t)$ is the instantaneous carrier density.

Figure 4-5: Schematic of Microwave Photoconductivity Decay System [62]
The effective lifetime measured by the µPCD technique is a composite of the bulk recombination lifetime, the time required for carriers to diffuse to the front and rear surfaces and the surface recombination lifetime as described in Eq. (2.17).

In the case of thin, high purity silicon substrates, the surface recombination lifetime dominates the effective lifetime, and thus the measurements made on equivalent wafers provide a basis for comparison of surface recombination velocity.

4.3 Device Precursor Fabrication

4.3.1 Symmetric \(i\)-a-Si:H Passivated Lifetime Samples

Excellent surface passivation is a perquisite for high photoelectric conversion in solar cells, and in particular in rear emitter solar cells as previously discussed. Initially the \(n\)-type crystalline silicon passivation experiments were conducted in the Gen 1 DCSF PECVD to obtain minority carrier lifetimes of > 1 ms, as required for effective collection in rear emitter solar cells. The properties of intrinsic a-Si:H films deposited in the Gen 1 DCSF PECVD have been previously reported by our group [63], as have surface passivation properties of intrinsic and \(n\)-type doped layers deposited as symmetric structures on \(n\)-type Topsil, FZ 1 Ω-cm, double side polished (100) wafers deposited in the Gen 2.1 system [64].

As it has been shown that the efficiency of LFE cells increases with increasing base resistivity, [22] high resistivity \(n\)-type wafers were selected as the base material for our experiments. A substantial body of work has been completed by our group on the passivation of low resistivity \(n\)-type wafers (0.5-1 Ω-cm), while the passivation of higher resistivity wafers has not been explored. In this work, initially the passivation of two different single crystalline silicon wafer types was explored: Siltronic FZ \(n\)-type 20 Ω-cm (100) double side etched having a thickness of 195 μm, and Siltronic FZ 75 Ω-cm (111) single side polished having a thickness of 160 μm. These wafer resistivities correspond to dopant densities of \(2.2\times10^{14}\) cm\(^{-3}\) and \(5.9\times10^{13}\) cm\(^{-3}\), respectively.
Passivation of these wafers was explored using symmetric $i$-a-Si:H depositions. The wafers were first cleaned using the standard RCA method. Immediately prior to being loaded into the deposition chamber the wafer was immersed in 5% HF for 1 minute to remove any native oxide that formed during wafer storage. Additionally, the HF etch acts to terminate the dangling bonds at the surface with hydrogen.

The intrinsic a-Si:H layers were deposited in the tetrode configuration, thereby keeping the substrate remote from the plasma region as discussed in section 4.2.2. Once the deposition chamber had reached a vacuum of a minimum pressure of $10^{-6}$ Torr, the heater was set to a temperature of 250 °C, and a minimum pre-heat period of 3h was allowed for the substrate holder to reach a steady state temperature of 180 °C. The intrinsic a-Si:H was deposited with a 30 SCCM flow of pure silane (SiH$_4$), and an anode current of 17.5 mA corresponding to an anode voltage of about 550 V at the start of the deposition and an ending anode voltage of about 560 V depending on the duration of deposition. The increase in the anode voltage is due to the increase in resistance associated with the buildup of a-Si on the electrodes. The sample substrate holder temperature begins at 170 °C and rises to 190 °C depending again on the duration of deposition.

An exploratory time scan was completed, combined with an annealing step, yielding excellent passivation results of up to 3 ms on the 20 Ω-cm substrate. Minimal passivation of < 10 µs was attained on the 75 Ω-cm wafers. The existence of an a-Si:H layer was confirmed on the 75 Ω-cm with a Spectroscopic Ellipsometry (SE) measurement. The reason for poor passivation on the higher resistivity (111) wafers is unclear, and would require a thorough parameter scan to determine the cause. One possible explanation is the build-up of charge on the high resistivity wafer causing ions to accelerate and thus causing ion damage at the interface.

Minority carrier lifetimes of 60 to 950 µs were attained on the 20 Ω-cm wafers with 20 and 25 minute depositions, representing a film of approximately 30 nm. A post-deposition annealing step consisting of annealing the sample for 40 minutes on a hotplate at 240 °C in air, served to increase the lifetime of the samples to a range of 1 to 3 ms with maximum passivation occurring for 20 minute depositions as shown in Figure 4-6. The thermal energy provided by annealing increases diffusion of hydrogen within the amorphous network. The increased passivation
quality of a-Si:H films with thermal annealing is due restructuring of Si-H bonding at the c-Si interface, resulting in an increase in monohydride bonding at the c-Si surface [65]. This improvement in passivation quality is clearly illustrated by the lifetime maps of Figure 4-7, where annealing of the a-Si:H passivation layers results in an excellent effective carrier lifetime of 3.5 ms, or an SRV of < 2.5 cms$^{-1}$ calculated by Eq. (2.17).

**Figure 4-6:** Effective minority carrier lifetime for symmetric i-a-Si:H samples as a function of deposition time and annealing for 20 Ω-cm crystalline silicon wafers.

Assuming near perfect material properties of the FZ wafers used, the bulk lifetime can be assumed to be Auger recombination limited, corresponding to a minority carrier lifetime of >20 ms for a doping density of 2.2x10$^{14}$ cm$^{-3}$ and a minority carrier excess carrier density of 1x10$^{15}$ cm$^{-3}$. Thus, it is seen that the minority carrier lifetime of the a-Si:H samples is still surface recombination limited. For 20 Ω-cm $n$-type FZ material, which corresponds to a minority carrier diffusivity of 12.1 cm$^{2}$s$^{-1}$ [35], and using an effective minority carrier lifetime of 1 ms in Eq. (2.18) we obtain a diffusion length of 1100 µm as illustrated in Figure 2-6. This is 5.5 times the thickness of the wafer and is a sufficiently large diffusion length for the efficient collection of carriers (holes) to the back side emitter.
4.3.2 Asymmetric $i$-$a$-Si:H/$n$-$a$-Si:H Passivated Device Precursors

Having realized sufficiently high minority carrier lifetime on 20 $\Omega$-cm $n$-type wafers with symmetric $i$-$i$ test structures, attention was turned to achieving high minority carrier lifetimes on 20 $\Omega$-cm $n$-type wafers with the asymmetric passivation structures required for the device. In this case the device passivation was comprised of an $i$-$a$-Si:H layer on one surface and an $n$-$a$-Si:H layer on the opposing surface. For all devices the $i$-$a$-Si:H layer was deposited first at the conditions outlined in section 4.3.1. The wafer was marked upon removal from the deposition chamber in order to identify the $i$-$a$-Si:H side. Immediately prior to being loaded into the deposition chamber the wafer was immersed in 5% HF for 1 minute. The same deposition parameters were used for the $n$-$a$-Si:H layer, with the exception of the precursor gas composition. Phosphine (PH$_3$) was introduced into the gas stream as the donor precursor for $n$-type doping of

Figure 4-7: Symmetric lifetime sample comprised of 20 minute $i$-$i$ depositions, demonstrating; a) &b) 950 $\mu$s pre-annealing effective lifetime, and c & d) 3.5 ms post-annealing effective lifetime.
the film. A preliminary scan of deposition time was conducted with a PH$_3$ concentration of 0.75%. Unannealed lifetimes of 15-22 $\mu$s and annealed lifetimes of 25-122$\mu$s were achieved for $i$-a-Si:H deposition times of 25 min and $n$-a-Si:H deposition times of 12-18 min. An increase of PH$_3$ concentration to 1.5% was found to increase lifetime to a minimum of 300 $\mu$s for annealed samples. Thus, all subsequent depositions were conducted with a 1.5% PH$_3$ gas composition.

While the importance of front surface passivation is clear in the context of rear emitter cell concepts, it is important to minimize absorption of carriers in the amorphous front surface field. Light absorbed in this layer is unlikely to contribute to the photocurrent. The low carrier mobilities in $n$-a-Si:H on the order of 1 cm$^2$V$^{-1}$s$^{-1}$ and high defect density of $10^{18}$ cm$^{-3}$ [44], in comparison to those of c-Si, mean that carriers generated in the amorphous layer are less likely to be separated and collected than if absorbed in the base. This is further exacerbated by the direct like band gap of a-Si:H, resulting in an absorption depth of 100 nm for 500nm light [54]. Thus, the thickness of the layer must be minimized while maintaining adequate passivation.

A scan of $n$-type deposition durations of 8-14 minutes was conducted. The reduced deposition time combined with a known reduction in growth rate of phosphorous doped $n$-type a-Si:H [66], resulted in thin n-doped layers. This time span was scanned on both sets of wafers with 20 and 25 minute intrinsic a-Si:H depositions. A monotonic increase in passivation as a function of increased deposition time resulted for both i-layer thicknesses as illustrated in Figure 4-8. Here the maximum passivation was obtained for an n-layer deposition time of 14 min, corresponding to a FSF thickness of $\sim$15 nm. It can be assumed that the optimal passivation layer thickness was not reached, but sufficient lifetime was achieved with a much thinner layer than that of the i-layer. The scatter in the results can be attributed at least in part to the rudimentary loading arrangement of the Gen 1 system. For any given lifetime sample, the deposition chamber is exposed to atmosphere twice, and the chamber lining, substrate holder, and grids are cleaned and installed twice. Thus, variability in deposition repeatability can be attributed to both variation in contamination from deposition to deposition, as well as loading related chamber configuration issues such as duplicating substrate holder thermal transfer and grid alignment.
Through the comparison of sample lifetime area maps, repeatedly non-uniformity in passivation was identified. Inspection of the substrate holder following deposition revealed a variation in colour due to thin-film interference. This variation of colour is presented for 6 different deposition times in Figure 4-9, clearly illustrating the non-uniformity in deposition at the few nanometers thickness level. Here thin-film interference was used to infer deposition thickness as samples were deposited on as-received etched wafers, and thus SE measurements were not possible.

**Figure 4-8**: Effective minority carrier lifetime of asymmetric passivation structures as a function of $n$-a-Si:H deposition time and annealing. Here presented for differing $i$-a-Si:H deposition times of 20 min, and 25 min.

**Figure 4-9**: Variation in thin-film interference of a-Si:H films deposited on a SS substrate, indicating non-uniformity deposition for varied a-Si:H deposition times.
The deposited thickness varies monotonically from thickest at the top to thinnest at the bottom of the substrate holder. This non-uniformity in deposition rate as a function of position can be attributed asymmetric positioning of the gas inlet located at the top and the outlet port at the side of horizontally mounted deposition chamber. The variation in deposition thickness, was confirmed through deposition of amorphous silicon on an aluminum coated, polished wafer as shown in Figure 4-10.

![Figure 4-10: Variation of a-Si:H thickness deposited on a Al/c-Si sample (polished wafer diameter 100mm), as a function of position.](image)

Here the thickness sample was deposited at standard deposition conditions, for 20 minutes and the resulting a-Si:H layer thickness was measured using SE. Film thicknesses of 15-27 nm resulted corresponding to a growth rate varying between 0.75 to 1.35 nm/min depending on the location on the wafer. This corresponds well with a previously measured growth rate of 1.05 nm for the same deposition condition, on a polished silicon wafer.

To investigate the influence that the growth rate and thus final thickness has on passivation properties of a-Si:H, wafers were appropriately rotated when loaded such that the higher growth rate occurred in the same region of the wafer on the two sides. In Figure 4-11, a 23 minute $i$-a-Si:H deposition is followed by a 14 minute $n$-a-Si:H deposition. A clear spatial variation of passivation is visible with minority carrier lifetime increasing from left to right on the wafer in a range from 25 – 600 $\mu$s, with an average lifetime of 292 $\mu$s. Following an annealing step at 240
°C for 40 min increased the average carrier lifetime increases to 1095μs, and the spatial variation of lifetime persists varying from 750 – 1300 μs.

**Figure 4-11:** Effective minority carrier lifetime of device precursor sample ID-1; a) & b) following a-Si:H deposition, and c) & d) following a 40 min, 240 °C anneal.

Both the deposition time scan results and the non-uniformity in the deposited thickness indicate that a thicker n-a-Si:H FSF leads to increased passivation. A deposition time of 14 min is expected to result in a n-a-Si:H layer of < 15 nm due to slower growth rate of n-a-Si:H than that of i-a-Si:H. Deposition times beyond 14 minutes were not explored as acceptable passivation results were obtained with a 14 minute n-a-Si deposition, and as previously stated, the thinnest, effective FSF was the design goal.

Unlike the FSF, the thickness of rear surface passivation has no effect on device performance except through its effect on passivation. Photons reaching the rear surface of the cell have energies well below the 1.7eV band gap of a-Si, and thus no absorption loss will occur. A scan of i-a-Si:H deposition times was conducted with the n-a-Si:H deposition time held constant at 12
and 14 minutes. In both cases a maximum in passivation was found for $i$-a-Si deposition time of 22-23 minutes as illustrated in Figure 4-12.

With the previously stated average growth rate of 1.05nm/min and maximum growth rate of 1.35 nm/min, a thickness of 24nm and no greater than 31nm was expected for the intrinsic layer on the rear side. A decrease in passivation quality of $i$-a-Si:H on c-Si as a function of thickness is reported to occur for a intrinsic amorphous silicon film thickness beyond 40 nm [48]. For films beyond this thickness an increase in interfacial defect density was observed which may result from increased mechanical stress of thicker layers, which accumulates at the c-Si/a-Si interface. In our case the film was thinner than the reported thickness for onset of passivation loss, nonetheless, the results demonstrated the expected trend. In support of the observed trend, a symmetric $i$-a-Si:H sample with a twenty minute deposition on both sides clearly showed higher lifetime on the portion of the wafer that had received a thinner layer of $i$-a-Si:H for both pre and post anneal measurements.

The apparent trend of decreased minority carrier lifetime for increased deposition time is not fully understood. The existence of a high lifetime sample for a 14 min $n$-a-Si:H layer and 30 min $i$-a-Si:H layer suggest that additional factors such as sample temperature, or sample and chamber cleanliness may have a role.

The highest sample lifetime was obtained with a 23 minute $i$-a-Si:H deposition followed by a 14 minute $n$-a-Si:H deposition, resulting in > 1ms post anneal lifetimes as illustrated in Figure 4-11. This minority carrier lifetime corresponds to a minority carrier diffusion length of 1.1mm, which is sufficiently large for efficient carrier collection by a rear emitter.
Figure 4-12: Effective minority carrier lifetime of asymmetric passivation structures as a function of \(i\)-a-Si:H deposition time and annealing. Here presented for differing \(n\)-a-Si:H deposition times of 12 min and 14 min.

4.3.3 Process Transfer to Gen 2.1 DCSF-PECVD System

Subsequent to achieving good passivation results in Gen 1.1, the process parameters were transferred to Gen 2.1, a more refined, vertical implementation of the DCSF PEVCD, equipped with a nitrogen atmosphere glove box and a chamber loadlock which provided a more controlled environment for a-Si:H depositions.

Passivation as a function of deposition time and deposition temperature have been characterized by our group on polished, \(n\)-type, (100), 1 Ω-cm wafers in the context of the Gen 2.1 system [Bahardoust PhD Thesis]. The results of these deposition parameter scans are presented in Figure 4-13.
Figure 4-13: Unannealed effective minority carrier lifetime of symmetric $i$-$a$-Si:H lifetime samples on $1 \, \Omega$-cm (100) $n$-type crystalline silicon wafers as a function of, a) temperature, for a deposition time of 30 min, b) time for a deposition temperature of 170 °C [Bahardoust PhD. Thesis].

Drawing on the results presented in Figure 4-13 and the physical differences of Gen 1 and Gen 2.1, appropriate parameters for the transfer of the process were determined. The parameters selected for deposition of the $i$-$a$-Si:H layer in Gen 2.1 were: 160mTorr chamber pressure, 30 SCCM SiH$_4$, heater temperature of 320 °C corresponding to a sample temperature of 170 °C, and an anode current of 34.5 mA (owing to the larger plasma volume in relation to Gen 1). For our devices, a deposition time of 30 min in Gen 2.1 was selected, which has been previously shown to provide 40 nm thick $i$-$a$-Si:H layer, and has demonstrated high lifetimes. For a symmetrical $i$-$i$ deposition on 20 $\Omega$-cm wafers we measured pre annealing and post annealing effective minority carrier lifetimes of 1139 $\mu$s and 1357 $\mu$s, respectively.

For our asymmetric device configuration we used the above described parameter set for the deposition of the $i$-$a$-Si:H layer on the rear side. For the $n$-$a$-Si:H layer we used the same the same parameters except for the introduction of 0.75% phosphine in the precursor gas and deposition time of 25 min. These were chosen on the basis of the parameters used for the back surface field developed in the context of the heterojunction device by our group [personal communication]. The resulting $n$-$a$-Si:H layer was visually thicker than samples created in Gen
1; this is perhaps not unexpected given that the heterojunction device research mentioned above uses the n-doped amorphous silicon layer for a back surface field where thickness is not a factor from an optical absorption perspective. These asymmetric i-n device precursors displayed pre-anneal lifetimes of 1 – 1.1 ms and post-annealed lifetimes of 1600-1800 μs.

Thus, a successful transfer of deposition parameters was completed from Gen 1 to Gen 2.1, resulting in higher annealed lifetimes and greater repeatability, albeit with a lower doped, thicker front surface field layer.

4.4 Light Management and Charge Extraction Layers.

A well passivated, thin substrate, with a minority carrier diffusion length much greater than substrate thickness is a perquisite for a high efficiency rear emitter solar cell. The realization of a solar cell requires charge extraction and light trapping features. In this section the experimental implementation of these features will be discussed.

4.4.1 Transparent Conductive Oxide Layer

As previously discussed, a front layer TCO is required in the context of an a-Si:H front surface field. The high resistivity of the a-Si:H layer has a minimal effect on cell performance if extracted carriers are required only to travel a vertical distance on the order of 10nm before collection in a low sheet resistance TCO where they can travel laterally a distance on the order of 1mm to the nearest front metal grids for charge extraction. As a TCO layer we selected indium tin oxide, a wide band gap semiconductor of 3.3 eV optical gap which is highly degenerately doped n-type with impurity tin and has an index of refraction of n~1.8. The sheet resistance of ITO is a function of both layer thickness and dopant density. As such there is a fundamental trade-off between transmittance of ITO and sheet resistance.

Due to the lower index of refraction of ITO compared to silicon, the TCO also provides an anti-reflection function. Optimal performance is realized for a single layer AR coatings by minimizing the normal reflection of 600 nm light [35]. For ITO the required thickness is
determined from Eq. (2.7) to be 85nm. We deposited ITO in the K.J. Lesker rf-sputtering system, using an indium tin oxide target with a composition of 10 weight percentage indium oxide. A base pressure of $10^{-8}$ Torr is used to ensure low contamination of the film, and the deposition is carried out at room temperature. Argon is used as the sputtering gas, at a flow of 30 SCCM, and a deposition pressure of 3 mTorr. An rf power of 100W results in a deposition rate of 0.4 Å/s. The film thickness of 100nm is deposited as reported by a resonant crystal thickness monitor.

The sheet resistance of TCO deposited on a sample of Corning 1917 glass is measured with a 4 point probe to determine the electrical properties of the film. Sheet resistances of 50 Ω/□ are obtained with a 260 °C for a 40 min anneal. This compares well to the 40-60 Ω/□ emitter sheet resistance of industrial cells. The average spectral transmission is 87%, but varies as a function of wavelength as illustrated by the spectral transmission of the ITO layer on Corning glass as illustrated in Figure 4-14 a). For ITO on silicon the spectral reflection is minimized at 650 nm and varies with wavelength as illustrated in Figure 4-14 b).

**Figure 4-14**: a) Spectral transmittance of 100 nm ITO layer on Corning glass b) spectral reflectivity of ITO/a-Si/Si structure

The deposition of ITO was found to cause a drastic, but recoverable reduction in passivation. The passivation quality was recovered with a subsequent annealing step, of 40 min at 260 °C. The mechanism causing this recoverable loss of passivation is not understood. An investigation
of the ITO/$n$-a-Si:H/c-Si stack using Secondary Ion Mass Spectrometry (SIMS) reports the redistribution of hydrogen from the a-Si:H layer into the ITO layer and Si substrate with the deposition of ITO, as well as the formation of intermediate layers of ITO:H, a-Si:H:O and Si:H [67]. Annealing is known to redistribute hydrogen in a-Si:H. Thus an ITO deposition induced redistribution of hydrogen in the system is deemed to be responsible for a recoverable reduction in passivation.

The uniformity of passivation has been reduced as illustrated in Figure 4-15, along with the total passivation quality. The change in passivation uniformity can be attributed to contamination of the wafer surfaces through handling.

**Figure 4-15:** Effective minority carrier lifetime of sample ID-1 a) & b) following ITO deposition with average lifetime of 92 µs, and c) & d) following subsequent 40 min, 240°C anneal with average lifetime of 860 µs.
4.4.2 Electrical Isolation Layer

A rear electrical isolation layer is required to prevent the shunting of the rear sheet metallization to the base via the i-a-Si:H rear passivation layer. The importance of SiO$_x$ as an isolation layer in the realization of acceptable $V_{OC}$ and thus efficiencies, is highlighted by Munoz recent demonstration of a fully a-Si:H passivated LFE device[49], and is discussed in section 3.2.1.

Dual passivation layers comprised of a-Si:H/SiO$_x$ layers have been studied in depth with excellent passivation results [19]. Additionally the rear surface reflectance in the IR is found to be highest for the a-Si:H/SiO$_x$ stack when compared to thermal oxide passivation and other dielectric passivation stacks [51].

We deposited the SiO$_x$ layer by rf-PECVD in an Oxford Instruments PlasmaLab 100 system. Starting with a base pressure of 1 mTorr, a gas mixture of 700sccm N$_2$O, and 5% mixture of SiH$_4$/N$_2$ at a flow rate of 30 SCCM maintains a chamber pressure of 400 mTorr, at a power of 30 W. The deposition rate was determined with a deposition time scan on polished wafers with subsequent thickness measurements performed with SE. A growth rate of 7.1 nm/min was determined. Electrical measurements confirmed that 105 nm films provided >2MΩ electrical isolation, which is sufficient to prevent shunting loses at the rear of the device. An acceptable loss in passivation quality was found to result from these deposition conditions as illustrated in Figure 4-16.

![Figure 4-16](image)

**Figure 4-16**: Effective minority carrier lifetime of Sample ID-1 following a SiO$_x$ deposition
As the deposition of the SiO_x layer effectively completes the encapsulation of the a-Si:H passivation layers, we investigated if a post SiO_x anneal might increase the passivation properties of the completed structure. Samples were annealed for 40 minutes at temperature intervals of 50 °C. A marginal gain of 3% in lifetime is observed for an annealing temperature of 250 °C, which matches the SiO_x deposition temperature. Temperatures beyond this result in a reduction in passivation. Through this experiment we concluded that post SiO_x annealing did not result in a significant increase in minority carrier lifetimes, given our SiO_x deposition parameters.

Considering this finding, deposition was carried out immediately following the anneal of the ITO layer to maximize lifetime. The passivation quality of samples possessing only an ITO layer passivation was observed to degrade from a maximum lifetime following annealing, with exposure to ambient conditions. This degradation was monitored through a series of lifetime measurements subsequent to the standard annealing step.

Our optimized PECVD SiO_x deposition induced a reduction in minority carrier lifetime of 5-15% which was not recovered through annealing in air. Despite this associated loss in lifetime, lifetime after the realization of the rear surface a-Si:H/SiO_x dielectric stack was found to be sufficient for our purposes.

4.4.3 Front and Rear Metallization

Both front and back metallization were applied by e-beam evaporation using a K.J. Lesker e-beam evaporation system.

The front metallization is composed of a stack of chromium and silver. A 5 nm layer of Cr is deposited onto the ITO to improve adhesion of Ag at a rate of 0.02 nm/s. Subsequently, silver is deposited at deposition rates of 0.2 nm/s for the first 100 nm, 1 nm/s for the following 100 nm and 3 nm/s for all following silver deposition. For depositions thicker than 1 μm, a 5 minute cooling period could be included to reduce the total thermal load on the wafer. This is implemented by closing the substrate shutter and reducing the e-beam power to 5%, thereby allowing the substrate to cool.
The front metallization pattern was defined using a laser machined silicon shadow mask, fabricated on a 200 μm silicon wafer to eliminate wet chemical processing in the cell fabrication. The front metallization pattern defined a 1x1 cm device, with six 7.5 mm x 0.08 mm fingers spaced at 1.5 mm center-to-center and a busbar of 0.130 mm width. Spreading of the features, as is expected with the use of a shadow mask, resulted in 0.12 mm finger widths for 1 μm Ag deposition and 0.17 mm finger widths for 4 μm Ag depositions. This corresponds to 8.3% and 11.1% shadowing coverage of the cell surface.

The rear metallization was comprised of a continuous 2μm Aluminum layer. This layer was deposited from 99.999% purity aluminum. Similarly to the Ag deposition, aluminum was deposited with a graded deposition rate, where the first 100 nm were deposited at 0.2 nm/s, the next 100 nm were deposited at 1 nm/min and the remaining layer thickness was deposited at 1.5 nm. Again a 5 minute cooling period could be included for depositions > 1μm.

4.5 Lifetime as a Function of the Device Precursor Fabrication Process

The maintenance of passivation quality through the entire device fabrication process is essential to the realization of an efficient device. Here the variation of passivation resulting from the required fabrication steps is presented for both Gen1 and Gen 2.1 samples. Notwithstanding the recoverable loss of lifetime associated with the deposition of ITO, an acceptable degradation of lifetime from initial post a-Si anneal lifetime was demonstrated. Variations in degradation of lifetime throughout the process are attributed to wafer handling and possible contamination during delays between process steps.

While a full optimization of each process step within the context of this device is beyond the scope of this work, post SiOₓ deposition lifetimes of > 800 μs were demonstrated for samples prepared in both Gen 1 and Gen 2.1 DCSF PECVD systems as illustrated in Figure 4-17. This corresponds to a minority carrier diffusion length of ~ 1mm.
Figure 4-17: Effective minority carrier lifetime of device precursors with a-Si:H layers deposited in Gen 1 and Gen 2.1 DCSF-PECVD systems as a function of fabrication process step.

Thus we find that for an $n$-type 20 $\Omega$-cm (100) FZ base, minority carrier lifetimes of > 1ms can be obtained utilizing an asymmetric $n$-a-Si:H / $i$-a-Si:H passivation deposited using the both the Gen 1 and Gen 2.1 implementations of the unique DCSF PEVCD system. This passivation was stabilized and largely maintained through the process of ITO and SiO$_x$ depositions. The resulting pre-metallization device precursors demonstrated minority carrier diffusion length sufficient for complete carrier collection in the context of a 200 $\mu$m thick base[22].
Chapter 5
Laser Fired Emitter Processing and Analysis

5.1 Introduction
In this research we demonstrate the formation of a laser diffused, localized aluminum emitter using a dielectric stack (a-Si:H/SiO\(_x\)), for the first time. Aluminum has been fired through a range of single and dual layer passivation stacks in the context of the LFC, and has been fired through thermal SiO\(_2\), as reviewed in section 1.2. Recently, Munoz has reported an LFE device utilizing an a-Si:H passivation layers but without the use of an electrically insulating layer [49]. Despite the body of work that exists regarding both the LFC and LFE, optimized firing parameters have not been reported.

The following sections will introduce the fundamentals of lasers as they apply to laser materials processing and describe the optical setup used in the experiments. This is followed by a discussion of the LFE parameter space, LFE formation and performance trends found through initial laser parameter scans using small area test devices.

5.2 Laser Material Processing Theory
The acronym LASER stands for “Light Amplification by Stimulated Emission of Radiation”. The precondition for light emission from an atomic or molecular material is that the material exist in an excited state. Emission of photons from an excited state may occur by spontaneous or stimulated emission. The unique requirement for lasing is the existence of a population inversion, such that there is a greater population in an excited state then in the ground state. Under these condition an emitted photon has a higher probability of stimulating the emission of a second photon than of being reabsorbed in the medium. This is accomplished with a multi-level system, that possess a lifetime of the high excited state, and a low lifetime of the lower energy state of the transition.
In the case of stimulated emission, a photon interacts with an atom initially in an excited state resulting in the emission of photon. The resultant photon has the same frequency, phase and polarization as the stimulating photon. The amplification of stimulated emission is accomplished by creating a resonant cavity surrounding the active lasing medium using mirrors. Thus photons traveling parallel to the axis of the laser cavity are amplified through multiple passes. The cavity is chosen as a multiple of the wavelength transition wavelength, so as to produce a standing wave in the cavity.

An inherent property, due to the requirement of an optical resonator for amplification, is the existence of multiple resonance modes. In materials processing applications the transverse electromagnetic (TEM) modes are of interest as they define the energy distribution in the beam. The TEM\textsubscript{00} mode poses a radial Gaussian energy distribution, described by Eq. (5.1) and poses the smallest associated beam diameter.

\[
I_L(r) = I_{L,\text{max}} \exp\left(\frac{-2r^2}{w^2}\right) \tag{5.1}
\]

Here \(I_{\text{max}}\) is the maximum intensity of the distribution, \(w\) is the radius at which the intensity is 86% of its maximum value and \(r\) is the radius of interest. The TEM\textsubscript{00} mode can be focused to the minimum spot size, resulting in the highest power and energy density at the material surface. As the TEM\textsubscript{00} mode has the smallest diameter within the laser cavity, it can be selected by the exclusion of higher order TEM modes with the placement of an appropriate diameter aperture in the cavity.

The instantaneous power of a laser can be increased significantly by periodically switching the quality factor of the cavity, referred to as Q-switching. Pulses of relatively short duration and high power are created by reducing the quality factor of the cavity, thus preventing oscillations and allowing the accumulation of a highly inverted population. By introducing a switchable, high loss element in the cavity, the lasing medium can be pumped to an inversion population well beyond the lasing threshold, assuming that the carrier lifetime is sufficiently long. When the lossy element is switched from a high loss to a low loss state, the cavity returns to oscillation, and the highly inverted population results in a rapid discharge of the cavity.
It is found that increasing population inversion results in reduced cavity discharge time. Thus at a set frequency, an increased laser pump current will result in increased pulse energy and a reduced pulse duration, and thus a higher peak power output. Logically, an increase in pulse repetition rate at a given laser pump current results in a reduced population inversion and thus a reduction in pulse energy and an increase in pulse duration.

The unique materials processing capabilities of laser radiation stem from the properties of a laser beam. Laser beams exhibit, among other traits, low divergence, and monochromatic composition, resulting in diffraction limited minimum focused spot size. For distances from the beam waist of greater than the Rayleigh range the beam radius varies linearly with distance from the beam waist as described by Eq. (5.3):

\[
w(x) = \frac{\lambda x}{\pi w_w}
\]  \hspace{1cm} (5.2)

Here \( w(x) \) is the beam radius at position \( x \) along the beam path, and \( w_w \) is the radius of the beam waist and \( \lambda \) is the wavelength. This is known as the far-field region. The divergence angle of the beam is calculated with Eq. (5.4):

\[
\theta_d = \frac{\lambda}{\pi w_w}
\]  \hspace{1cm} (5.3)

The divergence angle (\( \theta \)) is lowest for the TEM\(_{00} \) mode. The minimum spot size assuming a diffraction limited lens, for a given wavelength for a TEM\(_{00} \) mode is predicted by Eq. (5.5):

\[
d_0 = (M^2) \frac{4\lambda f}{\pi w}
\]  \hspace{1cm} (5.4)

Here \( M^2 \) is the beam quality factor, \( f \) is the focal length of the lens and \( w \) is the beam diameter at the lens. The focus spot size, \( d_0 \) is defined as the width of the Gaussian beam at \( 1/e^2 \) of the peak intensity.
5.3 Experimental Setup

A commercially available micromachining laser system manufactured by Optek Systems was used for the fabrication of the LFE devices. The laser and beam delivery are described in the following sections.

5.3.1 Laser Specifications

The Spectra Physics BL6S 106Q, diode pumped, Q-switched, Nd:YVO₄ laser, emitting at 1064 nm was used, with a frequency doubling option. The BL6S 106Q laser is an end pumped resonator, providing a Gaussian TEM₀₀ mode output. The laser resonator is pumped by a 40 W diode bar, fiber coupled to the resonator. The lasing medium of Nd:YVO₄ is comprised of a neodymium doped yttrium orthovanadate crystal, in which triply ionized neodymium ions, Nd³⁺, replaces yttrium atoms. The quality factor of the resonator is modified with an acousto-optic modulator (AOM), supporting pulse repetition rates from 5 kHz – 200 kHz. The technical specification of the laser are summarized in Table 5-1.

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</table>
5.3.2 Beam delivery

The output of the 1064 nm laser head was delivered to the working surface by one of two optional paths depending on wavelength selection. The beam leaving the laser head optionally passed through the frequency doubler, then a mechanical shutter. The beam was directed onto a vertical optical breadboard from which it was directed to the working surface by way of an optically selective mirror, allowing for real time monitoring via a camera. The final objective was mounted on a vertically oriented linear stage with a 0.5 μm resolution, providing focusing functionality. A 50 mm achromatic doublet was used as the final objective. The chromatic aberration of 1064 nm light resulted in the IR focal point residing +0.5 mm with respect to the visible focal point. The system set up is illustrated in Figure 5-1.

![Figure 5-1: Laser micromachining set up.](image)

An x-y stage was used to scan the beam across the material surface. The stage provides 1 μm minimum step size in both axis, and a maximum travel speed of 220 mm/s. The minimum repetition rate of the laser of 5 kHz, and required minimum pitch of 100um, would require a minimum material feed rate of 500 mm/s. As such the use of an x-y stage necessitates the gating of the laser on and off at each firing position. This gating increases processing time and increases pulse to pulse energy variation. A more appropriate implementation would be the utilization of a galvanometric mirror system. In this implementation the limitation on scan speed would be removed, allowing a full 100 x 100 mm wafer to be processed in less than 3 seconds.
assuming a contact pitch of greater than 125 μm and a laser repetition rate of 200 kHz or greater. Thus, with an appropriate choice of laser and beam delivery, the formation of the cell emitter could occur in-line, in an industrially accepted processing time of 2-3 seconds.

5.3.3 Laser Characterization

The pulse energy to diode pump current and pulse to pulse repeatability with the required laser gating procedure were measured using a Coherent Energy Max J-25MT 10 kHz, pyroelectric sensor. The measurement bandwidth of the sensor is 10 kHz, limiting the characterization of the laser to single pulses for frequencies beyond 10 kHz. Thus, the pulse energy as a function of frequency was inferred from manufacturer’s data.

The relationship of pulse energy to laser pump current was found to be essentially linear within the laser pump current range of 25-28 A as illustrated in Figure 5-2, with pulse energy varying from 0.106 mJ to 0.142 mJ delivered to the sample. The pulse energy repeatability was found to have a standard deviation of <3 μJ for all measured laser diode pump currents.

![Figure 5-2](image)

**Figure 5-2:** Mean Pulse Energy as a function of laser pump current at a repetition rate of 35 kHz.

The pulse energy to operating frequency relationship is illustrated in Figure 5-3. At a laser pump current of 28 A, the pulse duration varies essentially linearly in the range 10 kHz to 90 kHz from
6 to 14 ns. There is good agreement for the pulse energy at 35 kHz, and 28 A presented in Figure 5-2.

Figure 5-3: Average pulse energy and average pulse power of the BL6S-106HQ at laser pump current of 28 A [68]

5.4 Laser Fired Emitter Formation

5.4.1 Laser Material Interactions

Laser processing in the ns pulse range is largely a thermal processing technique. A portion of the incident laser light is reflected as dictated by the Eq. (2.7) for a flat surface. Reflection is particularly high for metallic surfaces in the IR, but is dependent on properties of the surface as well as the optical properties of the metallic thin film. Light that is not reflected is transmitted or absorbed through a range of material dependent excitations. In the case of metals, absorption is dominated by free electron absorption, leading to high absorption coefficients of 120 µm⁻¹ for Al at 1064 nm[69], and corresponding absorption depths of 10 nm as governed by Eq. (2.6). In the context of single pulse craters where the irradiation is absorbed in the 2µm Al layer, the process should be wavelength independent as the absorption depth in the Al is much thinner than the Al layer. In contrast, absorption in silicon is strongly wavelength dependent. For a wavelength of
1064 nm absorption of photons is comprised of a combination of inter band and intra band excitations such that the absorption depth in Si is dependent on dopant and defect density of the material which is on the order of 1 mm. In both metal and semiconductor, the thermal relaxation time of the exited carriers is on the order of $10^{-12}$s, thus the laser-induced material processing occurs through thermal mechanisms [39]. The 10 ns pulse duration and power densities of $10^9$-$10^{10}$ W/cm$^2$ place our processing in the laser machining/drilling parameter space of laser material processing as shown in Figure 5-4.

![Figure 5-4: Power density and interaction time for various laser processes [70]](image)

In the case of an Al/SiO$_2$/c-Si stack, the laser light absorbed in the Al, causes the heating, melting and then vaporization of a portion of the Al, and with sufficient incident laser energy, melting and vaporization of a portion of the Si. The thermal diffusion length in Al and Si, for a 10 ns pulse can be approximated using Eq. (5.6) as 2μm and 3μm, respectively [39, 71].

$$l_t = \sqrt{\frac{4k \tau_p}{\rho c}}, \quad \kappa = \frac{k}{c \rho} \quad (5.5)$$

Here $k$, $c$, $\rho$, $\tau_p$ are the thermal conductivity, specific heat capacity, density, and pulse duration, respectively.
Based on the thermal diffusion length, the heating can be assumed uniform through the thin Al layer, while minimal lateral conduction will occur when compared with the diameter of the heat affected area. Silicon as deep as 3 μm below the aluminum will be heated significantly. With sufficient laser energy, the Al will melt and vaporize. The pressure created by this phase change acts to eject a portion of the Al from the melt zone. At the center of the crater, where the heating is most intense, both the SiO₂ and a portion of the silicon substrate may melt, and be ejected as well. The portion of the Al that is not ejected from the crater will mix in the liquid phase with Si and a portion will diffuse into the unaltered crystalline substrate beneath the melt.

While thermal simulations have not been reported for Al/SiO₂/Si stacks, simulations of heat distribution for 50 ns laser pulses on Si have been reported for 355, 512, and 1064 nm wavelength lasers [72]. Here the 355 nm is more representative of an Al layer on Si, as the absorption of light is confined to the surface layer. Simulated results presented in Figure 5.5 a) represent a laser pulse with an energy density that causes melting but not vaporization. For a 355 nm pulse, represented by the blue line, a melt depth of 0.5 μm and a solidification time of < 0.5 μs are found. For a 1064 nm pulse, represented by the red line, a melt depth of 1 μm and solidification time of > 1 μs is calculated due to the weak absorption of 1064 nm light in the silicon, leading to a deeper heating of the substrate, and thus a reduced cooling rate. This is representative of successive pulses in the case of multi pulse firing parameter. Here the Al has already been largely removed by the initial laser pulse, hence a much deeper thermal distribution and longer cooling time can be expected for subsequent pulses. The thermal distribution of a 1064 nm pulse on bare silicon is illustrated in Figure 5.5 b). The simulation predicts greater melt depth for an equal pulse energy but with an increased pulse length [73].
5.4.2 LFE Structure and Composition

The structure, composition and electrical properties of laser fired contacts have been studied using Secondary Ion Mass Spectrometry (SIMS) [15, 74-76], Transmission Electron Microscopy (TEM) [74], Scanning Electron Microscopy (SEM) [75, 76], Energy-Dispersive X-ray spectroscopy (EDX) [76], Electron Beam Induced Current (EBIC) [39, 76], Lock-in Thermography (LIT) [76] and X-ray Diffraction (XRD) [74]. EBIC images have confirmed that an electrically active junction is formed when the energy density is sufficient to destroy the SiO₂ layer; the junction is localized at the center of the crater. The dielectric ring that remains as a result of the ablation of the majority of Al would isolate the electrically active crater center, but has been shown to be shunted by ablated Si that is deposited on the SiOₓ. Thus, the ejected Si provides a conductive path between the electrically active center of the crater and the aluminum back conductor [74, 76]. This shunting effect from deposited Si is seen to increase with decreasing pulse length.

Where the SiOₓ is opened, a melt forms, allowing the mixing of Al and Si. The depth of the melt is energy and pulse length dependent, but ideally is on the order of 1 μm. This resolidified layer is shown to be comprised of both Al and Si crystallites, ranging from 0.1μm to a nanocrystalline phase [74]. A silicide is not observed due to the miscibility gap in the Al-Si phase diagram.
Instead a highly disordered region is formed by the rapid quenching of the melt. A diffusion of Al is found deeper into the Si substrate, in the undisturbed crystalline bulk [74, 75] to depths of 3 μm (using SIMS) at concentrations of $10^{-18}$ atoms/cm$^3$. Using EBIC Al concentrations of $10^{-14}$ atoms/cm$^3$ are found at depths of 7 μm for laser pulse lengths in the >100 ns. The depth of diffusion is found to increase with increased pulse energy as well as pulse length, but is accompanied by intensive mixing in the melt region in the case of increased pulse energy[75]. The diffusion of Al into Si is found to occur as a plume, with asymmetries caused by non-homogeneous laser-induced diffusion of Al into c-Si as illustrated in Figure 5-6. The diffusion of Al under the influence of Q-switched lasers is found to be a non-equilibrium phenomena where the diffusion coefficient is indicative of pipe dislocation diffusion rather than volume diffusion [15].

![Figure 5-6: ToF-SIMS depth profile of aluminum distribution for 700ns long 2.5 mJ pulse at 1) 0.325 μm below crater bottom, 2) crater bottom, 3) 0.325 μm above crater bottom, 4) 1μm above crater bottom [76]](image)

5.4.3 Crater Formation Parameter Space

The laser processing parameters available for direct control are laser pump current, pulse repetition rate, beam diameter, beam energy distribution, focal length of lens and focus state of lens as illustrated in Figure 5-7. In our experimental set up the available parameters are pump
current, pulse repetition rate and position of focus. The effects of beam diameter ($D_0$), objective focal length ($f$) and focus state, jointly determine diameter of the laser spot at the work surface.

Increasing laser pump current has the effect of increasing the pulse energy and decreasing the pulse duration, thus a dual influence on pulse power. An increase in pulse repetition rate will result in an increase in pulse length and decrease in pulse energy, again presenting a dual influence on pulse power. An increase in pulse duration has been shown to increase melt depth, as has increased pulse energy. Together the pulse duration, pulse energy and focus diameter determine the energy and power density delivered to the substrate and thus the depth and diameter of the crater.

![Diagram showing interdependencies of LFE laser parameters](image.png)

**Figure 5-7:** Interdependencies of LFE laser parameters

It should be noted that the Gaussian distribution of a TEM$_{00}$ mode results in an energy density significantly beyond the melt threshold at the center of the spot. Thus there is more intensive melting at the center of the crater which can be expected to result in deeper Al diffusion as well as more laser-induced damage in the substrate. The ideal beam profile would be a “flat top” or
“top hat” intensity profile. Such a beam profile delivers a uniform intensity across the entire diameter of the irradiated spot, and thus the threshold energy could be delivered to the entire surface of the spot. In this way damage associated with the excessive energy at the center of the crater would be avoided. The application of a “top hat” beam profile has not yet been reported in the context of the LFC or LFE but presents an interesting opportunity for future investigation.

5.5 Crater Formation and Morphology

The effect of laser parameters on crater morphology is presented here. Illustrated in Figure 5-8 are the typical structural features of an LFE crater.

![Figure 5-8: Optical image of LFE crater at 500x magnification a) aluminum surface b) bottom of crater](image)

The crater rim indicates the diameter within the Gaussian beam at which the incident irradiation is insufficient to melt the Al, which has been reported by Grohe as 7.5 J/cm² [73]. Moving toward the center of the crater, there is an exposed SiOₓ region, from which the Al has largely been ablated, evidence of which is seen in the debris surrounding the crater. This region is identified as the visible blue ring at the perimeter of the crater, corresponding to the expected thin-film interference of the SiOₓ on Si of 105 nm. The width of this ring depends on pulse energy and tends to be maximized at pulse energies that are at the threshold of crater formation. Within the exposed SiOₓ ring, at the crater center, the Al-Si alloyed region is found. Here the c-
Si substrate is exposed, and has experienced a melt cycle, in which Al has been introduced. The uneven crater bottom indicates both melt and some ablation of silicon.

At 35 kHz the effect of energy density on crater morphology was explored by conducting a defocus scan in increments of 100 μm, for pulse energies of 0.142 mJ, 0.130 mJ, 0.118 mJ, and 0.106 mJ. Figure 5-9 shows the variation of crater diameter as a function of defocus for a single 0.142 mJ pulse. Here a negative de-focus value indicates moving from the focal point towards the objective, and a positive de-focus value indicates moving the focal point away from the objective. At the IR focus, a circular crater with an inner diameter of 22 μm diameter and 6μm depth is created, with significant material ejected from the crater. The crater diameter corresponds well with diffraction limited spot size of 19.7 μm for our experimental setup.

![Crater width as a function of defocus height](image)

**Figure 5-9:** Crater width as a function of defocus height

With increasing defocus crater diameter grows, but not equally in all directions. When the material is moved closer to the final objective (negative defocus), the crater elongates horizontally and eventually develops two distinct regions of intensity, suggesting an imperfect TEM₀₀. A defocus of +/- 600μm is shown to decrease the energy density sufficiently that the aluminum is not ablated sufficiently to expose the SiOₓ layer.

Treating the crater as an ellipse, we see uniform change in area for positive and negative defocus distance. Crater area as a function of defocus for a 0.142 mJ pulse is presented in Figure 5-10 as
well as the average energy density for a 0.142 mJ pulse as a function of inner crater diameter. From this it can be concluded that an average energy density of 3 J/cm² is required for the penetration of the SiOₓ layer. A scan of pulse energies over this defocus range demonstrates the dominance of defocus in determining energy density, with differences in pulse energy only visible in the reduced penetration of the SiOₓ layer at +/-500 μm defocus for lower pulse energies.

**Figure 5-10**: Variation of inner crater area, total crater area and calculated energy density as a function of defocus distance.

The deviation of the outer crater diameter trend from that of the inner crater at 0.0 mm defocus and 0.5 mm defocus can be explained by an energy density argument. At ±0.5 mm defocus the energy density is marginal and thus minimal material is ejected from the crater. Thus, the inner and total crater diameter vary little. The opposite is true at 0.0 mm where the high energy density causes significant ablation, and thus the total crater area including the rim grows.

It can be assumed that the energy beyond the threshold for penetration resulted in a greater melt depth and increased ablation of the c-Si substrate. This trend is shown clearly in Figure 5-11, with crater depth decreasing with energy density reduction, which is associated with increased
defocus. Here the crater diameter appears to be relatively static, but this is a product of the elliptical shape of the craters with defocus, where the craters have been intersected on their short axis.

Figure 5-11: SEM images of single pulse craters fired at varying defocus heights of; a) focused b) -0.1 mm defocus c) -0.5 mm defocus

As the laser machining system used for the experiments did not provide absolute z-position, it was required that the IR focus set-point be set prior to each use. This was accomplished by firing a defocus scan from 1.5 mm above the visible focus to the visible focus in increments of 0.1 mm. This procedure was limited by the operator’s ability to accurately determine the visible focus, for which a repeatability error of approximately ± 25μm was found.

The effect on crater morphology of multiple pulses was investigated by setting a defocus of -0.5 mm, and firing a series of samples at increasing pulse counts. As is illustrated in Figure 5-12 while a single pulse is insufficient to ablate the Al layer, a series of pulses initially penetrated the SiOₓ layer, and with increased pulses, a deep central crater is produced.
5.6 Exploratory Devices

The sensitivity to laser parameters for the formation of an acceptable laser fired emitter is far greater than that of laser fired contacts. The LFC acts as a majority carrier contact, as well as a back surface field. Thus the minority carrier density is low in the vicinity of the LFC, and as a result recombination is also low, even in the presence of a significant density of recombination centers. The LFE in contrast, is a minority carrier contact, and thus laser induced defects in the vicinity of the LFE become active recombination centers. The sensitivity of the LFE to laser processing parameters is highlighted by Glunz. Two sets of laser parameters show a difference in $V_{OC}$ values of 10 mV for the LFC process and more than 300 mV for the LFE process[18].

To explore the laser parameter space, small illuminated devices were created without front metallization. These test devices had an active emitter area of 2x2 mm², fired at a pitch of 150 μm. The TCO was used as the front contact, adding significant series resistance and thus detrimentally affecting device performance. Despite the small area and high series resistance, these test samples served the purpose of exploring the laser parameter space.

Three initial scans were competed to investigate the effect of:

1. Pulse repetition frequency and pulse number at the highest and lowest laser pump current.
2. Multiple pulses for pulse energy densities at the threshold of crater formation.
3. The influence of energy density through variation of the focus relative to the sample.
5.6.1 Pulse and Frequency Scan

A rough scan of pulse count and pulse repetition frequency was completed for pulse counts of 1, 3 and 5 pulses at pulse repetition frequencies of 10, 50 and 90 kHz. This scan was conducted at laser pump currents of 28 A and 25 A. Maximum efficiency was observed for a single pulse for all pulse repetition rates at a laser pump current of 28 A. All device performance parameters are shown to degrade with increasing pulse count for this maximal pulse energy case. An efficiency minimum is observed for the 50 kHz samples largely due to the low $J_{SC}$ observed for these samples. This is a surprising result as single pulse energy measurements made at 28 A and varying pulse repetition rate settings show no variation in pulse energy.

In contrast, the performance peaks for 3 pulses in the 25 A case. The higher power single pulse craters outperform the multi pulse craters formed with lower pulse energy as shown in Figure 5-13. For the scans completed at a laser pump current of 25 A, a degradation of $V_{OC}$ with pulses is observed, but a maximum in current is observed for 3 pulses for all pulse repetition rates scanned. The increase in $J_{SC}$ is sufficient to offset the reduction in $V_{OC}$, resulting in an efficiency maximum for all pulse repetition rates as observed for 3 pulses.

As no pulse energy variation is seen with pulse repetition rate setting in the case of a single pulse, and minimal variation in cell performance is seen with pulse repetition rate for multi-pulse craters for the highest performing samples, further experiments are conducted with a pulse repetition rate of 35 kHz for which the laser is optimized. A more thorough evaluation of the effect of pulse repetition rate and pulse duration is justified in the context of a laser with a pulse length variation capability of greater than $\sim$10 ns, but is beyond the scope of this exploratory work.
5.6.2 Pulse Scan

The increase in performance associated with multiple pulses for low laser pump currents indicates that for marginal energy densities, multiple pulses may lead to increases in device performance. To explore this possibility a pulse scan was conducted at defocus corresponding to a marginal energy density and a pulse repetition rate of 35 kHz.

A defocus of -0.5 mm was selected, and a scan of 1 to 5 pulses was conducted for laser pump currents of 28, 27, 26 and 25 A. The very low \( J_{SC} \) values for 26 A and 25 A for 1 pulse presented in Figure 5-14 show that these pulse energies are insufficient to form an emitter. This is visible with only a fraction of the craters penetrating the dielectric layer. The low \( J_{SC} \) is mirrored in the spread of the \( V_{OC} \) and \( FF \) values, clearly demonstrating an increase in \( V_{OC} \) with increasing power again indicating that the diffusion of Al at the lower laser pump currents is insufficient to establish an acceptor concentration that would create a significant built-in field as described by EQ.(2.2).
A second pulse establishes a higher $V_{OC}$ for all pump currents less than 28 A, suggesting that the acceptor concentration is increased sufficiently by the in diffusion of Al with a second pulse to establish an acceptable built-in field. However, the $V_{OC}$ for the 28 A sample degrades with a second pulse. This degradation of $V_{OC}$ is seen for all laser pump currents for pulse counts $> 2$, suggesting that the increased laser damage, or ablation of Al rich Si is detrimental to the built-in voltage. The short circuit current peaks for all samples at 2 pulses, indicating that carrier collection is maximized for 2 pulses. The peak in current is expected to accompany the increase in $V_{OC}$ as a functional emitter is formed with the second pulse and an increase in carrier separation and collection is expected. All cell performance parameters degrade for pulse counts beyond 2 pulses for all tested laser pulse currents. The continued ablation of the crater bottom negatively affects the performance, likely due to a combination of increased laser-induced damage and ejection of Al-rich Si.
Thus, it is demonstrated that at threshold energy densities an increase in device performance is attained with multiple pulse which are required for the formation of a viable emitter. Pulse counts beyond this optimal, here found to be two pulses for the energy densities investigated, degrade device performance. It should be noted that the best results are obtained with the highest energy density investigated, suggesting that performance may increase with increased energy density and minimized pulse count.

5.6.3 Focus Scan

The results of section 5.6.1 and 5.6.2 demonstrate that, within our limited parameter scan, performance is maximized with the formation of LFE’s with a single pulse for pulse energy densities above threshold values. Investigating this LFE parameter set further, a scan of defocus from 0.5mm to -0.5mm was conducted for 1 pulse with a pulse energy of 0.142 mJ. This leads to a power density variation from 3J/cm² to 9 J/cm² as illustrated in Figure 5-9. Intensive mixing has been reported for energy densities > 9 J/cm² [75]. The resulting device performance parameter trends show rough symmetry about the 0.0 mm focus as would be expected for a single pulse crater where optical absorption occurs in the Al layer. For multi-pulse craters positive and negative defocuses might not be equivalent, as for the negative defocus the focal point would be within the material. A local minimum in performance is seen at a focus state of 0.0 mm. Clearly the excessive energy density fails to form an ideal emitter. Crater depth for the focused state was measured with SEM to be > 6 μm.
A trend of increased performance with decreased energy density is seen, resulting in a local maximum at a defocus of ±0.2mm, corresponding to an average energy density of 6 J/cm², followed by a decrease in performance with decreasing energy density. This can be understood as an optimum in power density above which ablation and damage to the base, as well as potentially a poor connection between emitter and rear metallization could lead to a reduction in performance. Below this optimum, insufficient diffusion of Al occurs to form an acceptable emitter. With the variation in energy density and the associated variation in crater area, $V_{oc}$ dominates the performance. It is interesting to note that better performance is obtained for negative defocus values, which have been shown to be more elliptical and to have less radial energy uniformity than in the positive defocus. This suggests that the more even distribution of laser energy may lead to improved performance but can only be properly studied in the context of beam profile modification.
Chapter 6
Device Results and Analysis

In the preceding section we explored the correlation between laser parameters and the electrical characteristics of small, un-metalized test device samples. This initial characterization of the laser parameter space now provides a basis with which to investigate the implication of laser pulse energy density and LFE pitch on the performance of 1x1 cm² photovoltaic solar cells. In this chapter we study the influence of both annealing and laser firing parameters on device performance. Reproducibility of devices is explored in the context of one set of laser firing parameters on a single device precursor; also the reproducibility of a given firing parameter set is examined. Finally, device performance variation as a function of our evolving device precursor is explored using an optimized firing parameter set as well as the device efficiency that might be realized with minimal modifications of our current process.

6.1 Effect of Thermal Annealing on Device Performance

The importance of annealing in obtaining an optimal LFE has been reported in the context of an LFE structure passivated with thermal SiO₂. The thermal stability of SiO₂ permits high temperature annealing steps, resulting in a 100% efficiency increase for an annealing temperature of 425 °C \[22\]. In the context of a thermal SiO₂ passivation, for which an anneal temperature of 425 °C does not increase minority carrier lifetime, the improvement in efficiency is attributed to the annealing of defects in the laser damage region. As shown in section 3.5, the thickness of the laser damaged region has the largest effect on performance of all considered cell parameters. The elimination of laser-induced electrically active point defects by thermal annealing has been reported by Benton \[77\]. The concentration of point defects at energies of 0.19 eV and 0.33 eV associated with laser-induced melting of a bulk Si surface, are found to be reduced with annealing temperatures of 350 °C and 650 °C respectively\[78\].
In the context of our hydrogenated amorphous silicon passivated structure, a maximal annealing temperature is expected due to the thermal instability of a–Si:H/c-Si passivation at higher temperatures. The thermal stability of a-Si:H/SiOₓ has been investigated in the context of LFC devices, showing a steady reduction of passivation quality with annealing time at 400 °C in forming gas. A minimum minority carrier lifetime of >600 μs lifetime was obtained for a 30 minute anneal, which is not sufficient to degrade cell performance [51]. Cell performance, however, was seen to degrade significantly for an annealing temperature of 450 °C, bringing into question if annealing improvements at 425 °C anneal could be realized with an a-Si:H/SiOₓ stack.

An initial annealing temperature scan was conducted in air. For each temperature scanned an unmetalized sample was annealed simultaneously, to annealing effect on carrier lifetime. The annealing temperature scan consisted of 40 minute anneals at increments of 50 °C for hotplate set points of 150 °C to 400 °C, based on previously demonstrated passivation increase with annealing [64]. The maximum performance enhancement for air annealed samples occurred at an annealing temperature of 185 °C. The $V_{OC}$, and $J_{SC}$ continued to increase with increasing annealing temperature, until both reached a maximum at a temperature of 275 °C suggesting an improvement in both junction and passivation quality. The fill factor increased only marginally before beginning to fall after 235°C. The degradation in fill factor proved to be the dominant parameter, resulting in a reduction in cell efficiency for temperatures greater than 235 °C. The accompanying lifetime samples showed a marginal increase in lifetime up to 235 °C and loss of passivation beyond this point which culminated in a 50% reduction in minority carrier lifetime. This result indicates that the loss of efficiency occurred prior to the loss of passivation. This was attributed to thermal oxidation of rear aluminum contact resulting in increased series resistance and thus a reduction in fill factor.

The above experiment was repeated in a nitrogen environment to prevent oxidation in the device structures. The annealing time was reduced to 10 minutes, again to reduce the influence of oxidation in the event that oxygen was present in the annealing enclosure. As illustrated in Figure 6-1 efficiency peaks, in this case, at 235°C, and enhancement in $J_{SC}$ proves to be the dominant factor in the attainment of maximum increase in cell performance. The peak in $J_{SC}$ and cell efficiency correlates with the loss of passivation for temperatures > 235 °C. Both the $V_{OC}$ and fill factor continue to increase to a temperature of 274 °C. A reduction in $FF$ beyond 274 °C
results from the increase in $R_s$. The continued increase in $V_{OC}$ beyond 235 °C suggests that the quality of the junction continues to improve, while the passivation of the cell interfaces begins to degrade. The results were fit with both a one and two diode model. The two diode model reported the anticipated trends of a minimum of the bulk recombination diode $I_{01}$, at 235 °C and monotonic reduction in reverse saturation current of the space charge recombination diode, $I_{02}$, with increasing annealing temperature. The values of $I_{01}$ were unrealistically low however, which is partly a function of the reduced emitter area, but highlights the inappropriate use of fixed ideality factors to model high ideality factor devices. These values are presented in Appendix A, for the interested reader. When fitted with a one diode model ideality factors of $>2$ are found for all cells, indicative of high defect induced recombination. The fitting results presented in Table 6-1 demonstrate a minimum for both reverse saturation current and ideality factor for an annealing temperature of 235 °C. This supports the hypothesis that the thermal stability of the amorphous passivation ultimately limits the annealing temperature, and thus the performance gains associated with annealing of a-Si:H/SiO$_x$ stacks.

**Figure 6-1:** Device performance parameters and relative lifetime of passivation sample as a function of annealing temperature
The effect of annealing time was investigated to determine the optimal annealing duration. A temperature of 210 °C was selected to accentuate time dependency of annealing reactions. The annealing sample was annealed for 6 consecutive 10 minute increments. A relative performance increase of 8% is found in the first 10 minute anneal, with a marginal continued performance increase culminating in maximal relative increase of 9% at 40 minutes and a 1.5% relative decrease in the following 20 minutes. From these results the annealing protocol for all subsequent annealing was set as 40 minutes in a N₂ atmosphere at a hotplate setting of 250 °C, and a surface temperature of 235 °C.

Table 6-1: Variation of one diode fitting parameters with annealing temperature

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<th>22 °C</th>
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<th>185 °C</th>
<th>235 °C</th>
<th>275 °C</th>
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<td>26</td>
<td>26</td>
<td>27</td>
<td>25</td>
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<td>18</td>
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<td>1.16</td>
<td>1.68</td>
<td>3.7</td>
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</tbody>
</table>

The passivation of our unoptimized a-Si:H/SiOₓ stacks was shown to begin to degrade for an annealing temperature < 275°C in air. Annealing performance improvements might be realized in the context of a hydrogenated amorphous silicon passivated device through the use of an a-Si:H/SiNx stack. Thermal stability of a-Si:H/SiNx passivation layers has been demonstrated for temperatures in excess of 700 °C [24]. Additionally, one may also consider the use of low temperature hydrogen plasma annealing. Hydrogen plasma anneals at 100 °C-300 °C have been shown to remove all electrically active point defects associated with Q-switched laser melted silicon [77], and thus offer a potential means of reducing defect density within the stable temperature range of our a-Si:H/SiOₓ stack. The reported hydrogen plasma anneal was completed on intrinsic c-Si, and thus the effect of hydrogen plasma anneal in the context laser damaged Si with Al impurities warrants investigation.
6.2 Device Results as a Function of Laser Parameters

Using the basis provided by the exploratory laser parameter scans presented in chapter 5, further refinement of firing parameters was completed in the context of full cell structures. Given the observation of superior performance of single pulse LFE, further efforts were focused on single pulse LFE, with an emphasis placed on energy density. Presented in the following subsections are parameter scans of defocus and defocus combined with pulse energy variation, followed by a scan of LFE pitch to determine the optimal density of optimized LFEs.

6.2.1 Focus Scan

Given the demonstrated dominant influence of energy density as varied by defocus in the context of single pulse LFE, a scan of defocus was repeated in the context of full-sized 1x1 cm² cells with the added variable of annealing. A maximal pulse energy of 0.142 mJ was selected and focus set points of ± 0.4, ± 0.2 and 0.0 mm investigated with the results presented in Figure 6-2.

A performance minimum is confirmed at the focused state, with local maximum in performance found again at ±0.2 mm defocus. A negative defocus was seen to outperform a positive defocus again, with the performance enhanced by a 40min 250 °C anneal in N₂ as the -0.2 mm defocused device experienced an 8% increase in $J_{SC}$. The sample fired with a positive defocus demonstrated minimal performance increases with annealing. In the case of the +0.4 mm sample, no performance increase was observed due to a high pre-anneal $FF$ and low post anneal $FF$. This was a surprising result that may be attributed to measurement error.
6.2.2 High Resolution Energy Density Scan

In light of the influence of energy density, a scan of both defocus and pulse energy was conducted to determine the optimal energy density. Since both variables influence power density a simultaneous variation of both parameters results in a finer resolution scan of energy density while minimizing LFE diameter variation. De-focus set points of 0, -0.1, -0.2 mm were scanned at pulse energies of 0.142 mJ, 0.130 mJ, 0.118 mJ and 0.106 mJ resulting in a range of energy density of 5 to 10 J/cm$^2$. Clear trends can be inferred from the results presented in Figure 6-3 despite the existing scatter. A maximum in annealed cell efficiency is observed for an energy density of 7.4 J/cm$^2$, demonstrating an efficiency of 11.1%. This peak in efficiency is dominated by enhancement in the cell’s short circuit current, which shows a broad maximum between energy densities of 7 to 8 J/cm$^2$. The annealed fill factor is seen to be stable across the full range of energy densities, but displays a reduction with increasing energy density for the unannealed samples. The open circuit voltage of the cell is seen to degrade monotonically with increased energy density. This is in agreement with the results presented in the previous section for the 0 to -0.2 mm defocus range.

Figure 6-2: Device performance as a function of defocus and annealing
Figure 6-3: Device performance parameters as a function of pulse energy density and annealing for a single pulse LFE.

The variation of cell performance as a function of defocus set-point shows a maximum in performance at a defocus of -0.1 mm as illustrated in Figure 6-4. A steady increase in performance with increased defocus at the highest pulse energy is observed as well.

Figure 6-4: Cell efficiency with varying pulse energies as a function of defocus set-point
6.2.3 Pitch Scan

The pitch or spacing of LFEs is a device level parameter which is assumed to be independent of the properties of the LFE; tacit in this investigation is the assumption that the optimized LFE provides a sufficiently large built in field. An increased pitch is expected to result in an increase in carrier lifetime and a reduction in the reverse saturation current as discussed in section 3.5. These performance improving factors compete with the effects of an increased collection volume for each LFE. As pitch increases, the collection volume of each LFE increases until the minority carrier diffusion length is insufficient for complete carrier collection, beyond which point dead areas of the cell begin to emerge.

Figure 6-5: Device performance parameters as a function pitch and annealing for a single 0.13 mJ pulse.
Using optimized firing parameters of 27 A and -0.1 mm defocus, devices were fired with pitches from 100-200 units in 25 \( \mu \)m increments as well as 250 \( \mu \)m and 300 \( \mu \)m. A monotonic increase of \( V_{OC} \) shown in Figure 6-5 for increasing pitch. This increase in \( V_{OC} \) is owing to a monotonic decrease of \( I_0 \) confirmed by the fitting data presented in Table 6-2. The reverse saturation current is found to be linear with the decreases in total emitter area, as a function of pitch. The \( J_{SC} \) is seen to peak at 125 \( \mu \)m pitch. For lower pitch, increased defect density leads to carrier recombination and reduced current collection. LFE pitches greater than 125 \( \mu \)m result in reduced carrier collection due to insufficient minority carrier diffusion length. Thus, \( J_{SC} \) is found to dominate cell performance and the highest efficiency is found at 125 \( \mu \)m for both unannealed and annealed samples. These results demonstrate the performance trends predicted by the simulation, but at a different optimal pitch value. This variation in optimal pitch value can be attributed to the non-idealities of the proof of concept device.

**Table 6-2:** IV fitting results of devices with varying LFE pitch

<table>
<thead>
<tr>
<th>Pitch (( \mu )m)</th>
<th>100</th>
<th>125</th>
<th>150</th>
<th>175</th>
<th>200</th>
<th>250</th>
<th>300</th>
</tr>
</thead>
<tbody>
<tr>
<td>( J_{ph} ) (mA-cm(^{-2}))</td>
<td>27</td>
<td>27</td>
<td>26</td>
<td>25</td>
<td>25</td>
<td>24</td>
<td>22</td>
</tr>
<tr>
<td>( I_0 ) (10(^{-6}) A)</td>
<td>7.99</td>
<td>3.16</td>
<td>3.31</td>
<td>1.96</td>
<td>1.67</td>
<td>0.96</td>
<td>0.82</td>
</tr>
<tr>
<td>( n )</td>
<td>2.6</td>
<td>2.5</td>
<td>2.5</td>
<td>2.4</td>
<td>2.4</td>
<td>2.3</td>
<td>2.3</td>
</tr>
<tr>
<td>( G_{sh} ) (10(^3) S)</td>
<td>0.98</td>
<td>1.1</td>
<td>1.1E</td>
<td>1.2</td>
<td>1.2</td>
<td>1.4</td>
<td>1.4</td>
</tr>
<tr>
<td>( R_s ) (( \Omega ))</td>
<td>0.63</td>
<td>0.49</td>
<td>0.55</td>
<td>0.58</td>
<td>0.63</td>
<td>0.64</td>
<td>0.66</td>
</tr>
</tbody>
</table>

### 6.2.4 Firing Repeatability

The repeatability of both the cell results for a given set of parameters and the reproducibility of a given set of parameters have been tested. To test repeatability, five samples from the same wafer were fired with the same firing parameters of a single pulse at a laser pump current of 27 A at a pitch of 125 \( \mu \)m and a defocus of -0.1 mm. The resulting pre and post anneal cell performance data are presented in Figure 6-6. While the pre-anneal results show an average of 9.27 % and a standard deviation of 0.12%, the post-anneal results show an average of 10.23% and a standard deviation of only 0.08%. Thus the process is found to have high repeatability for a single set of firing parameters given consistency in the pre-fired device.
The reproducibility of a given setting is found to be somewhat more difficult to ascertain within the context of the current optical setup. Pulse energy is found to be highly reproducible and is monitored prior to each set of experiments. The lack of absolute position for the vertically mounted linear stage results in variation in the z-focus set point. As this is shown to be the dominant variable in pulse energy density, the uncertainly in z-position of ±25 μm within the current z-calibration technique leads to a level of uncertainly in energy density that limits reproducibility. This limited reproducibility is observed in the results of the repeatability samples fired at 27 A and -0.1 mm defocus. This parameter set demonstrated 10.7% cell efficiency in the energy density scan data presented in section 6.2.2 while a cell efficiency of 10.3% was attained in the repeatability study. Thus, with the demonstrated sensitivity of the laser firing process to energy density and the reasonable repeatability of the defocus technique, the repeatability is considered to be sufficient for proof of concept research presented in this work. However, for a more detailed exploration of the laser firing parameter space improved reproducibility of the settings is essential. As an example, a more appropriate optical set up would maintain a fixed position of the final objective and vary the energy density at the sample surface using a variable beam expander to modify the diameter of the spot according to Eq. (5.4). The implementation of this configuration was beyond the scope of this work.
6.3 LFE Device Precursor Scan

The evolution of the fabrication process is investigated by applying the optimized firing parameters to each device precursor wafer completed. Throughout the work the fabrication processes changed incrementally. The effect of these improvements are visible in Figure 6-7 as a steady progression of device performance.

![Figure 6-7: Variation in IV curve as a function of device precursors and annealing.](image)

Both hydrogenated amorphous silicon passivation layers for device structures ID-1 and ID-2 were carried out in the Gen1 DCSF PECVD system. Both used 1.5\% phosphine doping, and they achieved post a-Si:H deposition anneal lifetimes of 1300 and 400 μs, respectively. ID-1 varied from the standard process with a 210 nm SiO\textsubscript{x} isolation layer, and photolithographically defined front metallization of 2 μm Ag. ID-2 possessed an 18 μm Ag front metallization, applied in error during e-beam evaporation. This over-deposition caused overheating of the sample and reduced performance due to thermal damage. As such the results are not presented here.

The hydrogenated amorphous silicon passivation for device structures ID-3 and ID-4 were carried out in the Gen 2.1 DCSF PECVD system, with a dopant concentration of 0.75\% phosphine for the \textit{n}-a-Si:H layer. The post deposition anneal was conducted on an SiO\textsubscript{x} coated dummy wafer and samples attained post anneal lifetimes of 1856 μs and 956 μs, respectively. A 1 minute, 5\% HF dip was introduced immediately prior to ITO deposition to remove any native
oxide from the $n$-a-Si:H interface. A cooling step was introduced in the e-beam metallization procedure, following the deposition of each 1 $\mu$m of Al and the deposition of each 1.5 $\mu$m of Ag.

The effect of an increase in front metallization thickness from 1 to 4.5 $\mu$m was conclusively determined to reduce the series resistance by an order of magnitude, and increase fill factor $> 14\%$ relative; this was carried out through the firing of a single set of laser parameters on two ID-4 devices with differing front metallization thicknesses. The effect of front metallization thickness is seen in the fitting results presented in Table 6-3, where $R_s$ is seen to increase with decreasing metal thickness.

The effects of deposition system, doping density, pre-ITO HF dip, and e-beam cooling step cannot be determined conclusively as they were introduced in combination as a result of parallel efforts in our laboratory. The a-Si:H passivation of Gen 2.1 provided similar minority carrier lifetimes to that of Gen 1, hence differences in initial passivation are not expected to play a significant role. The reduction in doping of the front surface field would lead to increased film resistivity, but a reduced defect density in the $n$-a-Si layer. Thus, an improved blue response may contribute to the increased $J_{SC}$ seen in Gen 2.1 deposited devices. The removal of the native oxide prior to ITO deposition is expected to reduce the series resistivity of the front contact stack.

A reduction in passivation degradation through the reduced thermal load associated with thick e-beam depositions is expected to contribute significantly to the difference in $J_{SC}$ between ID-1 and ID-3,4. Passivation degradation post metallization cannot be determined accurately using photo conductance decay methods, and thus the effect was not quantified.

Fitting of the IV data demonstrates that ID-4 has the lowest reverse saturation current and lowest ideality factor. Thus ID-4 exhibits the lowest recombination, and the highest fill factor. The influence of front metallization thickness on series resistance is clearly shown, where ID-3 has $\frac{1}{4}$ the front metal of ID-4 and $\frac{1}{2}$ that of ID-2.
Table 6-3: One diode fitting results for differing device precursors

<table>
<thead>
<tr>
<th></th>
<th>ID-1</th>
<th>ID-3</th>
<th>ID-4</th>
</tr>
</thead>
<tbody>
<tr>
<td>$J_{ph}$ (mA cm$^{-2}$)</td>
<td>20.6</td>
<td>26.7</td>
<td>27.3</td>
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<tr>
<td>$I_0$ (10$^{-6}$ A)</td>
<td>334</td>
<td>22.2</td>
<td>6.73</td>
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<tr>
<td>$n$</td>
<td>3.7</td>
<td>3.1</td>
<td>2.68</td>
</tr>
<tr>
<td>$G_{sh}$ (10$^{-4}$ S)</td>
<td>22.0</td>
<td>9.32</td>
<td>5.66</td>
</tr>
<tr>
<td>$R_s$ (Ω)</td>
<td>0.83</td>
<td>6.09</td>
<td>0.56</td>
</tr>
</tbody>
</table>

6.4 Status of Cell Performance

In this proof of concept work, we have calculated the potential for a $> 20\%$ photovoltaic device conversion efficiency through modeling using Sentaurus, and have demonstrated a 1cm$^2$ photovoltaic device with a conversion efficiency of $11.1\%$ efficiency. This device was comprised of ID-4 wafer, with 1 μm Ag front metallization, fired with an energy density of 7.4 J/cm$^2$ at a pitch of 150 μm. The cell performance is illustrated by the IV curve in Figure 6-8. The cell possessed an annealed $V_{OC}$ of 595 mV, a $J_{SC}$ of 27.6 mA/cm$^2$, and a $FF$ or 68%. Fitting of the IV curve reveals that it’s superior performance of this cell in relation to the others produced is largely due it possessing the lowest reverse saturation current of the cells produced.

Based on this result, the current process could achieve an efficiency of $>13.5\%$ with modifications to the front surface. The series resistance of 0.97 Ω can be decreased with increased front metallization thickness and accordingly improving the fill factor up to 14%. The application of front side texturization would result in a relative $J_{SC}$ increase of up to 15%. These factors combined with a reduction of the current front metallization coverage from 8% to 4% would increases the cells potential performance to $\sim>13.5\%$. Efficiencies in excess of 13.5% are expected with the optimization further optimization of the device pre-cursor, laser firing parameters or annealing protocol.
Figure 6-8: Pre and post anneal IV curve of 11.1% device

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unannealed</th>
<th>Annealed</th>
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<tbody>
<tr>
<td>$V_{OC}$ (V)</td>
<td>0.572</td>
<td>0.595</td>
</tr>
<tr>
<td>$J_{SC}$ (mA/cm$^2$)</td>
<td>25.6</td>
<td>27.6</td>
</tr>
<tr>
<td>FF</td>
<td>66</td>
<td>68</td>
</tr>
<tr>
<td>$\eta$ (%)</td>
<td>9.7</td>
<td>11.1</td>
</tr>
</tbody>
</table>
Chapter 7
Conclusions

7.1 Thesis Summary and Conclusions

In this work we have proposed, modeled and demonstrated a novel all–low-temperature-processed, laser fired emitter, high efficiency silicon photovoltaic device concept using a hydrogenated amorphous silicon and silicon dioxide dielectric passivation stack. Using 2D Sentaurus computational modeling we predict a potential device efficiency of > 20% and demonstrate a proof of concept device with 11.1% efficiency.

Device simulations show that efficiency increases with increasing base resistivity and with reduced laser-induced damage; a maximal device performance of > 20.5% for the limiting case of no laser-induced damage is obtained. With respect to the absorber thickness, base resistivity and emitter pitch, it is shown that maximum device performance occurs for a base thickness of 150 µm, base resistivity of 100 Ω-cm and an LFE pitch of 500 µm. These results indicate the high efficiency potential for the proposed device architecture.

A low temperature device precursor fabrication process was developed for high resistivity \( n \)-type silicon wafers using the unique DCSFP ECD system. Excellent effective minority carrier lifetimes in excess of 1.5 ms were demonstrated for asymmetrically passivated wafers (\( n \)-a-SiH / \( n \)-c-Si / \( i \)-a-SiH) annealed in air. Subsequent unoptimized depositions of indium tin oxide and silicon oxide degraded the passivation effectiveness of the a-Si:H layers, however this was largely recovered and through subsequent annealing steps which resulted in > 800 μs lifetime for pre-metallization device precursors. This corresponds to an effective minority carrier diffusion length of more than four times the base thickness, which is sufficient for complete carrier collection in the context of a rear emitter device and thus high efficiency potential.

A laser induced diffusion process for aluminum on dielectric stacks was developed. Within the limits of the laser system used and the parameters scanned, laser fired emitters formed with a single pulse demonstrated superior device conversion efficiency to those formed with multiple
pulses. The use of multiple laser pulses for crater formation in general led to reduced performance except for pulse energies near the threshold for crater formation. Near the threshold energy density for emitter formation a local maximum in performance was found for 2-3 pulses, but with a device efficiency lower than that of an LFE device created with a single, sufficiently energetic pulse. We found the device conversion efficiency to be highly sensitive to pulse energy density with optimal device performance for single pulse craters occurring at pulse energy densities of 7.5 J/cm². The change in efficiency as a function of energy density was found to be dominated by the resulting change in \( J_{SC} \).

A saturation in the improvement of \( V_{OC} \) with increasing pitch was predicted by the model and experimentally realized; this is in contrast to previously reported \( V_{OC} \) results for amorphous passivated LFE devices. These results confirm the importance of our proposed rear electrically insulating layer in the context of an amorphous passivated LFE device. An optimal pitch of 125 \( \mu \text{m} \) was found for our experimental device precursors, indicating the tradeoff between the competing processes of reduced recombination, and reduced carrier collection with increasing pitch.

Annealing in \( \text{N}_2 \) at temperatures of 235 °C resulted in a 15% increase in device performance increase; annealing at higher temperatures however led to a decrease in performance. Reduction in passivation for temperatures greater than 235 °C was seen in lifetime samples, corresponding to the reduction in device performance. Analysis using the one-diode model showed that the an increase in both ideality factor and reverse saturation current, for annealing temperatures above 235 °C. Thus, the degradation in performance for temperatures beyond 235 °C is attributed to the limited thermal stability of the passivation presented by the ITO/\( n \)-a-Si:H/\( n \)-c-Si/i-a-Si:H/SiO\(_x\) device precursor.

A device efficiency of 11.1% was realized for a single pulse LFE with an energy density of 7.5 J/cm², on a device precursor prepared in our Gen 2.1 DCSF PECVD system with a pre-metallization minority carrier lifetime of > 900 \( \mu \text{s} \). The ideality factor of this device, like the others in the study, was greater >2, indicating recombination due to defects is currently limiting performance. A high series resistance of 0.6 \( \Omega \) in conjunction with the laser induced damage effects result in a fill factor of 68%. A \( J_{SC} \) of 27.6 mA/cm² was realized, which could be
increased with the application of surface texture and reduction of front metallization coverage and further optimization of surface passivation of the device precursor. Likewise the $V_{OC}$ of 595 mV could be increased with increased generation and reduced surface recombination.

The proof of concept device provides a fabrication process comprised of device precursor fabrication and initial characterization of LFE parameters as a basis for further optimization efforts of this novel device structure.

7.2 Future Work

Further optimization efforts are required to realize the performance potential of the hydrogenated amorphous silicon passivated LFE. Optimization efforts expected to increase understanding of the device function and thus achieve performance improvements include:

1) Investigation of the effect of $n$-a-Si:H front surface field doping and layer thickness on device performance.

2) Optimization of ITO and SiO$_x$ depositions to further reduce passivation degradation associate with these depositions.

3) Optimization of device performance through the exploration of base resistivity and base thickness.

4) Enhanced optical trapping through the use of a substrate with front surface texturization, possibly rear surface texturization, and optimization of the front grid coverage. Additionally, in this context, the viability of a bi-facial cell can be explored by the use of a transparent conducting oxide in conjunction with an appropriately defined and fired aluminum grid on the rear surface.
5) An exhaustive scan and optimization of laser firing parameters in the context of a superior optical set-up that allows the pulse energy, pulse duration, pulse energy density and crater diameter to be modified independently within the limits of the laser output. This could be realized with the modification of the optical set-up to include a waveplate and polarizer combination for pulse energy control, a fast shutter such as an acousto-optic modulator to allow continuous operation of the laser with pulse selection by the fast shutter, and a beam expander for spot size control.

6) Investigation of the effects of annealing, with the exploration of hydrogen plasma annealing, rapid thermal annealing, and the application of more thermally stable a-Si:H/dielectric stacks such as a-Si:H/a-SiNx:H. Associated with this effort, the characterization of the types and concentrations of laser-induced defects as a function of laser parameters and subsequent annealing in the context of a dielectric stack would provide the fundamental basis for optimization of the device. Indeed, the ultimate objective here would be to undertake an in-depth investigation of the opto-thermal-material physics with an eye to possible attainment of a laser induced diffusion emitter with minimal laser-induced defects.
References


68. *BLS Short Pulse Q-switched Laser - 1064 nm, 532 nm, 355 nm and 266 nm*. 2006, Spectra-Physics: Mountain View, CA.


Appendix A

The annealing temperature scan, as well as the pitch and device precursor data were fitted using a two diode model employing a fitting routine available from Energy research Center of the Netherlands (ECN) [32]. The fitting routine implements fixed ideality factors of $n_1=1$ and $n_2=2$, or a variable ideality for the diffusion based diode ($n_1$).

The fitting returned interesting results, particularly in the context of the annealing temperature scan. Here the reverse saturation current of the bulk recombination diode $I_{01}$, shows a minimum for 250 °C in Table A-1. The reverse saturation current of the space charge recombination diode, $I_{02}$, continues to decrease until a temperature of 350 °C, suggesting that the defect density surrounding the emitter continues to decrease after the surface passivation has begun to degrade. This supports the hypothesis that the thermal stability of the amorphous passivation ultimately limits the annealing temperature, and thus the performance gains associated with annealing of a-Si:H/SiO$_x$ stacks.

| Table A-1: Variation of Two Diode Fit Parameters with Annealing |
|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| $J_{ph}$ (A·cm$^{-2}$) | 22 °C  | 138 °C  | 185 °C  | 230 °C  | 274 °C  | 320 °C  | 368 °C  |
| $I_{01}$ (A)     | 1.8e-16 | 2.7e-16 | 8.7e-17 | 3.7e-17 | 1.0e-16 | 2.1e-16 | 9.6e-16 |
| $I_{02}$ (A·cm$^{-2}$) | 4.5e-7 | 4.6e-7 | 3.7e-7 | 3.6e-7 | 2.7e-7 | 2.2e-7 | 2.3e-7 |
| $G_{sh}$ (S)    | 1.3e-3  | 1.2e-3  | 9.9e-4  | 1.0e-3  | 1.3e-3  | 1.7e-3  | 1.7e-3  |
| $R_s$ (Ω)       | 0.87    | 1.2     | 0.98    | 1.23    | 1.31    | 2.24    | 5.92    |
| $J_{mpp}$ (A·cm$^{-2}$) | -2.3e-2 | -2.3e-2 | -2.3e-2 | -2.3e-2 | -2.2e-2 | -2.0e-2 | -1.5e-2 |
| $V_{mpp}$ (V)   | 0.43    | 0.42    | 0.44    | 0.43    | 0.44    | 0.43    | 0.39    |

In Table A-1 the diode currents are represented as currents and not current densities. As the LFE is a localized emitter, the total emitter area is substantially less than the area of the cell. As the active area of the LFE was not investigated, the total emitter area coverage for a given pitch and
laser parameter set can only be estimated using the diameter of the craters. A more thorough determination of emitter active area would require EBIC mapping of the LFE.

The magnitude of the diffusion recombination reverse saturation current ($J_{01}$) is found to be 4 to 6 orders of magnitude lower than expected $J_{01}$ current densities of $10^{-10}$-$10^{-12}$ A/cm$^2$. Emitter coverage is between 1 – 0.1% for the sample used in the anneal temperature study (150 µm pitch). Thus while this area argument brings $I_{01}$ to a more reasonable value in the context of $J_{01}$, it does not explain the full variation from the expected magnitude of $J_{01}$. Further investigation of both total active emitter area and appropriateness of fitting local emitters with a two diode with fixed ideality factors is required.

The same low value of $I_{01}$ is seen in the two diode fitting data for both the pitch scan (Table A-2) and the two diode fitting data of the device scan(Table A-3).

| Table A-2: Two Diode Model fitting results of devices with varying LFE pitch |
|-----------------|--------------|-------------|-------------|-------------|-------------|-------------|-------------|
|                 | 100 µm       | 125 µm      | 150 µm      | 175 µm      | 200 µm      | 250 µm      | 300 µm      |
| $J_{ph}$ (A·cm$^{-2}$) | -2.7e-2      | -2.7e-2      | -2.6e-2      | -2.5e-2      | -2.5e-2      | -2.4e-2      | -2.2e-2      |
| $I_{01}$ (A·cm$^{-2}$)   | 2.1e-16      | 8.9e-17      | 5.8e-17      | 4.1e-17      | 4.0e-17      | 3.5e-17      | 3.3e-17      |
| $I_{02}$ (A·cm$^{-2}$)   | 4.8e-7       | 4.0e-7       | 2.9e-7       | 2.4e-7       | 2.1e-7       | 1.8e-7       | 1.6e-7       |
| $G_{sh}$ (S)            | 1.3e-3       | 1.3e-3       | 1.4e-3       | 1.4e-3       | 1.4e-3       | 1.5e-3       | 1.6e-3       |
| $R_s$ (Ω)              | 7.8e-1       | 5.7e-1       | 6.5e-1       | 6.7e-1       | 7.3e-1       | 7.2e-1       | 7.4e-1       |
| $J_{mp}$ (A·cm$^{-2}$)  | -2.4e-2      | -2.4e-2      | -2.3e-2      | -2.2e-2      | -2.2e-2      | -2.1e-2      | -1.9e-2      |
| $V_{mp}$ (V)            | 4.3e-1       | 4.4e-1       | 4.5e-1       | 4.6e-1       | 4.6e-1       | 4.7e-1       | 4.7e-1       |
Table A-3: Two diode fitting results for differing device precursors

<table>
<thead>
<tr>
<th></th>
<th>ID-1</th>
<th>ID-3</th>
<th>ID-4</th>
</tr>
</thead>
<tbody>
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<tr>
<td>$I_{01}$ (A)</td>
<td>2.6e-15</td>
<td>1.5e-15</td>
<td>5.4e-17</td>
</tr>
<tr>
<td>$I_{02}$ (A)</td>
<td>5.0e-7</td>
<td>4.8e-7</td>
<td>3.3e-7</td>
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<tr>
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<td>1.4e-3</td>
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<td>$R_s$ ($\Omega$)</td>
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<td>6.9e+</td>
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<td>$J_{mpp}$ (A·cm$^{-2}$)</td>
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