CIRCUITS FOR MM-WAVE RADIO AND RADAR TRANSCEIVER FRONT-ENDS

BY

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GRADUATE DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
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ABSTRACT

This thesis presents the design and implementation of 140 GHz to 170 GHz transceivers in SiGe HBT technologies and a 95 GHz receiver in 65 nm CMOS technology. Optimization and modeling of all passive components and transistor biasing at peak-\( f_T \) and peak-\( f_{MAX} \) current densities are employed to obtain higher frequency operation of circuit blocks compared to state of the art. These circuit blocks include static and dynamic frequency dividers, voltage-controlled oscillators, and tuned mm-wave amplifiers. Design procedures for a 100 GHz static divider, a 136 GHz dynamic divider, as well as low-power divider topologies are presented. A methodology for the design of quadrature voltage-controlled oscillators in CMOS and SiGe technologies is described, together with a technique for reduced-power LO-path design. Tuned 5-stage 140 GHz, 160 GHz, and 170 GHz amplifiers with more than 15 dB in SiGe HBT technology are reported.

Using these circuit building blocks, a 95 GHz receiver in 65 nm CMOS technology with 12.5 dB gain, 7 dB noise figure, and 206 mW. Also, several 165 GHz transceivers are implemented in SiGe HBT technology. The 165 GHz transceivers that include an oscillator, a divider, RX, LO, and TX amplifiers, and a mixer, were designed with and without on-chip antennas. They have -3 dB conversion gain, all achieved at RF, and -3.5 dBm output power. Following
that, a 140 GHz fully-integrated transceiver and a 140 GHz transceiver array with on-chip patch antennas were designed in a 0.13 µm SiGe BiCMOS technology, demonstrating the highest integration levels at this frequency in silicon to date. These transceivers feature 136-145 GHz voltage-controlled oscillators, 20 dB receive-amplifiers and mixers, transmit-amplifiers with amplitude-shift keying modulation, and variable-gain IF amplifiers. At 140 GHz the transceivers have up to 32 dB conversion gain and -8 dBm output power. Wireless data transmission at 4 Gb/s was demonstrated over 1.15 m with off-chip horn antennas, and over 2 cm with the on-chip antennas. With on-chip antennas, the transceiver could detect a Doppler shift of as little as 25 Hz. Both transceivers were also operational in frequency-modulated continuous-wave radar mode.
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<td>BER</td>
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<td>CW</td>
<td>Continuous-Wave</td>
</tr>
<tr>
<td>DEMUX</td>
<td>De-multiplexer</td>
</tr>
<tr>
<td>DFF</td>
<td>Data Flip-flop</td>
</tr>
<tr>
<td>DUT</td>
<td>Device Under Test</td>
</tr>
<tr>
<td>ECL</td>
<td>Emitter-Coupled Logic</td>
</tr>
<tr>
<td>EF</td>
<td>Emitter Follower</td>
</tr>
<tr>
<td>FET</td>
<td>Field-Effect Transistor</td>
</tr>
<tr>
<td>$f_{\text{MAX}}$</td>
<td>Unity Power Gain Frequency</td>
</tr>
<tr>
<td>FMCW</td>
<td>Frequency-Modulated Continuous Wave</td>
</tr>
<tr>
<td>FOM</td>
<td>Figure of Merit</td>
</tr>
<tr>
<td>FSM</td>
<td>Finite State Machine</td>
</tr>
<tr>
<td>$f_T$</td>
<td>Unity Current Gain Frequency</td>
</tr>
<tr>
<td>HBT</td>
<td>Hetero-junction Bipolar Transistor</td>
</tr>
<tr>
<td>IF</td>
<td>Intermediate Frequency</td>
</tr>
<tr>
<td>Acronym</td>
<td>Definition</td>
</tr>
<tr>
<td>---------</td>
<td>------------</td>
</tr>
<tr>
<td>ILFD</td>
<td>Injection-Locked Frequency Divider</td>
</tr>
<tr>
<td>LFSR</td>
<td>Linear Feedback Shift Register</td>
</tr>
<tr>
<td>LO</td>
<td>Local Oscillator</td>
</tr>
<tr>
<td>LOS</td>
<td>Line of Sight</td>
</tr>
<tr>
<td>MAG</td>
<td>Maximum Available Gain</td>
</tr>
<tr>
<td>MIM</td>
<td>Metal-Insulator-Metal</td>
</tr>
<tr>
<td>MMIC</td>
<td>Monolithic Microwave Integrated Circuit</td>
</tr>
<tr>
<td>MOM</td>
<td>Metal-Oxide-Metal</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal Oxide Semiconductor FET</td>
</tr>
<tr>
<td>MUX</td>
<td>Multiplexer</td>
</tr>
<tr>
<td>NFET</td>
<td>N-channel Field-Effect Transistor</td>
</tr>
<tr>
<td>NLOS</td>
<td>Non Line of Sight</td>
</tr>
<tr>
<td>NRZ</td>
<td>Non-Return to Zero</td>
</tr>
<tr>
<td>PAE</td>
<td>Power Added Efficiency</td>
</tr>
<tr>
<td>PLL</td>
<td>Phase-Locked Loop</td>
</tr>
<tr>
<td>PRBS</td>
<td>Pseudo-Random Bit Sequence</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>RX</td>
<td>Receiver</td>
</tr>
<tr>
<td>SCFL</td>
<td>Source-Coupled FET Logic</td>
</tr>
<tr>
<td>SERDES</td>
<td>Serializer-Deserializer</td>
</tr>
<tr>
<td>SF</td>
<td>Source Follower</td>
</tr>
<tr>
<td>SiGe</td>
<td>Silicon-Germanium</td>
</tr>
<tr>
<td>SOF</td>
<td>Self-Oscillation Frequency</td>
</tr>
<tr>
<td>SRF</td>
<td>Self-Resonance Frequency</td>
</tr>
<tr>
<td>TFF</td>
<td>Toggle Flip-flop</td>
</tr>
<tr>
<td>TIA</td>
<td>Transimpedance Amplifier</td>
</tr>
<tr>
<td>TX</td>
<td>Transmitter</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage-Controlled Oscillator</td>
</tr>
<tr>
<td>VGA</td>
<td>Variable-Gain Amplifier</td>
</tr>
</tbody>
</table>
The invention of radio in the end of the 19\textsuperscript{th} century and the invention of radar in the beginning of the 20\textsuperscript{th} century demonstrated the advantages of wireless communication and enabled access to new information. Advances in technology have led to the ubiquitous use or radios in modern electronic devices. As the electronics industry continues to make progress, higher bandwidth communication is needed to satisfy the requirements of consumer and industrial applications. Inevitably, to meet this demand for bandwidth, the front-end radio circuits have to operate at increasingly higher frequencies. Operation at higher frequencies is also beneficial for industrial radar sensors applications by enhancing their precision.

The mm-wave spectrum, the range of frequencies from 30 GHz to 300 GHz and wavelength from 10 mm to 1 mm, has previously been the domain of discreet components and circuits implemented in III-V technologies [2–5]. The size and cost of such systems made them suitable only for niche applications affordable by government and military organizations. However, as predicted by Gordon Moore [6], advances in silicon (both CMOS and SiGe) technologies keep increasing the transistor $f_T$ and $f_{MAX}$ to frequencies far above 300 GHz. Therefore, it becomes possible to fully integrate radio and radar transceivers together with their passive devices and antennas on a single chip. This opens the possibility for novel applications that make use of multi-Gb/s wireless connectivity and sensor arrays.

This thesis focuses on the design of mm-wave single-chip transceiver front-ends in silicon technologies. Emphasis is made on simple, yet robust architectures that can be combined into arrays. They are shown to work at 95 GHz in 65 nm CMOS and at 140-170 GHz in SiGe BiCMOS technologies. Radar experiments and wireless data transmission at 4 Gb/s are described. Techniques for reducing the power consumption of mm-wave circuit blocks are also introduced.
1.1. Motivation

The ongoing evolution of integrated-circuits enables the processing of increasing volumes of information in both personal computing and industrial environment. This trend fuels the demand for data-transfer technologies, many of which are wireless. The International Technology Roadmap for Semiconductors (ITRS) reflects this growing demand by projecting an exponential increase of CMOS and SiGe HBT transistor $f_T$ and $f_{\text{MAX}}$, as illustrated in Figure 1.1 [7]. The “dotfive” project [8] (supported by the European Commission) is focused on mm-wave applications and aims at producing a 500 GHz device faster than is predicted by ITRS. The goal of the “dotfive” project is to fabricate SiGe HBTs with $f_{\text{MAX}}$ of 500 GHz in research environment by the end of 2010, and to put them in production in 2013.

Although Figure 1.1 predicts a faster exponential increase of the $f_T$ and $f_{\text{MAX}}$ of CMOS devices compared to SiGe, recent data suggests that this prediction might not materialize. The latest CMOS nodes have failed in exponentially increasing the device speed. For example, 32 nm transistors are only marginally faster than 65 nm transistors. This is because scaling rules have not been strictly applied due to manufacturability constraints and to keep reasonable supply voltages. Thus, it seems that future CMOS nodes will be useful for reducing the area of digital circuits, but might not be beneficial for mm-wave applications. In addition to raw active device speed, which is currently approximately the same in state-of-the-art SiGe and CMOS technologies, the backend-of-line has a tremendous impact on mm-wave circuit performance. In this respect, CMOS technologies, which often have digital backends with thin closely spaced metals, significantly lack behind SiGe, which in most cases is targeted towards mm-wave ap-

![Figure 1.1: ITRS projection for CMOS and SiGe HBT transistor $f_T$ and $f_{\text{MAX}}$, and “dotfive” project goal for SiGe HBT transistor $f_{\text{MAX}}$.](image-url)
1.2 State of the Art

Applications and thus has a dedicated backend. A better backend allows implementing higher quality passive components, which directly affect system parameters such as link margin, gain, noise figure, phase noise and output power.

The availability of active devices with cutoff frequencies in excess of 300 GHz in silicon technologies motivates and enables many applications of mm-wave radios and radars for everyday use. These applications include high data-rate wireless communications, imaging and radar sensors, and radio astronomy.

High data rate radios are being implemented today at 60 GHz [9]. However, even more bandwidth, and hence higher data rate, is available at 140 GHz [10]. Furthermore, by moving to higher frequencies, the antennas become smaller, and can be integrated on the die. Integrated, small size, radios can be combined into arrays for even higher data rates, beam steering, or transmission over larger distances. These radios can potentially be used for chip-to-chip interconnect over a few centimeters, or, with the addition of power amplifiers, serve as last-mile links.

MM-wave radiation can propagate through clothing and other thin dielectric materials. Also, in this frequency range the millimeter-size wavelength allows forming images with millimeter resolution [11, 12]. Images formed with mm-wave radars are used for security reasons to detect concealed weapons [13, 14]. They are also used for industrial quality control of surfaces including semiconductor wafers [15], packages [16], timber [17], and paint [18, 19]. MM-wave imaging can potentially be used for detecting anomalies in dental and medical applications [20–22]. Passive mm-wave imaging is widely employed in astronomy and remote sensing applications [14, 23, 24]. Other uses of mm-wave transceivers include automotive radars and other speed and position detection sensors.

The motivation for this thesis is to design mm-wave (140 GHz to 170 GHz) transceivers in silicon technologies that target some of these applications, and to demonstrate that large integration levels are possible in SiGe HBT technologies at these frequencies.

1.2. State of the Art

Currently, mm-wave systems in the D-band (110 GHz to 170 GHz) and above are primarily the domain of III-V semiconductor technologies. At the time the work for this thesis was started (2005), state of the art circuit blocks, including small-signal amplifiers, dividers power amplifiers and mixers in III-V technologies were published in the 160 GHz to 220 GHz frequency range [25–27]. With advances in research, in the last year or two, III-V device performance was improved to almost $1 \text{THz} f_T$. Consequently, circuit modules operating at 300 GHz and above
have been published [28–30]. In October 2010, an amplifier module with more than 10 dB at 550 GHz designed in an InP technology with $f_{\text{MAX}}$ of 1.2 THz was published [31]. Circuits in InP or GaAs technologies do not achieve large scale integration. They are most often designed as separate amplifiers, oscillators, dividers, multipliers, or mixers MMICs (Monolithic Microwave Integrated Circuits). These MMICs are then packaged into waveguide modules that are connected together to form systems.

Even though CMOS and SiGe designs are starting to appear in the D-band, they do not have as much integration as the designs that will be presented in this thesis. The 140 GHz receiver front-end in 65 nm CMOS technology features on-chip LNA, mixer, IF amplifier and antenna, but does not have on-chip LO generation [32]. The designs recently published in [33] include quadrature 160 GHz transmitter and receiver, however, unlike the designs in this thesis, the transmitter and receiver are not integrated together. Also, the LO is generated at one third of the operating frequency and is multiplied up. The highest frequency SiGe circuit, a $\times 18$ multiplier chain up to 325 GHz was published recently and includes active gain circuits up to 162.5 GHz [34].

1.3. Design Challenges and Approaches

The design of circuits operating at 160 GHz with transistors that have $f_{\text{MAX}}$ of 300 GHz, requires pushing the technology to its limits. One of the challenges in doing that, is accurate modeling of all inductive, capacitive, and resistive parasitics. Due to the high-frequencies involved, even a few micrometers of interconnect have significant inductance to affect the frequency response of a circuit. Therefore, the design must account for the inductance, capacitance, and resistance of every piece of interconnect. Time-wise, it is not realistic to simulate all the metal pieces in a 3-D electromagnetic solver. A modeling procedure that is quick and allows for multiple adjustments to the design is required. Multiple adjustments and iterations of the passives are often necessary to minimize their loss, and thus conserve the little gain available from the active transistors.

In any transceiver system, distribution of the local oscillator (LO) signal to the transmitter and receiver parts is often a power- and area-consuming task. Both the transmitter and the receiver require a large LO signal (0 dBm or more) for proper operation. They are also usually separated from each other by some distance for isolation. The oscillator circuit usually employs significant current to produce a low-phase-noise signal at high frequency. Thus, in order to not deteriorate the oscillator signal but to amplify it, the LO distribution circuit must consume even more current than the oscillator. The current (and thus power) consumption is further
compounded by the fact that the LO distribution must drive a large load (the receiver, the transmitter and often a divider of a PLL).

Another challenge that arises during the integration process is the routing of power supply and ground connections to the individual circuit blocks. This routing must aim at presenting power and ground supplies to the circuit that are as close to ideal as possible. Parasitics in the supply connections change the impedance at those nodes and result in reduced gain or oscillations.

After the circuit is fabricated, its characterization and measurement process is not straightforward. Whereas complete solutions for testing exist in the lower mm-wave frequency range (up to 67 GHz), they are not always available above 100 GHz.

1.4. Thesis Outline

The remainder of this thesis consists of seven chapters. Chapter 2 provides a background for this dissertation through an overview of the operation principles of radio and radar systems, and state-of-the-art. Chapters 3 through 7 present the main contributions of this work. Chapter 3 presents the design parameters of passives, which are key components of mm-wave circuits. Chapter 4 presents several frequency divider topologies and design examples at 100 GHz and above. Chapter 5 describes the analysis and design procedure of 80/160 GHz voltage-controlled oscillators. In Chapter 6 a design methodology of D-band (110-170 GHz) tuned amplifiers is given, along with record-breaking amplifier designs. Chapter 7 presents the main contributions of this work, which are a 95 GHz double-sideband receiver implemented in 65 nm CMOS and a family of 140-170 GHz transceivers designed in SiGe BiCMOS technologies, the highest frequency in CMOS and SiGe BiCMOS. Finally, Chapter 8 concludes this thesis and discusses potential future research directions in the area of mm-wave circuits.
This chapter presents the basic concepts of radio communications and radars. The operation of
radios and radars relevant to this thesis is reviewed. The first section explains how zero-IF radio
transmitters and receivers with amplitude-shift keying modulation work. The second section
describes the principles of Doppler and FMCW radars. Transceivers working in the 140 GHz
to 160 GHz frequency range that implement the concepts of this chapter will be described in
Chapter 7.

2.1. Radio Communications

As illustrated in Figure 2.1, a basic radio system consists of a transmitter and receiver with
their antennas that are separated by a distance $R$. The quality of this wireless link depends on
several factors related to the transmitter, the receiver, and the medium through which the signal
propagates (ether).

A zero-IF (intermediate frequency) transmitter architecture is shown in Figure 2.2. In the
transmitter, a local oscillator (LO) circuit generates the carrier signal $S_{LO}(t) = \cos(2\pi f_{LO}t)$.
In the case of data communication, the IF signal represents the data bit stream $S_{IF}(t) = A_{IF}(t)$.
Before the IF data can be transmitted, it must modulate the carrier frequency. This operation
is usually performed with a multiplication of the IF signal by the LO to form the RF (radio
frequency) signal $S_{RF} = A_{IF}(t)\cos(2\pi f_{LO}t)$. The multiplication can be carried out with an
2.1 Radio Communications

upconverter mixer or a direct modulator. A power amplifier, which increases the power of the RF signal, is the last stage of the transmitter.

The most important parameters that define the transmitter are its output power (the amount of RF power generated by the PA) and the LO phase noise. The phase noise $L(f_m)$ is defined as

$$L(f_m) = \frac{\text{noise power in 1 Hz bandwidth at } f_m \text{ offset from carrier}}{\text{carrier signal power}}$$ (2.1)

A corresponding zero-IF receiver system is given in Figure 2.3. In the receiver, the RF signal from the antenna is first amplified with a low-noise amplifier (LNA). As will be explained shortly, the LNA is required to increase the sensitivity of the receiver. The receiver also includes its own local oscillator, which should have the same frequency as that of the transmitter for direct conversion. To recover the IF signal, a down-conversion mixer “undoes” the modulation performed in the transmitter by multiplying it again by the LO signal.

$$S_{IF}(t) = S_{RF} \times S_{LO}(t) = A_{IF}(t) \cos(2\pi f_{LO}t) \times \cos(2\pi f_{LO}t) = \frac{A_{IF}(t)}{2} + \frac{A_{IF}(t)}{2} \cos(4\pi f_{LO}t)$$ (2.2)

The low-pass filter that follows the mixer filters second harmonic of the LO leaving just the IF information $S_{IF}(t) = A_{IF}(t)/2$. After the IF signal is recovered, it is further processed.
by the baseband circuitry. A receiver is characterized by its noise, gain, linearity and dynamic range.

The noise factor $F$ of a two-port network is defined in (2.3). The noise figure $NF$ is the noise factor with the input at room temperature, $T_{in} = 290K$.

$$F = \frac{SNR \text{ at input}}{SNR \text{ at output}}$$ \hspace{1cm} (2.3)

For a cascade of two-ports, each with gain $G_i$ and noise factor $F_i$, the total noise factor is given by [35]

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1G_2} + \cdots + \frac{F_N - 1}{\Pi_{i=1}^{N-1} G_i}$$ \hspace{1cm} (2.4)

Thus, to minimize the overall noise figure of a receiver, the mixer stage must be preceded by a low noise amplifier with sufficient gain to “shield” the impact of mixer noise.

A receiver is linear when the output signal amplitude is related to the input amplitude only by a multiplicative gain $S_{OUT} = G \times S_{IN}$. However, at some input power level, this relationship will no longer hold because the circuit cannot support such large power levels either at the input or at the output. For a cascade of $N$ two-port networks, each with an output 1 dB compression point $P_{1dB,i}$, input-referred third-order intercept point $P_{IIP3,i}$, and power gain $G_i$, the overall $P_{1dB}$ and $P_{IIP3}$ can be expressed as [36]

$$\frac{1}{P_{1dB}} = \frac{1}{P_{1dB,1}} + \frac{G_1}{P_{1dB,2}} + \frac{G_1G_2}{P_{1dB,3}} + \cdots + \frac{\Pi_{i=1}^{N} G_{i-1}}{P_{1dB,i}}$$ \hspace{1cm} (2.5)

$$\frac{1}{P_{IIP3}} \approx \frac{1}{P_{IIP3,1}} + \frac{G_1}{P_{IIP3,2}} + \frac{G_1G_2}{P_{IIP3,3}} + \cdots + \frac{\Pi_{i=1}^{N} G_{i-1}}{P_{IIP3,i}}$$ \hspace{1cm} (2.6)

From (2.5) it can be deduced that the last stage in the cascade has the most effect on the overall linearity, and thus should have the best linearity in the system.

The dynamic range of a receiver (or another circuit) is the range of acceptable input signal powers. It is defined by the circuit’s noise figure and linearity. The noise figure determines the minimum detectable signal, and the $P_{IIP3}$ determines the maximum signal the can be processed with tolerable distortion [37].

In addition to the transmitter and receiver non-idealities, the wireless system is also affected by the characteristics of the space through which the signal travels. Some of the impairments that signal experiences while propagating through the air are multipath, fading, Doppler shift, delay spread. In line-of-sight conditions, the power of the signal that arrives at the receiver is proportional to the inverse of the square of the distance $R$ between the transmitter and receiver antennas. It is given by [38]
2.1 Radio Communications

Figure 2.4: Approximate atmospheric attenuation in dry air in the mm-wave spectrum.

\[ P_r = \frac{A_{eff,r}A_{eff,t}}{\lambda^2 R^2} P_t \]  

(2.7)

In (2.7), \( P_t \) is the output power at the input of the transmitter antenna, \( P_r \) is the output power from the receiver antenna, \( \lambda = c/f \) is the wavelength, \( A_{eff,r} \) and \( A_{eff,t} \) are the effective areas of the receiver and transmitter antennas. The effective area \( A_{eff} \) of an antenna is proportional to its physical area and power gain \( G = \eta D \), where \( \eta \) is the antenna efficiency and \( D \) is its directivity.

\[ A_{eff} = \frac{\lambda^2 G}{4\pi} \]  

(2.8)

\[ P_r = \frac{G_r G_t \lambda^2}{(4\pi R)^2} P_t = \frac{G_r G_t}{(4\pi R)^2} \left( \frac{c}{f} \right)^2 P_t \]  

(2.9)

(2.9) results from substituting (2.8) into (2.7) and designating the receiver and transmitter antenna gains as \( G_r \) and \( G_t \). (2.9) indicates that the received power decreases with the square of the frequency. This illustrates the difficulty of building radios operating in mm-wave frequencies, especially when combined with the fact that transmitter output power drops with increasing frequency due to limitations in the active devices employed in the circuits.

The atmosphere also introduces frequency-dependent attenuation in addition to the free-space loss of (2.9). A plot of the atmospheric attenuation in the mm-wave frequency range is
given in Figure 2.4 [39,40]. Weather conditions such as dust, fog, and rain further increase this attenuation. The plot shows that low-attenuation “windows” are present in the 80-100 GHz, 140-160 GHz, and 220-280 GHz frequency ranges. In this thesis, receiver and transceiver circuits operating in the 90 GHz and 140-160 GHz frequency ranges will be described.

2.2. Radars and Imaging Systems

This section describes the operation principles of radars (such as Doppler and frequency-modulated continuous-wave radars) and imaging systems. A basic radar (or Radio Detection and Ranging) system is illustrated in Figure 2.5. The radar works by illuminating a target with the transmitted signal and receiving the back-scattered reflections from the target at distance $R$. When the transmitter and receiver employ separate antennas, the radar is called bistatic, when they share one antenna, it is called monostatic.

Radar operation is governed by the radar equation (2.10), which relates the received power to the transmitted power [41].

$$P_r = \frac{G_t G_r \lambda^2 \sigma}{(4\pi)^3 R^4} P_t$$  \hspace{1cm} (2.10)

Here $P_t$ and $P_r$ are the transmitted and received signal powers, $G_t$ and $G_r$ the antenna gains of the transmitter and receiver, and $\sigma$ is the target radar cross section. The radar cross section of a target has units of area and is defined as the ratio of the scattered power from the target to the incident power density on the target $\sigma = P_s / S_{\text{incident}}$.

A Doppler radar, or continuous-wave (CW) radar, can be used to detect moving targets and measure their velocity relative to the radar. It operates by transmitting a continuous wave signal of frequency $f_0$, receiving the Doppler-shifted frequency $f_0 \pm f_d$, and calculating the

![Figure 2.5: Radar system illustration.](image-url)
target velocity from the Doppler shift \( f_d \). The relative velocity of the target is given by (2.11), where \( c \) is the speed of light [41].

\[
v_r = \frac{f_d c}{2f_0}
\]  

(2.11)

For example, a Doppler frequency of 28 Hz, and a CW signal of 140 GHz give a target velocity of 3 cm/sec. A Doppler radar, however, cannot be used to measure the target range. One way to measure both distance and velocity is to use a frequency-modulated continuous-wave (FMCW) radar.

The signals involved in the FMCW radar are shown in Figure 2.6 [42]. Here, the transmitted signal is varied linearly in frequency over a bandwidth \( B = f_2 - f_1 \) with a repetition period \( T_R \). The received signal is delayed in time due to the distance to the target and is shifted in frequency due to the target motion. After the received signal is multiplied with the original transmitted signal, the resulting IF has two “beat frequencies” \( \Delta f_1 \) and \( \Delta f_2 \) repeating with the period \( T_R \) and corresponding to the difference in frequency between the transmitted and received signals.

When the target is stationary, \( \Delta f_1 = \Delta f_2 = f_R \). The distance \( R \) to the target can be calculated from \( f_R \) as follows.

\[
R = \frac{cT_R f_R}{4B}
\]  

(2.12)

When the target is moving, the two beat frequencies are related by

\[
\begin{align*}
\Delta f_1 &= f_R + f_d \\
\Delta f_2 &= f_R - f_d
\end{align*}
\]  

(2.13)
In this case the target range $R$ can be obtained from (2.13) and $2f_R = \Delta f_1 + \Delta f_2$. The target velocity $v_r$ can be calculated from (2.11) and $2f_d = \Delta f_1 - \Delta f_2$. The accuracy of range and velocity measurements in an FMCW radar depends on the linearity of the frequency ramps. One way to correct for the non-linearity of the VCO tuning characteristic is to use a divided-down VCO signal to observe the non-linearity and then to correct the tuning controls to make it linear.

A modification of the FMCW radar, that enables position detection, is illustrated in Figure 2.7. In this configuration, the transmitter sends a FMCW signal, this signal is reflected from a stationary target, and is received with a receiver array. After the distance to the target is calculated from the data in each receiver, the location of the target can be obtained. A two-receiver array gives enough information to calculate the angle to the target in a 2-D plane, and a three-receiver array can locate the target in 3-D space. Note that for this application the receivers need only be separated by some distance from each other, and that a phased array is not required.

In imaging systems, the goal is to form a mapping of the power intensity that is re-radiated back from the object being imaged. In passive imagers, the reflection of power from the sky is received and processed. In active imagers, the object is first illuminated by a continuous-wave transmitter. Active imagers can also be used to form images through the object by placing the transmitter and receiver on opposite sides of the object. In all cases, the image can be formed by either mechanically moving the transmitter and receiver from pixel to pixel, electrically steering the antenna beam to different pixels, or employing an array of transceivers. Imaging systems, both passive and active, benefit from higher frequency operation which increases the resolution, and from wider bandwidth which allows to better distinguish materials that have different spectral responses.
2.3. Conclusion

In this chapter basic radio and radar concepts were reviewed as a background for the following chapters. The following chapters will present methods and implementation examples of mm-wave circuits that can be used to build the radios and radars of this chapter.
The design of mm-wave circuits relies heavily on passive components. In fact, in most circuits in this thesis, there are more passive components than there are active transistors. Thus, an accurate yet fast simulation and modeling procedure is required for passive components. This chapter gives examples of inductors, transformers, capacitors and varactors from the circuits designed during this work. The geometry, model, simulations, and measurement results are given for the passive components in this chapter.

3.1. Inductors

Inductors are perhaps the most-often used passive components in mm-wave circuits. They are employed in VCOs, tuned amplifier stages, mixers, broadband stages and other places. Due to the extensive use of inductors, a quick procedure for their design and modeling is essential. In this section, several inductor designs and their models will be presented. The ASITIC [43] program is employed for the design of inductors and other passives described in this chapter. Although it is not a full 3D electro-magnetic simulator, it is best suited for a quick turn-around time between geometry definition and model extraction for circuit simulation purposes. For circuit simulation, 2-π models, extracted from simulated Y parameters according to [44], are employed.

The first example is a 50 pH inductor designed for a 160 GHz push-push oscillator tank. To minimize the phase noise of the Colpitts oscillator, the quality factor $Q_{EFF} = \frac{\Im(\frac{1}{Y_{11}})}{\Re(\frac{1}{Y_{11}})}$ of the tank must be maximized. For on-chip inductors the achievable $Q$ values vary between 15 and 20, depending on the technology backend. To maximize the $Q$, the loss of the tank inductor was reduced by implementing the inductor coil with 2 metals shunted together (Alucap and Metal 6), and with a Metal 5 underpass (Figure 3.1). An inductor geometry with 2.8 µm metal width, 2 µm spacing, and an inner diameter of 9 µm was chosen to push the self-resonance frequency above twice the frequency of operation. The inductor coil was placed directly over the silicon
substrate, without any polysilicon or metal shield. Microstrip transmission lines (3.6 µm-wide Metal 6 signal line over Metal 1 and Metal 2 ground plane) were employed to symmetrically connect the four tank inductors of the oscillator together.

The 2-π model, extracted from the ASITIC-simulated Y-parameters, is shown in Figure 3.1. Figure 3.2\(^1\) compares the measured \(L, R\) and effective \(Q\) of the inductor to those simulated using ASITIC and modeled with the 2-π model. The measurement was performed using two network analyzers covering the 1 GHz to 70 GHz, and the 57 GHz to 94 GHz frequency ranges. The measured inductance value increases below 10 GHz due to imperfect probes and contact resistance. Except for the scatter in the measured \(Q\) data in the 57 GHz to 94 GHz range due to the difficulty of measuring resistance with less than 0.1 Ω accuracy, the agreement between simulations and measurements is very good.

Another example of an inductor geometry and model are shown in Figure 3.3. It was employed in the LNA of a 90 GHz receiver front-end designed in a 65 nm CMOS technology. This 88 pH inductor was implemented in the top metal of the technology backend to reduce capacitive parasitics and increase the self-resonance frequency of the inductor. The measured and simulated inductance and quality factor of this inductor are reproduced in Figure 3.4.

3.2. Transformers

Transformers can be used at mm-waves for single-ended to differential signal conversion, impedance transformation and AC-coupling. This section gives several transformer examples implemented in different technology backends. As with other passive structures, the transformer performance depends significantly on the backend available. The backend affects both

---

\(^1\)Thanks to Kenneth Yau for providing the inductor measurement data.
3.2 Transformers

Figure 3.2: Comparison of inductor $L$, $R$, and $Q$ simulated using ASITIC, modeled with 2-$\pi$ model, and measured over two frequency ranges using two different VNAs.

Figure 3.3: 90 GHz inductor geometry (left) and model (right) implemented in a 65 nm CMOS technology.
3.2 Transformers

the quality factor of each coil and the achievable coupling between the coils for a given coil inductance. In turn, both these parameters affect the signal loss through the transformer.

3.2.1. 160-GHz 1-to-1 Transformer

A 160 GHz 1-to-1 transformer was designed for single-ended to differential signal conversion at the RF and LO ports of a mixer. Passive transformers are preferred to other methods of single-ended to differential conversion, such as differential pairs, since they do not consume any DC power. Furthermore, due to their symmetry, transformers have better common mode rejection than differential pairs at mm-wave frequencies. In this transceiver, transformers are also used to AC-couple the RF and LO inputs to the mixer because they facilitate biasing of the mixer through the transformer center tap.

The transformer geometry and its model are shown in Figure 3.5. The primary and the secondary coils consist of one square turn with an inner diameter of 20 \( \mu \text{m} \) and with 2.5 \( \mu \text{m} \) metal width. The transformer coils are placed directly above the silicon substrate, with the top coil implemented in the top aluminum (Alucap) layer, and the lower coil in Metal 6, which is made of copper. The top coil has a center tap (shown as a short extension in the center of the top winding) for biasing circuits connected to the transformer. The ASITIC [43] program (version 3.19.00) was employed to simulate the transformer geometry and to optimize it for lowest loss around 160 GHz. A list of ASITIC commands used to define the transformer structure is given.
in Appendix A. Because of the small transformer footprint, the simulated silicon area below and around the transformer was reduced to $64 \mu m \times 64 \mu m$ to produce a sufficiently fine grid in the metal windings, as required to ensure good accuracy.

A lumped equivalent circuit, consisting of frequency-independent circuit elements, was extracted for the transformer (Figure 3.5) and was employed in all circuit simulations. It comprises a 2-$\pi$ model for the coils and 2-$\pi$ models for each of the short wires connected to the transformer coils. The 2-$\pi$ models were obtained by following the procedure outlined in [44]. The simulated self-resonance frequency of the transformer is approximately 400 GHz. Figure 3.6 compares the transformer S-parameters simulated with ASITIC, those obtained with the extracted 2-$\pi$ model in SpectreRF, and the measured $S_{21}$ and MAG [41] (Maximum Available Gain - essentially the transformer loss) in the 1 GHz to 70 GHz, 57 GHz to 94 GHz, and 116 GHz to 184 GHz frequency ranges. Good agreement of both $S_{21}$ and MAG is achieved, within the measurement accuracy. Although $S_{21}$ is approximately -4 dB, MAG represents the transformer loss as it is used in the circuit, when all ports are matched. Thus the true transformer loss is below 2 dB.

Maximum Available Gain is defined as:

$$MAG = \left( K - \sqrt{K^2 - 1} \right) \times \frac{|S_{21}|}{|S_{12}|} \quad \text{for} \quad K > 1$$

(3.1)

Where $K$ is the stability factor defined by

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}S_{21}|}$$

(3.2)

For measurements below 94 GHz, LRM calibration and T-line de-embedding were employed, as described in [45]. The scatter in the measured $S_{11}$ and $S_{22}$ data is due to the difficulty of accurately measuring and de-embedding parasitic capacitances (below 1 fF), resistances (below 0.1 $\Omega$) and inductances (below 1 pH). For example, errors or uncertainty in the probe-pad

![Figure 3.5: Transformer 2-$\pi$ model (left) and transformer geometry (right), not to scale.](image-url)
contact resistance of 0.1 Ω, parasitic inductance of 1 pH, and error in pad capacitance of 2 fF, can change the measured $S_{21}$, $S_{11}$, and $S_{22}$ by as much as 1 dB in either direction for the small inductors and transformers discussed in this chapter. Above 100 GHz, the transmission loss ($S_{21}$) of the transformer was obtained using a scalar transmission measurement.

### 3.2.2. 90-GHz Transformer

Another transformer was designed in a 65 nm CMOS digital backend to operate in the 90 GHz frequency range. Its geometry is illustrated in Figure 3.7. This transformer is employed for AC-coupling and power supply separation between circuit blocks in a 90 GHz CMOS imaging receiver (section 7.1). Compared to the 160 GHz transformer described in the previous section, this transformer has two loops in each coil, to increase the coil inductance and to bring the frequency at which peak $S_{21}$ occurs to 90 GHz.

The 2-π model of this transformer, which was used for circuit simulations is reproduced in Figure 3.8. The corresponding measured data and simulations of this transformer are shown in Figure 3.9.

### 3.2.3. A Transformer in an Aluminum Backend

The transformers presented in the previous two sections were designed in technology backends that have all copper metal layers. Copper allows finer geometries (tighter metal spacing and width) and thus gives the designer better control of the coupling and inductance of the transformer. However, in some technologies (IBM SiGe8HP), the top metal layers are made from aluminum, which has coarse DRC rules. In this case, there is very little coupling between the coils if the transformer is designed as in Figure 3.5 or Figure 3.7. The coupling is small because of the large physical distance between the coils in the horizontal direction (due to DRC rules) and in the vertical direction (due to the backend metal spacing).

One way to go around this problem is to build the transformer out of coupled lines. This is illustrated in Figure 3.10. This transformer is implemented in the top two aluminum metals of a 5-metal backend. Due to the large vertical spacing of the top two metals, the coupling between them is small. To increase the coupling, the transformer loop was constructed from four coupled lines, previously modeled in [46]. The width of the coils is 15 μm, the inner diameter of the transformer loop is 40 μm. Metal 3 is used for the slotted ground shield.
Figure 3.6: Comparison of transformer $S_{11}$, $S_{21}$, $S_{22}$ and MAG simulated using ASITIC (open circles), modeled with 2-$\pi$ model in SpectreRF (lines), and measured in 3 frequency ranges (dots) using two VNAs and power insertion loss measurements beyond 110 GHz.

Figure 3.7: Geometry of the 90 GHz transformer implemented in 65 nm CMOS technology (not to scale).
Figure 3.8: 2-$\pi$ model of the 90 GHz transformer shown in Figure 3.7

Figure 3.9: Measured S-parameters of the 90 GHz transformer in the 57 GHz to 94 GHz frequency range.
3.2.4. Horizontally and Vertically Coupled Transformer

In a backend where the top metals are far apart above each other, but are allowed to be tightly-spaced, a 1-to-1 transformer with high coupling can be constructed as shown in Figure 3.11. In this type of transformer, the primary (shown in red) and secondary (shown in blue) coils are coupled in both the vertical and the horizontal directions.

The transformers of Figure 3.11 benefit from having only one via in each coil and no underpasses, thus increasing the quality factor of the primary and secondary inductors and decreasing the total transformer loss. The vias also mark the center points (or AC-grounds) of each coil.

A disadvantage of the geometry suggested here is that it does not allow for an easy scaling to very low coil inductances. Also, this geometry results in having a relatively large capacitance between the coils, thus reducing the self-resonance frequency (SRF) of the transformer and restricting the frequency at which it can be used. Increasing the inter-coil spacing will reduce the inter-coil capacitance (but at the expense of reduced magnetic coupling) and will also make the transformer more robust to process metal width and spacing variations.

Transformers of type shown in Figure 3.11 were used successfully in the low-voltage 120 GHz dynamic and static dividers for AC-coupling between stages and for single-ended to differential signal conversion.
3.3 Capacitors and Varactors

Custom metal-over-metal capacitors were designed for tuned amplifier stages at 170 GHz. To tune all the resonant load circuits in all amplifier stages to 170 GHz, capacitors with values smaller than 30 fF are required. Since such small MiM capacitor values were not available in the design kit, custom Metal-Oxide-Metal capacitors were designed using ASITIC. Figure 3.12 illustrates the 3-D capacitor structure and the 2-$\pi$ model which was used in circuit simulations. The 2-$\pi$ equivalent circuit was derived from the simple-$\pi$ circuit employing a procedure similar to that described in [44], with the modification that the main design parameter is the capacitance and the inductance and resistance are parasitics. To minimize their inductance and the die area of the amplifier, all capacitors have a short aspect ratio, instead of the square layout typical of MiM capacitors.

The last (but not least) passive components described in this chapter are varactors. Varactors are essential elements for achieving frequency tuning in voltage-controlled oscillators. As such, their $Q_{EFF,VAR}$ and $C_{VAR,max} : C_{VAR,min}$ parameters both have to be maximized.

$$Q_{EFF,VAR} = \frac{\Im(-Y_{12})}{\Re(-Y_{12})} = \frac{1}{R \times \omega C_{VAR}}$$

$$C_{VAR} = \frac{1}{\omega \times \Im(-Y_{12}^{-1})}$$

The ratio of the maximum to minimum capacitance of the varactor, $C_{VAR,max} : C_{VAR,min}$,
3.4 Layout Techniques

This section presents some layout techniques employed in mm-wave circuits. For achieving good performance in these designs, proper layout is just as important as accounting for and modeling every piece of interconnect between devices. In all the designs described in this thesis, a metal mesh is employed for ground and supply distribution to each circuit block. This directly translates to the VCO tuning range. It can be maximized by building the varactors from mosfets with the minimum gate length available in the technology. To increase the $Q_{EFF}$ of the varactor, small finger width can be employed. For example, in the designs of this thesis, 0.8 $\mu$m finger width was used for varactors in 65 nm technology, and 1 $\mu$m finger width was used in a 0.13 $\mu$m technology. These finger widths were chosen such that at least 2 contacts fit on the source and drain to reduce the source and drain contact resistance. The varactor gate is contacted on both sides, also to reduce the gate resistance. To reduce the capacitive parasitics of the varactor, the source and drain side vias are constructed in a stair-case manner. A sample varactor layout is shown in Figure 3.13.

Figure 3.13 also illustrates the measured $C_{VAR}$ and $Q_{EFF}$ at 90 GHz of a 65 nm varactor. This varactor achieves a $Q_{EFF}$ of 6 to 8 at 90 GHz, and capacitance variation from 25 fF to 41 fF. This varactor was employed in a 90 GHz VCO, described in section 5.3.

Figure 3.12: Custom capacitor layout geometry (bottom, not to scale), the corresponding 2-$\pi$ capacitor model (top left), and the measured capacitance of the custom capacitor test structure in the BiCMOS9MW technology (top right).
mesh, shown in Figure 3.14, both reduces the parasitic resistance and inductance of the ground and supply nets, and creates a uniform distribution of metal layers over the entire chip, which helps to pass density DRC rules of modern technologies. In the mesh, metal 1 is used for ground and metal 2 for the supply. Other metals can be shunted to decrease the resistance. For example, metal 4 can be shunted with metal 2 for supply distribution and metal 5 can be shunted with metal 1 for ground distribution. The mesh can be reconfigured in different parts of a large chip depending on the requirements of the various supplies. For isolation between circuit blocks or for shielding of critical control lines the mesh can also be reconfigured to have ground on all metals. Substrate taps are connected to metal 1 (ground) everywhere under the mesh.

Figure 3.13: Varactor layout illustration (left) and measured varactor $C_{VAR}$ and $Q$ at 90 GHz in 65 nm CMOS.

Figure 3.14: Illustration of the ground and supply distribution metal mesh.
In addition to the mesh, decoupling capacitors are placed at every ground, supply, and bias connection of mm-wave circuits [47]. The value of these capacitors is chosen to filter noise, and at the same time to not resonate with any existing inductive parasitics below the frequency of operation of the circuit. For example, at 160 GHz, 200 fF to 300 fF decoupling capacitors are used.

\[
 f_{\text{resonance}} = \frac{1}{2\pi} \sqrt{\frac{1}{L_{\text{parasitic}}C_{\text{decoupling}}}} = \frac{1}{2\pi} \sqrt{\frac{1}{(2pH)(300fF)}} = 205GHz > f_{\text{operation}}
\]

The procedure for making a layout of a mm-wave circuit can be summarized in the following steps.

1. Make layouts of the transistors that will be employed in the circuit and extract them to obtain the RC parasitics. Different layouts should be made for CE/CS, CB/CG, EF/SF, and cascode configurations with and without degeneration. To optimize the device layout, the \( f_T \), \( f_{\text{MAX}} \) and NF of the extracted devices should be simulated and the layout repeated if necessary. This step creates a library of transistors, that includes device parasitics, with which schematic-level design is performed.

2. For each circuit stage, use the extracted devices and simulate to obtain preliminary values for the passive components required to create this stage.

3. Create geometries for the required passives in an EM simulator, and extract their \( 2\pi \) models. Although any EM simulator can be employed in this step, it was found that it is much faster to extract \( 2\pi \) models with ASITIC than with other simulators. The time advantage was considered more worthwhile than the accuracy of the results because there are uncertainties in the active models too. Note that \( 2\pi \) models, as opposed to S-parameter “black boxes”, are employed during the design because they give more insight to the designer about how the passive component’s parameters change with geometry. Appendix A and [44] give procedures for extracting \( 2\pi \) models of transformers and inductors.

4. Make a layout placement of the active devices and the passives of the circuit stage. Note that the decoupling capacitors should also be placed from the beginning of the layout, so that there is enough space for them. The initial placement indicates how the geometries of the passives should be modified in order to fit between the actives and the decoupling capacitors and/or ground/supply connections.
3.5 Summary

5. Modify the geometry of the passives such that they fit the layout placement and still have the value required from the simulation of step 2. Note that the geometry of the passive component must include every micron of metal in-between active devices and from extracted active device to the ground/bias/supply connection. This ensures that all metal pieces in the high-frequency path are accounted for, either with extraction or with modeling of passives.

6. Simulate the circuit stage with the $2\pi$ models of the passives that are in the layout. Adjust the values of the passives to bring the circuit stage back in spec. This requires updating the layout, repeating the passives simulations and $2\pi$ model extraction, and simulating again.

7. Once the simulation results with the passives from layout are satisfactory, the layout is finalized by connecting the ground, supply and bias nodes to the circuit stage and connecting the decoupling capacitors. Ample metallization must be used for ground and supply connections, especially in circuits with high current. A few microns away from the connections, the stage is connected to the mesh that distributes the ground and supply over the chip.

8. After completing the individual stages, they are formed into circuit block with mesh around them. The circuit block can then be abutted to each other to form the top-level block placement in the chip. The mesh is then used to fill the space between the pads and the circuits and to distribute power and ground from the DC pads to the circuits. Care must be taken to not interrupt the ground anywhere on chip and to minimize the resistance and inductance of ground and supply distribution.

3.5. Summary

This chapter presented design examples of passive components employed in mm-wave circuits. Suggestions for design options in different technologies were given for inductors and transformers. Optimum layout of varactors was described, followed by general circuit layout guidelines.
In this chapter, frequency divider circuits operating at 100 GHz and above are presented. First, a general description and comparison of various types of frequency dividers is given. Then the operation of static and dynamic frequency dividers is described, followed by characterized circuit examples. Finally, examples of novel low-power static and dynamic dividers are discussed.

4.1. Frequency Divider Topologies

Frequency dividers are essential components in many systems. They are employed in PLLs [48] for both radio and wireline transceivers. Dividers can be used in FMCW radars for observing and correcting the non-linearities in the frequency tuning curve of the VCO [49]. Static frequency dividers are a reliable way to generate signals in quadrature. They are also widely used as a circuit performance benchmark or figure-of-merit indicator to gauge a particular semiconductor technology’s ability to implement high speed digital and high performance mixed-signal circuits [50]. Extending the maximum frequency at which dividers can operate is thus important to the successful development of radio, radar, and other systems beyond 100 GHz.

Frequency dividers can be classified in three categories: static divider (Figure 4.1(a)), dynamic (or Miller) divider (Figure 4.1(b)), and injection-locked frequency divider (ILFD) (Figure 4.1(c)).
Their main properties are summarized qualitatively in Table 4.1. The divider bandwidth is the frequency range over which the divider divides correctly (i.e. the output tone has no noise “skirts” around the fundamental and no phase-flips occur). The bandwidth is related to the sensitivity of the divider - the input power required to divide correctly. In laboratory conditions, some dividers can be shown to operate at higher frequencies than when integrated into a system if high-power sources are available. However, in practical conditions, dividers must be sensitive enough to work with signals of around 0 dBm. For broad-band applications static dividers are preferred as they can be designed to work from DC up to the highest frequency of operation of the system. For PLLs, the dividers must have sufficient bandwidth to cover the VCO tuning range. In mm-wave applications, where signals are available only in certain waveguide bands, dividers do not need to be more broad-band than the waveguide band itself. In this case dynamic dividers can be employed to save power and/or operate at higher frequency compared to static dividers.

Divider noise is an important parameter for PLL applications, as the divider must not degrade the phase noise of the VCO. Both static and dynamic dividers can be designed to be low-noise. However, injection-locked dividers generally have higher noise because they operate as VCOs whose frequency is injection-locked from the natural frequency of oscillation [51]. This chapter will focus on the design of static and dynamic dividers only, as injection-locked frequency dividers are too narrow-band for many applications and often require a large number of tuning controls that limit their practicality.

### 4.2. Static Frequency Dividers

The general topology of a static frequency divider is shown in Figure 4.1(a). To date, static frequency dividers have been implemented up to 110 GHz in SiGe HBT technologies [52,53], up to 208 GHz in InP technologies [50,54,55], and up to 94 GHz in CMOS [1]. A static divider is composed of two (master and slave) latches connected in feedback. Both the switching speed of the latches and the delay through the feedback path determine the maximum and the

<table>
<thead>
<tr>
<th></th>
<th>Static</th>
<th>Dynamic</th>
<th>Injection-locked</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandwidth</td>
<td>Widest</td>
<td>Wide</td>
<td>Narrow</td>
</tr>
<tr>
<td>Sensitivity</td>
<td>High</td>
<td>High</td>
<td>High</td>
</tr>
<tr>
<td>Noise</td>
<td>Low</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>DC Power</td>
<td>High</td>
<td>Medium</td>
<td>Low</td>
</tr>
</tbody>
</table>

**Table 4.1:** Relative properties of different frequency divider topologies
4.2 Static Frequency Dividers

minimum operation frequency of the divider. For dividers to operate at mm-wave frequencies in a SiGe HBT technology, the latches are usually implemented in emitter-coupled logic (ECL) or in current-mode logic (CML), as illustrated in Figure 4.2.

Although the schematic of Figure 4.1(a) suggests that a static divider is simply a Toggle Flip-Flop (TFF) that should operate in the same way from DC to its maximum frequency, this is the case only with a square-wave input. Static dividers that are designed to operate at around 100 GHz and above often have a limited bandwidth ($F_{\text{div,min}}$ to $F_{\text{div,max}}$) over which they can divide with a sinusoidal input. They also have a Self-Oscillation Frequency (SOF) - the frequency at which the divider oscillates by itself with no clock input applied. The SOF is also the point of maximum sensitivity of the static divider. For static dividers, the SOF is correlated with the transistor parameters used to build the divider. This effect will be demonstrated experimentally in section 4.4.4. Thus the static divider circuit block is useful for evaluating the performance of a particular technology for mm-wave applications and for comparing technologies. Furthermore, the SOF of a static divider can be quickly and easily measured, because no high-frequency inputs have to be applied.

In an effort to increase the self-oscillation frequency and thus the maximum frequency at which the divider can operate correctly, one can employ one or more of the available techniques that decrease the latch output time constants: inductive peaking [56], split-resistor loads [57], voltage swing reduction, capacitive peaking [58], etc. However, together with increasing the divider SOF, these techniques also cause the divider to depart from purely static behaviour. Thus, it will not divide from DC to $F_{\text{div,max}}$, but from a certain frequency $F_{\text{div,min}}$ up to $F_{\text{div,max}}$. To examine the above-mentioned effect in more detail, a sample static divider with latch schematic of Figure 4.2(a) was simulated with varying $R_L$ (the load resistor) and $L$ (the peaking inductor). All other parameters, such as the device sizes, the bias current, supply voltage, etc. are kept constant. In the first simulation (illustrated in Figure 4.3), the peaking inductor value is swept to find the maximum possible SOF for each load resistor (from 10 Ω to 100 Ω). In this simulation, the latch is designed with 4 mA of bias current. Since the swing needed to switch an HBT in this technology is 300 mV, $R_L$ must be 80 Ω for static operation. As can be seen from Figure 4.3, the SOF of the divider can be increased significantly (more than $\times 2$) beyond that of the static case. In a second simulation, the frequency range over which the divider operates correctly is examined at the $R_L$ and $L$ points indicated by the black dots of Figure 4.3. At each of these points the maximum and minimum input frequencies ($F_{\text{div,max}}$ and $F_{\text{div,min}}$) at which the divider operates correctly are recorded for an input power $P_{in} = 0$ dBm (sinusoidal input). The results are reproduced in Figure 4.4, and demonstrate the reduction in the operating frequency range of the divider with the increase of the self-oscillation frequency. In the extreme case, the static divider becomes an oscillator and starts behaving like an injection-locked divider.
4.2 Static Frequency Dividers

![Diagram of ECL Latch and CML Latch](image)

**Figure 4.2**: Commonly used latch schematics implemented with bipolar transistors

![Graph showing self-oscillation frequency variation](image)

**Figure 4.3**: Simulation of the self-oscillation frequency variation of a static divider with $R_L$ and $L$
4.2 Static Frequency Dividers

![Graph showing frequency dividers and related parameters]

**Figure 4.4:** Simulation of the divider bandwidth with $P_{in} = 0$ dBm at the $R_L$ and $L$ points indicated in Figure 4.3

![Schematic diagram of a latch]

(a) Relevant part of a latch schematic

![Waveforms at different frequencies]

(b) At the center of the divider bandwidth
(c) At the maximum divider frequency
(d) At the minimum divider frequency

**Figure 4.5:** Sample waveforms inside a static divider
4.3 Dynamic Frequency Dividers

Figure 4.5 gives an explanation for the limited divider operating frequency range when extensive bandwidth extension techniques are employed in the latches. Figure 4.5(a) illustrates part of a latch, showing the relevant nodes. Figure 4.5(b) gives the waveforms at these nodes in the center of the divider bandwidth, when all devices switch to the full swing. At higher frequency, close to $F_{\text{div, max}}$, the output node of the latch does not have enough time to charge to full swing and therefore cannot fully switch the next device and divider operation stops (Figure 4.5(c)). Figure 4.5(d) shows the same waveforms for the low frequency case, close to $F_{\text{div, min}}$. In this case, the latch output node switches faster then the clock. If the clock signal samples the data output when it is below the values required to switch the next latch, then the divider will not work correctly.

4.3. Dynamic Frequency Dividers

The general topology of a dynamic (or Miller [59]) frequency divider is shown in Figure 4.1(b). It is composed of a mixer with a low-pass filter connected in feedback. Dynamic dividers can be designed to operate up to a higher frequency and with lower power than static dividers. This is primarily because only one mixer is required, as opposed to two latches for a static divider [60, 61]. To date, dynamic dividers that work up to 150 GHz have been implemented in InP technology [62] and up 136 GHz in SiGe technology [60, 63]. A 160 GHz divide-by-four circuit has also been demonstrated [61], but divide-by-two circuits are still necessary for many applications. Recently, a 168 GHz dynamic divide-by-two divider operating from 4 V was demonstrated in a SiGe Technology [64].

The frequency range over which a dynamic divider can divide is determined mainly by the cut-off frequency of the low-pass filter, assuming that the mixer is ideal. With an input signal of frequency $f_{\text{IN}}$ and output with frequency $f_{\text{OUT}}$, the mixer produces tones at frequencies $f_{\text{IN}} \pm f_{\text{OUT}}$. After the filter only the lower frequency tone remains resulting in $f_{\text{IN}} - f_{\text{OUT}} = f_{\text{OUT}}$. Thus $f_{\text{OUT}} = f_{\text{IN}}/2$. Note that for the frequency $f_{\text{IN}}/2$ to originate and for the divider to work, the divider must oscillate. This oscillation is then locked by the input frequency and the mixer with feedback to form the right output frequency. Assuming that the cut-off frequency of the low-pass filter is $f_C$, the maximum output frequency of the divider is $f_{\text{OUT, max}} = f_C$. The minimum output frequency occurs when the low-pass filter starts passing through the high-frequency harmonic from the mixer, causing incorrect operation of the divider $f_C = f_{\text{OUT, min}} + f_{\text{IN}} = f_{\text{OUT, min}} + 2f_{\text{OUT, min}}$. Thus a dynamic divider operates correctly over a 3:1 frequency range.
4.4 Implementation of Static Dividers and Experimental Results

\[
\frac{f_C}{3} \leq f_{OUT} \leq f_C \quad (4.1)
\]

\[
\frac{2f_C}{3} \leq f_{IN} \leq 2f_C \quad (4.2)
\]

The design of a dynamic divider at mm-waves (in the F-band or D-band) starts by designing a mixer with an output time constant that is as small as possible. Also, no explicit low-pass filter is added, and the low-pass nature of the mixer itself is employed for the division operation. Any down-converter mixer topology can be used in the divider core. If the mixer does not have enough bandwidth for a certain divider frequency, then bandwidth extension techniques such as inductive peaking, Cherry-Hooper capacitive peaking, or other can be added to the mixer. However, these techniques might prevent the divider from operating over the entire 3:1 frequency range.

4.4. Implementation of Static Dividers and Experimental Results

4.4.1. Circuit Design

A study of static divider performance in two SiGe technologies was performed. For a fair comparison, the same divider topology, shown in Figure 4.6, was maintained and the same supply voltage was used. The single-ended input is converted to a differential signal through an on-chip transformer. A 50 Ω, 250 mV_{PP} swing buffer is used at the output. Two different latch configurations are implemented in the core of the divider for comparison.

A 1:1 transformer similar to that in [57] was scaled to 100 GHz and realized with vertically-stacked, symmetrical square coils in the top two metal layers of the technology. The transformer diameter is 30 µm, with 2 µm stripe width and 1 µm spacing. The coupling coefficient between the two coils is 0.855. The role of the transformer is solely to facilitate divider measurements and to avoid the use of expensive and bulky test setups. A matching network consisting of an inductor and a capacitor was added to match the divider input to 50 Ω. Simulation results of the transformer with matching network are reproduced in Figure 4.7. S_{21} peaks at 100 GHz, with a maximum value of -3.5 dB, while S_{11} remains below 10 dB from 30 GHz to 110 GHz. This marked the first demonstration of an integrated transformer in a circuit operating at 100 GHz.
4.4 Implementation of Static Dividers and Experimental Results

Figure 4.6: Static 2:1 frequency divider topology

Figure 4.7: Simulated on-chip transformer performance
Two different ECL latches, with and without emitter followers (EF) on the clock input path, shown in Figure 4.8(a) and 4.8(b), respectively, were designed. Notice that, apart from peaking inductors operating at 100 GHz, no bandwidth improvement techniques, such as split-resistor load [57] or double emitter-followers in the feedback [65], are employed. The use of inductors is critical to reduce power dissipation while still achieving high frequency operation. The first version, with double EF on the clock input path, operates from 3.3 V and consumes 19.5 mA. The second latch consumes only 11.5 mA from 3.3 V.

4.4.2. Fabrication

Die photos of the two dividers are shown in Figure 4.9. Both dividers were fabricated in two SiGe HBT technologies with exactly the same circuit layout and without redesign between the two technologies. The first technology is a 0.13 \( \mu \)m SiGe BiCMOS process (referred to as BiCMOS9 [66]). Only the BiCMOS9 HBTs, with an \( f_T \) of 170 GHz and \( f_{MAX} \) of 200 GHz, were utilized. The second technology (referred to as BipX [67]) features HBTs with an \( f_T \) of 230 GHz and \( f_{MAX} \) of 300 GHz. Measured \( f_T \) and \( f_{MAX} \) curves for the two technologies are plotted versus collector current density in Figure 4.10. Dividers were also fabricated and tested in two other BipX process splits with \( f_T / f_{MAX} \) in the 220 GHz to 270 GHz range.

4.4.3. Test Setup

The test setup used for divider characterization is shown in Figure 4.11. All measurements were performed directly on wafer with 110 GHz GGB probes. An HP 83752A 0.01-20 GHz signal source and Millitech AMC 15 00000 \( \times 4 \) and AMC 10 00000 \( \times 6 \) frequency multipliers were employed to generate the input signal in the 50-75 GHz and 75-100 GHz frequency bands, respectively. Below 50 GHz, measurements were carried out with the Agilent E8257D PSG analog 250 kHz-67 GHz signal generator as the signal source. A 50 GHz Agilent E4448A PSA with an Agilent 11970W 75-110 GHz waveguide mixer was used to observe the spectrum and phase noise of the input and output signals.

4.4.4. Measurement Results for Static Dividers

All fabricated dividers operate from 3.3 V and consume 122 mW without the clock EF, and 145 mW with the emitter followers on the clock input. Their sensitivity curves are plotted
Figure 4.8: Schematics of the two types of latches employed inside the divider
Figure 4.9: Die photographs of the fabricated dividers

Figure 4.10: Measured $f_T$ and $f_{MAX}$ at $V_{CE} = 1$ V on transistors with 3 emitter stripes, 6 base, and 4 collector contacts in the two technologies (BiCMOS9 and BipX)
in Figure 4.12. In both technologies, the elimination of the EF stages from the clock input path results in a 20% increase in the self-oscillation frequency (SOF). This is in agreement with simulations and with the reduced voltage gain of the EF at high frequency [68]. Figure 4.12 also shows that the SOF is correlated with the speed of the technology. By moving to a faster technology, the transistor $f_{\text{MAX}}$ is increased $\times 1.5$ from 200 GHz to 300 GHz, and the SOF of the dividers increases from 54 GHz to 77 GHz. The results on different BipX splits, with $f_T$ of 230 GHz and 265 GHz, reveal lower divider SOF for the 265 GHz $f_T$ circuits, in agreement with the HBT power gain at 65 GHz, rather than its $f_T$. Measurements also indicate that the maximum divider frequency tracks its SOF. Therefore, it is recommended that the self-oscillation frequency be used to more fairly compare the performance of static dividers because it depends solely on the circuit parameters. On the other hand, the maximum operating frequency of the divider depends to a large extent on the test setup and on the power available from the signal source.

The fastest divider has a SOF of 77 GHz. At the time of publication it was the highest reported SOF for a divider in any SiGe HBT/BiCMOS technology [52]. It divides correctly up to at least 100 GHz. The spectrum of the 50 GHz divided-by-two output signal is shown in Figure 4.13.

In order to assess the noise added by the divider, the phase noise of the 100 GHz multiplier output signal was measured as a function of the multiplier input power at 16.667 GHz (Fig-
Figure 4.12: Measured sensitivity curves of the 2 static dividers in the BiCMOS9 and BipX technologies

(a) The entire spectrum showing the 50 GHz divider output and its harmonics
(b) Zoomed-in spectrum showing the phase noise at the divider output at 50 GHz

Figure 4.13: Measured spectrum of the divide-by-two signal, with 100 GHz input, obtained from the BipX divider without EF
4.5 Implementation of a Dynamic Divider and Experimental Results

The measurement accuracy is limited by the external downconverter mixer noise floor for low-power inputs, and by the mixer non-linearity for high-power inputs. Figure 4.15 shows a phase noise of -96.4 dBc/Hz at 100 kHz offset from the 50 GHz divider output. For comparison, the measured phase noise at a 100 kHz offset from the 100 GHz divider input signal is -90.4 dBc/Hz (with 0.3 dBc/Hz measurement error). This proves that the divider noise contribution is negligible since the phase noise is improved by an ideal 6 dB after the divide-by-two operation. This is an important result for PLL applications, where the phase noise of the VCO must not be degraded by the divider. Lack of a signal source with sufficient output power prevented divider testing above 100 GHz. The same divider was tested over temperature and found to divide up to 97 GHz at 50 °C and up to 91 GHz at 100 °C, Figure 4.16.

4.5. Implementation of a Dynamic Divider and Experimental Results

This section describes the design of a dynamic divide-by-2 circuit in a 210 GHz-\(f_T\) SiGe technology that operates from 74 GHz up to at least 136 GHz.

4.5.1. Dynamic Frequency Divider Architecture

The dynamic divider chip (Figure 4.17) consists of an input stage, the Miller divider core, and a 50 Ω output buffer.

The schematic of the dynamic divider core is shown in Figure 4.18. It is composed of a mixer followed by a low-pass filter. To increase the frequency of operation of the divider, a Cherry-Hooper amplifier [69, 70] is inserted into the mixer. Due to the addition of the Cherry-Hooper stage, on some HBT devices \(V_{CE} = 2V_{BE}\). In this technology, the collector-to-emitter breakdown with open-base (\(BV_{CEO}\)) is approximately 2 V [71]. Furthermore, since in the circuit the devices are connected to a finite impedance, and do not have the base open, the \(BV_{CEO}\) is not the limiting factor on the device \(V_{CE}\) [72]. The divider input is biased by a resistor divider. Two sets of emitter-followers act as the filter and also shift the DC component of the signal from the mixer output down to the mixer input. The dynamic divider works from a -3.3 V supply and consumes 72.6 mW.

The on-chip input network consists of a transformer (described in section 3.2.3) that converts the single-ended input signal to a differential signal, and an inductor that tunes out the pad capacitance and matches the divider input to 50 Ω. A single-ended input signal is preferred.
Figure 4.14: Phase noise of a 100 GHz signal measured using two methods. This 100 GHz signal was used as the divider input.

(a) Phase noise at the 50 GHz output of the divider without emitter followers fabricated in BipX

(b) Phase noise of the 100 GHz input of the divider without emitter followers fabricated in BipX

Figure 4.15: Phase noise at the input and output of the divider without emitter followers fabricated in BipX at 100 GHz
4.5 Implementation of a Dynamic Divider and Experimental Results

**Figure 4.16:** Sensitivity curves across temperature for the divider without EF fabricated in the BipX technology

**Figure 4.17:** Top level schematic of the dynamic divider chip

**Figure 4.18:** Schematic of the divider core
to allow simpler testing of the divider; a single input requires fewer external components and
is beneficial for reducing overall system cost when the divider is employed as a component in
bigger systems or instrumentation. All signals inside the chip are differential.

Figure 4.19 presents the simulated transformer loss and the input and output match of the
entire divider chip. The transformer has less than 2 dB loss over the entire frequency range of
interest. The simulated $S_{11}$ of the divider with the input network is -6 to -7 dB from 80 GHz to
140 GHz.

The output buffer (Figure 4.20) consists of two stages. The first stage is designed with
lower current to reduce its load on the divider core. This enables the dynamic divider core
to work up to a higher frequency. The second stage is designed as a 50 $\Omega$ output driver. The
output buffer is broadband and produces a signal that is large enough to drive another divider.
It works up to 70 GHz in simulation and at least 68 GHz in measurements. The 2-stage output
buffer requires 46.2 mW and operates from -3.3 V.

4.5.2. Fabrication and Test Setup

The dynamic divider was fabricated in the IBM SiGe8HP technology [71] with transistor $f_T$
of 210 GHz and $f_{MAX}$ of 260 GHz. The chip microphotograph is illustrated in Figure 4.21(a)
with layout details shown in Figure 4.21(b). The transformer, divider core and the output buffer
occupy an area of 380 $\mu$m × 280 $\mu$m.

The dynamic divider was characterized on-wafer, using 3 different test setups for different
frequency ranges, as shown in Figure 4.22. An Anritsu 68177C signal source together with ×6
or ×8 multipliers (Oleson S10MS and S08MS) were employed to produce the input signal. The
output signal was observed using both an Agilent 86100B oscilloscope with 70 GHz remote
sampling heads and an Agilent E4448A PSA up to 51 GHz. Above 51 GHz (the limit of the
PSA) an external amplifier and an external divider were used to bring the output spectrum into
the PSA range. De-embedding of the input power was done with a 75-110 GHz power sensor.
Due to the unavailability of a higher frequency power sensor, all power measurements above
110 GHz are not calibrated.

4.5.3. Measurement Results

The divider sensitivity curve is given in Figure 4.23. The dynamic divider is functional from
74 GHz up to at least 136 GHz, limited by the available signal source power. This covers almost
the entire F-band (90-140 GHz). Over the entire operating frequency range, the divider requires
4.5 Implementation of a Dynamic Divider and Experimental Results

![Graph showing frequency (GHz) vs. (dB) with transformer S\textsubscript{21} and divider S\textsubscript{11} and S\textsubscript{22}](image)

**Figure 4.19**: Simulated transformer $S_{21}$ and divider $S_{11}$ and $S_{22}$

![Output buffer schematic diagram](image)

**Figure 4.20**: Output buffer schematic

(a) Microphotograph of the dynamic divider. The pad-limited die area is $1.78 \text{ mm} \times 0.63 \text{ mm}$, the circuit area is $380 \mu\text{m} \times 280 \mu\text{m}$

(b) Layout details of the dynamic divider

**Figure 4.21**: Chip layouts of the dynamic divider
Figure 4.22: Test setups employed for characterization of the divider in different frequency ranges (synchronization of instruments and DC connections not shown)
an input power less than 0 dBm, lower than in previously published work [61] in SiGe bipolar technology. This input power level can realistically be generated by a VCO. In Figure 4.23, the sensitivity curve for setup #3 is lower than the others because the divider bias was adjusted to be able to divide with the lower signal power provided by the ×8 multiplier. The measured input sensitivity above 110 GHz was performed with an uncalibrated power meter. When simulated with constant input power of -5.14 dBm, the divider was dividing properly from 80 GHz to 140 GHz.

Stable operation of the divider is demonstrated with the help of Figure 4.24 at 96.6 GHz, 124.8 GHz and 136 GHz. In Figure 4.24, the output signal is captured on the oscilloscope for several minutes showing that no phase-flipping occurs during that time. Figure 4.24 also demonstrates that the divider output buffer produces over 100 mV swing in 50 Ω up to 68 GHz, enough to drive a second divider stage or other circuits.

Figure 4.25 shows two divider output spectra with 102 GHz and 131.2 GHz inputs. In the second case the shown spectrum is after an external amplifier and divide-by-2 (setup #3). For both inputs, there are no harmonics visible in the output signal. In Figure 4.26, the phase noise at the divider output with 102 GHz input and that of the 17 GHz signal source are shown. The phase noise at the divider output is -96 dBc/Hz at 100 kHz offset from 51 GHz. The phase noise at the signal source output is -107.3 dBc/Hz at 100 kHz offset. The 11.3 dB difference is close to the ideal 9 dB phase noise difference resulting from the ×3 shift in the carrier frequency. The 2.3 dB phase noise difference can result from either the frequency multiplier at the input, or from the divider under test. Figure 4.27 shows the divider output phase noise with 131.2 GHz input, after a further division by 2 and the 16.4 GHz signal source phase noise. Again, the difference between the output phase noise (-100.2 dBc/Hz at 100 kHz offset) and the source phase noise (-107 dBc/Hz at 100 kHz offset) is less than 1 dB (after accounting for a 6 dB shift in frequency), and can be attributed to measurement error, or to any of the instruments in the test setup.

4.6. Low-Power MM-Wave Divider Topologies

In previous sections, the design of frequency dividers operating from 3.3 V supplies was described. To reduce power consumption, circuit operation from a lower supply is helpful. Also, in larger systems, a 3.3 V power supply is not always available. This is especially true in BiCMOS technologies, where it is beneficial to operate the entire chip from a CMOS-compatible power supply, such as 1.2 V. This section presents two low-power divider designs operating at
Figure 4.23: Measured input sensitivity of the dynamic divider over frequency. Above 110 GHz (shaded area), the power measurements are not calibrated. Division was achieved at 136 GHz with the highest output power available from the signal source. The source could not provide enough power at higher frequency.

Figure 4.24: Measured single-ended output signal from the divider accumulated for several minutes.
Figure 4.25: Measured output spectra of the dynamic divider showing no harmonics at the output

(a) Output spectrum with 102 GHz input
(b) Output spectrum with 131.2 GHz input, after a further division by 2

Figure 4.26: Measured phase noise contribution of the divider with 102 GHz input

(a) Phase noise at the divider output at 51 GHz
(b) Phase noise of the signal source at 17 GHz

Figure 4.27: Measured phase noise contribution of the divider with 131.2 GHz input

(a) Phase noise at the dynamic divider output at 32.8 GHz including the external amplifier and divider
(b) Phase noise of the signal source at 16.4 GHz
4.6 Low-Power MM-Wave Divider Topologies

mm-wave frequencies. Low-power operation is achieved by first, “AC-folding” to reduce the supply voltage and second, by optimizing the current consumption.

The schematic of a low-power dynamic divider is illustrated in Figure 4.28(a). As was the case with the divider described in Section 4.5, the low-power dynamic divider also has an input biasing/matching circuit, a mixer core, and a low-pass filter part. However, in the low-power configuration, all the divider parts are AC-coupled using transformers. With the transformers, only one active transistor is stacked between the supply and ground, thus reducing the supply voltage to 1.5 V. Compared to AC-coupling with capacitors, the transformers facilitate biasing the three divider parts by connecting the bias currents to the transformer centre-taps. Transformers T2 and T3 in this divider are designed to have the lowest loss possible in this technology. Since the transformers are in the signal path, their loss and bandwidth directly affects the divider bandwidth. The transformers’ design and geometry are described in Section 3.2.4. “AC-folding” increases the number of bias currents required for the circuit. Therefore, in this design transistor sizes and bias currents were selected to minimize the total power consumption while still biasing at the peak-\( f_T \) current density. The total power consumption for the dynamic divider core is 32 mW.

A low-power static divider was also designed. The latch schematic employed in the static divider is shown in Figure 4.28(b). Here, a transformer is inserted between the input clock differential pair and the output quad, allowing to reduce the supply voltage to 1.2 V at the expense of doubling the bias current. The same transformer (described in Section 3.2.4) was also employed in the static divider latches. Due to the use of transformers, the divider is no longer truly static, and its bandwidth is reduced. The static divider core (consisting of two

![Schematic of a low-voltage dynamic divider](image1)

![Schematic of a low-voltage static divider latch](image2)

**Figure 4.28:** Low-voltage divider topologies
4.6 Low-Power MM-Wave Divider Topologies

![Die photo of a low-voltage dynamic divider breakout](image1)

![Die photo of a low-voltage static divider breakout](image2)

Figure 4.29: Die photos of the low-voltage dividers implemented in the BiCMOS9MW technology

The design of the low-power static and dynamic dividers starts by designing dividers with a conventional schematic, without the transformer AC-coupling. This design is optimized to be robust at the desired frequency of operation, 120 GHz in this case. Then transformers with the lowest possible loss (highest coupling) around the frequency of operation are designed in the given backend. If the transformer loss is too high, the gain in the divider loop will be too low to regenerate the signal and it will stop working. These transformers are then inserted into the dividers as shown in the schematics of Figure 4.28. Biasing currents through transformer center taps are adjusted using resistors to be the same as the bias currents in the non-AC-coupled case.

Both the dynamic and the static low-voltage divider breakouts were fabricated in the STMicroelectronics’ BiCMOS9MW technology [73]. Their die photos are illustrated in Figure 4.29. The dividers were characterized on-chip in a test setup similar to that described in Section 4.4.3 and Section 4.5.2. The measured sensitivity curves for both dividers are plotted in Figure 4.30. The static divider works from 79 GHz up to 109 GHz, the dynamic divider is operational in the 112-122 GHz frequency range. For both dividers, the maximum division frequency is limited by the power available from the signal source. At the time of writing, these are the lowest power static and dynamic dividers operating above 100 GHz in any SiGe technology. This is also illustrated in Table 4.2, where it is shown that the static and dynamic dividers of this section consume significantly less power than the other previously published dividers.
4.7 Summary

Static and dynamic divide-by-two stages were discussed in this chapter. This chapter described methods of increasing the frequency of operation of the dividers while not sacrificing their performance. Measured circuit examples were employed to prove the concepts. Low-power versions of static and dynamic dividers where only one transistor is stacked between the supply and ground were also described.
Oscillators are one of the main blocks in any wireless system. They are also essential in all frequency generation circuits. In this chapter, a topology for quadrature voltage-controlled oscillators is proposed. These oscillators are employed for generating 160 GHz signals in the transceivers of Chapter 7.

The chapter starts by presenting the concept behind the quadrature voltage-controlled oscillators. Then, circuit examples for VCOs are given at 80/160 GHz in SiGe and at 90 GHz in a 65 nm CMOS technology. In the end of the chapter techniques and examples of low-power 120 GHz VCOs are presented.

5.1. Quadrature Voltage-Controlled Oscillators

In this work, I have employed a quadrature oscillator to demonstrate that such a topology simplifies the LO distribution in transceiver arrays. However, it should be noted that in the transceiver topologies discussed here, the quadrature phase relationship between the two 80 GHz differential outputs of the oscillator is not critical for correct transceiver operation. In the past, quadruple-push oscillators were designed for the purpose of efficiently generating a fourth harmonic signal [74] using delay lines. By far the most common quadrature oscillator topology consists of two inter-locked cross-coupled LC oscillators [75]. However, experimental data have shown that differential Colpitts oscillators exhibit superior performance in terms of phase noise, tuning range, temperature stability, and operation at mm-wave frequencies [76–78]. To date, quadrature Colpitts oscillators have been implemented by injection locking two differential oscillators [79, 80], as opposed to a quadruple-push oscillator, and at lower frequency than the oscillator presented here.

Taking advantage of the Colpitts topology, and expanding on a 3-push oscillator concept [81], the quadrature oscillator topology illustrated in Figure 5.1 is proposed. It consists of two coupled differential Colpitts oscillators. In each differential oscillator, a common-mode
resistor $R_{\text{Diff}}$ ensures that its two outputs are $180^\circ$ out of phase [82]. By a similar approach, resistor $R_{\text{Quad}}$, common to both differential oscillators, i.e. shared by all four Colpitts sub-oscillators, will help to establish $90^\circ$ phase difference between the two differential halves of the quadrature oscillator. The common-mode resistors, along with the star-connection of the tank inductors at node $P$, ensure that the four oscillator outputs can be locked in quadrature, as will be shown next. The proposed oscillator can be analysed using modal analysis by extending the theory previously developed for push-push and triple-push oscillators [81, 83], and power amplifiers [84], to a quadruple-push oscillator. Note that, in this chapter the terms “even mode” and “common mode” are used interchangeably to mean the same thing. Similarly, “odd mode” and “differential mode” refer to the same circuit condition.

To start the analysis, the oscillator is represented as the four-port circuit of Figure 5.2(a). Each of the four Colpitts circuits, including their common-mode resistors, is modelled as a separate sub-oscillator. All four sub-oscillators are coupled with a network that consists of transmission lines and a load resistor $R_L$. The voltage, current, and impedance phasors of the 4-push oscillator topology are related by the following matrix equation: $[Z][I] = [V]$. Taking into account the symmetries that exist in the circuit, i.e. $Z_{ij} = Z_{ji}$ for $i, j = 1,4$ and $Z_{12} = Z_{14} = Z_{23} = Z_{34}$, $Z_{13} = Z_{24}$, the matrix equation can be recast as:

$$
\begin{bmatrix}
Z_{11} & Z_{12} & Z_{13} & Z_{12} \\
Z_{12} & Z_{11} & Z_{12} & Z_{13} \\
Z_{13} & Z_{12} & Z_{11} & Z_{12} \\
Z_{12} & Z_{13} & Z_{12} & Z_{11}
\end{bmatrix}
\begin{bmatrix}
I_1 \\
I_2 \\
I_3 \\
I_4
\end{bmatrix}
=
\begin{bmatrix}
V_1 \\
V_2 \\
V_3 \\
V_4
\end{bmatrix}
$$

(5.1)

The eigenvectors and eigenvalues of (5.1) represent all the oscillation modes of the circuit. The eigenvalues and eigenvectors obtained by solving (5.1) are given in Table 5.1. In each oscillation mode (i.e. even, odd, or quadrature), the phases and relative amplitudes of the
5.1 Quadrature Voltage-Controlled Oscillators

signals produced by the sub-oscillators are represented by the elements of the eigenvector that describes that mode. For example, the values of $I_1 = 1$ and $I_2 = -1$ in the odd mode, illustrate that sub-oscillators 1 and 2 produce signals of equal amplitude which are 180° out of phase. The impedance seen at the ports of the oscillator in a particular mode is given by the eigenvalue corresponding to that mode.

The quadrature oscillation mode is described by two eigenvectors which satisfy the equation $I_1 + I_2 + I_3 + I_4 = 0$ and, at the same time, comply with the symmetry of the circuit. The symmetry requires having equal-amplitude oscillations in all four sub-circuits. The two eigenvectors are

<table>
<thead>
<tr>
<th>Mode</th>
<th>Eigenvector</th>
<th>Eigenvalue</th>
</tr>
</thead>
<tbody>
<tr>
<td>Even</td>
<td>$\begin{bmatrix} I_1 \ I_2 \ I_3 \ I_4 \end{bmatrix} = \begin{bmatrix} 1 \ 1 \ 1 \end{bmatrix}$</td>
<td>$Z_e = Z_{11} + 2Z_{12} + Z_{13}$</td>
</tr>
<tr>
<td>Odd</td>
<td>$\begin{bmatrix} I_1 \ I_2 \ I_3 \ I_4 \end{bmatrix} = \begin{bmatrix} 1 \ -1 \ 1 \end{bmatrix}$</td>
<td>$Z_o = Z_{11} - 2Z_{12} + Z_{13}$</td>
</tr>
<tr>
<td>Quadrature</td>
<td>$I_1 + I_2 + I_3 + I_4 = 0$</td>
<td>$Z_q = Z_{11} - Z_{13}$ (double root)</td>
</tr>
</tbody>
</table>
5.1 Quadrature Voltage-Controlled Oscillators

\[
\begin{bmatrix}
I_1 \\
I_2 \\
I_3 \\
I_4
\end{bmatrix} = \begin{bmatrix}
1 \\
e^{j\frac{\pi}{2}} \\
e^{j\pi} \\
e^{j\frac{3\pi}{2}}
\end{bmatrix}, \quad \begin{bmatrix}
I_1 \\
I_2 \\
I_3 \\
I_4
\end{bmatrix} = \begin{bmatrix}
1 \\
e^{-j\frac{\pi}{2}} \\
e^{-j\pi} \\
e^{-j\frac{3\pi}{2}}
\end{bmatrix}
\]

(5.2)

To establish correct circuit operation, the even- and odd-mode oscillations must be suppressed and the quadrature oscillation mode must be amplified. The conditions for quadrature oscillation can be derived by inspecting any of the quarter-circuits separately. In Figure 5.2(b) the quarter-oscillator is modelled as a single-port. Looking to the left, the impedance \(Z_D\) of the negative resistance device appears in series with \(R_E\), which represents the combination of \(R_{\text{Diff}}\) and \(R_{\text{Quad}}\), shown earlier in Figure 5.1. To the right, one sees \(Z_T\), which represents the oscillator tank, in series with the load \(R_L\).

The single-port sub-oscillator schematic of Figure 5.2(b) is redrawn for each of the oscillation modes in Figure 5.3, indicating the values of the various common-mode resistors seen in each case. Note that both nodes \(Q\) and \(P\) are common to all four sub-oscillators. In the quadrature oscillation mode, \(R_E = R_L = 0\) because nodes \(Q\) and \(P\) appear as virtual grounds. In the odd mode of oscillation, \(R_E = 2R_{\text{Quad}}\) and \(R_L = 2R\), because the resistors \(R_{\text{Diff}}\) cancel in differential mode. Since two waveforms add in phase across \(R_{\text{Quad}}\) and across \(R_L\) their values double in the odd mode of oscillation. Similarly, in the even oscillation mode, where all sub-oscillators are in phase, the common-mode resistors at nodes \(Q\) and \(P\) become \(R_E = 4R_{\text{Quad}} + 2R_{\text{Diff}}\) and \(R_L = 4R\), respectively.

By writing the conditions for suppressing even- and odd-mode, and enhancing the quadrature-mode oscillations, and after substituting the impedances from Figure 5.3, the following equations are obtained:

Even mode:

\[
\Re \{Z_{eD} + Z_{eT}\} > 0 \\
\Re \{-R_D + jX_D + 4R_{\text{Quad}} + 2R_{\text{Diff}} + R_T + jX_T + 4R\} > 0 \\
- R_D + 4R_{\text{Quad}} + 2R_{\text{Diff}} + R_T + 4R > 0
\]

(5.3)
5.1 Quadrature Voltage-Controlled Oscillators

![Equivalent circuit models for each oscillator mode](image)

**Figure 5.3:** Equivalent circuit models for each oscillator mode

Odd mode:

\[
\Re \{ Z_{oD} + Z_{oT} \} > 0
\]
\[
\Re \{ -R_D + jX_D + 2R_{Quad} + R_T + jX_T + 2R \} > 0
\]
\[
-R_D + 2R_{Quad} + R_T + 2R > 0
\] (5.4)

Quadrature mode:

\[
\Re \{ Z_{qD} + Z_{qT} \} < 0
\]
\[
\Re \{ -R_D + jX_D + R_T + jX_T \} < 0
\]
\[
-R_D + R_T < 0
\] (5.5)

\[
\Im \{ Z_{qD} + Z_{qT} \} = 0
\]
\[
\Im \{ -R_D + jX_D + R_T + jX_T \} = 0
\]
\[
jX_D + jX_T = 0
\] (5.6)

Finally, (5.7) describes the quadrature oscillation condition and is obtained from inequalities (5.3), (5.4), and (5.5) and from equation (5.6), where \(-R_D\) is the negative resistance of the active device.
\[ R_T < |−R_D| < R_T + 2R + 2R_{\text{Quad}} \] (5.7)

\[ jX_D + jX_T = 0 \]

It should be noted that, although the roles of \( R_{\text{Diff}} \) and \( R_{\text{Quad}} \) are not immediately apparent from the model of Figure 5.2(a), they are critical in determining the phases of the oscillator outputs in a circuit implementation. Since the order of the entries of the quadrature-mode eigenvectors of (5.2) can be interchanged without affecting the solution, \( R_{\text{Diff}} \) and \( R_{\text{Quad}} \) are responsible for establishing the exact phase relationships of the four outputs (i.e. which output is \( 0^\circ \), which is \( 90^\circ \), etc.). Furthermore, \( R_{\text{Diff}} \) and \( R_{\text{Quad}} \) help with suppressing the odd and even oscillation modes by significantly degrading the \( Q \) of the capacitor \( C_2 \) in Figures 5.3(a) and 5.3(b).

### 5.2. An 80/160 GHz Quadrature Oscillator in SiGe HBT Technology

Based on the concepts described above, the oscillator shown in Figure 5.4 was designed for quadrature operation at a fundamental frequency of 80 GHz. Since AMOS varactors were not available in this technology, the oscillator was designed to operate at a constant frequency. However, more recent work in CMOS [78] and SiGe BiCMOS [85] illustrates that it is straightforward to extend this oscillator to a voltage-tunable version. In this design, the load resistor \( R_L \) (of Figure 5.2(a)), where the fourth-harmonic signal is produced, is implemented with the bias resistors \( R_{B1} \) and \( R_{B2} \). Cascode transistors are employed to adequately isolate the quadrature outputs from the tank. They also allow combining the two differential 80 GHz signals into two second-harmonic signals at 160 GHz that are \( 180^\circ \) out of phase.

All transistors in the oscillator are biased at the peak-\( f_T \) current density of \( 14\ \text{mA/mm}^2 \) to obtain the maximum output swing. Particular attention was paid to the symmetry of the oscillator layout, both for differential and for quadrature signals, as is illustrated in Figure 5.5. A high-Q inductor (described in Section 3.1) was designed for the oscillator tank to achieve better phase noise.

The measured signals from the oscillator at the 80 and 160 GHz outputs are shown in Figure 5.6. At 84 GHz, the oscillator achieves a phase noise of -110.4 dBC/Hz at 10 MHz offset (Figure 5.6(a)). This phase-noise measurement is pessimistic because the low-noise power supply that was employed to power up the oscillator could supply only 60 mA whereas the oscillator required 70 mA for proper operation. At the 160 GHz output of the oscillator phase...
5.2 An 80/160 GHz Quadrature Oscillator in SiGe HBT Technology

Figure 5.4: Quadrature oscillator schematic

Figure 5.5: Layout detail of the 80/160 GHz quadrature oscillator implemented in SiGe HBT technology.
noise could not be measured due to higher noise and worse sensitivity of the test setup at this frequency. Figure 5.6(b) reproduces the oscillator signal at 164.5 GHz without de-embedding the setup losses.

The oscillator operates from 3.3 V, and consumes a total of 70 mA. To the best of my knowledge, this is the first quadrature oscillator at 80 GHz and the first differential oscillator at 160 GHz designed in a SiGe HBT technology.

5.3. A 90 GHz Quadrature VCO in 65 nm CMOS Technology

Building on the concepts described previously, a fundamental-frequency quadrature VCO was designed at 90 GHz in 65 nm CMOS technology. The schematic of the VCO is shown in Figure 5.7. The purpose of this VCO was to generate the LO signal in a receiver and to simultaneously drive both the mixer and a frequency divider circuit. Thus, both low noise and high output power are required from this VCO. To minimize the phase noise, a Colpitts topology is selected to implement the VCO [76]. Output buffers are added to increase the output power and to isolate the VCO core from its load.

As illustrated in Figure 5.7, the differentially tuned VCO is composed of four symmetrically coupled Colpitts oscillators. An RC filter is used in the VCO bias network to minimize the injection of supply noise, and thus prevent the degradation of the VCO phase noise. Four buffers, also shown in Figure 5.7, are used to increase the output power of the VCO, and to differentially drive the mixer on one side, and the divider on the opposite side. Each of the VCO buffers is implemented as a single-stage common-source amplifier, which is matched to 50Ω at the output. A differential buffer topology with common-mode current source is avoided in order to suppress common-mode instabilities and to maximize the gain.

The VCO was fabricated as a separate test structure and also together with the frequency divider, as can be seen in Figure 5.8. The VCO and static frequency divider operate from a nominal supply of 1.2V.

Figure 5.9 shows the tuning range and output power of the quadrature VCO over temperature, measured on a breakout of the VCO, which includes all buffers and the divider. The VCO can be tuned from 88.2 GHz to 91.2 GHz, irrespective of temperature. The tuning range remains constant over a wide range of temperatures thanks to the Colpitts topology, the use of lumped inductors, MOM capacitor $C_1$, and accumulation-mode MOS varactors, whose inductance and capacitance depend mostly on the metallization characteristics and dielectric permittivity, which hardly vary over temperature. The total output power of the VCO with four buffers is +2 dBm to +3 dBm in 50Ω at 25°C.
5.3 A 90 GHz Quadrature VCO in 65 nm CMOS Technology

(a) Oscillator phase noise (-110.4 dBc/Hz at 10 MHz offset) measured at the 80 GHz output.

(b) Oscillator signal measured at the 160 GHz output.

**Figure 5.6:** Oscillator signals at 80 GHz and 160 GHz.

---

**Figure 5.7:** Schematic of the 90 GHz VCO and buffers designed in 65 nm CMOS technology.
Figure 5.8: Layout of the 90 GHz CMOS VCO with buffers and divider

Figure 5.9: Measured tuning range and total output power of the 90 GHz CMOS VCO over temperature
To estimate the VCO tuning range in simulation, one can use (5.8), which is based on the VCO model in Figure 5.10, to calculate the frequency. After the parameters of Table 5.2 are plugged into (5.8), the calculated tuning range is from 96.7 GHz to 101 GHz. This is within 10% of the measured value, confirming that hand analysis can be quite accurate in predicting the VCO frequency provided all the passive component values are known. Table 5.3 summarises the VCO frequency obtained by hand-calculation and from simulations with and without parasitic extraction. Simulation with extraction gives the most accurate results.

$$\frac{1}{f_{OSC}} = 2\pi \sqrt{L \left( C_{GD} + \frac{C_{1} + C_{GS}}{(C_{1} + C_{GS}) + (2C_{VAR} + C_{SB} + C_{B} + C_{L})} \right)}$$

(5.8)

Figure 5.11 reproduces the measured phase noise using two different techniques. The VCO achieves a phase noise that is better than -95 dBc/Hz at 1 MHz offset from the 90.3 GHz carrier. The phase noise of this VCO was not measured over temperature.

To verify that the designed VCO can drive a static divider over its entire tuning range, the

**Table 5.2:** Measured component values for calculation of VCO frequency.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>32</td>
<td>pH</td>
</tr>
<tr>
<td>$C_1$</td>
<td>60</td>
<td>fF</td>
</tr>
<tr>
<td>NFET size</td>
<td>$72 \times 0.8 \mu m \times 60 \text{nm}$</td>
<td></td>
</tr>
<tr>
<td>NFET $C'_{GS}$</td>
<td>0.75</td>
<td>fF/$\mu$m</td>
</tr>
<tr>
<td>NFET $C'_{GD}$</td>
<td>0.4</td>
<td>fF/$\mu$m</td>
</tr>
<tr>
<td>NFET $C'_{SB}$</td>
<td>0.65</td>
<td>fF/$\mu$m</td>
</tr>
<tr>
<td>Varactor size</td>
<td>$34 \times 0.8 \mu m \times 60 \text{nm}$</td>
<td></td>
</tr>
<tr>
<td>Varactor $C'_{VAR}$</td>
<td>24→41</td>
<td>fF</td>
</tr>
<tr>
<td>Varactor $C'_{B}$</td>
<td>0.7</td>
<td>fF/$\mu$m</td>
</tr>
<tr>
<td>Varactor $C_L$</td>
<td>3</td>
<td>fF</td>
</tr>
</tbody>
</table>
Table 5.3: Estimation of VCO frequency.

<table>
<thead>
<tr>
<th></th>
<th>Upper Limit</th>
<th>Lower Limit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hand Analysis</td>
<td>101 GHz</td>
<td>96.7 GHz</td>
</tr>
<tr>
<td>Simulated (without extraction)</td>
<td>107.2 GHz</td>
<td>100.2 GHz</td>
</tr>
<tr>
<td>Simulated (with extraction)</td>
<td>91.5 GHz</td>
<td>88.4 GHz</td>
</tr>
<tr>
<td>Measured</td>
<td>91.2 GHz</td>
<td>88.2 GHz</td>
</tr>
</tbody>
</table>

(a) Measured using zoom-in and averaging
(b) Measured using the Phase-Noise utility of the spectrum analyzer

Figure 5.11: Measured phase noise of the 90 GHz CMOS VCO

Figure 5.12: Divider operation over the VCO tuning range
output of the divider was observed while changing the VCO control voltages. As shown in Figure 5.12, the divider works over the entire VCO tuning range at 25 °C. However, at 50 °C, the divider is not sensitive enough (or the VCO does not have enough output power) to work over the entire VCO tuning range. This result is consistent with a measurement of the divider by itself, which worked up to 90 GHz [1].

5.4. Low-Power MM-Wave VCO Topologies

The bipolar VCO described in this chapter (section 5.2) consumed significantly more power than the CMOS VCO (section 5.3) primarily because of the requirement for 3.3 V or higher power supply for biasing bipolar cascodes. In this section two bipolar VCO topologies that operate from a 1.8 V supply will be shown. Both VCOs are differential, designed to oscillate at 120GHz and differ in the tank configuration.

The first one is an Armstrong VCO (Figure 5.13(a)), where the tank is composed of a transformer and varactors for frequency tuning. The second VCO has a Colpitts configuration (Figure 5.13(b)) with the tank consisting of an inductor and varactors. The benefit of the Colpitts VCO is its stable output power over the oscillation frequency range. However, with a low supply voltage, the Colpitts VCO is hard to control with a charge-pump inside a PLL because the common-mode voltage of the varactors is equal to the voltage at the emitters, which is close to ground and does not allow to fully swing the varactors above and below the common mode. In the case of the Armstrong VCO, the varactors are connected at the base node, which is close to the centre between the supply and ground, making it more compatible for control with a charge-pump. At the same time however, the output power of the Armstrong VCO can vary by as much as 10 dB over the oscillation frequency range, thus requiring significant buffering when integrated in a system.

Both the Armstrong and the Colpitts VCOs of Figure 5.13 were fabricated in STMicroelectronics’ BiCMOS9MW technology [73]. Their die photos are shown in Figure 5.14. The VCOs were characterized on wafer, in a D-band test setup. The measured results for frequency tuning, output power and phase noise are reproduced in Figure 5.15 for both VCOs and their performance is summarized in Table 5.4.

The Armstrong VCO (Figure 5.15(a)) is tunable over 4 GHz from 107 GHz to 111 GHz. Its output power varies from +1 dBm to +5 dBm into 50 Ω. It achieves a phase noise of -104 dBc/Hz at 1 MHz offset. The Colpitts VCO oscillates at a higher frequency, from 119.5 GHz to 123 GHz, has a larger output power of +3 dBm to +7 dBm into 50 Ω, and achieves record-
5.4 Low-Power MM-Wave VCO Topologies

(a) Low-power 110 GHz Armstrong VCO schematic  (b) Low-power 120 GHz Colpitts VCO schematic

Figure 5.13: Low-power VCO schematics

(a) Die photo of the low-power 110 GHz Armstrong VCO designed in BiCMOS9MW technology
(b) Die photo of the low-power 120 GHz Colpitts VCO designed in BiCMOS9MW technology

Figure 5.14: Die photographs of the VCO breakouts

Table 5.4: Low-power Armstrong and Colpitts VCO performance summary.

<table>
<thead>
<tr>
<th></th>
<th>Armstrong VCO</th>
<th>Colpitts VCO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Consumption</td>
<td>36 mW</td>
<td>72 mW</td>
</tr>
<tr>
<td>Oscillation Frequency</td>
<td>107 - 111.2 GHz</td>
<td>119.5 - 123 GHz</td>
</tr>
<tr>
<td>Output Power (in 50 Ω)</td>
<td>+1 to +5 dBm</td>
<td>+3 to +7 dBm</td>
</tr>
<tr>
<td>Phase Noise (at 1 MHz offset)</td>
<td>-104 dBc/Hz</td>
<td>-112 dBc/Hz</td>
</tr>
</tbody>
</table>
low (at the time of writing) phase noise of -112 dBc/Hz at 1 MHz offset. The best phase noise results of the Armstrong and Colpitts VCOs are reproduced in Figure 5.16.

5.5. Summary

In this chapter, a topology for quadrature voltage-controlled oscillators is proposed. This oscillator topology is useful for 160 GHz LO signal generation and distribution in the transceivers of Chapter 7. Circuit examples for VCOs are given at 80/160 GHz in SiGe and at 90 GHz in a 65 nm CMOS technology. Techniques and examples of low-power 120 GHz VCOs are also presented.
5.5 Summary

Figure 5.15: Measured results for the Armstrong and Colpitts VCOs

Figure 5.16: Measured phase noise spectra of the Armstrong and Colpitts VCOs with 100 averages.
D-Band Amplifiers

The subject of this chapter is the design of D-band (110 GHz to 170 GHz) tuned amplifiers. Amplification stages are employed in most radio and radar systems to combat losses and signal attenuation, reduce system noise figure, and increase output power. This chapter starts by providing the amplifier design procedure and hand-analysis equations for gain. Then, several amplifier designs at 140 GHz and 170 GHz are presented. The chapter finishes with a description of a 20 dB gain 160 GHz amplifier with built-in amplitude modulation that works up to 4 Gb/s.

6.1. Design of 140-180 GHz Amplifiers

Amplification of signals is necessary in several places in a transceiver or a radar system. To increase the sensitivity of the system, the received signal must be amplified with minimal noise and distortion before it can be processed. In the transmitter, the output signal needs to be boosted to increase the output power and thus improve the link margin over larger distances. Gain stages are also required in the LO signal distribution path at mm-wave frequencies to drive the mixers.

Amplification, however, is not easily achievable at mm-wave frequencies. At 160 GHz for example, a common-emitter (CE) stage in the BiCMOS9MW technology has a maximum available power gain (MAG) of 2-3 dB, while a cascode stage has a MAG of 4-5 dB. Thus, to build an amplifier with a gain of 15-20 dB, at least 4 stages are required. Furthermore, conjugate matching must be employed between stages to maximize the power transfer from the input to the output. In the case of high-output power stages, it is preferable to have CE stages to allow for larger signal swings, save DC power, and increase power added efficiency (PAE). PAE is defined as the ratio of the RF output power from an amplifier to the total power put into it.
For the transceiver system that will be described in Chapter 7, a 5-stage amplifier was designed with the schematic of Figure 6.1. The amplifier design begins at the last stage and steps backwards towards the input. The bias current and size of transistors in each stage are progressively scaled (increased) from the input to the output. Interstage matching is employed to maximize the power gain. The last two stages of the amplifier employ a common-emitter topology for higher output power, while the first three stages are implemented with cascodes to obtain larger gain. Each of the inductors shown in the amplifier schematic was simulated in ASITIC and its corresponding 2-π equivalent circuit was extracted from the simulated Y-parameters.

The last stage consists of a CE transistor biased at 30 mA to obtain a +2 dBm (0.8 V\textsubscript{PP}) signal in a 50 Ω load. Due to the large current that has to flow through this device and its metallization, it was implemented as two transistors connected in parallel, each with an emitter length of 7.5 μm. The pieces of interconnect leading to the parallel-connected devices are shown in the schematic as 5.18 pH inductors. The load of the 5\textsuperscript{th} stage is split in two to provide space in the layout for the load and for the output matching network. The last stage has an input impedance of 7Ω – j2.2Ω, which is conjugately matched to the output of the fourth stage. It, too, uses a CE transistor with inductive load, whose emitter length and bias current are scaled down by a factor of 2 compared to the last stage, and presents an impedance of 13Ω – j4.3Ω to the third stage.

In each cascode stage the output matching network consists of series and shunt inductors, and a series capacitor. The analysis and design of each of the amplifier stages can be carried out either in the traditional microwave way with the Smith Chart [41], or analytically, employing a lumped high-frequency equivalent circuit for the transistor, which includes the parasitic emitter and base resistances \(R_E\) and \(R_B\).

The first approach that uses the Smith Chart is illustrated graphically in Figure 6.2. In Figure 6.2(a) the output impedance of the common-base transistor of a cascode stage in the

![Figure 6.1: Detailed schematic of the 140 GHz amplifier (biasing not shown)](image-url)
amplifier is indicated by point $A$ on the Smith chart. The series inductor connected to output moves the impedance to point $B$. Then, the shunt inductor first reflects point $B$ to $B'$ and then brings the impedance to point $C$ on the $1 + jx$ circle. Finally, a series capacitor is employed to cancel the remaining imaginary part and to complete the match at point $D$. Input matching, illustrated in Figure 6.2(b), is accomplished with inductive degeneration and a series inductor at the base. Inductive degeneration is used to transform the impedance from point $A$ to point $B$, which is located on the $1 + jx$ circle. Then, a series base inductor brings the impedance to point $C$ at the centre of the Smith chart. The inductors were restricted to small values to ensure high self-resonance frequencies. The interstage matching capacitors that are smaller than 27 fF (The smallest value allowed by the design kit pcell) were implemented with two MiM capacitors in series.

For the second, analytical analysis approach, one has to start with the simplified high-frequency equivalent circuit of the transistor that includes the parasitic emitter and base resistances $R_E$ and $R_B$. To improve the accuracy of this simplified equivalent circuit at mm-wave frequencies, we rely on the measured or simulated effective cutoff frequency, $f_{T,\text{eff}}$, and transconductance, $g_{m,\text{eff}}$, where

$$f_{T,\text{eff}} = \frac{f_T}{1 + g_m R_E}; \quad g_{m,\text{eff}} = \frac{g_m}{1 + g_m R_E} \tag{6.1}$$

Note that in Figure 6.3(a) and 6.3(b), the input capacitance of the transistor or of the cascode stage are described by $g_{m,\text{eff}}/f_{T,\text{eff}}$, and includes the Miller effect. The reverse isolation is not captured by this circuit. However, it remains very low because $C_{bc}/C_{\pi} < 10$. In this case, the input impedance and current gain are given in (6.2) and (6.3).
(a) Transistor small-signal model.

(b) Transistor small-signal model with inductive degeneration.

(c) Small-signal model of an amplifier stage.

(d) Impedance transformation using split inductor load.

Figure 6.3: Small-signal modelling of an amplifier stage

\[ Z_{in} = R_B + R_E + \frac{\omega_{T,eff}}{j\omega g_{m,eff}} \]  \hspace{1cm} (6.2)

\[ A_I = \frac{i_{sc}}{i_{in}} = -\frac{f_T}{jf} \]  \hspace{1cm} (6.3)

When inductive degeneration is used, as in the amplifier stage under consideration, the input impedance can be derived by looking at the equivalent circuit in Figure 6.3(b) and is given in (6.4).

\[ Z_{in} = R_B + R_E + \omega_{T,eff} L_E + \frac{\omega_{T,eff}}{j\omega g_{m,eff}} + j\omega L_E \]  \hspace{1cm} (6.4)

For conjugate matching at the input, first, \( L_E \) is chosen such that the real part of \( Z_{in} \) is equal to \( Z_0 \). Then, a base inductor \( L_B \) is added to cancel the imaginary part of \( Z_{in} \). From (6.4), its value must be \( L_B = \frac{\omega_{T,eff}}{\omega^2 g_{m,eff}} - L_E \).

To find the gain of the stage, its model is redrawn in Figure 6.3(c) assuming that it is conjugately matched, so that \( Z_{in} = Z_0 \). The losses at the output of the amplifier stage, including the transistor and the output matching network, are represented by a parallel resistor \( R_P \) at resonance. The power gain is given by (6.5).

\[ G = A_V A_I^* = \left( \frac{-f_T}{2jf} \frac{R_P}{Z_0 + Z_{in}} \frac{i_{sc}}{i_{in}} \right)^* \left( -\frac{1}{2jf} \frac{R_P}{Z_0} \right) \left( -\frac{f_T}{jf} \right)^* = \frac{1}{2} \frac{R_P}{Z_0} \left( \frac{f_T}{f} \right)^2 \]  \hspace{1cm} (6.5)
6.1 Design of 140-180 GHz Amplifiers

When the transistor parasitics and the load of the next stage are neglected, it can be shown that, to a first order, the voltage gain of an amplifier stage can be approximated by the ratio of the collector and emitter inductors (6.6).

$$\frac{V_C}{V_{in}} = \frac{\omega T i_{in} (j \omega (L_{C1} + L_{C2}))}{Z_{in} i_{in}} \approx \frac{\omega T (L_{C1} + L_{C2})}{\omega T L_E}$$ (6.6)

Finally, when the voltage division of the output matching network is taken into account, the complete voltage gain of the stage can be expressed as in (6.7).

$$\left| \frac{V_{OUT}}{V_S} \right| = \left| \frac{R_P}{2Z_0} \left( \frac{f_T}{f} \right) \frac{j \omega L_{C2}}{j \omega L_{C1} + j \omega L_{C2}} \frac{Z_0}{Z_{in}} \right| = \frac{R_P}{2Z_0} \left( \frac{f_T}{f} \right) \frac{L_{C2}}{L_{C1} + L_{C2}} \sqrt{1 + \omega^2 Z_0^2 C_C^2}$$ (6.7)

To find the power gain of the stage, its model is redrawn in Figure 6.3(c) assuming that it is conjugately matched, so that $Z_{in} = Z_0$. The losses at the output of the amplifier stage, including the transistor and the output matching network, are represented by a parallel resistor $R_P$ at resonance. The available power gain in a matched load (to $R_P$), is given by (6.8).

$$G = A_V A_I^* = \left( -\frac{f_T}{4jf} \frac{R_P}{Z_0} \right) \left( \frac{i_{sc}}{2i_{in}} \right) = \left( -\frac{1}{4} \frac{f_T}{f} \frac{R_P}{Z_0} \right) \left( \frac{f_T}{f} \right)^2$$ (6.8)

Table 6.1: Measured small signal model parameters of amplifier transistors.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>$l_E = 4 \mu m$</th>
<th>$l_E = 7.5 \mu m$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$g_{m,\text{eff}}$</td>
<td>148 mS</td>
<td>278 mS</td>
</tr>
<tr>
<td>$f_{T,\text{eff}}$</td>
<td>236 GHz</td>
<td>237 GHz</td>
</tr>
<tr>
<td>$f_{T,\text{eff}}$ (Cascode)</td>
<td>218 GHz</td>
<td>218 GHz</td>
</tr>
<tr>
<td>$\tau_F$</td>
<td>0.52 ps</td>
<td>0.52 ps</td>
</tr>
<tr>
<td>$R_B$</td>
<td>17.9 $\Omega$</td>
<td>9.57 $\Omega$</td>
</tr>
<tr>
<td>$R_E$</td>
<td>2.51 $\Omega$</td>
<td>1.34 $\Omega$</td>
</tr>
<tr>
<td>$R_C$</td>
<td>28.7 $\Omega$</td>
<td>15.3 $\Omega$</td>
</tr>
<tr>
<td>$C_{cs}$</td>
<td>5.92 fF</td>
<td>11.1 fF</td>
</tr>
<tr>
<td>$C_{bc}$</td>
<td>17.0 fF</td>
<td>31.8 fF</td>
</tr>
<tr>
<td>$C_{bc}$</td>
<td>8.36 fF</td>
<td>15.7 fF</td>
</tr>
<tr>
<td>$C_{\text{diff}} = \tau_F \times g_{m,\text{eff}}$</td>
<td>74.3 fF</td>
<td>139 fF</td>
</tr>
<tr>
<td>$C_{\pi} = C_{bc} + C_{\text{diff}}$</td>
<td>91.3 fF</td>
<td>171 fF</td>
</tr>
</tbody>
</table>
To evaluate the accuracy of the hand-design equations (6.2)-(6.8) and of the simplified equivalent circuit of the transistor, an HBT test structure with 5.74 \( \mu \text{m} \) emitter length was measured on the same wafer with the amplifier. Its extracted small signal model parameters were scaled for transistors with emitter lengths of 4 \( \mu \text{m} \) and 7.5 \( \mu \text{m} \) and listed in Table 6.1. The accuracy of the input capacitance prediction for a CE stage using the simplified equivalent circuit was estimated by comparing the measured \( C_\pi + C_{bc} \) with \( g_{m,\text{eff}}/\omega T_{\text{eff}} \) for the 7.5 \( \mu \text{m} \) device. Less than 10% error was found. By substituting the values of Table 6.1 into (6.4), the input impedance of stage 3 of the amplifier can be calculated as \( Z_{\text{in}} = 135 + j56.8 \Omega \) at 140 GHz. The 16 fF series capacitor in front of stage 3 cancels the imaginary part of this impedance, thus presenting a load of \( Z_L = 135 \Omega \) to stage 2. Similarly, the input impedance of stage 2 can be calculated as \( 70.2 + j3.8 \Omega \), leading to \( Z_0 = 70.2 \Omega \) for stage 2. The two 27.6 pF inductive loads of stage 2, along with \( C_{\text{out}} \) that consists of transistor and inductor parasitics, transform \( Z_L \) to \( 264 + j274 \Omega \). These values, together with \( f_{T,\text{eff}} = 236 \text{GHz} \) can now be substituted into (6.8) to obtain the gain for stage 2 as 4.3 dB. This value is close to the simulated gain of 3 dB to 4 dB per stage, leading to a total gain of 20 dB for the five amplifier stages.

The impedance transformation that occurs in the split load of an amplifier stage can be explained by (6.9), which gives the impedance looking from the input of a following stage towards the \( R_P \) of a preceding stage, as shown in Figure 6.3(d). From (6.9) it is apparent that to cancel the imaginary part of \( Z \), \( R_P^2 \) must be equal to \( 2\omega^2L^2 \). In this case the real part of \( Z \) becomes \( \Re(Z) = R_P/6 \). Thus, by employing split inductor loads, \( R_P \), which is seen at the collector, can be transformed to a much lower impedance that exists at the input of the next amplifier stage.

### 6.2. 140 GHz Amplifier Implementation and Results in BipX Technology

A tuned 5-stage amplifier, whose schematic is illustrated in Figure 6.1, was designed according to the procedure described in the previous section. It was designed at a centre frequency of 160 GHz, but due to model inaccuracies, the actual fabricated amplifier was centred at 140 GHz. The stand-alone amplifier was fabricated in the “BipX” SiGe HBT bipolar technology on multiple wafer splits, where the transistor \( f_T \) was varied between 230-290 GHz and
transistor $f_{\text{MAX}}$ was varied between 260-290 GHz [67]. The process also features a digital CMOS backend with 6 copper layers and a regular thickness, top aluminum layer. A die photo of the amplifier is reproduced in Fig. 6.4.

The amplifier design starts at the last stage and proceeds backwards towards the input. The bias current and size of transistors in each stage are progressively scaled (increased) from the input to the output. Interstage matching is employed to maximize the power gain. The last two stages of the amplifier employ a common-emitter topology for higher output power, while the first three stages are implemented with cascodes to obtain larger gain. Each of the inductors shown in the amplifier schematic was simulated in ASITIC and described by its corresponding 2-π equivalent circuit in simulation.

All transistors are biased at the peak-$f_T$ current density of $14 \text{ mA/\mu m}^2$. This choice of biasing and transistor sizing helps to maximize the power transfer between stages because the $Z_{\text{IN}}$ of each stage (6.4) is approximately equal to the $Z_{\text{OUT}}$ of the previous stage. The imaginary part (which is smaller than the real part) is cancelled using interstage series capacitors. To minimize gain variability, all inductors were implemented with identical geometry and ratioed sizes. To reduce the parasitic inductance between the CE and CB devices of a cascode stage, both devices were laid-out in a single trench and as close as possible by the DRC rules.

All bias voltages, supply and ground are distributed on metal mesh planes (similar to the illustration in Figure 3.14) with ample substrate contacts everywhere on chip. The metal mesh adds capacitance between the bias planes and ground [86]. For additional de-coupling, MiM capacitors of 0.5 pF (that are divided into 250 fF capacitors in parallel to avoid resonance) are positioned near each DC node of the circuit. The amplifier is AC-coupled for simpler testing.

Measurements of the amplifier were conducted on wafer using 110-170 GHz and 140-220 GHz waveguide probes. A 110-170 GHz OLM signal source, an Agilent E4448A PSA in conjunction with a Farran 140-220 GHz down-convert mixer, and an ELVA 110-170 GHz power sensor were employed for signal generation, spectral, and power measurements. The set-up with power sensor is illustrated in Figure 6.5. Since the signal source generates multiple tones in the 110-170 GHz band, the power and gain measurements where conducted twice, once with the power sensor and once with the PSA and Farran mixer (Figure 6.6). A 0-30 dB variable attenuator was used in the linearity measurements.

Note that due to the unavailability of a 110-170 GHz network analyzer, the gain of the amplifiers presented in this and in the following sections was obtained only using transmission measurements. $S_{11}$ and $S_{22}$ could not be measured. The transmission measurements employed a two-step process. First, the signal source was connected through an on-chip “thru” structure to a power sensor or a spectrum analyzer. (The power sensor allows for faster measurements, but the spectrum analyzer has more dynamic range, especially in a narrow span of 1 MHz
6.2 140 GHz Amplifier Implementation and Results in BipX Technology

Figure 6.4: Die photograph of the fabricated 140 GHz amplifier. The circuit area is 200 \( \mu \text{m} \times 400 \mu \text{m} \)

Figure 6.5: 110-170 GHz on-wafer test setup showing the signal source on the left, applied at the amplifier input through 110-170 GHz waveguide probes. The 110-170 GHz power sensor is at the right, for output power measurements.
and with averaging applied. The frequency of the signal source was swept and the measured power, which includes all setup losses, was recorded. In the second step, the amplifier was probed instead of the “thru”, the signal source frequency was swept while keeping the same power as in the previous step. Then the power recorded in step 1 was subtracted from that in step 2 to obtain the gain of the amplifier. $S_{12}$ was attempted to be measured in the same way, but no signal could be observed at the input of the circuit when applying power at its output. To confirm that the amplifier is stable, the same gain measurement procedure was repeated in fine 100 MHz steps to see if there are any spikes in output power. The output was also examined with no signal applied at the input. No instabilities were observed.

The gain of the amplifier was measured at 25 °C on several dies from two “nominal” wafers from two different runs. The gain remains above 15 dB from 126 GHz to 144 GHz with less than 1 dB variation between the two wafers (Figure 6.6). There is a 15% reduction in the centre frequency between measurements and simulation which may be explained by the fact that the models were extracted on 2-year old silicon [67] and from S-parameter measurements below 110 GHz. Figure 6.7 reproduces the measured gain as a function of temperature. At 140 GHz, the gain decreases from 17 dB at 25 °C to 4 dB at 125 °C while in the 125-135 GHz range it remains above 10 dB for all temperatures. Finally, the amplifier gain was measured across 14 different process wafer splits in order to identify the best HBT profile for circuits operating above 100 GHz (Figure 6.8). The wafer splits differ in the SiGe HBT $f_T/f_{MAX}$ values which vary in a correlated manner between 230/290 GHz and 290/260 GHz. Similar to the temperature behaviour, the gain variation is small at the lower end and increases at the
**Figure 6.7:** Amplifier gain over temperature measured using a D-band power sensor.

**Figure 6.8:** Amplifier gain curves measured on 14 wafer splits.
Figure 6.9: Amplifier linearity measurements at 3 frequencies.

Figure 6.10: Measured $f_T$, $f_{MAX}$, and amplifier gain at 130 GHz, 135 GHz, and 140 GHz plotted for four process splits where only the HBT collector doping is varied.
upper end of the bandwidth, with the gain tracking closely the $f_{\text{MAX}}$ of the SiGe HBT. This behaviour is similar to that of tuned SiGe HBT and CMOS amplifiers at 80 GHz and 60 GHz, where the gain at the higher frequencies depends on transistor $f_{\text{MAX}}$ and load $Q$ and rapidly degrades with temperature, whereas, at the lower end of the amplifier bandwidth, the gain is primarily controlled by the ratio of the collector load and emitter degeneration inductors.

Linearity measurements, conducted using the $\times 12$ multiplier source, the attenuator, and the D-band power sensor are illustrated in Figure 6.9. The output $P_{1dB}$ is -1 dBm at 140 GHz and +1 dBm at 130 GHz.

To correlate the effect of the HBT $f_T$ and $f_{\text{MAX}}$ with the amplifier performance, several wafer splits were selected where only one HBT profile parameter, the collector doping, is varied. The $f_T$ and $f_{\text{MAX}}$ of devices in those splits, which have opposite trends, are plotted versus the relative collector doping in Figure 6.10, along with amplifier power gain at 3 frequencies, 130 GHz, 135 GHz, and 140 GHz. As can be observed, the amplifier gain tracks closely the $f_{\text{MAX}}$ of the SiGe HBT, both decreasing with increasing collector doping.

### 6.3. 170 GHz Amplifier Implementation and Results in BipX Technology

A frequency-scaled version of the five-stage 140 GHz amplifier in [87] was designed to operate in the 160 GHz to 180 GHz range [88]. Its schematic is illustrated in Figure 6.11 and the layout is shown in Figure 6.12. As before, the amplifier consists of three cascode stages followed by two common-emitter stages. The last stage is composed of two devices, with CBEBC layout configuration, connected in parallel to achieve higher output power. Several versions of this amplifier were designed with different input and output matching networks. These matching networks were tuned to conjugately match the circuits at the amplifier interface. The standalone version of the amplifier was matched to 50 $\Omega$ on the input and output.

Scaling this amplifier in frequency from 140 GHz to 170 GHz was accomplished by adjusting component values and reducing inductive, resistive, and capacitive layout parasitics. To tune all the resonant load circuits in all amplifier stages to 170 GHz, capacitors with values smaller than 30 fF are required. Since such small MiM capacitor values were not available in the design kit, custom Metal-Oxide-Metal (MOM) capacitors were designed using ASITIC. Figure 3.12 illustrates the 3-D capacitor structure and the $2\pi$ model which was used in circuit simulations. The $2\pi$ equivalent circuit was derived from the simple-$\pi$ circuit employing a procedure similar to that described in [44]. To minimize their inductance and the die area of the
6.3 170 GHz Amplifier Implementation and Results in BipX Technology

Figure 6.11: 170 GHz amplifier schematic

Figure 6.12: Die photo of the stand-alone 170 GHz amplifier. The circuit area is 150 µm × 290 µm

Figure 6.13: Measured $f_T$ and $f_{MAX}$ vs. current density and temperature for an HBT with an effective emitter size of 0.11 µm × 5.55 µm
amplifier, all capacitors have a short aspect ratio, instead of the square layout typical of MiM capacitors.

This version of the amplifier was fabricated in a SiGe HBT technology [89] with \( f_T \) of 270 GHz and \( f_{MAX} \) of 340 GHz. The measured \( f_T \) and \( f_{MAX} \) are plotted in Figure 6.13 at 25°C and 125°C. The process features 6 copper layers and one aluminum cap layer used for pad openings. MiM capacitors and poly resistors are also provided. The top Cu layer is 0.9 µm thick and is 4.5 µm above the silicon substrate. \( SiO_2 \) is employed as the inter-metal dielectric. The amplifier was measured on-wafer in a D-band waveguide setup similar to that shown in Figure 6.5.

Figure 6.14 shows the measured amplifier gain and simulated S-parameters over temperature up to 125°C. The gain is higher than 15 dB from 166 GHz to 174 GHz and the 3 dB bandwidth exceeds 10 GHz. Figure 6.15 summarises the amplifier linearity measurements in the 160-170 GHz range at 25°C. The maximum output power of 0 dBm occurs at 164 GHz to 165 GHz and the best input \( P_{1dB} \) is -12 dBm at 164 GHz. The amplifier DC power consumption is 135 mW.

### 6.4. 160-GHz Amplifier with Gain Control in BiCMOS9MW technology

The amplifiers presented in sections 6.2 and 6.3 can be employed in several places in a continuous-wave (CW) imaging or radar transceiver. Those amplifiers can be placed as an LNA, a PA, or to boost other signals inside the transceiver. However, the previously described amplifier topology can also be adapted to create a transceiver for data communication applications using amplitude modulation (amplitude-shift keying). This can be accomplished by inserting gain control functionality into the amplifier to allow turning the RF signal on or off.

The schematic of such an amplifier is shown in Figure 6.16. Here, the gain control is implemented by replacing the common-base transistor in the second stage with a differential pair and directing the signal either to the next stage or to AC ground. Next, the data is applied to the bases of the diff pair devices. The circuit that drives the diff pair variable gain stage (“VGA driver”) is designed to completely switch the amplifier on and off with less than 100 mV swing in the “data” control input.

To prevent oscillations in the amplifier due to the use of cascode stages, all bases of the cascode transistors are decoupled with large MiM capacitors. As shown in the inset of Figure 6.16, each decoupling capacitor is split into a smaller one (150 fF) that is placed right at the base, in parallel with a larger one (500 fF), but a few microns away from the signal path.
6.4 160-GHz Amplifier with Gain Control in BiCMOS9MW technology

(a) Measured gain over temperature

(b) Simulated S-parameters over temperature

**Figure 6.14:** Measured and simulated gain of the 170 GHz amplifier vs. frequency over temperature

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**Figure 6.15:** Measured gain, saturated output power, and input $P_{1dB}$ of the 170 GHz amplifier at 25°C
This arrangement ensures that there is less than 1 pH of inductance between the base of the cascode transistor and the decoupling capacitor, without interfering with the layout of the RF signal path.

Preventing potential oscillations in the cascodes of the variable-gain stage is complicated by a conflicting requirement for supporting large data rates in the modulator. The bandwidth at node $A$ of Figure 6.16 is approximately given by (6.10), where $R_L$ is the load resistance of the VGA driver circuit and $C_D$ is the capacitance that decouples the cascode bases.

$$BW = \frac{1}{R_L C_D} = \frac{1}{200 \Omega \times 200 \text{fF}} = 4 \text{GHz}$$  \hspace{1cm} (6.10)

To support a 4 GHz bandwidth, $R_L$ is chosen to be 200 $\Omega$ to have sufficient voltage swing (200 mV) to switch the amplifier stage with 1 mA of bias current in the VGA driver (6.11).

$$R_L = \frac{V_{\text{SWING}}}{I_{\text{BIAS}}} = \frac{200 \text{mV}}{1\text{mA}} = 200 \Omega$$ \hspace{1cm} (6.11)

From (6.10) and (6.11) the bandwidth, and thus the maximum data rate of the modulator, are determined by $C_D$ for a given $I_{\text{BIAS}}$. For proper decoupling, $C_D$ is chosen to be 200 fF so that its resonance frequency $f_{\text{RES}}$ is above the second harmonic of the 160 GHz signal frequency in the presence of a 1 pH parasitic inductance $L_P$ (6.12).

$$f_{\text{RES}} = \frac{1}{2\pi \sqrt{C_D L_P}} = \frac{1}{2\pi \sqrt{200 \text{fF} \times 1 \text{pH}}} = 356 \text{GHz}$$ \hspace{1cm} (6.12)

To ensure that the parasitic inductance in the layout is less than 1 pH, the load $R_L$ is implemented as two 400 $\Omega$ resistors in parallel. Half of the resistance is placed right near the cascode bases and the decoupling capacitors, and the other half is placed near the VGA driver circuit. As a result, the long inductive lines that connect the VGA driver with the amplifier are terminated with resistors on both sides and do not cause oscillations. The layout of the complete 160 GHz amplifier with gain control is reproduced in Figure 6.17.

The amplifier was fabricated in a STMicroelectronics’ BiCMOS9MW process technology with a dedicated mm-wave back-end, 130 nm MOSFETs, and HBT $f_T$ of 230 GHz and $f_{\text{MAX}}$ of 280 GHz [73]. The back-end features six copper layers with the top two being 3 $\mu$m thick.

The simulated S-parameters and the measured gain of this amplifier as a function of frequency are shown in Figure 6.18 for the full-gain case. The measured peak gain of this amplifier is 21 dB at 160 GHz, which establishes a record for silicon technology. The gain remains larger than 15 dB from 143 GHz up to 175 GHz.

The simulated gain variation of the amplifier at the centre frequency as a function of the “data” control signal is illustrated in Figure 6.19. It proves that the amplifier can be completely
Figure 6.16: Schematic of the 160 GHz amplifier with gain control

Figure 6.17: A snapshot die photo of the 160 GHz amplifier with gain control
turned off or on with only about 50 mV swing on the “data” input. Finally, Figure 6.20 demonstrates the amplitude modulation functionality of the amplifier. In this simulation, the RF signal is at 170 GHz, and the modulation data rate is at 6.7 Gb/s. The output amplitude ratio between the “ON” and “OFF” states (Figure 6.20(b)) is 30 dB.

The same 160 GHz amplifier, but without gain control, was also fabricated in a next-generation experimental technology “B3T”. Compared to BiCMOS9MW, the B3T technology is bipolar-only, with transistor $f_T$ of 280 GHz and $f_{MAX}$ of 330 GHz. The back-end of line is identical in both B3T and BiCMOS9MW. Figure 6.21 presents the measured S-parameters of the 160 GHz amplifier in the BiCMOS9MW and B3T technologies. From the plot, the measured gain of the amplifier in B3T is 28 dB at 165 GHz. This is the highest amplifier gain above 150 GHz reported to date in any silicon technology.

6.5. Summary

In this chapter, D-band amplifier design methodology was presented, followed by implementation examples of amplifiers in the 130 GHz to 170 GHz frequency range. The amplifiers were fabricated in a few variants of a SiGe HBT technology differing in the device speed and the metal backend. A method for introducing amplitude modulation in the amplifier was also described.

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1Thanks to Kenneth Yau for providing the measured S-parameters of the “B3T” amplifier.
Figure 6.19: Simulated gain variation of the 160 GHz amplifier versus the “data” control input

Figure 6.20: Simulated data transmission at 6 Gb/s using the 160 GHz amplifier with gain control
Figure 6.21: Measured S-parameters of the 160 GHz amplifier in BiCMOS9MW technology and $S_{21}$ of the same amplifier fabricated in B3T technology. The corresponding simulated S-parameters of the amplifier in BiCMOS9MW technology are shown in Figure 6.18
After describing design methodologies and examples of mm-wave building blocks (dividers, VCOs, amplifiers) in earlier chapters, this chapter focuses on system integration. It starts by describing a 95 GHz double-sideband receiver in a 65 nm CMOS technology. The remainder of the chapter presents a collection of 160 GHz and 140 GHz transceivers with various levels of integration implemented in several flavours of STMicroelectronics’ SiGe BiCMOS technology.

First, a transceiver consisting of just a mixer (for the receiver) and oscillator (for the LO and the transmitter) is described. Due to the broadband nature of the mixer and because the oscillator produces both 80 GHz and 160 GHz signals, the first transceiver operates on both of these frequencies. The second version of this transceiver works at 160 GHz, features integrated RF, LO, and TX amplifiers, and achieves more receiver gain and transmitter output power. This 160 GHz was also fabricated in a version with on-chip antennas.

The third generation of the transceiver operated at 140 GHz and included a VCO instead of an oscillator, IF variable-gain amplifier, and amplitude modulation in the transmitter. This transceiver is shown to work in wireless Doppler and radio experiments with off-chip horn antennas and with on-chip patch antennas in an array configuration.

### 7.1. A 95 GHz Receiver with Fundamental-Frequency VCO and Static Frequency Divider in 65 nm Digital CMOS

Recently, several integrated radio receivers and transmitters operating at 60 GHz have been developed in SiGe BiCMOS [90] and CMOS [91–93] technologies, by both industry and academia. As CMOS transistor gate lengths continue to scale downward, integration becomes possible at even higher frequencies. This section presents a fully integrated receiver, with LNA, mixer, IF amplifier, fundamental-frequency quadrature VCO, and static frequency divider, operating at 95 GHz in a 65 nm general-purpose (GP) CMOS technology. The receiver consumes
7.1 A 95 GHz Receiver with Fundamental-Frequency VCO and Static Frequency Divider in 65 nm Digital CMOS

206 mW from a 1.2 V/1.5 V supply. With large RF and IF bandwidths of over 19 GHz and 16 GHz, respectively, it is suitable for passive-imaging applications, and for wireless chip-to-chip communication at data-rates exceeding 20 Gb/s. Together with the recently reported 60 GHz receiver in 90 nm CMOS [93], this 95 GHz receiver in 65 nm CMOS demonstrates that scaling of entire mm-wave receivers is possible in both frequency coverage and across technology nodes, as predicted by Gordon Moore in the last paragraph of [6]. Furthermore, with the reduction of the die area occupied by lumped passives at higher frequencies, and with the intrinsic speed improvement anticipated in future CMOS technology nodes, one can expect that entire CMOS transceivers can be scaled to 120 GHz in 45 nm, and to 160 GHz in 32 nm technologies, and can be integrated with antennas and other systems as wireless I/Os for chip-to-chip communication at 40 Gb/s.

The architecture of the fabricated receiver is illustrated in Figure 7.1. It uses an improved version of a shunt-series transformer-feedback 3-stage cascode LNA with a measured peak gain of 13 dB and noise figure of 6 dB to 7 dB [94]. The LNA is coupled to a double-balanced Gilbert-cell mixer through transformer $T_1$ which performs single-ended to differential conversion. The insertion loss of the transformer, measured on a separate test structure, is 1.7 dB in the 57-to-94 GHz range. A differential CML pair with 50 $\Omega$ loads is used as the broad-band IF amplifier. The LO signal is fed to the mixer using short transmission lines and transformer $T_2$. A static-frequency divider [1] is connected to the VCO to demonstrate the feasibility of a robust integrated 90 GHz PLL. Due to space limitations, only one of the two divider outputs is made available for testing, and the other is terminated on-chip. A fundamental-frequency quadrature VCO, which was described in section 5.3, is used to generate the LO signals on-chip. The VCO buffers differentially drive the mixer on one side, and the divider on the opposite side. The LNA, mixer, and IF amplifier, employing topologies with two vertically stacked transis-

![Figure 7.1: Top-level block diagram of the 95 GHz receiver chip](image-url)
7.1 A 95 GHz Receiver with Fundamental-Frequency VCO and Static Frequency Divider in 65 nm Digital CMOS

The LNA, mixer and IF amplifier were designed by Mehdi Khanpour and Keith Tang [95]. The divide-by-two circuit was designed by Ricardo Aroca [1]. The design of the VCO and its buffers, and the integration of the entire receiver together were done by me.

The entire receiver, along with several breakouts, was fabricated in a 65 nm GP CMOS technology, with a 7-metal copper backend. In this technology, an \( f_T \) of 170 GHz and \( f_{\text{MAX}} \) of 250 GHz were measured for devices with a 1 \( \mu \)m gate finger width contacted on one side of the gate and biased at a \( V_{DS} \) of 0.7 V (Figure 7.2)\(^1\). To overcome the problem of integrating the receiver blocks together, without degrading their performance, ample ground metallization and vias were used everywhere to minimize parasitic source degeneration and gate resistances. Metal-over-metal (MoM) capacitors of 0.5 pF were placed close to each circuit block to provide local ground and supply decoupling. A dense alternating-metal mesh was used for ground, bias, and power-supply distribution and decoupling. The mesh was designed to meet the stringent metal-density manufacturing rules. The receiver was measured on-wafer and characterized over temperature from 25 \( ^\circ \)C up to 100 \( ^\circ \)C.

Figure 5.9 shows the tuning range and output power of the VCO over temperature, measured on a breakout of the VCO, which includes all buffers and the divider. The VCO can be tuned from 88.3 GHz to 91.3 GHz, irrespective of temperature. The tuning range remains constant over a wide range of temperatures thanks to the Colpitts topology, the use of lumped

\(^1\)Thanks to Kenneth Yau and Alexander Tomkins for providing the device measurement data.
inductors, MOM capacitor $C_1$, and accumulation-mode MOS varactors, whose inductance and capacitance depend mostly on the metallization characteristics and dielectric permittivity, which hardly vary over temperature. The total output power of the VCO with four buffers is $+2$ dBm to $+3$ dBm in $50\ \Omega$ at $25^\circ C$. The VCO achieves a phase noise of $-95$ dBc/Hz at 1 MHz offset from the 90.3 GHz signal. The single-side-band (SSB) conversion gain, measured using a spectrum analyzer, is plotted in Figure 7.3, along with the input return loss of the receiver. At the nominal supply voltage of 1.5 V for the LNA, mixer, and IF amplifier, and 1.2 V for the VCO and divider, the peak gain is 12.5 dB and the 3 dB bandwidth of the receiver is 19 GHz, from 76 GHz to 95 GHz. In the receiver, the gain of the mixer compensates for the losses of the transformers that couple the LNA and VCO to the mixer. The $S_{11}$ of the receiver (measured on the LNA breakout) is lower than $-15$ dB from 77 GHz up to at least 94 GHz.

Figure 7.4 illustrates the double-side-band (DSB) noise figure and gain of the receiver, plotted versus the current density in the first stage of the LNA at 3 temperatures. The optimal bias current density for lowest noise figure is $0.25\ mA/\mu m$. In Figure 7.5, the DSB noise figure and conversion gain, measured using an Agilent N8975A noise-figure analyzer and a 75-to-110 GHz ELVA noise source, are plotted versus the IF frequency for different supply voltages of the LNA, mixer, and IF amplifier, and up to 100 $^\circ C$ with the nominal 1.5 V supply. The DSB noise figure is 7 dB to 8 dB for the nominal bias and temperature, and increases by 2.2 dB at 75 $^\circ C$. All components of the receiver are verified to work from 25 $^\circ C$ up to 100 $^\circ C$, except the divider, which divided the VCO signal only up to 50 $^\circ C$. The input 1 dB compression point of the receiver was measured to be $-18$ dBm (Figure 7.6). The DC power consumption of the
7.1 A 95 GHz Receiver with Fundamental-Frequency VCO and Static Frequency Divider in 65 nm Digital CMOS

**Figure 7.4:** Measured receiver conversion gain and NF variation with the current density of the LNA input transistor (LO = 89 GHz and IF = 6.3 GHz DSB)

**Figure 7.5:** Measured receiver gain and NF plotted versus IF with LO = 89 GHz
receiver is summarized in Table 7.1. The total dissipated power is 206 mW from the nominal 1.2 V (for the VCO and divider) and 1.5 V (for the LNA, mixer and IF amplifier) supplies, with 28% of the power in the VCO, 17% in the LNA, 11% in the divider, and 6.5% in the mixer. A die micro-photograph of the receiver chip is shown in Figure 7.7, demonstrating that a small active circuit area of $225 \mu m \times 940 \mu m$ is achieved by using only lumped transformers, inductors and capacitors in the design.

<table>
<thead>
<tr>
<th>Block</th>
<th>Current (mA)</th>
<th>Supply (V)</th>
<th>Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LNA</td>
<td>24</td>
<td>1.5</td>
<td>36</td>
</tr>
<tr>
<td>Mixer</td>
<td>9</td>
<td>1.5</td>
<td>13.5</td>
</tr>
<tr>
<td>50 Ω IF amplifier</td>
<td>19</td>
<td>1.5</td>
<td>28.5</td>
</tr>
<tr>
<td>Quadrature VCO</td>
<td>48</td>
<td>1.2</td>
<td>57.6</td>
</tr>
<tr>
<td>4 VCO buffers</td>
<td>24</td>
<td>1.2</td>
<td>28.8</td>
</tr>
<tr>
<td>Divider</td>
<td>18.6</td>
<td>1.2</td>
<td>22.4</td>
</tr>
<tr>
<td>Divider 50 Ω driver</td>
<td>16.3</td>
<td>1.2</td>
<td>19.6</td>
</tr>
<tr>
<td>Total:</td>
<td></td>
<td></td>
<td>206.4 (158)</td>
</tr>
</tbody>
</table>

**Figure 7.6:** Measured receiver 1 dB compression point with the RF frequency at 85 GHz and the VCO at 89 GHz
In active imaging applications it is customary to use several receivers and transmitters in an array configuration, to increase the resolution of an imager [96]. Integrating such an array at frequencies above 100 GHz poses a significant challenge in terms of LO clock distribution, power, and area. One possible system architecture relies on generating four quadrature signals at the fundamental frequency (80 GHz) together with a differential signal at the second harmonic (160 GHz). Since only one VCO is involved, all its six outputs can be locked to a single 80-GHz PLL, thus saving power and area.

A simplified version of that system was implemented as the single-chip transceiver whose schematic is illustrated in Figure 7.8. In the receiver, the RF signal is converted through an on-chip transformer to a differential signal that drives the down-convert mixer. The 160 GHz LO signal is generated on chip using the quadrature oscillator described in section 5.2. One of the 160 GHz signals drives the mixer differentially through another on-chip transformer. The second 160 GHz oscillator signal provides the 160 GHz transmitter output, while two of the 80 GHz quadrature signals form the 80 GHz differential output of the transmitter. The remaining two 80 GHz outputs of the oscillator can be used to drive a divider chain [52] as part of a PLL, but in this version of the transceiver they were terminated on-chip. Thus, simultaneous 80 GHz and 160 GHz transmitter and receiver operation is achieved.

A double-balanced Gilbert cell topology [97] mixer with on-chip RF and LO baluns is
employed in the receiver part of the transceiver. Its schematic is shown in Figure 7.9. The baluns, described in detail in section 3.2, perform single-ended to differential conversion. The bias for the RF differential pair and for the LO quad is applied to the centre tap of the secondary coil of each transformer. Inductors $L_E$ are used instead of a current source to achieve larger voltage headroom, better linearity, and help to match the RF input to $50\,\Omega$ at 160 GHz. Series 36 pH inductors are inserted between the collectors of the RF pair transistors and the emitters of the mixing quad to suppress the second harmonic (320 GHz) of the RF and LO signals over a broad band. The reactance of the LO and RF inputs is tuned out by employing shunt capacitors and series inductive transmission lines, which are part of the interconnect. The mixer schematic includes several inductors that model every piece of interconnect line in the mixer. Lines over the silicon substrate are modelled using the inductor 2-$\pi$ model, while interconnect that passes over metal is described as transmission lines. Furthermore, all metal-to-metal overlap capacitances are extracted using ASITIC and are included in the simulation schematic. They are not shown here for clarity.

There is no IF amplifier at the mixer output. Instead, the differential IF output is matched to $50\,\Omega$ at each side over a broad bandwidth (DC to 10 GHz) with the help of a network of inductors, capacitors ($L_C$ and $C_C$) and on-chip $50\,\Omega$ resistors. A broad IF bandwidth is required for communications at data rates above 10 Gb/s and for applications such as radio astronomy and imaging. In each IF matching network two identical inductors, $L_C$, are employed instead of a single large inductor, to increase the self-resonance frequency of those inductors beyond 50 GHz. Shunt capacitors $C_C$ tune the impedance to $50\,\Omega$.

Simulations of the mixer are reproduced in Figure 7.10. In Figure 7.10(a), the solid line shows the RF bandwidth, where the LO and RF frequencies are swept together with an IF of 1 GHz. The simulated peak voltage gain is 14 dB at 105 GHz, with a 3 dB RF bandwidth of
almost 100 GHz. The filled squares and empty circles show the IF bandwidth at 140 GHz and 160 GHz, simulated by keeping the LO constant and sweeping the RF frequency (and consequently the IF). The 3 dB IF bandwidth is 28 GHz at 140 GHz and at 160 GHz. Figure 7.10(b) shows the simulated mixer linearity at 140 GHz and 160 GHz with a 1 GHz IF. The 1 dB compression point is -7 dBm at both these frequencies.

The mixer layout (illustrated in Figure 7.11) is fully symmetric with respect to the LO-to-RF line. Symmetry is essential for proper double-balanced mixing operation, for impedance matching, and for achieving high isolation at mm-wave frequencies. The mixer operates from 3.3 V and consumes 15 mA. All transistors have the same size ($l_E = 4 \mu m$, $w_E = 0.13 \mu m$) and are biased at the peak-$f_T$ current density of $14 mA/\mu m^2$. Thanks to its balanced multiplier structure, this mixer works up to a record 180 GHz.

The 80/160 GHz transceiver was fabricated in a SiGe HBT technology with $f_{MAX}$ of 300 GHz and $f_T$ of 230 GHz [67]. The process features a digital CMOS backend with 6 copper layers and a regular thickness, top aluminum layer. A die photo of the transceiver is reproduced in Figure 7.12.

The output spectrum of the transmitter at 80 GHz is shown in Figure 7.13(a), with phase noise less than -100 dBc/Hz at 10 MHz offset. The signal measured at the 160 GHz transmitter output is shown in Figure 7.13(b) without de-embedding the test-setup losses. The measured and de-embedded TX output power and frequency at the 160 GHz output are plotted in Fig-
7.2 An 80/160 GHz Transceiver in SiGe Technology

(a) Simulated mixer voltage gain showing the IF and RF bandwidth.

(b) Simulated mixer linearity at 140 GHz and 160 GHz with 1 GHz IF.

Figure 7.10: Simulated 160 GHz mixer voltage gain and linearity.

Figure 7.11: Layout snapshot of the down-converter mixer
7.2 An 80/160 GHz Transceiver in SiGe Technology

Figure 7.12: Transceiver die photo occupying an area of 650 μm × 700 μm, including pads

(a) Measured phase noise of the single-ended 84 GHz output of the transmitter  
(b) Measured signal at the 164 GHz output of the transmitter

Figure 7.13: Measured signals at the 80 GHz and 160 GHz transmitter outputs
Figure 7.14: Single-ended power and frequency of the 160 GHz output of the transmitter vs. the oscillator power supply voltage

Even though this system employs a fixed-frequency oscillator, the frequency still changes with power supply variation. The maximum single-ended transmitted power occurs at 160.5 GHz and is -10 dBm.

The measured differential down-conversion gain of the receiver is shown in Figure 7.15. The RF bandwidth is 10 GHz for receiver operation at 80 GHz, and 8 GHz for operation at 160 GHz. The RF bandwidth of the receiver at 160 GHz is limited by the available power from the RF signal source and by the noise floor of the test setup. The measured and simulated transceiver performance is summarised in Table 7.2. The measured output power from the oscillator is lower than in simulation due unavailability of accurate transistor models. The measured down-conversion gain differs significantly from the simulated value due to insufficient LO power from the oscillator to drive the mixer.

Table 7.2: 80/160 GHz Transceiver Performance

<table>
<thead>
<tr>
<th></th>
<th>Measured</th>
<th>Simulated</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transceiver DC power consumption</td>
<td>295 mW</td>
<td>280 mW</td>
</tr>
<tr>
<td>Tx power at 80 GHz (single-ended)</td>
<td>-0.5 dBm</td>
<td>+6 dBm</td>
</tr>
<tr>
<td>Tx power at 160 GHz (single-ended)</td>
<td>-10 dBm</td>
<td>-3.9 dBm</td>
</tr>
<tr>
<td>Down-conversion gain at 80 GHz (differential)</td>
<td>-20.5 dB</td>
<td>-11.9 dB</td>
</tr>
<tr>
<td>Down-conversion gain at 160 GHz (differential)</td>
<td>-23.5 dB</td>
<td>-22 dB</td>
</tr>
<tr>
<td>Phase noise at 80 GHz, 10 MHz offset</td>
<td>-100 dBc/Hz</td>
<td>N/A</td>
</tr>
</tbody>
</table>
7.3 A 165 GHz Transceiver in SiGe Technology

This 165 GHz single-chip transceiver builds on the transceiver described in the previous section. In addition to the oscillator and mixer, it also includes three 165 GHz amplifiers and an 80 GHz static frequency divider, as illustrated in Figure 7.16. The three amplifiers are identical except for their input and output matching networks. The design, simulation, and measurement results of these amplifiers were described in section 6.3.

At the time of publication [May 2008], it marked the highest level of integration in silicon above 100 GHz. In this transceiver, the single-ended input is amplified by the receive-amplifier and is converted to a differential signal by transformer T1 before reaching the mixer. A differ-

![Figure 7.15: Differential down-conversion gain of the receiver, losses at IF were not de-embedded](image)

![Figure 7.16: Block diagram of the 165 GHz transceiver.](image)
7.3 A 165 GHz Transceiver in SiGe Technology

A differential 165 GHz LO signal is generated using the 82.5 GHz quadrature oscillator. This 165 GHz differential LO is treated as two single-ended signals, each of which is amplified separately. Transformer T2 connects the amplified LO signal to the mixer, while the second amplified LO signal is used as the 165 GHz transmitter output. The quadrature oscillator also produces two differential 82.5 GHz signals. One of the 82.5 GHz differential outputs drives the static frequency divider [52], while the other is terminated with 50 Ω resistors on-chip. However, in a future version of this chip, the latter can also be used to integrate an 80 GHz transceiver on the same die. The mixer, oscillator and transformers are identical in both this transceiver and the transceiver from section 7.2.

The 165 GHz transceiver was fabricated in an experimental SiGe HBT technology with $f_{\text{MAX}}$ of 340 GHz and $f_T$ of 270 GHz. The process features a digital CMOS backend with 6 copper layers and a regular thickness, top aluminum metal layer. MiM capacitors and polysilicon resistors are also available. A die photo of the transceiver, highlighting the main blocks is reproduced in Figure 7.17.

Measurements were conducted on wafer using 110-170 GHz waveguide probes. A 110-170 GHz OLM ×12 multiplier signal source, an Agilent E4448A power spectrum analyzer (PSA) in conjunction with a Farran 110-170 GHz down-convert mixer, and an ELVA 110-170 GHz power sensor were employed for signal generation, spectral, and power measurements. A 0-30 dB variable attenuator was used in the linearity measurements.

The measured differential down-conversion receiver gain of the 165 GHz transceiver is shown in Figure 7.18 for 25°C to 125°C temperature variation. All receiver down-conversion measurements were performed with a fixed (on-chip) LO signal by sweeping the RF frequency. The measurements were performed with a spectrum analyzer and de-embedded by subtracting the cable and probe losses from the measured input RF power and output IF power. The circuit pads were not de-embedded. The maximum gain at 25°C is -3 dB. Although the gain is reduced to -11 dB at 75°C, and to -25 dB at 125°C, the transceiver is still functional. At room temperature, the gain of this receiver is improved by more than 20 dB compared to that of the previous version (Figure 7.15). The gain improvement is due to the integrated RF input amplifier and the LO amplifier that provides a larger LO power level to the mixer. However, even more amplification of the LO might be needed to bring the LO power at the mixer to the optimal 0 dBm to 2 dBm level. Even though the mixer is the same in both transceivers, the 3 dB bandwidth of the 165 GHz transceiver is limited to 9 GHz by the RF amplifier. Note that IF amplifiers are not integrated on-chip, thus all the gain is achieved at the RF frequency of 165 GHz. Figure 7.19 illustrates the receiver linearity as a function of temperature. At 25°C, the input $P_{\text{1dB}}$ of the receiver is -20 dBm. The linearity, like the receiver gain, degrades significantly above 100°C.
Figure 7.17: Die photo of the 165 GHz transceiver.

Figure 7.18: Measured receiver gain of the 165 GHz transceiver over temperature.
The signal power and frequency at the 160-GHz transmitter output of the transceiver is plotted in Figure 7.20 as a function of the oscillator supply voltage. After de-embedding cable and probe losses, the single-ended transmitted power of -3.5 dBm at 165 GHz.

The measured total DC power consumption of the 165 GHz transceiver with amplifiers and divider is 0.9 W. Out of that, 340 mW are consumed by the oscillator, 100 mW by the static frequency divider and its output buffer, 32 mW is dissipated in the mixer, and each of the three amplifiers requires 145 mW. The 165 GHz transceiver performance is summarized in Table 7.3.

The same transceiver was also fabricated in a version with on-chip antennas, as shown in Figure 7.21. Several on-chip antenna variants were characterized before fabricating this transceiver with antennas\(^2\). These antennas are shown in Figure 7.22, and their measurement results are summarized in [88]. In [88] it is shown that the patch antenna has more loss than the other two antennas. The two exponentially-tapered dipole antennas have the same loss of around 25 dB at 165 GHz. The benefit of the antenna with metal fill (Figure 7.22(c) and 7.22(d))

\(^2\)Thanks to Keith Tang for the antenna design.

<table>
<thead>
<tr>
<th>Table 7.3: 165 GHz Transceiver Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transceiver DC power</td>
</tr>
<tr>
<td>----------------------</td>
</tr>
<tr>
<td>Tx output power at 160 GHz (single-ended)</td>
</tr>
<tr>
<td>Down-conversion gain at 160 GHz (differential)</td>
</tr>
<tr>
<td>Phase noise at 84 GHz, 10 MHz offset</td>
</tr>
</tbody>
</table>
is smaller area due to smaller effective dielectric thickness [98]. It is also compliant with density-DRC rules and therefore was chosen to be employed in the transceiver. It is important to emphasize that all the antennas of Figure 7.22 and the transceiver of Figure 7.21 were designed and fabricated in a SiGe technology with a “digital” backend, where the top (thickest) metal is only 0.9 µm thick and 4.5 µm above the substrate [89]. The exponentially-tapered dipole antennas [99] are coupled to the transmitter and receiver through transformers. To measure the transceiver with antennas, the transmitter or receiver probe was hovered above the respective antennas in several positions. The receiver gain with several probe-above-antenna positions is compared to the receiver gain without antennas in Figure 7.23. In this figure, the difference between the plots with and without antennas comes from the 25 dB antenna loss, which is not de-embedded. Similarly, the transmitter output power at different probe positions above the transmit antenna is plotted in Figure 7.24. In both the receiver and the transmitter measurement with antennas, the free-space loss is not de-embedded from the measurement. The 165 GHz transceiver measurements could not be performed in far-field due to high antenna loss, free-space attenuation and insufficient test setup sensitivity in these frequencies.
7.4 A 140 GHz Double-Sideband Transceiver with Amplitude and Frequency Modulation Operating over a few Meters

Figure 7.21: Die photo of the 165 GHz transceiver with on-chip antennas.

(a) Die photo of a 165 GHz on-chip patch antenna.  (b) Die photo of a 165 GHz on-chip exponentially-tapered dipole antenna.

(c) Die photo of a 165 GHz on-chip exponentially-tapered dipole antenna with metal fill.  (d) Illustration of a 165 GHz on-chip exponentially-tapered dipole antenna with metal fill.

Figure 7.22: Various 165 GHz on-chip antennas fabricated in a 6-metal-layers digital backend.
Figure 7.23: Measured receiver gain in the 165 GHz transceiver with on-chip antennas.

Figure 7.24: Measured transmitter output power from the 165 GHz transceiver with on-chip antennas.
This section describes the first demonstration of Doppler detection and data transmission through the air using a single-chip silicon transceiver at frequencies above 100 GHz. Although this chip does not target a single application, it demonstrates the capability of doing frequency modulation, amplitude modulation, transmission, and reception of signals without errors through the air at 140 GHz in a silicon technology. The circuit was fabricated in a SiGe BiCMOS process with a dedicated mm-wave back-end, 130 nm MOSFETs, and HBT $f_T$ 230 GHz and $f_{MAX}$ of 280 GHz [73]. The back-end features six copper layers with the top two being 3 $\mu$m thick.

The transceiver architecture, illustrated in Figure 7.25, builds on the design presented in [100] (section 7.3). Compared to the transceiver in [100], which was realized in an experimental HBT-only process with digital back-end, the new IC features (i) a variable gain IF amplifier with over 25 dB of gain control, (ii) a push-push voltage-controlled oscillator with differential outputs at 140 GHz and quadrature outputs at 70 GHz, (iii) a static divide-by-64, and (iv) a 140 GHz direct amplitude modulator. The single-chip transceiver can be used either as an FMCW Doppler or pulsed radar for position and motion detection, or as a gigabit-rate radio with ASK modulation. VCO frequency tuning and modulation are implemented with AMOS varactors.

For ASK modulation, the sensitivity $S_i$ of the receiver is calculated in (7.1) for a data rate of 4 Gb/s, noise figure of 12 dB, and SNR of 11 dB, corresponding to a bit error rate of $10^{-3}$.

$$S_i = 10 \log(kT) + 10 \log BW + NF + SNR = -174 + 96 + 12 + 11 = -55dBm \quad (7.1)$$}

Combined with a transmitter output power of -8 dBm at 140 GHz, and with transmit and
receiver horn antenna gains of 25 dBi, this transceiver can operate over a LOS distance of 2 m with a link margin of 16 dB.

\[
\text{Link Margin} = P_{RX} - S_i \\
= P_{TX} + G_{TX} + G_{RX} + 10 \log(\frac{\lambda}{4\pi R}) - S_i \\
= -8 + 25 + 25 - 81 + 55 \\
= 16dB
\] (7.2)

In the transceiver, two of the 70 GHz LO signals are used to drive the 6-stage static divider chain that could become part of a PLL in a radio or active imager, or can be employed to monitor the VCO frequency in a FMCW radar [101]. One of the 140 GHz VCO outputs drives the transmitter and passes through a 5-stage amplifier which also acts as an amplitude modulator. The ASK modulation is implemented with a differential switch in the 2\textsuperscript{nd} amplifier stage (described in detail in section 6.4) which either amplifies the signal or diverts it to ground (Figure 6.16). In the receiver, the LO and RF signals are first amplified and then converted to differential signals with the use of transformers, before driving a double-balanced Gilbert cell mixer. The mixer is followed by a 5-stage differential IF amplifier with gain control whose schematic is reproduced in Figure 7.26.
The IF variable-gain amplifier (VGA) consists of three “×1 scale” stages, followed by a “×2 scale” stage that drives the output 50 Ω buffer. In the “×2 scale” stage all currents and devices are multiplied by 2 and the resistor values are divided by 2 compared to the “×1 scale” stages. In all gain stages, the gain control is implemented in a Gilbert cell, where the current is steered between the path with the load that produces gain, and the path that directs the signal to AC ground. All stages, including the output buffer, employ degeneration resistors for better linearity. A simulation of the IF VGA is reproduced in Figure 7.27. In simulation, this amplifier has 35 dB gain with a bandwidth of 20 GHz. The gain can be varied from 0 dB to 35 dB.

The die photo of the transceiver chip is shown in Figure 7.28. It occupies an area of 0.9 mm × 1.6 mm. A breakout of the 5-stage 160 GHz amplifier, redesigned in the new technology, was fabricated together with the transceiver and characterized in a setup similar to that described in [100]. The measured gain is presented in Figure 6.18 as a function of frequency and establishes a record for silicon of 21 dB at 160 GHz. It remains larger than 15 dB from 143 GHz up to 175 GHz.

The VCO in the transceiver has a measured tuning range of 135.9 GHz to 142.2 GHz, and the transmitter has an output power of -8 dBm in this frequency range. A simulation of the transmitter operation is reproduced in Figure 7.29. Figure 7.29(a) shows the 169 GHz, 300 mV_{PP} output from the VCO. Next, the modulating data input at 5 Gb/s is shown in Figure 7.29(b). Finally, the modulated transmitter output (driving 50 Ω) is shown in Figure 7.29(c). The simulated output power of the transmitter is -1 dBm at 169 GHz.

In the receiver part, the measured peak down-conversion gain is 32 dB with a 3 dB receiver
Figure 7.28: 140 GHz transceiver micro-photograph. The pad-limited area is $910 \mu m \times 1570 \mu m$

(a) Simulated LO signal input at 169 GHz into the transmitter.

(b) 5 Gb/s modulating data input into the transmitter.

(c) Simulated transmitter output driving 50 $\Omega$.

Figure 7.29: Transient simulation of the transmitter.
Variable IF gain was demonstrated in both small-signal (Figure 7.30) and large-signal (Fig-ure 7.31(b)) measurements. Figure 7.31(a) reproduces the simulated receiver gain, extracted from transient simulations. The large difference between the simulated and measured receiver gain is explained by the frequency shift of the VCO from the simulated 169 GHz to the measured 140 GHz. In simulation, the receiver gain is composed of the 35 dB IF amplifier gain, the 20 dB RF amplifier gain, and the 5 dB mixer gain. In the real chip, however, the RF amplifier gain was 10 dB at 140 GHz (see Figure 6.18). Similarly, the output power of the LO amplifier has reduced, providing sub-optimal LO power into the mixer and reducing its gain.

Transceiver operation in FMCW mode with 1 kHz frequency modulation was characterized using the set-up in Figure 7.32 where loop-back between the transmitter and the receiver was realized through the air using two horn antennas with 25 dBi gain each, placed 13.5 cm apart. An additional off-chip opamp with a low-frequency cutoff of 30 Hz and 40 dB gain was connected at the baseband output to further boost the received signal beyond 1 V_{pp}. The 1 kHz IF signal was captured with an oscilloscope showing a swing of 8 V_{pp} (Figure 7.33(b)). The phase noise, lower than -65 dBc/Hz, was measured at 100 Hz offset with a spectrum analyzer (Figure 7.34(a)). When compared to the phase noise of -116 dBc/Hz at 1 MHz offset measured
7.4 A 140 GHz Double-Sideband Transceiver with Amplitude and Frequency Modulation Operating over a few Meters

(a) Simulated receiver down-conversion gain with different gain settings in the IF amplifier. LO frequency is 169 GHz.

(b) Measured receiver down-conversion gain in large-signal setup with different gain settings in the IF amplifier. The peak gain is smaller than that in Figure 7.30(a) due to difficulties in measuring absolute powers at 140 GHz.

**Figure 7.31:** Simulated and measured receiver gain.

**Figure 7.32:** Transceiver setup in loop-back through the air. The VCO control voltage is connected to a 1 kHz modulating input.
7.4 A 140 GHz Double-Sideband Transceiver with Amplitude and Frequency Modulation Operating over a few Meters

(a) IF output signal (20 mV_{PP}) in a loop-back setup with the VCO modulated at 1 kHz.

(b) IF output signal (8 V_{PP}) in a loop-back setup with the VCO modulated at 1 kHz. The output passes through a 40 dB off-chip opamp.

Figure 7.33: Time-domain IF output from the receiver with the transceiver configured in loop-back as in Figure 7.32.

(a) Measured phase noise at the IF output when the transceiver is configured in loop-back, as in Figure 7.32.

(b) Measured phase noise of the VCO at the output of the static divide-by-64 chain.

Figure 7.34: Frequency-domain IF output and divider chain output from the transceiver.
at the divide-by-64 output of the transmitter, corresponding to -80 dBc/Hz VCO phase noise, (Figure 7.34(b)), evidence of phase noise cancellation due to range correlation [102] becomes immediately apparent.

Next, the Doppler effect was demonstrated with the help of the test setup of Figure 7.35. The Doppler shift was observed by measuring the IF frequency with a slowly-moving reflector with an area of 0.17 m$^2$. The reflector was placed up to 2 m above the transmit and receive antennas. A frequency shift of as low as 30 Hz was observed on an oscilloscope.

Finally, the measured transmitter output spectrum at 140 GHz with an ASK modulation of 100 Mb/s is shown in Figure 7.36(a). Due to the high loss (over 40 dB) of the external down conversion mixer used in this test setup, spectra corresponding to higher data rates drop below the sensitivity floor of the spectrum analyzer. However, looking at the received IF spectrum (Figure 7.36(b)) in a setup similar to Figure 7.32, signals with data rates of at least 4 Gb/s can be observed.

Another test setup with 1.15 m total distance between the transmitter and receiver antennas is illustrated in Figure 7.37 (45 cm from transmitter to reflector, 70 cm from reflector to receiver). The transmitted and received time-domain signals at 4 Gb/s in this setup are shown in Figure 7.38. The signals from the 4 Gb/s eye diagram were also plotted in the form of a bit sequence in Figure 7.39. Figure 7.39 shows that a 4 Gb/s error-free $2^7 - 1$ PRBS pattern is received from a 1.15 m distance at 140 GHz.
(a) Measured 100 Mb/s ASK spectrum at the 140 GHz output of the transmitter.

(b) Measured 4 Gb/s ASK spectrum at the output of the receiver with the transceiver configured in loop-back, as in Figure 7.32.

Figure 7.36: Measured ASK spectra at RF and IF.

Figure 7.37: Test setup showing the PRBS generator board, the transmitter and receiver horn antennas, the reflector, and the eye diagrams on the oscilloscope.
Figure 7.38: Measured eye diagrams with the transceiver in the setup of Figure 7.37. Top - 4 Gb/s signal that modulates the transmitter output. Bottom - demodulated output from the receiver.

Figure 7.39: Measured error-free $2^7 - 1$ PRBS data stream with the transceiver in the setup of Figure 7.37. Top - 4 Gb/s signal that modulates the transmitter output. Bottom - demodulated output from the receiver.
7.5. A 140 GHz Double-Sideband Transceiver Array with on-Chip Antennas

Following on the 140 GHz transceiver presented in the previous section, a transceiver array with on-chip patch antennas was also designed. The array consists of two receivers and one transmitter, each with their own patch antenna. The receivers and transmitter are integrated from the same blocks as the transceiver in section 7.4, except for a new LO distribution amplifier.

Since all transceiver blocks are reused from the previous transceiver, their parameters remain the same. For a 2 Gb/s transmission at 140 GHz with a noise figure of 12 dB, the receiver sensitivity is -57 dBm. With on-chip patch antennas that have around 0 dB gain (simulated), and a transmitter output power of -8 dBm this transceiver can operate over a LOS distance of 10 mm with a link margin of 14 dB.

\[
\text{Link Margin} = P_{RX} - S_i = P_{TX} + G_{TX} + G_{RX} + 10 \log\left(\frac{\lambda}{4\pi R}\right) - S_i = -8 + 0 + 0 - 35 + 57 = 14 dB
\] (7.3)

A simulation of the on-chip patch antenna employed in this transceiver array is reproduced in Figure 7.40. This patch antenna has much better performance compared to the on-chip antennas described in Section 7.3 thanks to the dedicated MM-Wave backend employed for this design. The MM-Wave backend features top two copper metal layers that are 3 \(\mu\)m thick, and a top metal layer that is 10 \(\mu\)m above the substrate. The antenna is implemented in the top metal layer, which is slotted to meet DRC rules, above a ground shield made from metal 1 and metal 2 shunted together. Density DRC rules were waived for metals 3, 4, and 5, which are absent between the ground plane and the antenna.

The block diagram of the transceiver array is shown in Figure 7.41. As before, the LO signal is generated with a push-push 140 GHz VCO. One side of the 140 GHz LO is fed to the transmitter amplifier which includes ASK modulation for data transmission. The other side of the VCO output connects to the LO distribution amplifier that amplifies and splits the signal to the two receivers. In each of the two receivers, the LO and the amplified RF signals are converted to differential with the use of transformers and are fed into the down-converter mixers. The mixers are followed by variable-gain IF amplifiers. No divider is included on this

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\(^{3}\)Thanks to Ioannis Sarkas for the antenna design and simulation results
7.5 A 140 GHz Double-Sideband Transceiver Array with on-Chip Antennas

version of the chip due to unavailability of probes for biasing the divider in addition to all other circuits.

The transistor-level schematic of the LO distribution amplifier is reproduced in Figure 7.42. It is based on the 160 GHz tuned amplifiers described in chapter 6. In this amplifier, the signal first passes through three cascode stages for gain. Then, the signal is split in two, and is amplified again in each of the two parallel paths. The three stages after signal splitting are designed with scaled currents to drive the mixer. The transformers that convert the single-ended LO signals to differential are used as loads in the last amplifier stages. All amplifier stages are conjugately matched to each other.

Simulations of the LO distribution amplifier are reproduced in Figure 7.43 and Figure 7.44. Figure 7.43 shows the gain from the input to each of the two outputs of the amplifier and its stability. The input and outputs of the LO distribution amplifier are not matched to 50 Ω, but rather to the impedance of the circuits that it is driving. Figure 7.44 illustrates a transient simulation of the same amplifier, showing that it has enough swing at the both outputs to drive two mixers in the receivers.

The on-chip patch antennas for this transceiver array were designed by Ioannis Sarkas. The measured antenna $S_{11}$ is reproduced in Figure 7.45. The antenna pattern could not be measured due unavailability of suitable equipment.

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4Thanks to Ioannis Sarkas for providing the antenna measurement data.
Figure 7.41: Block diagram of the 140 GHz transceiver array with on-chip antennas.

Figure 7.42: Schematic of the LO distribution amplifier. Biasing details are not shown.
Figure 7.43: S-parameter simulation of the LO distribution amplifier.

Figure 7.44: Transient simulation of the LO distribution amplifier with an input of -20 dBm at 178 GHz. The output signal is 720 mVpp from each of the two outputs.
Figure 7.45: Measured $S_{11}$ of the patch antennas employed in the transceiver array.

Figure 7.46: Die photo of the 140 GHz transceiver array with on-chip antennas. The circuit occupies a 2.5 mm × 1.7 mm area, including the antennas.
The transceiver array with antennas was fabricated in the STMicroelectronics’ BiCMOS9MW technology [73]. The technology features SiGe HBTs with $f_T$ of 230 GHz and $f_{\text{MAX}}$ of 280 GHz, 0.13 $\mu$m MOSFETs, poly resistors, MiM capacitors, and a 6-layer copper backend with two 3 $\mu$m thick top layers. The chip photo of this transceiver is shown in Figure 7.46. The size, including the antennas is 2.5 mm × 1.7 mm.

The use of on-chip antennas for all mm-wave signals not only makes it easier to get signals on- and off-chip, but also defines one ground reference for all circuits inside the transceiver. I.e. the ground plane of the antennas (with respect to which the signals are received and transmitted) is also the ground plane of the entire chip. This fact becomes important if this transceiver array were to be packaged. When antennas are employed, the inductance of the ground leads introduced by the package does not appear on the signal path. Therefore it does not degrade the gain and other performance metrics of the chip. Furthermore, since the interface to the chip consists of only IF and DC signals, a low-frequency package would be sufficient. This is in contrast to the transceiver described in Section 7.4, where 140 GHz signals would need to propagate through the package and force the ground to be defined on the board, thus adding inductance in series with the chip ground and deteriorating performance. The effect of ground inductance on a single amplifier circuit (with the schematic of Figure 6.1) is demonstrated in Figure 7.47. In this figure, the s-parameters of the amplifier are simulated with zero ground inductance and with 50 pH added between the global ground and the amplifier ground. From this simulation it is apparent that ground inductance has a significant effect on the stability and gain of circuits and must be taken into account in the design process.

The VCO inside the transceiver array is tunable over a 9 GHz range, from 136.5 GHz to 145.5 GHz. The measured tuning range is reproduced in Figure 7.48. Several experiments were performed with the transceiver array to demonstrate its operation through the air. The experiments included detection of Doppler frequency and wireless data transmission.

In the first experiment, functionality of the two receivers was verified. As shown in Figure 7.49, a signal source with -10 dBm output power and a 25 dBi horn antenna was positioned at a 1 m distance from the transceiver on the probe station. This signal was received by both receivers in the array and the two IF outputs were observed on two spectrum analyzers. IF signals up to 9 GHz could be observed.

After verifying the operation of the receivers, the transceiver was configured for a Doppler experiment, similar to the setup shown in Figure 7.35. However, compared to the setup of Figure 7.35, no horn antennas were used, the microscope was raised, and a smaller target was moved in the space between the transceiver array chip and the microscope. The target area was 10 cm × 10 cm and its distance to the chip was 10-15 cm. An off-chip opamp circuit with 40 dB gain was employed after the IF amplifiers to boost the output signal to levels observable on the
Figure 7.47: Simulated amplifier S-parameters with and without ground inductance.

Figure 7.48: Measured VCO tuning range in the transceiver array.
7.5 A 140 GHz Double-Sideband Transceiver Array with on-Chip Antennas

Figure 7.49: Test setup for receiver demonstration.

Figure 7.50: Doppler experiment results.

(a) An $8 \, V_{pp}$, 76 Hz Doppler shift signal.  
(b) A $6 \, V_{pp}$, 25 Hz Doppler shift signal.
oscilloscope. The results of the Doppler experiment are shown in Figure 7.50. Figure 7.50(a) shows an 8 V$_{PP}$, 76 Hz signal, and Figure 7.50(b) shows a 6 V$_{PP}$, 25 Hz Doppler shift signal.

Finally, a wireless data transmission experiment at 145 GHz was performed with the help of the test setup in Figure 7.51. Figure 7.51(a) shows the probe station, the received ASK-modulated spectra from the two IF outputs on the spectrum analyzers, and received 2 Gb/s eye diagram from receiver 1. Figure 7.51(b) is a zoomed-in photo of the probes contacting the transceiver array and the reflector that is used to reflect the transmitted signal back to the two receivers. Figures 7.52 and 7.53 reproduce the received IF ASK-modulated spectra from receiver 1 and receiver 2 respectively. According to the spectra, both receiver channels can operate up to at least 3 Gb/s.

Measured eye diagrams of the received signals are shown in Figure 7.54. A 2 Gb/s transmitted and received eye (accumulated over a few seconds) is shown in Figure 7.54(a). When the oscilloscope is locked to the incoming data pattern, multiple accumulated patterns can be averaged. Received eye diagrams with averaging at 3 Gb/s from both channels are shown in Figure 7.54(b). The signal amplitude from receiver 2 is smaller than the amplitude of receiver 1 because receiver 2 could not be terminated symmetrically due to layout constraints. With averaging, an eye diagram can be observed up to 5 Gb/s.

The received time-domain 2$^7$ – 1 PRBS bit patterns from receiver 1 are shown in Figure 7.55 at different data rates. The received patterns are error free up to 4 Gb/s. At 5 Gb/s, the bit pattern is deteriorated by noise and bandwidth limiting.

Table 7.4 summarizes the power consumption of the 140 GHz transceiver array with on-chip antennas. The most power-hungry circuit block is the LO generation and distribution. The total power consumption of the chip is 1.42 W.

Table 7.5 gives the count of the various active and passive devices employed in the 140 GHz transceiver designs described in section 7.4 and in this section 7.5. Although not all devices

Table 7.4: Power consumption breakdown of the 140 GHz transceiver array with on-chip antennas.

<table>
<thead>
<tr>
<th>Component</th>
<th>Supply Voltage</th>
<th>DC Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage-controlled oscillator</td>
<td>3.3 V</td>
<td>366 mW</td>
</tr>
<tr>
<td>Mixers and IF amplifiers</td>
<td>3 V</td>
<td>345 mW</td>
</tr>
<tr>
<td>140 GHz LO and RF amplifiers</td>
<td>1.5 V/3.3 V</td>
<td>513 mW</td>
</tr>
<tr>
<td>140 GHz TX amplifier</td>
<td>1.5 V/3.3 V</td>
<td>150 mW</td>
</tr>
<tr>
<td>TX modulator</td>
<td>3.3 V</td>
<td>16.5 mW</td>
</tr>
<tr>
<td>Various bias currents</td>
<td>-</td>
<td>33 mW</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td>-</td>
<td><strong>1.42 W</strong></td>
</tr>
</tbody>
</table>
7.5 A 140 GHz Double-Sideband Transceiver Array with on-Chip Antennas

(a) Test setup showing the probe station, the received ASK-modulated spectra from the two IF outputs on the spectrum analyzers, and received 2 Gb/s eye diagram from receiver 1.

Figure 7.51: Test setup for 140 GHz wireless data transmission experiment.

(b) Zoomed-in photo showing the probes contacting the transceiver array and the reflector that is used to reflect the transmitted signal back to the receivers.

Figure 7.52: Received ASK-modulated spectra from receiver 1.

Figure 7.53: Received ASK-modulated spectra from receiver 2.
7.5 A 140 GHz Double-Sideband Transceiver Array with on-Chip Antennas

Figure 7.54: Measured eye diagrams from the two receivers inside the transceiver array.

(a) Transmitted (bottom) and received with receiver 1 (top) 2 Gb/s eye diagrams.
(b) Receiver 1 (top) and receiver 2 (bottom) 3 Gb/s eye diagrams with averaging.
(c) Transmitted (bottom) and received with receiver 1 (top) 5 Gb/s eye diagrams with averaging.

Figure 7.55: Received (with receiver 1) $2^7 - 1$ error-free PRBS data patterns up to 5 Gb/s.
require the same amount of design effort, a high integration level of almost 1000 devices is demonstrated in both chips.

### 7.6. Summary

This chapter described a 95 GHz CMOS receiver and a family of mm-wave double-sideband transceivers operating in the 140 GHz to 160 GHz frequency range. The transceivers were designed in stages, starting from the most simple (mixer with oscillator) configuration, and ending with a fully integrated front-end transceiver array with on-chip antennas. Table 7.6 summarizes the performance of the four transceivers. The final transceiver featured integrated mm-wave amplifiers, ASK modulation in the transmitter, frequency modulation, variable-gain IF amplifiers, and a divide-by-64 chain. Using this transceiver, FMCW and Doppler effects were demonstrated at 140 GHz through the air at 2 m using horn antennas, and at 15 cm using on-chip patch antennas. Furthermore, wireless data transmission was successfully demonstrated at 140 GHz with a 4 Gb/s data stream.

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6 Several performance metrics were not measured for the 140 GHz transceiver array because of the antennas. However, these metrics are expected to have the same values as those for the 140 GHz transceiver without antennas because most circuit blocks are the same. Equipment to measure the antenna gain was not available.

6 Phase noise for the 80/160 GHz transceiver and the 165 GHz transceiver was measured at the fundamental frequency of the oscillator (around 80 GHz) due to smaller equipment losses at this frequency. At the second harmonic frequency (around 160 GHz) the losses prevent phase noise measurements. For the 140 GHz transceiver, the phase noise was measured at the divider output, since the VCO outputs were not provided off chip.

#### Table 7.5: Number of devices in the 140 GHz transceivers of section 7.4 and section 7.5.

<table>
<thead>
<tr>
<th></th>
<th>140 GHz transceiver (section 7.4)</th>
<th>140 GHz transceiver array with on-chip antennas (section 7.5)</th>
</tr>
</thead>
<tbody>
<tr>
<td>HBTs</td>
<td>322</td>
<td>243</td>
</tr>
<tr>
<td>MOSFETs</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Varactors</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>MM-wave capacitors</td>
<td>25</td>
<td>33</td>
</tr>
<tr>
<td>Inductors</td>
<td>94</td>
<td>143</td>
</tr>
<tr>
<td>Transformers</td>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>Resistors</td>
<td>282</td>
<td>283</td>
</tr>
<tr>
<td>DC capacitors</td>
<td>140</td>
<td>223</td>
</tr>
<tr>
<td>Patch antennas</td>
<td>-</td>
<td>3</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td>873</td>
<td>937</td>
</tr>
</tbody>
</table>
Table 7.6: Performance summary of D-band transceivers described in this chapter.

<table>
<thead>
<tr>
<th></th>
<th>80/160 GHz transceiver (section 7.2)</th>
<th>165 GHz transceiver (section 7.3)</th>
<th>140 GHz transceiver (section 7.4)</th>
<th>140 GHz transceiver array (section 7.5)^2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency (GHz)</td>
<td>160.5 - 164.5</td>
<td>164 - 174</td>
<td>135.9 - 142.2</td>
<td>136.5 - 145.5</td>
</tr>
<tr>
<td>Phase Noise (dBc/Hz)^6</td>
<td>-100 at 10 MHz offset from 80 GHz</td>
<td>-110 at 10 MHz offset from 84 GHz</td>
<td>-80 at 1 MHz offset from 142 GHz</td>
<td>not measured</td>
</tr>
<tr>
<td>Receiver Gain (dB)</td>
<td>-23.5</td>
<td>-3</td>
<td>Variable up to 32</td>
<td>not measured</td>
</tr>
<tr>
<td>Receiver NF (dB)</td>
<td>not measured</td>
<td>22</td>
<td>12.3</td>
<td>not measured</td>
</tr>
<tr>
<td>Receiver BW (GHz)</td>
<td>12</td>
<td>9</td>
<td>6</td>
<td>not measured</td>
</tr>
<tr>
<td>Transmitter $P_{OUT}$ (dBm)</td>
<td>-10</td>
<td>-3.5</td>
<td>-8</td>
<td>not measured</td>
</tr>
<tr>
<td>Data Rate (Gb/s)</td>
<td>-</td>
<td>-</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>DC Power (W)</td>
<td>0.295</td>
<td>0.9</td>
<td>1.5</td>
<td>1.42</td>
</tr>
</tbody>
</table>
Conclusion

This thesis has shown the implementations of several 140 GHz to 160 GHz mm-wave transceiver front-ends and described the design procedure for their building blocks. A 65 nm, 95 GHz CMOS receiver was also presented. Several wireless experiments were performed with the fabricated transceivers employing on-chip and off-chip antennas. The experiments included a 4 Gb/s data transmission, Doppler, and FMCW radar operation.

The circuit building blocks that compose these transceivers have achieved record performance for SiGe circuits at the time of their publication. These circuit blocks include a static frequency divider operating up to 100 GHz, and 140 GHz and 160 GHz tuned amplifiers. A quadrature VCO design that aids in the LO distribution at mm-wave frequencies was described. The CMOS receiver and SiGe transceivers demonstrate integration levels that have never been achieved before at these frequencies in the respective technologies.

8.1. Thesis Contributions

A number of contributions to the field of millimetre-wave integrated circuit design have been made in this thesis. These include:

1. A comparison study of static divider topologies with and without emitter followers on the input clock path. It was concluded that the use of emitter followers is inferior to the simple resistive divider for input biasing. As a result of this study, a static frequency divider with a self-oscillation frequency of 77 GHz, correct division bandwidth of 20 GHz to 100 GHz, and power consumption of only 122 mW was built. The static dividers were published in the 2006 IEEE Bipolar / BiCMOS Circuits and Technology Meeting [52]. A dynamic divider operating up to 136 GHz with 73 mW power consumption was also designed and published in [63].
2. Development of a fully integrated receiver, with LNA, mixer, IF amplifier, fundamental-frequency quadrature VCO, and static frequency divider, operating at 95 GHz in a 65 nm general-purpose (GP) CMOS technology. The receiver consumes 206 mW from 1.2 V and 1.5 V supplies. It was characterized on wafer up to 100°C and achieved a down-conversion gain of 12.5 dB with 19 GHz bandwidth, VCO tuning range of 88.3 GHz to 91.3 GHz, phase noise of -95 dBc/Hz at 1 MHz offset, and a noise figure of 7 dB. The receiver was published at the 2008 IEEE International Solid-State Circuits Conference [78].

3. A family of 165 GHz transceivers was developed in a SiGe HBT technology with transistor $f_T$ of 230 GHz, $f_{MAX}$ of 300 GHz and CMOS-like backend. The first version of the transceiver operated at both 80 GHz and 160 GHz and demonstrated the feasibility of D-band (110 GHz to 170 GHz) SiGe circuits. It consisted of an oscillator and a mixer and was published at the 2007 IEEE Radio-Frequency Integrated-Circuits Symposium [87]. A second version of the transceiver also included three integrated 165 GHz amplifiers and a static divider, demonstrating high integration levels at 165 GHz and robust LO distribution technique. This transceiver achieved -3 dB conversion gain and -3.5 dBm output power and was published in the IEEE Journal of Solid-State Circuits in 2008 [100]. The same 165 GHz transceiver was also fabricated with on-chip exponential-tapered dipole antennas and was published at the 2008 IEEE Radio-Frequency Integrated-Circuits Symposium [88].

4. The design of a 140 GHz transceiver consisting of a 140 GHz voltage-controlled oscillator, static divider chain, transmitter with ASK modulation, receiver amplifier, mixer and variable-gain IF amplifier. Correct operation of this transceiver was verified through several wireless experiments, the first performed at this frequency with silicon circuits. The experiments included wireless transmission of a 4 Gb/s signal over a 1.15 m distance, FMCW operation, and measurement of a Doppler frequency shift of as low as 30 Hz. The transceiver was published at the 2009 IEEE Bipolar / BiCMOS Circuits and Technology Meeting [85]. It was followed by a design of 140 GHz transceiver array (consisting from two receivers and one transmitter) with on-chip patch antennas. The array was built from the same circuit blocks as the single transceiver. The same experiments were repeated with the on-chip antennas and successfully demonstrate large integration levels of D-band circuits in silicon. The transceiver array was not published yet.
5. As part of the developed mm-wave transceivers, 140 GHz to 170 GHz tuned amplifiers were designed. The amplifiers had 15 dB to 20 dB gain, which was a record for silicon technologies at these frequencies at the time of publication.

6. After the design of the 140 GHz transceivers, techniques to reduce the power consumption of select mm-wave circuit blocks were developed. Specifically, novel low-power static and dynamic frequency divider topologies were introduced. With these low-power topologies a static divider was designed to operate up to 109 GHz while consuming 26 mW from 1.2 V. A low-power dynamic divider worked in the 112 GHz to 122 GHz frequency range and consumed only 32 mW from a 1.5 V supply. Low-power topologies were also developed for fundamental-frequency VCOs operating in the D-band. These VCOs (one Armstrong VCO and one Colpitts VCO) achieved record-low phase noise while operating from 1.8 V. The low-power dividers and VCOs were not published on their own, but were included in a 120 GHz radar sensor system that was published in [103].

7. During the transceiver design, an LO distribution methodology was proposed whereby the LO is generated with a push-push oscillator that produces quadrature signals at the fundamental frequency and a differential signal at the second harmonic frequency of 160 GHz. This differential signal is then used as two single-ended LO signals, that are amplified and are subsequently converted to differential signals with the help of transformers. This scheme reduces the amount of spurs on the chip compared to a lower-frequency VCO with multiplier architecture. Also, power consumption is reduced by employing passive transformers instead of active elements on the LO path.

8.2 Future Directions

In section 7.5, it was shown that the developed transceiver array is fully functional. Furthermore, thanks to its on-chip antennas, it have only DC and low-frequency inputs and outputs, which makes it easy to package. If these transceivers are packaged, higher-accuracy radar experiments for position and velocity measurements can be performed. Also, with the help of appropriate signal processing, the packaged transceivers can be used to form mm-wave images.

The natural extension of the mm-wave receivers and transceivers developed in this thesis, is to design phased-array transceivers. In addition to the circuit blocks designed in this work, a phased array would require only the addition of a phase shifter. As demonstrated in sec-
tion 7.5, the extension of the transceivers into arrays is relatively straightforward, but is rather demanding on the LO distribution circuitry.

The power consumption of the SiGe transceivers can be significantly reduced by employing the low-voltage techniques developed for dividers in section 4.6 and for VCOs in section 5.4. This way, the entire transceiver can be operated from 1.8 V. For cascode stages used in the mm-wave amplifiers, AC-coupled CE-CB stages can be used. The power supply voltage of the mixer can also be reduced to 1.8 V by inserting an AC-coupling transformer between the RF pair and the LO quad, similar to the mixer inside the dynamic divider.

With the development of faster devices, further scaling in frequency of the entire transceiver should be possible. As was shown in Figure 6.21, more than 25 dB gain can be achieved at 170 GHz in a next-generation SiGe technology. This indicates that, with an optimized design, a 200 GHz transceiver is realistic.

8.3. List of Publications

The work presented in this thesis has been published in the following refereed IEEE journals and international conferences.

8.3.1. Refereed IEEE Journal Articles


8.3.2. Refereed International Conference Proceedings

1. E. Laskin, P. Chevalier, B. Sautreuil, and S.P. Voinigescu, "A 140-GHz Double-Sideband Transceiver with Amplitude and Frequency Modulation Operating over a few Meters,"
IEEE Bipolar / BiCMOS Circuits and Technology Meeting, pp. 178-181, Capri, Italy, October 2009.


Bibliography


A.1. Asitic Examples

To define a transformer, the following set of commands can be used (version 2.2 of asitic).

\begin{verbatim}
chip 64 64
symsq name=a:len=25:w=2.5:s=2:n=1:metal=6:metal2=5:ilen=4:
xorg=18:yorg=18
symsq name=b:len=25:w=2.5:s=2:n=1:metal=5:metal2=4:ilen=4:
xorg=18:yorg=18:orient=180
wire name=c:len=8:w=2.5:metal=6:xorg=10:yorg=28:orient=180
wire name=d:len=8:w=2.5:metal=6:xorg=10:yorg=34.5
join a c
join a d
wire name=e:len=8:w=2.5:metal=5:xorg=43:yorg=28:orient=180
wire name=f:len=8:w=2.5:metal=5:xorg=43:yorg=34.5
join b e
join b f
\end{verbatim}

After the transformer is defined, it is simulated at low frequency (0.5 GHz) and at the frequency of operation (160 GHz) using the “pix” command. The “k” command is used to obtain the coupling coefficient between the primary and secondary coils.

\begin{verbatim}
pix a 0.5 (1)
pix b 0.5 (2)
pix a 0.5 b (3)
k a b (4)
\end{verbatim}

The “pix” commands and their output are reproduced below.
A.1 Asitic Examples

Pix a 0.5 (1)
Pi Model at f=0.50 GHz:  \( Q = 0.401, 0.401, 0.401 \)
\( L = 0.0365 \ \text{nH} \)
\( R = 0.286 \)
\( C_{S1} = 2.39 \ \text{fF} \)
\( R_{S1} = 3.81 \times 10^4 \)
\( C_{S2} = 2.44 \ \text{fF} \)
\( R_{S2} = 3.39 \times 10^4 \)
\( f_{\text{res}} = 539.20 \ \text{GHz} \)

Pix b 0.5 (2)
Pi Model at f=0.50 GHz:  \( Q = 0.425, 0.425, 0.425 \)
\( L = 0.0387 \ \text{nH} \)
\( R = 0.286 \)
\( C_{S1} = 3.29 \ \text{fF} \)
\( R_{S1} = 3.82 \times 10^4 \)
\( C_{S2} = 3.38 \ \text{fF} \)
\( R_{S2} = 3.42 \times 10^4 \)
\( f_{\text{res}} = 446.16 \ \text{GHz} \)

Pix a 0.5 b (3)
Pi Model at f=0.50 GHz:  \( Q = 0.401, 0.401, 0.401 \)
\( L = 0.0365 \ \text{nH} \)
\( R = 0.286 \)
\( C_{S1} = 3.88 \ \text{fF} \)
\( R_{S1} = 3.2 \times 10^3 \)
\( C_{S2} = 3.63 \ \text{fF} \)
\( R_{S2} = 2.55 \times 10^3 \)
\( f_{\text{res}} = 423.12 \ \text{GHz} \)

K a b (4)
Coupling coefficient of A and B:  \( k = 0.51274 \) and \( M = 0.01925 \ \text{(nH)} \).

From this simulator output, the 2-\( \pi \) model (Figure A.1) that can be used in circuit simulations can be extracted by the following procedure [44].

From command (1), the primary coil inductance and resistance parameters are obtained:

\[
L_{P1} = L_{P2} = \frac{L_{\text{command1}}}{2}; \quad R_{P1} = R_{P2} = \frac{R_{\text{command1}}}{2}
\]

\[\text{Figure A.1: Transformer 2-}\pi \text{ model.}\]
The secondary coil inductance and resistance parameters are obtained from command (2). This command also gives the oxide capacitance between the secondary (bottom) coil and the substrate.

\[ L_{S1} = L_{S2} = \frac{L_{\text{command2}}}{2}; \quad R_{S1} = R_{S2} = \frac{R_{\text{command2}}}{2} \]

\[ C_{OX11} = \frac{C_{S1\text{command2}}}{2}; \quad C_{OX22} = \frac{C_{S2\text{command2}}}{2}; \quad C_{OX12} = C_{OX11} + C_{OX22} \]

The substrate resistance is also given in command (2). The substrate capacitance is calculated from the substrate resistance and the dielectric relaxation time of the substrate. \( \varepsilon_0 \) is the permittivity of free space, \( \varepsilon_r = 11.7 \) is the relative permittivity of silicon, and \( \rho_{SI} \) is the substrate resistivity in \( \Omega \times m \).

\[ R_{S11} = 2 \times R_{S1\text{command2}}; \quad R_{S22} = 2 \times R_{S2\text{command2}}; \quad R_{S12} = R_{S11} || R_{S22} \]

\[ C_{S11} = \frac{\varepsilon_r \varepsilon_0 \rho_{SI}}{R_{S11}}; \quad C_{S22} = \frac{\varepsilon_r \varepsilon_0 \rho_{SI}}{R_{S22}}; \quad C_{S12} = \frac{\varepsilon_r \varepsilon_0 \rho_{SI}}{R_{S12}} \]

The coupling capacitance is obtained from the \( C_s \) parameter of the third command.

\[ C_{C11} = \frac{C_{S1\text{command3}}}{2}; \quad C_{C22} = \frac{C_{S2\text{command3}}}{2}; \quad C_{C12} = C_{C11} + C_{C22} \]

Finally, the coupling coefficient between the two coils is taken directly from the fourth command.