LOW-POWER MULTI-Gb/s WIRELINE COMMUNICATION

by

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A thesis submitted in conformity with the requirements for the degree of Doctor of Philosophy
Graduate Department of Electrical and Computer Engineering
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Abstract

This thesis discusses low-power wireline receivers with particular focus on clocking circuitry and architectures. These clocking solutions can be used for a 1-D partial response channel as well as for a conventional DC coupled channel. The receiver front end for a 1-D channel requires more consideration to recover an NRZ signal from the received narrow pulses. Two possible solutions are presented. First, a full-rate detection technique is presented, where the speed is limited by the settling time of a latch circuit which has to be less than 1 UI. Second, a novel demuxing technique is introduced. It is demonstrated through theory, simulation and measurement results that the half-rate architecture can improve maximum achievable speed by a factor of 1.6.

The distribution and alignment of high-frequency clocks across a wide bus of links is a significant challenge in modern computing systems. A low power clock source is demonstrated by incorporating a buffer into a cross-coupled oscillator. Because the load is isolated from the tank, the oscillator can directly drive 50-Ohm impedances or large capacitive loads with no additional buffering. Using this topology, a quadrature VCO (QVCO) is implemented in 0.13 um digital CMOS. The QVCO oscillates at 20 GHz, consumes 20 mW and provides 12% tuning range.

Injection locked oscillators (ILOs) are an attractive clocking tool for low-power area-efficient wireline receivers. In this work, we explored their use as a clock deskew
element, a clock recovery unit and a programmable jitter filter. A study of both LC and ring ILOs indicates significant variation in their jitter tracking bandwidth when used to provide large phase shifts. By selectively injecting different phases of a quadrature-LC or ring VCO, this problem is obviated resulting in reduced phase noise.

First, an ILO based half-rate clock recovery technique is presented, which can be used for AC coupled links where low frequency signal components are attenuated by the channel. The nonlinear path comprises a hysteresis latch that recovers the missing low frequency content and a linear path that boosts the high frequency component by taking advantage of the high pass channel response. By optimally combining them, the front-end recovers NRZ signals up to 13 Gb/s burning only 26 mW in 90 nm CMOS. A simple theory and simulation technique for ILO-based receivers is discussed. The clock recovery technique is verified with experimental results at 5-10 Gb/s in 90 nm CMOS consuming 70 mW and acquiring lock within 1.5 ns.

Second, a clock forwarded 65nm CMOS receiver uses two ILOs to frequency- multiply, deskew, and track correlated jitter on a pulsed clock forwarded from the transmitter. Different data rates and latency mismatch between the clock and data paths are accommodated by a jitter tracking bandwidth that is controllable up to 300MHz. Each receiver consumes 0.92 pJ/bit operating at 7.4 Gb/s and has a jitter tolerance of 1.5 UI at 200MHz.
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1 Introduction

Portable, high performance consumer products are a current focus of microelectronics research. Such systems require long battery life, hence target lower power consumption. On the other hand, high performance requires fast data processing which demands more power consumption. Fortunately, aggressive scaling of CMOS devices has come a long way to meet these competing requirements: shorter gate length provides area-efficient and faster computation while consuming less power. As a result, per pin bandwidth requirements are ever increasing. In addition, the shrinking periphery of integrated circuits (ICs) with reduced die size demands much higher interconnect density. In summary, next generation portable devices require advanced power reduction technique and highly integrated interconnect solutions.

1.1 Motivation

1.1.1 Low power clock generation and distribution

To reduce the overall power consumption of a transceiver it is constructive to break down its total power consumption into different components as shown in Table 1.1. In high-speed transceivers clocking circuits include VCO, PLL, DLL, clock distribution network and clock deskew circuits such as phase interpolators. These are the dominant power consuming parts which consistently consume more than 50% of the total transceiver power. This remains the case at different data rates for different technologies and supply voltages. Thus low power clock generation is a focus of this work.
Table 1.1: Summary of total power and clock circuit power consumption on high-speed transceiver

<table>
<thead>
<tr>
<th>Data rate</th>
<th>[M. 00]</th>
<th>[H. 03b]</th>
<th>[G. 07]</th>
<th>[G. 07]</th>
<th>[G. 07]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.25um</td>
<td>0.11um</td>
<td>65nm</td>
<td>65nm</td>
<td>65nm</td>
</tr>
<tr>
<td>Total Transceiver Power</td>
<td>90 mW</td>
<td>Rx-129 mW</td>
<td>13.5 mW</td>
<td>36 mW</td>
<td>75 mW</td>
</tr>
<tr>
<td>Power consumed by clocking circuits</td>
<td>50 mW</td>
<td>90 mW</td>
<td>8 mW</td>
<td>25 mW</td>
<td>60 mW</td>
</tr>
</tbody>
</table>

1.1.2 Burst mode for power reduction

A conventional approach to power minimization in digital circuits is to reduce the supply voltage. Using this approach, performance is traded to save energy. The high variability, lower dynamic range and increasing leakage power of nano-scale devices pose significant challenges that motivate novel circuit topologies and innovative architectures. In the last few years, as leakage power has become a major concern, multiple $V_{th}$ devices are used to minimize idle power in the digital circuits which partially address this issue. Taking a different approach, high speed I/Os can use a scalable supply where $V_{DD}$ is adjusted according to the speed [G. 07]. Unfortunately, as the leakage to dynamic power ratio increases, most of these techniques are becoming ineffective. Therefore, it is necessary to turn ‘OFF’ the circuits to reduce leakage current while in standby. For example, Renesas mobile processor uses Ultra-standby (U-standby) and Resume-standby (R-standby) modes to combat leakage current [T. 04] Fig. 1.1. Compared to a conventional approach, in this application R-standby reduces the leakage current from 2.2 mA to 86 uA proving to be more effective. The main challenge of this approach is that the processor must have a fast recovery time requirement to ensure uninterrupted data processing. The recovery time is broken down in Fig. 1.2, where the most significant time lag is introduced by the clock recovery units, namely the PLL and DLL. From initiation to the lock acquisition, the link can’t be used to send information. During this time, the transmitter generally sends a training pattern which preambles the data burst. Longer lock times require more preamble bits, which result in reduced burst efficiency. For example, in a 10Gb/s (bit period = 100ps) link, 1ms lock time requires $10^6$ bits of preamble which is a significant portion of the
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Figure 1.1: Powerdown options in Renesas mobile processor.

Figure 1.2: Breakdown of recovery time in R-standby mode [T. 04](slide-19 visual supplement). PSW is abbreviated form of power supply switch data burst. The reported PLL/DLL clock time in Renesas processor is around 1ms. However, state of the art CDR systems have reduced the lock time in the order of us [H. 04]. Therefore, the effectiveness of this method can be significantly improved and potentially be extended in other applications by introducing faster locking techniques
that can recover timing information within several bit periods (UI).

1.1.3 Future of Interconnects

Replacing DC interconnects between a transmitter and receiver with AC counterparts provides several advantages: first, the requirement for a solid common ground reference, which is difficult to realize at very high frequencies, is removed. Second, AC coupling allows us to interface between devices that use different supply voltages and common modes. As a result, the overall system can be optimized using the most appropriate supplies at either end of the link. In addition, some interconnect standards, such as fiber channel and PCI express require AC Coupling. The conventional implementation of these capacitors are off-chip, where they are built using surface mount technology (SMT). These off-chip capacitors do not allow for a highly integrated solution and also introduce several signal integrity issues. As a result at 10 Gb/s or beyond and for very high interconnect densities, off-chip AC coupling becomes a bottleneck and embedded capacitors are desirable.

Existing methods for realizing embedded capacitors are (i) moving the capacitor within the die [Y. 07] and (ii) using an additional dielectric layer in the PCB to realize buried capacitors [B. 08]. However, capacitance densities provided by these alternatives are not sufficient. For example, PCI express requires a 220 nF coupling capacitor which is not realizable with on-chip or buried capacitor technology. The 220nF capacitance value for PCI express is rather conservative. This choice is motivated by several reasons: First, PCI express needs to support data rates 2.5Gb/s, 5Gb/s and 8Gb/s. Effect of AC coupling is more prominent for lower bit rate. To reduce DC droop less than 5 mV coupling capacitance needs to be in the order of nF. Second, in most existing PCI express solutions AC coupling capacitance is off-chip. So, area penalty for 220 nF off-chip capacitance is considered negligible. To study the effect of capacitance value on signal integrity, we modeled a 20 cm AC coupled PCB trace link. Transfer functions and corresponding step responses for different capacitor values are shown in Fig. 1.4. Due to AC coupling, the step input results in a pulse at the receiver side. The width of this pulse depends on the coupling capacitor ($C_{AC}$) and this in turn defines the signaling technique that can be supported. To clarify different signaling options,
Figure 1.3: Channel model of AC coupled link over 20 cm PCB trace

Figure 1.4: Frequency domain Transfer function and corresponding step response for different coupling capacitor

normalized pulse width have been plotted as a function of coupling capacitance in Fig. 1.5. In addition, the corresponding eye diagram at 10 Gb/s is also provided for different coupling capacitances in Fig.1.6. For larger capacitors ($C_{AC} > 400\text{pF}$), the high pass cutoff frequency is on the order of several MHz which provides a sufficiently flat frequency response and pulse width greater than 50 UI. As a result, DC droop can be eliminated using a run length limited code such as 8B10B (where the maximum run length is 5). Therefore, conventional NRZ signaling can still be used as shown in corresponding eye diagram. As we decrease the capacitance value, pulse width also decreases and the resulting DC imbalance increases the ISI penalty. When the pulse width decreases down to several UI, existing coding methods including 8B10B can no longer mitigate baseline wander. In such cases introduced DC droop causes complete eye closure at the receiver end. Therefore, a high speed DC restoration technique is the only effective solution to recover data [E. 07] when capacitor value is between 3 to
10 pF.

As the coupling capacitor decreases to less than 1 pF, the flat portion of the frequency response diminishes and therefore NRZ signaling cannot be supported. For such low values of capacitance, the frequency response is very similar to a 1-D dicode partial response channel. Due to the DC null in the frequency spectra, only positive and negative pulses appear at the receiver side on each data transition. This signaling technique is described as pulse mode signaling [L. 05]. In case of $1 - D$ channel, inter symbol interference (ISI) is caused by the prolonged tail of the step response. For capacitance value 3 pF to 5 pF the tail spreads over several UI (3 UI - 5 UI) causing complete eye closure. To reduce this ISI components, for a given data rate high pass cutoff frequency ($1/(2\pi RC)$) should be greater than baud frequency ($f_{Ba}$). Reducing capacitance value pushes the high pass pole at higher frequency and reduces ISI terms and hence improves eye opening. With the optimum capacitor value, the amplitude of the step response is large enough to be detected by the receiver and the pulse width of the step response should be less than 1 UI to avoid ISI. Clearly, a smaller coupling capacitor can support higher data rates so long as the receiver can provide the required sensitivity.

Applications of Pulse signaling

Pulse mode signaling has several applications.

- First, due to smaller capacitance requirements (100fF - 500fF) integrated capacitors can be used for AC coupled links that traditionally employ off-chip capacitors which leads to a low cost highly integrated solution [Y. 07].

- Second, this signaling method can be used for 3D integration, where, ICs are proximity coupled with a small capacitance or mutual inductance [K. 03],[R. 04]. These proximity coupled interconnects are cost effective, detachable and scalable.

- Finally, compared to NRZ, pulse mode signaling uses only the higher frequency portion of the spectra. This allows remaining spectra to be used for other applications.
However, the major challenge in this case is to recover NRZ signals from the received narrow pulses which requires a non-conventional receiver. Historically, such receivers have been used for magnetic storage read channels which are significantly slower compared to conventional wireline chip-to-chip links and consumes higher power compared to DC coupled receivers.

1.1.4 Summary

This thesis explores several concepts:

- First, low power clock generation is critical for reducing power consumption in transceiver. Thus in this work we will investigate power reduction techniques for
VCOs and phase interpolators.

- Second, we want to explore fast locking concepts which can significantly reduce the system’s power consumption by turning transceivers ‘off’ during idle periods.

- Third, we want to investigate a receiver architecture that can recover the data and clock from a 1-D type channel response such as is provided by AC coupled interconnects.

In this work, we first study these concepts separately. Then, they are synergistically combined into a single receiver architecture targeting even greater improvements on the performance of low power CMOS receiver architectures. Generally, in AC coupled receivers the received pulse stream is amplified and then converted to a NRZ data stream using non-linear circuit techniques. This recovered NRZ bit stream is then retimed and demuxed with a recovered clock (Fig.1.7). Injection locking is an attractive solution for such receivers due to favorable channel response. It was found in this work that the higher bandwidth jitter tracking and phase noise filtering properties of the ILOs are also attractive for other conventional NRZ receivers. Such possibilities are explored in both clock forwarded links where one dedicated link carries the clock from the transmitter side, (Fig.1.8), and embedded clock links where the receiver needs to recover clock from the available data stream.

1.2 State-of-the-Art burst mode and pulse mode receivers

1.2.1 Status of burst mode receiver

Burst mode clock recovery is extensively used in passive optical network (PON) systems where the clock needs to be extracted within a few bits of preamble. The present status of high-speed burst mode clock recovery is summarized in Table 1.2. In most cases they are not power and area efficient which limits their usefulness. Power and area efficient burst mode signalling is also used for chip-to-chip links. In [N.M08] burst
mode signalling simply relies on matching the delays in a forwarded clock path and a data path. The use of this approach is very limited and not usable for clock embedded links. Thus, a true burst mode capability will require ‘fast locking’ of a recovered clock.

1.2.2 Status of pulse mode receiver

For low power applications, a relevant figure of merit is mW/Gb/s or equivalently pJ/bit. The power efficiency of recently published transceivers (including all clock power amortized over the total number of links) is plotted in Fig. 1.9 versus data rate. Complete NRZ transceivers have already demonstrated high-speed (>20Gb/s) and excellent power efficiency (<5mW/Gb/s) [R.S07]. Compared to NRZ, pulse re-
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<th>Table 1.2: Comparison of state-of-the-art burst mode clock recovery technique</th>
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<td><strong>Pulse/NRZ</strong></td>
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receivers are several years behind. For example a complete Pulse receiver reported in [L. 05] consumes 117 mW to achieve 3 Gb/s data rate. Burning less power, simple NRZ receiver reported in [E. 06] achieves 10 Gb/s data rate which also reduces interconnect density requirement to achieve higher aggregate data rate. Present research in pulse mode receivers mainly focuses on the front-end circuits which recover NRZ signals from the pulsed signals. However, the maximum speed reported was 10 Gb/s. In summary, compared to existing NRZ receivers, pulse mode receivers are slower, consume higher power and have relatively poor sensitivity. This poor performance of the pulse mode receivers can be explained as follows:

1. Due to the 1-D channel response, pulse mode signaling uses a higher frequency portion of the available spectra. Therefore, to amplify the received narrow pulses, the front-end amplifier needs to provide higher bandwidth compared to NRZ receivers.

2. From the received stream of pulses, NRZ signals are recovered using a hysteresis latch, which is functionally equivalent to a DFE [R. 78], but without a clock. The speed of this recovery method is limited by the settling time of the feedback loop which needs to settle within 1 UI. Any latency in the feedback loop results in ISI, jitter and eventually completely closes the eye.
3. Clock recovery techniques used in pulse mode receivers apply conventional timing recovery approaches to the recovered NRZ signals. As explained above, the recovered NRZ signal itself suffers from significant ISI and jitter, so extracting a low jitter clock is even more challenging.

As mentioned before, the performance of pulsed receivers is significantly worse than their NRZ counterparts. The power consumption and area requirements of these links are prohibitive in high density chip to chip interconnects. In addition, most of the existing pulsed receivers are not capable of burst-mode operation.

1.3 Outline

Three major challenges in pulse mode receivers are speed, power and sensitivity. In addition, we also want to enable burst mode operation. With that motivation, we separate the problem in several sections.

Chapter 2 focuses on NRZ signal recovery from the received narrow pulses. Several architectures are studied that can provide this functionality. To overcome their speed limitations, two approaches are considered. In the first approach, using the full-rate
architecture the threshold settling and output settling are improved to achieve higher speed. In the second approach, the imposed limitation is alleviated by introducing a half-rate architecture which can potentially which can double the achievable data rate. Analysis, simulation and measurement results for both architectures are given in chapter 2. Injection locking is studied as a way to achieve burst mode capability in chapter 3. In this chapter, we study transient locking behavior, jitter transfer and jitter tolerance characteristics with a goal to use an injection locked oscillator (ILO) as a clock recovery unit. In addition, an ILO can also be used as clock deskew block, replacing phase interpolators. A theoretical framework for ILO behavior is provided in this chapter that is VCO topology-independent, so that it can be used for both LC and ring VCOs. Finally, the theory developed in chapter 3 is applied for two applications: a clock forwarded and clock embedded receiver in chapter 4 and in chapter 5 respectively. In chapter 4 a complete AC coupled receiver is implemented which utilizes the architecture developed in chapter 2 and 3. Chapter 5 explores clock forwarded link where high jitter tracking bandwidth of the ILO is utilized to achieve higher jitter tolerance. For this implementation simple NRZ signalling is considered which allows simpler comparison with other clock forwarded links.
2 Highspeed 1-D Receiver Architecture in CMOS

2.1 Introduction

There are many new and emerging applications for dicode (1-D) partial response signaling. Dicode partial response signaling was applied to magnetic storage channels [M. 70]. More recently, a similar channel response has been observed in multi-Gbps wireline communication applications such as Passive Optical Networks (PON) and AC coupled chip-to-chip links that have spectral nulls at DC.

A brief background on $1-D$ partial response channel will be provided in section 2.2. General bit-by-bit decoding techniques for dicode channels are presented in section 2.3. The proposed half-rate architecture, introduced at the end of section 2.3 relaxes the speed bottleneck introduced by feedback in full-rate architectures. In section 2.4, a full-rate implementation in 0.18um CMOS is described. It is based on the architecture introduced in [M. 07] but modified to accommodate threshold adjustability and improve sensitivity. Section 2.5 describes the circuit level implementation of the half-rate architecture introduced in Section 2.3. Using this technique the receiver can potentially improve the speed by a factor of 2, at the expense of increased power consumption. The 0.18-um CMOS prototype operates up to 5Gb/s, 50% faster than the full-rate architecture. Targeting chip-to-chip applications, 90 nm implementation of these architectures are presented in section 2.6. Finally, these two architectures are compared in the conclusion in section 2.7.
2.2 Background

One interesting area where partial response signaling has been applied is chip-to-chip links. For example, it was used for a high speed multi drop bus with magnetically coupled receivers [J. 03]. Capacitive coupling has also been used in chip-to-chip links within a package [R. 04] and over PCB traces up to 20 cm in length [L. 05]. AC coupling has also been used for bidirectional signaling [A. F07], as a wireless link for modulated data [Q. 07] and for power transfer [C. 06a]. For these applications, the speed of receivers are generally limited by the settling time of a latch circuit. This shortcoming is addressed in this work with two novelties: first, an improved latch circuit provides faster settling time; second, a parallel architecture permits the positive- and negative-going pulses to be detected separately, thus alleviating the feedback settling time requirements on the latches. Magnetic storage channels exhibit non-linear ISI distortion which can significantly degrade receiver’s performance compared to a similar channel with purely linear distortion as observed in recent AC coupled links [N. 94]. To overcome such channel impairments RAM-DFE [P. 95] and analog DFE [M. 99] are proposed. In all these cases multiple taps were required to equalize the channel. Modern AC coupled links are significantly better behaved which requires only a single tap to achieve 5+ Gb/s. However, main limitation in this case is the feedback loop latency which must be less than 1 UI. Focus of this work is to overcome this limitation and achieve 2x speed improvement. Previously deterministic mapping is used to achieve half-rate data detection in a magnetic storage channel [J. 90]. However, this technique is only applicable for miller-square coded data pattern, hence not applicable for conventional NRZ data.

Another area of interest is burst mode applications. In a PON system, the receiver at the Optical Line Terminal (OLT) needs to recover data from different Optical Network Units (ONU). The packets of data from ONUs arrive in bursts at the OLT end and their signal strength varies significantly. For high data rates such as 10Gb/s, the receiver used in OLT end needs to correct the DC offset in less than 1 ns. To avoid the difficulty associated with fast DC offset cancelation loop, 1-D channel is used to suppress the DC content [M. 05].
Partial response channel receivers can be broadly classified in two categories: sequence detectors and bit-by-bit detectors. Sequence detectors, such as those using the Viterbi algorithm make a decision based on a sequence of observations spanning several symbol intervals \([G. 72]\). Sequence detectors generally out-perform bit-by-bit detectors and are now therefore dominant in magnetic storage applications. However, they demand sophisticated signal processing and power consumption which is generally intolerable for multi-Gb/s wireline communication applications of \((1 - D)\) partial response signaling. The remainder of the paper will, therefore, focus on bit-by-bit detectors.

All of the multi-Gbps wireline applications shown in Fig. 2.1 have behaviorally similar channel responses. The capacitively-coupled link in \([L. 05]\), the inductively-coupled link in \([K. 03],[N.M08]\), and the burst mode link in \([M. 05]\) are all dominated by a first-order highpass characteristic with a cutoff frequency of 1 to 5 times the bit rate, \(f_{Bu}\). As a result, transitions in the transmitted data appear as narrow electrical pulses at the receiver while consecutive identical bits result in no signal at the receiver.

Measured and modeled responses of such an AC coupled channel are shown in Fig. 2.2 for a 50-fF coupling capacitor and 50-Ohm termination resistor. The channel suffers from 40 dB of loss at 0.05\(f_{Bu}\) and more than 15 dB of loss at 2.5\(f_{Bu}\). The measured capacitively coupled channel response closely follows an ideal 1-D channel within the band of interest (DC-6 GHz). Corresponding time domain signals with NRZ transmitted data are shown in Fig. 2.3. Note that unlike modern magnetic storage
channels, only a small amount of ISI is introduced. However, the sensitivity of the receiver has to be sufficient to capture the small received pulses. Modern AC coupled channels uses small coupling capacitance (< 500 fF). Such small capacitance with the termination resistance creates the high pass pole above 5 GHz. As a result the pulse width of the step response is less than 1 UI which indicates negligible ISI. However, downside of using such small capacitance is the small signal amplitude at the receiver input. In this case, for a 50 fF coupling capacitor and 10 Gb/s data, the signal suffers more than 20 dB of loss which means that the receiver needs to detect only few tens of mV. Since the received pulse width is only a fraction of the bit period, receiver circuits will generally require higher gain and bandwidth than a NRZ receiver at the same data rate without ac coupling. Furthermore, the received signal is a 3-level signal, so additional decoding is needed to recover the transmitted data.

Different applications of 1 − D signaling have different requirements. Chip-to-chip links require low power and area-efficient circuits with moderate sensitivity and dynamic range. On the other hand, a burst mode PON application requires higher sensitivity and fast recovery. Without targeting a specific application, this work first explore 1 − D receiver architectures which can be adapted to meet the requirements of either application. The bottleneck that limits the maximum achievable speed of this type receiver is then identified. Improved receiver architecture is then proposed that obviates
These receiver architectures are implemented and compared for two particular applications: In the first implementation we target 40 mV sensitivity and >10 dB dynamic range which is required for G-PON systems [T. 07]. The two receivers implemented in 0.18 um CMOS serve as experimental validation of the theoretical discussion regarding full-rate and half-rate architectures. Their relatively high sensitivity requires large pre-amp gain, hence increases power consumption. Thus the implemented full-rate and half-rate prototypes in 0.18 um CMOS consumes 72 mW and 110 mW for 3.33 Gb/s and 5 Gb/s respectively. Although this power consumption is comparable to other existing burst mode receivers[M. 06], chip to chip links require much lower power consumption.

For chip-to-chip interconnects, we target 80 mV sensitivity and higher bit-rate(10+ Gb/s). To improve power efficiency and achieve higher speed we implement the proposed receivers in 90nm CMOS. An implemented full-rate architecture consumes 32 mW and operates upto 10 Gb/s without any equalization. On the other hand simulated half-rate architecture consumes 50 mW and operates upto 16.67 Gb/s. Achieved
power efficiencies of 3.2 mW/Gb and 3.0 mW/Gb are comparable to the DC coupled receivers at these speeds.

2.3 1-D receiver architecture

In this section, dicode (1-D) partial response bit-by-bit receiver architectures are reviewed.

2.3.1 Decision feedback equalization (DFE)

For un-coded binary data transmitted over a 1-D channel, the data can be recovered using a 1-tap decision feedback equalizer, as shown in Fig. 2.4 [R. 78][J. 88]. In this architecture the received signal, \( s(n) = z(n) - z(n-1) \), is compared to a threshold level that is updated based on the immediate previous bit.

\[
v_{th}(n) = \beta V(n-1)
\]  

(2.1)

A hardware efficient implementation of this technique is discussed in [R. 04][L. 05] where this functionality can be achieved at high speed utilizing a hysteresis latch. Compared to a conventional DFE, this architecture provides several advantages: (i) Since there is no clock required, this architecture can be implemented with less complexity and lower power consumption. (ii) Since there is no D-FF in the feedback path, it will settle faster than a clocked 1 tap DFE. However, there is still a feedback path that must settle and the highest achievable speed of this architecture is generally also limited by the settling time of that loop which must be less than 1 UI.

2.3.2 Full-rate pre-coder and decoder

A pre-coding method for 1-D partial response channel is proposed in [M. 70]. The pre-coder output, \( y \), is related to the data to be transmitted, \( z \), by:

\[
y(n) = z(n) \oplus y(n-1)
\]  

(2.2)
One possible architecture is shown in Fig. 2.5. A similar architecture was presented for a duobinary \((1 + D)\) channel in [J. 04a] and more recently discussed in [M. 08b]. The decoder converts the 3- level received signal, \(s(n)\), to a 2 level binary output using the following decision criteria:

\[
|S(t)| > |V_{th}| \implies v(n) = 1 \quad (2.3)
\]
\[
|S(t)| < |V_{th}| \implies v(n) = 0 \quad (2.4)
\]

This is accomplished using a conventional peak detection receiver shown in Fig. 2.5. It may be shown that, in the absence of noise causing decision errors, \(v(n) = z(n)\).

In some applications, such as burst mode Passive Optical Network (PON) systems, where the transmitter does not provide the pre-coding functionality, the pre-coder can be moved to the receiver side as shown in Fig. 2.6. The thresholds, \(V_{th}\), are chosen so that the received signal amplitude, \(|s|\), only exceeds \(|V_{th}|\) when there has been a
transition in the transmitted bit stream. \( i.e. \ z(n) \neq z(n-1) \). In this case,

\[
\begin{align*}
  u_1(n) &= z(n)\overline{z(n-1)} \\
  u_2(n) &= \overline{z(n)}z(n-1)
\end{align*}
\]

Hence, the output of the first XOR operation is,

\[
w(n) = u_1(n) \oplus u_2(n) = z(n) \oplus z(n-1)
\]

and the decoder output \( v(n) \) is

\[
v(n) = v(n-1) \oplus w(n) = v(n-2) \oplus w(n-1) \oplus w(n)
\]

Using (2.7) and (2.8), the decoded output \( v(n) \) can be expressed as a function of transmitted symbol \( z(n) \):

\[
v(n) = z(n) \oplus v(n-2) \oplus z(n-2)
\]

This equation can be iteratively extended back in time to the first transmitted symbol to time \( n = 0 \):

\[
v(n) = z(n) \oplus v(0) \oplus z(0)
\]

Thus if the initial transmitted symbol \( z(0) \) and initial decoder output \( v(0) \) are the same, equation (2.10) reduces to \( v(n) = z(n) \) and the decoder output is indeed equal to the transmitted data. Comparing the transceiver architectures in Fig. 2.4, Fig. 2.5
Figure 2.7: The proposed half-rate receiver architecture for 1-D partial response signaling.

and Fig. 2.6, the highest achievable speed is always limited by the delay of a feedback loop which must be one bit period or less.

2.3.3 Receiver with half-rate decoder

To ease the settling-time requirements of all the above architectures, the half-rate decoder is introduced shown in Fig. 2.7. This architecture is a natural progression from the one shown in Fig. 2.6, where the feedback loop is shifted before the XOR operation.

The operation of the half-rate receiver in Fig. 2.7 is best understood by recognizing that the top path, through \( u_1 \) and \( w_1 \), is responsible for receiving positive peaks in \( s \), whereas the bottom path through \( u_2 \) and \( w_2 \) receives only the negative peaks in \( s \). Every positive peak in \( s \) (corresponding to a rising-edge of \( z \)) must be followed by a negative peak (corresponding to a falling-edge of \( z \)). Hence, the top path can never be active in two consecutive bit periods. Similarly, all negative peaks are followed by a positive peak, so the negative path is never active for two bit periods in a row. Hence, the feedback loops have twice as long to settle: 2 UI. The front-end of the receiver is unchanged from Fig. 2.6, so equations (2.5) and (2.6) are still valid. Now the decoder output \( w_1(n) \) and \( w_2(n) \) can be written as:

\[
    w_1(n) = w_1(n - 1) \oplus (z(n)z(n - 1)) \tag{2.11}
\]

\[
    w_2(n) = w_2(n - 1) \oplus (z(n)z(n - 1)) \tag{2.12}
\]
The full-rate decoded output \( v(n) \) is then related to \( w_1(n) \) and \( w_2(n) \) as follows:

\[
v(n) = w_1(n) \oplus w_2(n)
= (w_1(n) \oplus (z(n)z(n-1))) \oplus (w_2(n) \oplus (z(n)z(n-1)))
\]  

(2.13)  

(2.14)

Note that,

\[
(z(n)z(n-1)) \oplus (z(n)z(n-1)) = z(n) \oplus z(n-1)
\]  

(2.15)

Substituting (2.15) into (2.14),

\[
v(n) = w_1(n-1) \oplus w_2(n-1) \oplus z(n) \oplus z(n-1)
= v(n-1) \oplus z(n) \oplus z(n-1)
\]  

(2.16)  

(2.17)

similarly \( v(n-1) \) can be written as:

\[
v(n-1) = v(n-2) \oplus z(n) \oplus z(n-2)
\]  

(2.18)

substituting (2.18) into (2.17) results in,

\[
v(n) = z(n) \oplus v(0) \oplus z(0)
\]  

(2.19)

Thus the decoder can correctly recover the transmitted symbol \( v(n) \) if the initial decoder output and initial transmitted symbol are the same, \( v(0) = z(0) \), the same requirement obtained for the full-rate architecture in Fig. 2.6. Notice that pulses are generated at \( u_1 \) (\( u_2 \)) whenever a rising (falling) edge is observed on the channel data, \( z \). Hence, these signals can be used as inputs to a phase detector in a conventional clock recovery loop. Alternatively, they can be used to injection-lock an oscillator in the simulations of section 2.5.

In summary, present low complexity 1-D decoders generally include feedback loops which must settle in less than 1 UI. However, this requirement can be relaxed by using the half-rate architecture proposed in Fig. 2.7. The remainder of this paper describes a prototype of the half-rate decoder and compares it to a full-rate decoder in the same
2 Highspeed 1-D Receiver Architecture in CMOS

Figure 2.8: (a) Receiver architecture from [M. 07] (b) Hysteresis latch from [M. 05] (c) Proposed hysteresis latch

technology. Error propagation of such receivers is same as a conventional DFE. Just as in DFE-based partial response receivers, so long as a sufficiently low Bit Error Rate (BER) is maintained there is no observable degradation performance.

2.4 Full-rate Bit-by-Bit detection

The receiver architecture shown in Fig. 2.8(a) was introduced in [M. 07]. Notice the linear amplifier in parallel with the Hysteresis latch, which improves the receiver’s overall speed. With this in place, the receiver’s speed is determined by the settling time of the hysteresis latch, and the bandwidth of the pre-amplifier.
2.4.1 Implementation

In the hysteresis latch, the received signal is compared to a threshold level provided by a feedback path. The polarity of the threshold is determined by the most recently detected bit. The circuit used for this purpose in [M. 05] is shown in Fig. 2.8(b). This circuit demonstrates hysteresis, if the following condition is satisfied:

\[ g_m R_L > 1 \]  \hspace{1cm} (2.20)

where, \( g_m \) is the small signal transconductance of the feedback differential pair. In practice, to ensure operation in the presence of noise and process variations, \( g_m R_L \) is made nominally greater than 2. In addition, to accommodate both large and small inputs, the threshold levels should be adjustable. However, this simple circuit suffers from two main challenges. First, the critical output node is heavily loaded by the capacitance of \( g_m \) and the following stages which limits its settling time. To reduce the time constant at the critical nodes cascode devices were used. Due to this transistor stacking VDD was increased to 2.5 V in a 0.13-\mu m CMOS process. In this work the time constant is improved within the process nominal VDD. The second challenge with using the hysteresis circuit in Fig. 8(b) is that adjusting the threshold level will also effect other aspects of the design, such as its settling time. Hence, to provide programmability several copies of the circuit were operated in parallel in [M. 06]. The proposed circuit is shown in Fig. 2.8(c). An additional differential pair, \( g_{m2} \), is introduced in the latch which provides several advantages: First, note that the condition for hysteresis is now,

\[ g_{m1} R_1 g_{m2} R_H > 1 \]  \hspace{1cm} (2.21)

Compared with the condition for the previous circuit in (2.22), there is additional flexibility to choose gain of each stage, \( R_1 \) and \( R_H \) to minimize the settling time. Second, \( g_{m2} \) also works as a buffer between the critical node and the following stages. Finally, this architecture also allows adjustment of the threshold levels, as shown in Fig. 2.9(a).

Also note the use of a “split-load” at the output [Y. 99] so that the feedback is taken
from the fast-settling node with low impedance while the output is taken from the node with larger swing. Hence, the feedback loop settling time is dominated by the time constant \( R_H C_H \) whereas the “output settling time” is dependent on the time constant \((R_1 + R_2)C_L\). This allows design flexibility and relaxes the tradeoffs between speed, sensitivity and noise immunity. Detail implementation of this latch is discussed in section 4.2.1 with the Fig. 4.3. Simulations of the hysteresis latch in Fig. 9(b) indicate that the split-load improves the settling time by >20% in this circuit. The targeted sensitivity of the receiver is 40mV differential input. The hysteresis comparator thresholds can be adjusted from 150mV to 400mV differential input. In PON applications, the receiver threshold can be adjusted based on a training preamble which precedes each data burst.

A 5 stage pre amplifier providing 24 dB differential gain is used in front of the hysteresis latch. Budgeting 30mW of power for the pre amplifier, without inductive peaking the achieved bandwidth is only 2.5 GHz resulting in excessive data-dependent jitter. Hence, inductive peaking was used to extend the bandwidth to 3.5 GHz.

2.4.2 Experimental results

A die photo of the receiver front end is shown in Fig. 10. Measurements were made with a channel comprising an approximately 3-ft long SMA cable and a 50-fF ac-coupling capacitor on-chip which, together with the 50-Ohm on-chip termination, forms the high-pass filter characterized in Fig. 2 and 3. The measured results are obtained with single ended excitation only. The receiver’s dynamic range was tested by varying the input amplitude from 40mV to 200 mV. For a 40 mV input, the threshold level was adjusted to 70 mV, and for a 180 mV input, the threshold level was adjusted to 180 mV. The receiver demonstrated error-free data recovery at 3.3 Gb/s for a PRBS 2^{10} – 1 pattern at both signal amplitudes (Fig. 2.11(a) and Fig. 2.11(b)).
2.5 Half-rate detection

The speed of the architecture in section III is limited by the finite bandwidth of the pre-amplifier and the threshold settling time. To further increase the speed of $(1-D)$ partial response receivers, the parallel half-rate architecture described in section II is used. The block diagram of a CMOS implementation of this architecture is shown in Fig. 2.13. The front end is comprised of two major circuit blocks: a slicer and a toggle flip-flop (T-FF). The T-FF provides the feedback and XOR operation shown in each
2 Highspeed 1-D Receiver Architecture in CMOS

Figure 2.10: Full-rate receiver die photo in 0.18 um CMOS

path of Fig 2.7. The circuit outputs Demux1 and Demux2 correspond to $w_1$ and $w_2$ in Fig 2.7. These may be XORed to recover the full-rate data or further demultiplexed for digital decoding at a much slower rate. One possible implementation is shown in Fig 2.13, where recovered half-rate clock is used to further demultiplex Demux1 and Demux2. These demuxed bit streams are then XORed at a half-rate to decode even and odd bit streams. Half-rate clock can be recovered from the transition information provided by $u_1$ and $u_2$.

2.5.1 Implementation

The first stage of the slicer is a differential difference amplifier that compares the input to $V_{th}$. The detected pulses are then passed through 5 inductively-peaked amplifier stages providing 26 dB gain. Fortunately, due to the half-rate architecture lower bandwidth can be tolerated here than in the full-rate pre-amplifier. Hence, the total current consumption is only 9 mA from a 1.8 V supply for each amplifier chain providing 2.2 GHz bandwidth.

High speed T-FFs have been widely used as dividers in both wireline and wireless applications. Conventional CML T-FFs employ two back-to-back D-latches as shown in Fig. 2.13(d). A typical implementation of the D latch is shown in Fig. 2.14(a). This type of T-FF exhibits self oscillation which allows it to operate as a high-frequency divider. A typical sensitivity curve is shown in Fig. 2.14 (a). Unfortunately, noise around the self-oscillation frequency can cause the output to toggle erroneously during
Figure 2.11: Measured output eye of the full-rate receiver at 3.3 Gb/s for different input amplitude (a) 40 mV (b) 200 mV

periods when there is no transition in the received data, resulting in bit errors in the decoded sequence. Thus self oscillation in the T-FF must be avoided to use it as a decoder in this application. In addition, the buffer $A_L$ is needed to drive a capacitive load without loading the latch nodes.

To alleviate both of these problems, the buffer is brought within the feedback loop as shown in Fig. 2.14(b). The gain of $A_L$ is easily made adjustable to allow variable latching strength and, hence, T-FF sensitivity. The modified architecture provides frequency-independent sensitivity characteristics, as shown in Fig. 2.14(b). Further-
Figure 2.12: Results for a PRBS $2^{10}−1$ pattern: (a) a segment of the transmitted and recovered sequences and (b) BER bathtub plot

more stage $A_L$ effectively buffers the critical latch node and eliminates the requirement of an additional buffer.

Thus the proposed latch circuit does not consume additional power compared to a
2.5.2 Experimental results

A prototype receiver in 0.18 um CMOS is shown in Fig. 2.15. In this implementation same 50 fF coupling capacitor and 50 ohm resistance are used as a highpass filter to provide the 1-D partial response. The receiver provided error-free operation for a PRBS $2^{10} - 1$ pattern up to 5Gb/s. Eye diagrams of the demultiplexed outputs at 3.33 Gb/s and 5 Gb/s are shown in Fig. 2.16 and Fig. 2.17 respectively. Portions of actual PRBS $2^{10} - 1$ transmitted and recovered sequences are shown in Fig. 2.18. Note that none of the eye diagrams show any ringing which indicates that the proposed T-FF implementation strongly suppresses self oscillation.
2.6 90nm implementation

For chip-to-chip applications, the sensitivity and dynamic range requirements are relaxed. 80 mV sensitivity is targeted in a 90-nm CMOS process resulting in greatly improved power-efficiency. No inductors were used in these designs as chip-to-chip applications demand compact circuitry.

2.6.1 Full-rate Bit-by-Bit detection

The full-rate architecture of section III achieves 80 mV sensitivity with a 5-stage preamplifier that consumes only 10 mW. The hysteresis latch consumes 7 mW and operates up to 10 Gb/s. For experimental study the implemented full-rate receiver in [M. 07] is used. Similar to section III, only non-linear path is used for NRZ recovery. Due to
the relaxed dynamic range, a fixed threshold in the latch is used. Recovered NRZ data measured with the same channel as in sections III and IV is shown in Fig. 2.19 at 10 Gb/s. The total power consumption is 32 mW from a 1.2-V supply.

2.6.2 Half-rate receiver

Simulations of the half-rate architecture in 90-nm CMOS are used to demonstrate: (a) a speed improvement over the full-rate architecture, commensurate with that observed in 0.18-um CMOS, is possible; and (b) clock recovery and 1:2 demultiplexing is readily feasible within this architecture. The same circuits described in Fig. 2.13 are ported to a 90-nm process. Following the T-FF, all remaining circuitry is implemented using full-swing CMOS logic. The Spectram of the signals $u_1$ and $u_2$ contain tones at the baud rate which can be utilized for clock recovery using a PLL. Phase locking can also be done using an injection locked oscillator or gated VCO which provides the fast locking required for burst mode applications. Injection locking a half-rate clock relaxes the VCO design compared to a full-rate VCO. In the proposed architecture the signals $u_1$ and $u_2$ are used to injection-lock a half-rate ring oscillator which operates
at 8.33 GHz. The recovered half-rate clock is then used to demultiplex and retime the data. Proper recovery of the even and odd data is demonstrated using this technique in simulations at 16.67 Gb/s in Fig. 2.20. This represents a 67% increase in data rate over the full-rate measurements, which is very comparable to the measurement results from the 0.18-um prototypes where the half-rate architecture offered a 50% increase in data rate, from 3.3 Gb/s to 5 Gb/s. The total simulated power consumption, including clock recovery, demultiplexing, and required logic, is 110 mW from a 1.2-V supply.

Figure 2.16: Measured de-muxed eye at 3.3 Gb/s
2.7 Conclusion

In recent years, there has been significant effort to improve sensitivity and speed of AC coupled receivers. This trend is driven by desires to use small ac-coupling capacitors, achieve higher data rates, and/or accommodate lossy channels. Thus high preamp gain and bandwidth are required at the cost of additional power and area. A more detailed comparison of the proposed receivers and state-of-the-art receivers with high sensitivity is given in Table 2.1. Sensitivity is measured by the minimum signal amplitude required
Figure 2.18: Transmitted and de-muxed data streams: demuxed data streams are overlaid to demonstrate the decoding functionality

Figure 2.19: Recovered 10 Gb/s NRZ eye from full-rate receiver implemented in 90 nm CMOS

for error free detection at receiver. For comparison of different implemented receivers, a Figure of Merit (FoM) is used, which is defined as:
Table 2.1: Comparison of state-of-art 1-D receivers

<table>
<thead>
<tr>
<th></th>
<th>[M. 06]</th>
<th>[L. 05]</th>
<th>This work</th>
<th>This work</th>
<th>This work</th>
<th>This work</th>
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</thead>
<tbody>
<tr>
<td><strong>Full-rate</strong></td>
<td>0.13um</td>
<td>0.18um</td>
<td>0.18um</td>
<td>0.18um</td>
<td>90nm</td>
<td>90nm</td>
</tr>
<tr>
<td><strong>Half-rate</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Technology</strong></td>
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<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td><strong>Channel</strong></td>
<td>On-chip L-R</td>
<td>Proximity coupled</td>
<td>On-chip C-R</td>
<td>On-chip C-R</td>
<td>On-chip C-R</td>
<td>On-chip C-R</td>
</tr>
<tr>
<td><strong>Pre-amp Gain</strong></td>
<td>26 dB</td>
<td>—</td>
<td>23 dB</td>
<td>22 dB</td>
<td>17 dB</td>
<td>17 dB</td>
</tr>
<tr>
<td><strong>Bit-rate</strong></td>
<td>10 Gb/s</td>
<td>3 Gb/s</td>
<td>3.33 Gb/s</td>
<td>5Gb/s</td>
<td>10 Gb/s</td>
<td>16.67 Gb/s</td>
</tr>
<tr>
<td><strong>VDD</strong></td>
<td>2.5 V</td>
<td>1.8 V</td>
<td>1.8 V</td>
<td>1.8 V</td>
<td>1.2 V</td>
<td>1.2 V</td>
</tr>
<tr>
<td><strong>Receiver Power Consumption</strong></td>
<td>500mW Includes Logic + Buffer power</td>
<td>10mW Includes buffer power</td>
<td>110mW Includes buffer power</td>
<td>32mW</td>
<td>50mW with clock recovery (110mW)</td>
<td></td>
</tr>
<tr>
<td><strong>Area</strong></td>
<td>2.72mm²</td>
<td>—</td>
<td>0.97mm²</td>
<td>1.08mm²</td>
<td>0.045mm²</td>
<td>—</td>
</tr>
<tr>
<td><strong>Sensitivity</strong></td>
<td>40 mV</td>
<td>120 mV</td>
<td>40 mV</td>
<td>40 mV</td>
<td>80 mV</td>
<td>80 mV</td>
</tr>
<tr>
<td><strong>FoM(pJ/Bit)</strong></td>
<td>50</td>
<td>3.33</td>
<td>21.8</td>
<td>22</td>
<td>3.2</td>
<td>3.0</td>
</tr>
</tbody>
</table>

\[
\text{FoM(pJ/Bit)} = \frac{\text{Power consumption}}{\text{Bit rate}}
\]  

Compared to the 10 Gb/s receiver, the presented full-rate and half-rate receivers achieve similar sensitivity with significant power reduction. On the other hand, power and area efficiency can be further improved in 90nm implementation. Compared to full-rate architectures, the proposed half-rate architecture can potentially achieve twice the speed at the cost of additional hardware complexity and power. In this work, a 50% improvement in speed is achieved at the cost of a 30% increase in power. Clearly, the half-rate architecture is particularly useful when the targeted speed is not achievable.
Figure 2.20: Transistor level simulation results of the 90-nm half-rate receiver at 16.67 Gb/s. Even samples are generated by the rising edge of the recovered clock (dashed arrow) and odd samples are generated by the falling edge (solid arrow)

Another potential application of the half-rate architecture is for clock-less demultiplexing which was proposed for burst mode applications in [B. 05] to relax the lock time requirements of the subsequent clock and data recovery circuitry. In [B. 05], a finite state machine performs sophisticated processing resulting in high power consumption. On the other hand, the half-rate receiver proposed in this work demultiplexes the bit stream based on edge detection which in this work is actually performed by the passive 1-D channel, thus providing reduced power consumption.
3 Low Power Clock Generation and Clock Deskew Techniques

3.1 Introduction

The energy efficiency of high-speed parallel I/Os is limited by the power consumption of the clocking circuits including clock source, buffers, delay elements and duty cycle correctors. To reduce the power consumption per link, a shared clock source may be used where the phase of the VCO is locked to an external low-jitter reference [H. 03b][B. 06]. Due to the significant capacitive loading on the clock distribution network, several CML and CMOS inverters are used as buffers [F. 06]. In this work, we propose a VCO with an inherent buffer that re-uses the VCO bias current and provides large driving capacity without additional power consumption. Section 3.2 will discuss low power VCO architectures: Colpitts, cross-coupled and proposed VCO. Implementation and experimental results will also be given in this section.

Each link’s receiver must compensate for the link’s skew with a deskew circuit [R. 05][C. 06b] (Fig. 3.1). Apart from phase alignment, the deskew block also provides amplification, duty cycle correction and jitter filtering to recover high quality clock. An injection locked oscillator (ILO) is an efficient way of providing all these functionalities; by detuning the oscillator’s free-running frequency away from the input frequency, a controlled phase shift is introduced to the clock path [L. 06]. A problem with this approach has been that for large phase shifts considerable variation is observed in the jitter tracking bandwidth and output clock amplitude [F. 08]. In this work, by selectively injecting either one or the other side of a quadrature VCO (QVCO), the required phase adjustment range is cut in half. Section 3.3 will provide some theoretical ground work for ILO-based clock deskewing, demonstrating that the variation in jitter
3 Low Power Clock Generation and Clock Deskew Techniques

Figure 3.1: Shared clocking for high density I/O [1-4].

Figure 3.2: (a) Conventional cross-coupled LC VCO (b) Equivalent half circuit

tracking bandwidth is fundamental to both LC and ring ILOs. Following that, section 3.4 will discuss the deskew technique including experimental results for both LC and ring oscillators.

3.2 Background

We will first discuss two existing LC VCO topologies: cross-coupled and Colpitts. Finally, the proposed architecture which combines the benefit of both topologies will be discussed.

3.2.1 Cross-Coupled oscillator

A cross-coupled LC VCO topology and its equivalent half circuit is shown in Fig. 3.2. Here, the ideal gain of -1 is furnished by the cross-coupling to provide a negative
resistance of $-g_m$. The tank consists of an inductor $L$ and tunable capacitance $C_{var}$. The tank loss is mainly dominated by the inductor series resistance $R_S$ which also determines the inductor quality factor $Q_L = \omega L / R_S$. The series resistance $R_S$ can be converted to its parallel equivalent, $R_P = (Q_L^2 + 1) R_S$. To meet the oscillation condition, the negative resistance must compensate the tank loss:

$$g_m \geq \frac{1}{R_P} \approx \frac{Q_L}{\omega_0 L (Q_L^2 + 1)}$$  \hspace{1cm} (3.1)

In the above expression $Q_L$ is the quality factor at the resonance frequency, $\omega_0$. Assuming this condition is met, the oscillation frequency is determined by the inductance and the capacitance of the tank,

$$\omega_0 \approx \frac{1}{\sqrt{LC_{eq}}} = \frac{1}{\sqrt{L(C_{var} + C_L)}}$$  \hspace{1cm} (3.2)

Here, $C_L$ models any additional capacitance connected to the tank node. The tank amplitude ($V_{tank}$) is related to the dissipated energy at the tank ($E_{tank}$) by the energy conservation theorem,

$$V_{tank}^2 = 2E_{tank}/C = 2E_{tank}\omega_0^2 L$$  \hspace{1cm} (3.3)

The expression indicates that in the current limited region, for a given energy, tank swing increases with inductance. The design and optimization of cross-coupled oscillators are governed by above equations (3.1-3.3). As explained in [M. 01], for a given frequency (i.e. $LC_{eq}$ constant), increasing $L/C_{eq}$ results in higher tank impedance at resonance and as a result oscillation amplitude increases. Thus one can maximize $L/C_{eq}$ ratio to achieve larger tank swing, lower phase noise and lower power consumption [M. 01]. This optimization technique is useful until the oscillator’s voltage swing is limited by supply headroom constraints. Beyond that, increasing $L/C_{eq}$ can degrade VCO performance [D. 01]. However, applying this approach to a 20+ GHz VCO design in 0.13 um CMOS results in a very small $C_{eq}$. Since most of $C_{eq}$ will be consumed by the load capacitance $C_L$, the varactor must be made small resulting in small tuning range [K. 07]. On the other hand, reducing the $L/C_{eq}$ ratio significantly compromises
3. Low Power Clock Generation and Clock Deskew Techniques

Figure 3.3: (a) Conventional Colpitts VCO (b) Modified Colpitts VCO (c) Equivalent half circuit

tank amplitude, phase noise and power consumption. An additional buffer stage is often used to reduce $C_L$ at the cost of additional power consumption.

3.2.2 Colpitts VCO

Colpitts VCOs, are widely used in wireless applications due to their robustness to parasitics. Fig. 3.3 shows the single ended implementation of two variants of the Colpitts VCO: Fig. 3.3(a) is the well known conventional Colpitts and Fig. 3.3(b) is a CMOS implementation of the bipolar microwave oscillator discussed in [N. 92]. The implementation in Fig. 3.3(b) provides inherent buffering [N. 92]: the tank is coupled to the load only through $C_{GD}$, whereas, in 3.3(a) the load capacitance ($C_L$) is directly across the tank. This is the main advantage of this modified Colpitts VCO. Considering $g_m$ as the small-signal transconductance of $M_1$ and ignoring the effect of $C_{GD}$, the input impedance ($Z_{in}$) looking into the gate of $M_1$ can be written as:

$$Z_{in} = \frac{-g_m}{\omega^2 C_1 C_{var}} + \frac{1}{j\omega} \left( \frac{1}{C_1} + \frac{1}{C_{var}} \right)$$  \hspace{1cm} (3.4)
This leads to the equivalent circuit representation as shown in Fig. 3.3(c). If $R_S$ models series tank losses, the condition to ensure oscillation of the Colpitts VCO is:

$$\frac{g_m}{\omega^2 C_1 C_{var}} \geq R_S$$  \hspace{1cm} (3.5)

The frequency of oscillation can also be derived from the equivalent circuit shown in Fig. 3.3(c):

$$\omega_o \approx \frac{1}{\sqrt{L C_{eq}}} = \frac{1}{\sqrt{L C_1 C_{var}}}$$  \hspace{1cm} (3.6)

Note that, unlike the cross-coupled topology, the oscillation frequency is independent of load capacitance ($C_L$), which signifies the inherent buffering of the modified Colpitts oscillator. The oscillation condition can be written as a function of the equivalent parallel resistive losses $R_P$

$$g_m \geq \frac{\omega_o^2 L (C_1 + C_{var})}{R_P}$$  \hspace{1cm} (3.7)

Combining (3.6) and (3.7), the oscillation condition can be written as:

$$g_m \geq \frac{1}{R_P} \frac{(C_1 + C_{var})^2}{C_1 C_{var}}$$  \hspace{1cm} (3.8)

The factor $(C_1 + C_{var})/(C_1 C_{var})$ can be minimized by choosing $C_1 = C_{var}$, which leads to the minimum required transconductance to ensure oscillation: $g_m = 4/R_P$. Compared to the cross-coupled topology, the Colpitts oscillator requires 4x additional transconductance which translates into significant additional power consumption. This becomes a concern in wireline applications such as high-speed I/Os, where typically the inductor Q is less than 5.

In summary, the Colpitts topology provides good tuning range and output power but consumes a lot of power. On the other hand, cross-coupled VCOs consume less power, but require an additional buffer and are more susceptible to load parasitics [K. 06].
3.2.3 Proposed VCO

Cross-coupled and Colpitts VCOs have been previously combined in [R. 02] as shown in Fig. 3.4. In [R. 02], the bottom cross-coupled pair is used to relax the oscillation condition and improve noise performance. However, note that the tank in this case incorporates the VCO’s output node making it impossible for this topology to be used to directly drive large capacitive or small-resistance loads. The circuit behaves basically as a Colpitts oscillator with improved noise performance. In this work the oscillations are sustained mainly by $M_1$ which is designed to contribute larger negative resistance than $M_2$, hence it primarily behaves as a cross-coupled oscillator but the tank buffered from the load by $M_2$.

In this work we proposed the topology shown in Fig. 3.5, which combines the useful properties of both Colpitts and cross-coupled VCO topologies: the inherent buffering of the Colpitts VCO and the low-power oscillation of the cross-coupled VCO. In this architecture, transistor $M_2$ is introduced in the tank to provide several functionalities: (a) as in the modified Colpitts topology, it decouples the LC tank from the load capacitance; (b) it provides a negative resistance which relaxes the oscillation condition and improves the effective $Q$ of the tank; and (c) unlike the cross-coupled oscillator, the buffer capacitance $C_{GS}$ is in series with $C_{var}$. For small $C_{var}$ and $C_{eq}$, as in the case of
20+ GHz VCOs, this combination can absorb more buffer capacitance and still maintain the required tuning range. Effectively, $M_2$ serves as a buffer which can directly drive 50-ohm or large capacitive loads. Since it uses the same VCO bias current, there is no additional DC power consumption. Output signal swing is determined by the VCO current and load impedance. $R_L = 50\Omega$ provides direct output matching at the cost of headroom. If higher output swing is required, high impedance tuned load can be used. To maximize the swing and to avoid additional noise contribution, we do not include a current source in the bottom of the cross-coupled differential pair [M. 01]. This poses no problem if the power supply is well decoupled or regulated.

To identify the effect of $M_2$ on tank impedance, the equivalent circuit is drawn in Fig. 3.5(b), from which the following nodal equations may be written.

\begin{align}
  i_x &= -v_1(g_{m2} + sC_{GS}) \quad (3.9) \\
  v_x &= -v_1(1 + s^2LC_{GS}) \quad (3.10)
\end{align}

The equivalent admittance looking into the source of $M_2$ is

\begin{equation}
  y_x = \frac{i_x}{v_x} = \frac{g_{m2} + sC_{GS}}{1 + s^2LC_{GS}} \quad (3.11)
\end{equation}
If $R_P$ models total tank losses, the equivalent tank admittance is

$$y_{tank} = y_x + y_{varactor} + y_{loss} \approx \frac{g_{m2} + s(C_{GS} + C_{var} + s^2LC_{GS}C_{var})}{1 + s^2LC_{GS}} + \frac{1}{R_P} \quad (3.12)$$

At resonance, the tank admittance must be real. Thus, the oscillation frequency can be found by equating the imaginary part to zero,

$$\omega_{osc} = \frac{1}{\sqrt{LC_{eq}}} = \frac{1}{\sqrt{L\frac{C_{GS}C_{var}}{C_{GS} + C_{var}}}} \quad (3.13)$$

To sustain oscillation at this frequency, the bottom cross-coupled transistors must provide sufficient negative resistance to overcome the tank losses,

$$g_{m1} + \frac{C_{var}}{C_{GS}}g_{m2} \geq \frac{1}{R_P} \quad (3.14)$$

This oscillation condition is same as the cross-coupled case with one additional factor: the negative resistance contributed by $g_{m2}$, which allows additional power savings. Note that there are two sources of negative resistance here: the bottom cross-coupled pair provide a negative transconductance, $-g_{m1}$ and the top transistors $M_2$ provide $-(C_{var}/C_{GS})g_{m2}$. As a result this oscillator has two possible modes of operation: (i) as a Colpitts VCO, when the negative resistance provided by $M_2$ is sufficient to compensate the tank losses, similar to [R. 02]; or (ii) as a cross-coupled VCO, when the negative resistance due to $M_1$ dominates the oscillation condition. The cross-coupled mode of oscillation requires less power consumption, and hence is the main focus of this work. In this configuration $C_{var}/C_{GS}$ is chosen to provide sufficient tuning range and $M_2$ is sized such that its gate drain capacitance is small enough to isolate the tank from the output nodes. As a result, the negative resistance of the top transistors is less than 30% of that contributed by the bottom pair. The effective quality factor ($Q_{tank}$) for this equivalent tank can be expressed as:

$$Q_{tank} \approx \frac{\text{Re}\{Z_{tank}\}}{\omega_0 L} = \frac{1}{\omega_0 L (\frac{1}{R_P} - \frac{C_{var}}{C_{GS} g_{m2}})} \quad (3.15)$$
It is useful to express this effective tank quality factor in terms of inductor quality factor, \( Q_L = \omega_0 L / R_S \).

\[
Q_{tank} \approx \frac{Q_L}{1 - R_P \frac{C_{var}}{C_{GS}} g_{m2}} \tag{3.16}
\]

Note that, in the absence of transistor \( M_2 (g_{m2} = 0) \), the tank quality factor is equal to the inductor quality factor. However, in the presence of \( M_2 \), it is possible to improve the tank quality factor well beyond \( Q_L \). For example, consider a 500 pH inductor with a quality factor of 4 used to design a 20 GHz VCO. Choosing \( C_{var}/C_{GS} = 0.25 \) and \( g_{m2} = 10 \) mS, we can improve the tank Q beyond 10, which results in a 2.5x improvement in tank swing. This is particularly useful when designing LC-VCOs in digital CMOS process, where the lossy substrate limits the inductor Q to approximately 4 or 5. For comparison, the proposed tank is simulated with and without \( g_{m2} \) as shown in fig. 6. Note that, the improvement in tank amplitude is a direct effect of the improved quality factor. Using similar approach as described in [A. 07a], oscillation amplitude can be derived from Fig. 3.5(b). In the current limited region, the single ended amplitude of the voltage across the inductor can be written as:

\[
V_G \approx \frac{2}{\eta \pi} \left( \frac{1}{R_P} - \frac{1}{1 - \eta G_{M2eff}} \right) I_{DC} \tag{3.17}
\]

\[
\eta = \frac{C_{var}}{C_{GS} + C_{var}} \tag{3.18}
\]

Here, \( G_{M2eff} \) is the large signal effective transconductance of the transistor \( M_2 \). The voltage across gate and source terminal of \( M_2 \) can be written as:

\[
V_{GS} \approx \frac{2(1 - \eta)}{\eta \pi} \left( \frac{1}{R_P} - \frac{1}{1 - \eta G_{M2eff}} \right) I_{DC} \tag{3.19}
\]

Simulated oscillation amplitude is in good agreement (within 15%) with these two expressions. The simulated phase noise of this 20 GHz VCO at 1 MHz offset was -105
Figure 3.6: (a) Simulated Tank with and w/o \( g_{m2} \) (b) Equivalent tank impedance (magnitude and phase) over the tuning range

Figure 3.7: Effect of load capacitance variation on (a) oscillation frequency (b) phase noise

dBC/Hz. The major noise contributors are summarized in Table 3.1. Simulation results also demonstrate that a ±20% variation in \( C_{var} \) is sufficient to provide greater than 10% tuning range. To study the effectiveness of \( M_2 \) as a buffer, we observed the VCO
Table 3.1: Phase Noise Contribution of each Noise Source

<table>
<thead>
<tr>
<th>Noise Source</th>
<th>Contribution</th>
</tr>
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<tbody>
<tr>
<td>$(M_1)$</td>
<td>42%</td>
</tr>
<tr>
<td>Inductor Loss</td>
<td>28%</td>
</tr>
<tr>
<td>$(M_2)$</td>
<td>20%</td>
</tr>
<tr>
<td>Varactor</td>
<td>6%</td>
</tr>
</tbody>
</table>

Table 3.2: VCO Topology Summary

<table>
<thead>
<tr>
<th>Topology</th>
<th>Frequency of Oscillation</th>
<th>Minimum Required $g_m$</th>
<th>Tank Quality Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cross-Coupled</td>
<td>$f_{osc} = (2\pi \sqrt{L(C_{var} + C_L)})^{-1}$</td>
<td>$\geq \frac{1}{R_P}$</td>
<td>$Q_{tank} \approx Q_L$</td>
</tr>
<tr>
<td>Colpitts</td>
<td>$f_{osc} = (2\pi \sqrt{L \frac{C_1 C_{var}}{C_1 + C_{var}}})^{-1}$</td>
<td>$\geq \frac{4}{R_P}$</td>
<td>$Q_{tank} \approx Q_L$</td>
</tr>
<tr>
<td>Proposed VCO</td>
<td>$f_{osc} = (2\pi \sqrt{L \frac{C_{GS} C_{var}}{C_{GS} + C_{var}}})^{-1}$</td>
<td>$\geq \left( \frac{1}{R_P} - \frac{C_{var}}{C_{GS} g_m^2} \right)$</td>
<td>$Q_{tank} \approx \frac{Q_L}{1 - \frac{C_{var} C_{gs}}{C_{GS} g_m^2}}$</td>
</tr>
</tbody>
</table>

Performance over a large variation of load capacitance from 100 fF to 1 pF. For $M_2 = 16$ um, the frequency variation is only 50 MHz, the phase noise variation is less than 0.5 dB, and the oscillation amplitude varies less than 3%. However, as we increase the size of $M_2$, its effectiveness as a buffer degrades. As shown in the Fig.3.7, for $M_2 = 30$ um, a load capacitance variation from 100 fF to 1 pF results in 200 MHz variation in frequency, 1.5 dB variation in phase noise and 7% variation in oscillation amplitude. Variation in the value of $R_L$ from 10 to 70 ohm has even less effect than variations in $C_L$. Larger values of $R_L$ will result in headroom issues. A comparison of key VCO parameters for all three topologies is summarized in Table 3.2, which supports the qualitative discussion: the proposed VCO essentially combines the benefits of both the cross-coupled and Colpitts topologies.
3.2.4 Cross-coupled vs proposed VCO: a design example

The advantages of the proposed VCO over a conventional cross-coupled VCO can be illustrated with a design exercise. The goal is to design a 20 GHz LC VCO with more than 15% tuning range, phase noise better than 100 dBc/Hz at 1 MHz offset with a 400 fF load capacitance and 500+ mVp-p differential output. To meet this requirement a cross-coupled VCO can be implemented as shown in Fig. 3.8:

To achieve 500 mVpp differential swing the buffer needs at least 4 mA current. The total fixed capacitance at the oscillatory node is dominated by M1 and M2 and is approximately 60 fF. An AMOS varactor’s max-min capacitance ratio is approximately 2:1. This leads to a varactor capacitance $160 \text{fF} - 80 \text{fF}$. Including the fixed capacitance, the total nominal capacitance is $120 \text{fF} + 60 \text{fF} = 180 \text{fF}$. To achieve 20 GHz oscillation, inductor L1 needs to be 350 pH. This leads to a $L/C$ ratio of 2,000 (Henry/Farad). Note that the minimum oscillation frequency is 18.2 GHz and the maximum oscillation frequency is 22.7 GHz. The bias current source is based on pMOS devices, and it is connected to the inductor center tap, as opposed to the source of the devices of the differential pair. This scheme allows to achieve a large differential output.
Figure 3.9: Proposed VCO schematic. Tank $Q$ is 5. VCO loading is approximated as 400 fF. L2 (500 pH) is a low $Q$ inductor with 50-ohm termination.

Voltage swing without the need of a dedicated supply voltage. Note that the parasitic capacitance due to the current source at the inductor central tap is not critical, and it can be conveniently used to filter out the high frequency noise contribution of the current source, avoiding its frequency down conversion and translation into phase noise.

In the proposed approach, the buffer capacitance, CGS, is in series with the varactor capacitance, Cvar. As a result the total equivalent capacitance can be written as 80 fF. This leads to an inductor L1 value at 800 pH. For the same varactor capacitance ratio 160 fF:80 fF, the minimum and maximum frequencies are 17.8 GHz and 22.9 GHz respectively. Note that the $L/C$ ratio in this case is 10,000 (Henry/Farad) which gives 5x improvement over a conventional implementation.

Next VCO performance is compared based on phase noise, tank swing and output.
signal swing at different VCO current settings. Notice that increasing the bias current increases tank swing in the current limited regime. As a result the phase noise improves - this is true for both topologies in this study. In addition, for a given bias current setting higher L/C ratio results in better phase noise, as shown in Fig. 3(a), until the VCO reaches a voltage-limited regime. Also using the regulator allows higher VCO swing which enables lower phase at 15 mA. Output swing, Vout in the cross coupled VCO is set by the buffer M2 and the corresponding trail current 4.5 mA. This additional current is not required in the proposed topology. Bias network for the proposed VCO is formed by connecting the current mirror node to the center tap of the inductor. Montecarlo simulation shows less than 5% variation of VCO current with this bias scheme. VCO’s phase noise and output swing is insensitive to this small variation of bias current. A noticeable limitation of the proposed architecture is the headroom limitation. Beyond 9 mA in the proposed VCO transistor M1 is pushed out of saturation due to limited head room and rds drops to less than 60 ohm. As a result, the effective Q of the tank is degraded and oscillations can’t be sustained. However,
the proposed VCO still meets all the design requirements consuming only 6 mA whereas the cross-coupled VCO would consume 7mA along with 4.5 mA in the buffer (total 12 mA) to meet the requirements.

### 3.2.5 QVCO Implementation

Three existing methods for generating quadrature clock signals are: a) A VCO followed by C-R, R-C filters, b) A differential VCO of twice the frequency followed by rising- and falling-edge triggered dividers, and c) A Q-VCO formed by coupling two differential VCOs. The first technique results in significant additional power consumption in the buffers driving the passive filter. The second technique requires the design of a 40 GHz VCO and dividers in 0.13 um digital CMOS which would be difficult and power consuming. Thus for quadrature signal generation at 20 GHz, we focus on the third approach: a Q-VCO. A quadrature version of the proposed VCO is implemented by coupling two differential VCOs operating at the same frequency. In-phase coupling, with a coupling factor greater than 0.25, ensures quadrature phase generation. Coupling was provided using additional devices $M_C$ (Fig. 3.11). Quadrature (4-phase) VCOs in general have several disadvantages compared to their differential (2-phase) counterparts: a) due to the additional DC power consumption in the coupling devices, the power consumption of a quadrature VCO is usually more than twice the power consumption of a differential VCO at the same frequency; b) in the quadrature implementation, both tanks operate
3 Low Power Clock Generation and Clock Deskew Techniques

Figure 3.12: Die photo of the implemented Q-VCO in 0.13 um CMOS

slightly off resonance due to mismatch which results in higher phase noise and reduced tank impedance compared to a differential implementation.

This QVCO is implemented in 0.13\(\mu\)m digital CMOS, typical for high speed I/Os (Fig. 3.12). There were 5 metal layers available with the top layer being less than 1 um thick. Poly, metal 1 and metal 2 is used as metal fill under the inductor and all metal layers (1-4) except metal 5 are used inside the inductor loop to meet the metal density. Both the single turn inductor used in the tank and the inductor in the load is built with the top Metal layer, metal 5. For a 500 pH inductor, a \(Q\) of 4 was achieved which translates to an \(R_P\) of 267 \(\Omega\). \(C_{GS}\) and \(C_{var}\) were chosen to be 360 fF and 140 fF respectively, which provide an equivalent capacitance of 100 fF. The minimum transconductance required to meet the oscillation condition was found to be 5 mS. With some safety margin, a transconductance of 10 mS was chosen with each transistor \((W_1 =16\ \text{um})\) consuming 3 mA of current. Each coupling device \(M_C\) \((W_C =5\ \text{um})\) consumes another 1 mA of current. Taking advantage of the transistor \(M_2\), no additional buffer is used and the VCO directly drives on-chip 50-ohm termination in parallel with 50-ohm off-chip termination. A 300-um length of transmission line connects the VCO outputs to probe pads. The complete Q-VCO consumes 16 mA of current from a 1.2 V supply and it can provide a clock swing of 200 mV peak-to-peak per side across 25 ohm effective loads. For comparison, we designed both Colpitts and cross-coupled
VCO with the same inductor and equivalent tank capacitances. The Colpitts VCO consumed four times additional power resulting in a total power consumption of 100 mW. On the other hand, the cross-coupled VCO consumed the same power as the proposed one. However, to provide the same swing at the load, an additional CML buffer was required, consuming an additional 16 mA of current and thus raising the total power consumption to 50 mW. Furthermore, the cross-coupled VCO had a lower tuning range because the buffer’s input capacitance is in parallel to the tuning capacitor and thus dominates the tank capacitance [K. 07].
3.2.6 Measured Results

Measured results of the QVCO are summarized in Fig. 3.13 and Fig. 3.14. The VCO can be tuned from 18.3 GHz to 20.75 GHz providing 12% tuning range. Including the on-die transmission line and pad, the total output load capacitance is estimated at 220 fF. The per-side output power measured in a 50-ohm environment varied from -11.5 dBm to -17.5 dBm over the tuning range. The reduced output power at higher frequency is due to reduced load impedance and reduced tank impedance. This also significantly increases phase noise. A captured spectra, the measured and simulated phase noise at 20 GHz is shown in Fig. 3.13. The phase noise over the tuning range is also shown in Fig. 3.13. For comparison, key performance metrics for different VCO topologies are summarized in Table 3.3. According to the ITRS 2003[Int03], the figure-of-merit for VCOs is:

\[
F_{oM} = 10 \log_{10}\left(\frac{f_{osc}}{\Delta f}\right)^2 \frac{1}{L(\Delta f)P_{diss}(mW)}
\]  (3.20)

Our earlier conclusion regarding Colpitts and cross-coupled VCOs are in good agreement with the measured results from [K. 06]: cross-coupled VCOs can achieve a significant advantage over Colpitts VCOs for low-power applications. However, this advantage is significantly compromised when the buffer is included in the performance metric. In addition, as pointed out in the previous section, there is significant performance degradation in cross-coupled QVCOs compared to their differential counterparts [S. 03b][F. 05]. Although the inductor Q in this VCO is much lower compared to the other VCOs listed in the table, this VCO topology still has a FoM better than other QVCOs in CMOS. The differential 10GHz Colpitts VCO designed in [K. 06] consumes more power than the 20GHz VCO designed in this work, which demonstrates the low power advantage of the proposed topology. The current consumption of the VCO is set by the gate voltage of transistor \(M_2\). Keeping the same supply voltage of 1.2 V, power consumption can be increased from 20 mW to 30 mW which results in 5 dB reduction in phase noise (Fig. 3.14).
### 3 Low Power Clock Generation and Clock Deskew Techniques

#### Table 3.3: Comparison of state-of-art CMOS VCOs

<table>
<thead>
<tr>
<th>Technology</th>
<th>[K. 07]</th>
<th>[K. 06]</th>
<th>[K. 06]</th>
<th>[S. 03b]</th>
<th>[F. 05]</th>
<th>This Work</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0.13-um CMOS</td>
<td>90-um CMOS</td>
<td>90-um CMOS</td>
<td>0.13-um SOI</td>
<td>0.13-um CMOS</td>
<td></td>
</tr>
<tr>
<td>Frequency</td>
<td>26GHz</td>
<td>10GHz</td>
<td>10GHz</td>
<td>10GHz</td>
<td>40GHz</td>
<td>20GHz</td>
</tr>
<tr>
<td>Topology</td>
<td>(G_m)Tuned</td>
<td>Colpitts</td>
<td>Cross-Coupled</td>
<td>Cross-Coupled</td>
<td>Cross-Coupled</td>
<td>Proposed VCO</td>
</tr>
<tr>
<td>Tuning Range</td>
<td>23.6%</td>
<td>12.2%</td>
<td>15.8%</td>
<td>15%</td>
<td>12.5%</td>
<td>12%</td>
</tr>
<tr>
<td>Inductor Q/Transformer Q</td>
<td>18</td>
<td>10</td>
<td>10</td>
<td>——</td>
<td>18</td>
<td>5</td>
</tr>
<tr>
<td>Phase Noise (dBc/Hz@1MHz)</td>
<td>-92.6</td>
<td>-117.5</td>
<td>-109.2</td>
<td>-95</td>
<td>-87</td>
<td>-101</td>
</tr>
<tr>
<td></td>
<td>@ 3MHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCO Power</td>
<td>43.6mW</td>
<td>36mW</td>
<td>7.5mW</td>
<td>14.4mW</td>
<td>——</td>
<td>——</td>
</tr>
<tr>
<td>VCO+ Buffer</td>
<td>50mW</td>
<td></td>
<td>17.5mW</td>
<td>81mW</td>
<td>20mW</td>
<td></td>
</tr>
<tr>
<td>FOM (VCO)</td>
<td>163.9</td>
<td>181.9</td>
<td>180.4</td>
<td>163.4</td>
<td>——</td>
<td>——</td>
</tr>
<tr>
<td>(dB)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FOM (VCO+ Buffer)</td>
<td>163.3</td>
<td>——</td>
<td>176.5</td>
<td>——</td>
<td>150.4</td>
<td>174.01</td>
</tr>
</tbody>
</table>

#### 3.3 Background on injection locking

Historically, injection locking has been used for low power frequency division [H. 99]. More recently, ILOs are also used as a jitter filter on high-frequency clocks [H. 03a] and as a clock deskew element [L. 06][F. 08]. Compared to traditional voltage-control delay elements, ILO-based deskew provides several advantages: (i) due to its high sensitivity, ILOs can operate with very small input amplitude - thus the reference clock can be distributed with low power; (ii) since an ILO behaves as a 1\textsuperscript{st} order PLL, it rejects high frequency jitter and is less susceptible to power supply noise; (iii) the clock can be deskewed by detuning the free running frequency of the ILO. To cover an entire clock
period, the required deskew range should be at least $\pm 180^\circ$. Assuming that phase-inversion of a differential ILO may be trivially accommodated, a deskew range of $\pm 90^\circ$ is required. Present ILO-based deskew techniques have several disadvantages. For small injected signals, the deskew range is less than $\pm 90^\circ$ [F. 08]. With large injection strength, it is possible to extend the deskew range but this requires a wide tuning range in the ILO. Furthermore, providing skews near $90^\circ$ results in considerable variation in the jitter tracking bandwidth and output clock amplitude [F. 08]. Previous theoretical studies on ILOs have focused on their lock range and the behavior of an ILO outside its lock range for both small injection [R. 46] and large injection [L. 65]. In this work we are specifically interested in the phase noise (and jitter) of the deskewed clock. We seek a general treatment applicable to both LC and ring VCOs.

With that motivation, we adopt the ILO model shown in Fig. 3.15 for any injection method and oscillator topology [H. 99][L. 65]. Here, $H_{VCO}$ is the VCO’s small-signal open loop frequency response and will depend on the VCO topology. In the case of an LC oscillator, $H_{VCO}$ is a tuned response, whereas, in case of a ring oscillator, $H_{VCO}$ is a low pass response. Nonlinearities associated with the VCOs are taken into account by the nonlinear block. The phasor diagram in Fig. 3.15 is taken with respect to the injected frequency, $\omega_{\text{inj}}$. The oscillator has a free running frequency of $\omega_0$ and, in steady-state, settles to $\omega_{\text{inj}}$. Let its instantaneous oscillation frequency be $\omega$ and $\Delta \omega$ is the inherent frequency difference, $\Delta \omega = \omega_0 - \omega_{\text{inj}}$. Thus, the oscillator output phasor $I_{\text{osc}} = |I_{\text{osc}}|e^{j\theta}$ rotates with an instantaneous angular frequency $\omega - \omega_{\text{inj}}$. The phasor $I_L$ is the vector summation of $I_{\text{inj}}$ and $I_{\text{osc}}$: $I_L = I_{\text{osc}} + I_{\text{inj}} = |I_L|e^{j(\theta - \Phi)}$. Here, $\Phi$ is the phase shift introduced by the $H_{VCO}$ to satisfy the oscillation condition, $\Phi = \ldots$
$\angle H_{VCO}(j\omega)$. It was shown in [L. 65] that

$$\tan \Phi = \frac{K \sin \theta}{1 + K \cos \theta} \quad (3.21)$$

where $K = |I_{inj}|/|I_{osc}|$ is the injection strength. We define,

$$A \equiv \frac{\tan \Phi}{\omega_0 - \omega} \quad (3.22)$$

By noting $\omega - \omega_{inj} = d\theta/dt$ and substituting $\Delta \omega = \omega_0 - \omega_{inj}$, this may be rearranged

$$\tan \Phi = -A\left(\frac{d\theta}{dt} - \Delta \omega\right) \quad (3.23)$$

Equating $\tan \Phi$ from equations (3.20) and (3.22),

$$\frac{d\theta}{dt} = -\frac{1}{A} \frac{K \sin \theta}{1 + K \cos \theta} + \Delta \omega \quad (3.24)$$

This is the same locking equation used in [R. 46] and [L. 65], but generalized so that all oscillator-topology dependence is captured by $A$. For the parallel RLC resonant tank [R. 46][L. 65],

$$A = \frac{2Q}{\omega_0} \quad (3.25)$$

where $Q$ is the quality factor of the tank circuit. For an LC resonant tank with resistive losses in series with the inductor, the appropriate value of $A$ is [M. 08a]:

$$A = \frac{Q}{\omega_0} (1 - 1/Q^2)^{1.5} \frac{\omega + \omega_0^2}{\omega_0^2} \omega \quad (3.26)$$

A simpler definition of $A$ may be obtained by taking a first-order expansion of $\tan \Phi$ around $\omega = \omega_0$ in (3.18). Since $\omega_0$ is the oscillator’s free-running frequency, $\tan \Phi = 0$. 

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at $\omega = \omega_0$. Hence,

$$A \approx -\frac{d\tan \Phi}{d\omega}|_{\omega = \omega_0}$$

(3.27)

The accuracy of this approximation diminishes as $\Delta\omega$ increases. For a ring oscillator, this approximation is used in the Appendix to show that:

$$A \approx \frac{n}{2\omega_0} \sin\left(\frac{2\pi}{n}\right)$$

(3.28)

where $n$ is the number of stages in the ring. With these expressions for $A$, we can use (3.23) as a general locking equation which is VCO topology-independent.

### 3.3.1 Clock deskew

Within the lock range, the steady state output frequency will always track the injected frequency, $\omega = \omega_{inj}$, and the phase difference between the injected and ILO output becomes constant, $d\theta/dt = 0$. Making these substitutions into equation (3.23),

$$\Delta\omega = \frac{1}{A} \left( -\frac{K \sin \theta_{ss}}{1 + K \cos \theta_{ss}} \right)$$

(3.29)

where $\theta_{ss}$ is the steady state phase shift between the injected and output clocks. The maximum value of $\Delta\omega$ is obtained when $\cos \theta_{ss} = -K$. Thus, we define lock range as,

$$\omega_{LOCK} = \frac{1}{A} \frac{K}{\sqrt{1 - K^2}}$$

(3.30)

Within lock range ($\Delta\omega < \omega_{LOCK}$) equation (3.28) is valid for any value of $K$ and $\Delta\omega$. For small injection strength i.e. $K \cos \theta_{ss} << 1$ the above relation can be simplified as [R. 46]

$$\theta_{ss} \approx \sin^{-1}\left(\frac{A}{K} \Delta\omega\right)$$

(3.31)

As (3.30) suggests, for small frequency offsets the phase shift is approximately linear.
with respect to $\Delta \omega$. This property is particularly useful for ILO-based clock deskew-
ing. Experimental and simulated deskew curves using the differential VCO topology discussed in the previous section are shown in Fig. 3.16. For experimental study we AC coupled an external 19 GHz clock to I-VCO only. Deskew curve was generated by detuning $I-VCO$ only. According to (3.30), the deskew angle $\theta_{ss}$ decreases with increasing injection strength $K$. Note that the validity of equation (3.30) is limited to small injection strength ($K$) only. For larger injection strength we can consider equation (3.29) where we see that the lock range increases with injection strength. In particular, larger injection strength increases the usable linear portion of the deskew curve, $\theta_{ss}$ vs. $\Delta \omega$. Finally, note that (3.30) predicts a maximum achievable achievable deskew of $\pm 90^\circ$; however, under very strong injection the approximations in (3.30) break down and slightly larger deskew angles are, in fact, achievable but accompanied by nonlinearity in the deskew curve and, as we shall see, variations in the jitter tracking bandwidth and oscillation amplitude.

### 3.3.2 Phase noise filtering

The transient phase response of the ILO can be obtained by integrating equation (3.23) with respect to time resulting in a first-order response [R. 46][L. 65].

$$\theta(t) = \theta_0 e^{-\omega_p t}$$

(3.32)
3 Low Power Clock Generation and Clock Deskew Techniques

In (31), $\theta_0$ is the phase difference at time $t = 0$ between the free running VCO output and the injected clock. Generalizing the result in [H. 99] to cover different oscillator topologies, $\omega_P$ can be estimated as:

$$\omega_P = \sqrt{\frac{K^2}{A^2} - \Delta \omega^2}$$  \hspace{1cm} (3.33)

For weak injection, $K \ll 1$, this simplifies to the same result as in [R. 46][L. 65], $\omega_P = K/A$. Thus, ILOs are functionally equivalent to a first order PLL [H. 99] where input phase noise is low pass filtered,

$$JTF_{INPUT} = \frac{1}{1 + \frac{j\omega_{jitter}}{\omega_P}}$$  \hspace{1cm} (3.34)

and VCO phase noise is high pass filtered,

$$JTF_{VCO} = \frac{j\omega_{jitter}}{1 + \frac{j\omega_{jitter}}{\omega_P}}$$  \hspace{1cm} (3.35)

Here $\omega_{jitter}$ is the jitter frequency. If $S_{inj}$ is the phase noise of the injected signal and $S_{VCO}$ is the VCO phase noise, then the phase noise of the deskewed clock is

$$S_{out} = |JTF_{input}|^2 S_{inj} + |JTF_{VCO}|^2 S_{VCO}$$  \hspace{1cm} (3.36)

Using the jitter transfer functions in (3.33) and (3.34),

$$S_{out}(\omega_{jitter}) = \frac{\omega_P^2 S_{inj} + \omega_{jitter}^2 S_{VCO}}{\omega_P^2 + \omega_{jitter}^2} = \frac{(\frac{K^2}{A^2} - (\Delta \omega)^2) S_{inj} + \omega_{jitter}^2 S_{VCO}}{\frac{K^2}{A^2} - (\Delta \omega)^2 + \omega_{jitter}^2}$$  \hspace{1cm} (3.37)

It is also desirable to express the phase noise of the deskewed clock as a function of deskew angle $\theta_{ss}$. This can be done using the relationship between frequency offset and
3 Low Power Clock Generation and Clock Deskew Techniques

Figure 3.17: (a) Simulated and predicted phase noise of the LC VCO at different deskew settings at $\omega_{\text{inj}} = 2\pi \times 19$ GHz (b) Simulated and predicted jitter transfer characteristics at different skew settings $\omega_{\text{inj}} = 2\pi \times 19$ GHz. For both simulations $Q=6$ and $K=0.15$

deskew angle:

$$S_{\text{out}}(\omega_{\text{jitter}}) = \frac{(K/A)^2 \cos^2 \theta_{ss} S_{\text{inj}} + \omega_{\text{jitter}}^2 S_{\text{VCO}}}{(K/A)^2 \cos^2 \theta_{ss} + \omega_{\text{jitter}}^2}$$  \hspace{1cm} (3.38)

This phase noise expression for the deskewed clock provides several insights: (a) the jitter tracking bandwidth of the ILO depends upon the frequency offset between the injected and free running VCO frequency, $\Delta \omega$, and hence upon the deskew angle, $\theta_{ss}$; (b) Close to the lock range ($\Delta \omega \approx K/A$), $S_{\text{OUT}} \approx S_{\text{VCO}}$, so no phase noise filtering will be observed. Taking a different approach, the same conclusion was obtained in [B. 04]. In terms of the phase shift, $\theta_{ss}$, effective phase noise filtering is achieved for small deskew angles, but for large deskew angles (e.g. $\theta_{ss} = \pm 90^\circ$) no phase noise filtering is achievable (i.e. $S_{\text{OUT}} \approx S_{\text{VCO}}$).

The LC VCO discussed in section II is simulated as an ILO by injecting a relatively low-jitter clock into the tank through a capacitive coupling. The injected clock frequency was 19 GHz and the free-running VCO frequency was detuned away from 19 GHz to obtain phase shifts. The predicted phase noise of the deskewed clock along with the simulated one is shown in Fig. 3.17(a). For this study a low noise clock is generated.
and injected to the differential VCO. Normalized jitter transfer functions are shown for different deskew angles in Fig. 3.17(b). Jitter Tracking Bandwidth (JTB) of the ILO as a function of the frequency offset and injection strength is shown in Fig. 3.18. The theoretical predictions are based upon a parallel RLC-tank model using the expression for $A$ in (3.21) with $Q = 6$. For small phase shifts, the theory and simulation results are in good agreement. Increasing discrepancies are observed at larger phase shifts because of the simplified parallel RLC-tank model. Regardless, at $\theta_{ss} = \pm 90^\circ$ very little jitter
filtering is observed. This was also experimentally verified by capturing phase noise plots of the injected signal, free-running VCO, and the deskewed clock under injection locking in Fig. 3.19.
Table 3.4: Summary of ILO based deskew parameters

<table>
<thead>
<tr>
<th></th>
<th>Phase Shift $\theta_{ss}$</th>
<th>Lock Range $\omega_{\text{LOCK}}$</th>
<th>Jitter Tracking BW $\omega_p$</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Ring Osc.</strong></td>
<td>$\sin^{-1}\left[\frac{n(\omega_{\text{inj}} - \omega_0)}{2K\omega_0}\sin\left(\frac{2\pi}{n}\right)\right]$</td>
<td>$\frac{2\omega_{\text{inj}}}{n\sin\left(\frac{2\pi}{n}\right)}\sqrt{1 - K^2}$</td>
<td>$\sqrt{\left[\frac{2\omega_{\text{inj}}K}{n\sin\left(\frac{2\pi}{n}\right)}\right]^2 - [\omega_{\text{inj}} - \omega_0]^2}$</td>
</tr>
<tr>
<td>[n=No. of Stages]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>LC Osc.</strong></td>
<td>$\sin^{-1}\left[\frac{2Q(\omega_{\text{inj}} - \omega_0)}{K\omega_0}\right]$</td>
<td>$\frac{\omega_0}{2Q}\sqrt{1 - K^2}$</td>
<td>$\sqrt{\left[\frac{\omega_0K}{2Q}\right]^2 - [\omega_{\text{inj}} - \omega_0]^2}$</td>
</tr>
<tr>
<td>[Q=Tank Quality Factor]</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### 3.3.3 Deskew with Harmonic Injection

Phase deskew can also be achieved when the VCO is injected with a super- or sub-harmonic clock such that $f_{osc} = mf_{inj}$. The phase noise expression in (3.33) becomes,

$$S_{out}(\omega_{jitter}) = \frac{m^2(K/A)^2\cos^2\theta_{ss}S_{\text{inj}} + \omega_{jitter}^2S_{\text{VCO}}}{(K/A)^2\cos^2\theta_{ss} + \omega_{jitter}^2} \tag{3.39}$$

If the oscillator is injected with $m$th order sub-harmonic, then the output phase noise will degrade by a factor $m^2$ within the jitter tracking bandwidth [X. 92]. On the other hand, super-harmonic injection improves the phase noise of the injected signal by $m^2$. For example, 2\textsuperscript{nd} harmonic of the oscillation frequency is injected in the tail of the four stage ring oscillator in Fig. 3.20(a). The phase noise of the deskewed clock and the corresponding jitter tracking bandwidth at different deskew angles is shown in Fig. 3.20(b-c) and compared with theoretical predictions based upon (3.38), the expression for $A$ derived in the appendix. Again theoretical predictions are in good agreement with the simulation results for small deskew phase angles. For large phase shifts, inaccuracies arise due to first-order approximation for $A$ applied in (3.23).

In summary, the theory, simulation and experimental study of the ILO-based deskew techniques have identified several limitations of existing techniques for large phase
deskew angles: (i) the phase steps are non-linear; (ii) the output clock amplitude varies significantly and (iii) there is little or no jitter filtering. However, if we restrict the frequency offset within $|\Delta \omega| < 0.5 \omega_{LOCK}$, above-mentioned limitations are not very significant. The derived phase noise expressions are applicable for any ILO topology with appropriate choice of $A$. The theoretical results are summarized for both ring and LC oscillators in Table 3.4.

### 3.4 Proposed deskew techniques

In the proposed architecture, a QVCO is used, where we can selectively inject either the in-phase or the quadrature portion of the VCO. This allows us to achieve $\pm 180^\circ$ using only half of the lock range. As a result, both jitter tracking bandwidth and clock amplitude suffers much less variation. This proposed technique can be implemented either with an LC QVCO or using a ring oscillator.

#### 3.4.1 Deskew with LC QVCO

The analysis of a differential ILO can be extended for a quadrature ILO as shown in Fig. 3.21. First we will study the case without injection and then, the effect of
injection will be discussed. Due to mutual coupling between the two VCOs, each of them oscillates at a frequency slightly offset from resonance. As a result, in a free running QVCO the tank introduces a phase shift $\delta_1$ between the output voltage $V_{Iosc}$ and current $I_{Iosc}$. Thus the mutual coupling between these two VCOs can be viewed as injection locking [A. 07b] and the general locking equation (3.23) can be applied to both the I-VCO and Q-VCO:

$$\frac{d(\theta_I - \theta_Q - \delta_1)}{dt} = -\frac{1}{A} \frac{K_c \sin(\theta_I - \theta_Q - \delta_1)}{1 + K_c \cos(\theta_I - \theta_Q - \delta_1)}$$

(3.40)

$$\frac{d(\theta_Q - \theta_I - \delta_2)}{dt} = -\frac{1}{A} \frac{K_c \sin(\theta_Q - \theta_I - \delta_2)}{1 + K_c \cos(\theta_Q - \theta_I - \delta_2)}$$

(3.41)

Here, we assume that both VCOs are identical (i.e. $\Delta \omega = 0$) and the phase difference between them is $\Delta \theta (\theta_Q - \theta_I = \Delta \theta)$. To find the final phase relationship between these two VCOs, we find the steady-state solution of the above equations:

$$\frac{K_c \sin(\Delta \theta - \delta_1)}{1 + K_c \cos(\Delta \theta - \delta_1)} = -\frac{K_c \sin(\Delta \theta + \delta_2)}{1 + K_c \cos(\Delta \theta - \delta_2)}$$

(3.42)

To further simplify the above equations, we consider two cases: Case $I$, when two loops are strongly coupled, $K_c \approx 1$:

$$\frac{\sin(\Delta \theta - \delta_1)}{1 + \cos(\Delta \theta - \delta_1)} = -\frac{\sin(\Delta \theta + \delta_2)}{1 + \cos(\Delta \theta - \delta_2)}$$

(3.43)

Substituting $\sin \alpha = 2 \sin(\alpha/2) \cos(\alpha/2)$ and $1 + \cos \alpha = 2 \cos^2(\alpha/2)$:

$$\tan \frac{\Delta \theta - \delta_1}{2} = -\tan \frac{\Delta \theta + \delta_2}{2}$$

(3.44)

$$\delta_1 - \delta_2 = 2\Delta \theta$$

(3.45)
Case : II, when two loops are weakly coupled, $K_c \ll 1$:

$$K_c \sin(\Delta \theta - \delta_1) = -K_c \sin(\Delta \theta + \delta_2) \quad (3.46)$$

This gives us the same relationship as before:

$$\delta_1 - \delta_2 = 2\Delta \theta \quad (3.47)$$

For quadrature output such as $\Delta \theta = \pi/2$, $\delta_1 = \delta_2 + \pi$ which leads to well known antiphase coupling. On the other hand in-phase coupling leads to $\Delta \theta = 0$. Traditionally, the antiphase coupling is implemented by simply crossing over the available differential outputs. Thus, $\delta_1$ and $\delta_2$ maintains static phase relationship which allow us to further simplify the differential equation:

$$\frac{d(\Delta \theta)}{dt} = -\frac{1}{A} K_c \sin(\Delta \theta) \cdot \frac{1}{1 + K_c \cos(\Delta \theta)} \quad (3.48)$$

The time domain phase variation between I-VCO and Q-VCO can be obtained by integrating with respect to time:

$$\tan(\Delta \theta/2) \sin^{K_c}(\Delta \theta) = e^{-K_c t/A} + \psi \quad (3.49)$$

Here, $\psi$ is an integration constant which is $\pi/2$ for antiphase coupling. For small $\Delta \theta$, we find a first order transient response:

$$\Delta \theta \approx \Delta \theta_0 e^{-K_c t/A} + \pi/2 \quad (3.50)$$

Here, $\Delta \theta_0$ is the initial phase difference at time $t = 0$. As $t \to \infty$, the phase difference $\Delta \theta$ exponentially approaches $\pi/2$. The significance of the of the above expression is that any jitter event in $\theta_I$ will be tracked with $\theta_Q$ (and vice versa) by a first order low pass response. The pole of this first order low pass response is:

$$\omega_Q = \frac{K_c}{A} \quad (3.51)$$
With that insight, now we can study the jitter transfer functions in the proposed deskew method shown in Fig. 3.21(b). To model the proposed deskew technique we consider two cases. First, phase noise at the output due to I-VCO injection ($S_{I-out}$) is observed. In this case, only in-phase injection ($I_{Iinj}$) is applied and $I_{Qinj}$ is set to zero. Second, we consider the phase noise at the output due to Q-VCO injection ($S_{Q-out}$). In this case quadrature injection ($I_{Qinj}$) is applied and $I_{inj}$ is set to zero. Similar to section III(B), to derive a closed form expression, small injection strength and frequency offset are assumed, $K << 1$ and $\Delta \omega << \omega_{Lock}$. Following the method described in section III(B), we can express the phase noise for I-VCO injection:

$$S_{I-out}(\omega_{jitter}) \approx \frac{\omega_p^2 S_{Iinj} + \omega_{jitter}^2 S_{VCO}}{\omega_p^2 + \omega_{jitter}^2}$$

(3.52)

Note that $\omega_p$ is the pole due to external injection defined in (3.32). The case of injection at I-VCO is very similar to injection of a single-phase differential VCO. Thus the pole of the jitter transfer function is set by the external injection strength, $K$, as expressed in equation (3.32). However, jitter transfer function at the Q-VCO output will be a function of both $\omega_p$ and $\omega_Q$. Since the Q-VCO output in turn injects back into the I-VCO, the coupling strength $K_c$ can have a secondary influence on the ILO jitter transfer function, but this higher-order effect is safely ignored in the analysis as verified by simulations. However, in the case of Q-VCO injection, we need to take into account the second pole $\omega_Q$ and thus the phase noise can be expressed as:

$$S_{Q-out}(\omega_{jitter}) \approx \frac{\omega_p^2 \omega_Q^2 S_{Qinj} + \omega_{jitter}^2 (\omega_{jitter}^2 + \omega_p^2 + \omega_Q^2) S_{VCO}}{(\omega_{jitter}^2 + \omega_p^2)(\omega_{jitter}^2 + \omega_Q^2)}$$

(3.53)

The accuracy of the above two expressions are verified with the theoretical and simulated jitter transfer functions for I-VCO injection and Q-VCO injection shown in Fig. 3.22. When the coupling factor between the in-phase and quadrature VCOs is much stronger than that of the injection, $K_c >> K$, $\omega_Q > \omega_P$ and the bandwidth of the jitter transfer function is mainly dominated by the $\omega_p$. However, for larger injection strengths, the effect of $\omega_Q$ becomes prominent. Note that for small injection strength of $K = 0.085$, there is no noticeable change in JTB where as for $K = 0.22$ Q-VCO
For $\omega_{\text{inj}} = 2\pi \times 20$ GHz. For both simulations $Q=6$ and mutual injection strength is $K_c = 0.5$

injection results in about 50 MHz reduction in JTB compared to I-VCO injection.

The proposed deskew technique utilizing an LC QVCO is shown in Fig. 3.23(a). The forwarded clock is injected to the in-phase VCO to achieve $0^\circ$ to $90^\circ$ phase shift only. For $0^\circ$ to $-90^\circ$, the injection is shifted to the quadrature VCO resulting in two deskew curves on Fig. 3.22(b). Thus we are using less than half of the lock range. Note that in the proposed QVCO based deskew scheme, we arbitrarily choose point C or D in the deskew curve as reference zero degree deskew. Since these two points have highest 200 MHz frequency offset from the free running VCO frequency, phase noise is

![Diagram](image_url)
Figure 3.23: Proposed phase deskew technique (a) Experimental setup with Q VCO (b) Corresponding deskew curve at $\omega_{inj}=2\pi \times 19 \text{ GHz}$ and $K=0.17$

Figure 3.24: Performance of proposed deskew technique (a) deskewed clock at different skew settings (b) corresponding measured phase noise $\omega_{inj}=2\pi \times 19 \text{ GHz}$
also highest in these two points. On the other hand, point B and E is used as +45° and -45° deskew respectively. Since the frequency offset is zero, lowest phase noise is achieved. Variation of the jitter tracking bandwidth with frequency offset (hence, deskew) is nonlinear (Fig. 3.18). For example, if K=0.17, a frequency offset of 150 MHz cause only 50 MHz reduction in JTB. It turns out that amplitude variation is also minimal in that range. Thus, the proposed technique allows us to accomplish -90° to +90° phase selection with linear phase steps and negligible amplitude variation, as shown in Fig. 3.24(a). Note that point D and A on the deskew curve Fig. 3.23(b) represents 0° and 90° phase shift. In the proposed technique, these two deskew angles are obtained by setting same frequency offset (200 MHz) and by switching the injection node from I-VCO to Q-VCO. As discussed earlier, switching the injection node from I-VCO to Q-VCO has little effect on JTB if $\omega_p << \omega_Q$. As a result only small variation of the phase noise of the deskewed clock in observed in Fig. 3.24(b). For comparison with a simple differential injection-locked VCO, the phase noise at 1 MHz offset is plotted versus deskew angle in Fig. 3.25 which verifies the advantage of the proposed technique. In the worst case condition (+90° or -90°) 8 dB of phase noise improvement is obtained. Note that in the plot of Fig. 3.24 the reference phase angle of 0° is shifted.

![Figure 3.25: Performance comparison: Phase noise @ 1 MHz offset for different skew angles $\omega_{inj}=2\pi \times 19 \text{ GHz}$](image-url)
by 45° in the Q-VCO case so that both plots cover the same ±90° range.

In a practical system, phase selection can be performed as in a conventional phase-locked or delay-locked loop. For example, in [J. 09] the ILO output is compared to a reference clock by a phase detector which in turn drives a loop filter that tunes the ILO. In a data recovery system, a data-driven phase detector would be required. Eventually the loop converges to a point either on the curve $A \rightarrow C$ or $D \rightarrow F$. Note that these two curves have overlap which may cause ambiguity in the control logic. For example, 0 phase deskew can be achieved either by choosing the point C or D. This problem can easily be solved by adding hysteresis in the control logic.

### 3.4.2 Deskew with ring oscillator

If the link needs to support wide range of data rates, ring oscillators are often preferred over LC-VCOs due to their wide tuning range. The proposed deskew technique is easily realizable for those applications. From Table 3.4, increasing the number of stages provides more nodes for injection thus the opportunity to restrict $\Delta\omega$ over a narrower range providing more linear phase adjustment. On the other hand, fewer stages provides lower power consumption and higher jitter tracking bandwidth. As a proof of concept, a four stage ring oscillator implemented in 90 nm CMOS is used in this study. The oscillator provides a tuning range from 2 GHz-7 GHz. The injection
Figure 3.27: (a) Generated skew curve as a function of free running frequency ($\omega_{inj} = 2\pi \times 10$ GHz and $K=0.25$) (b) Measured Phase noise for $\theta_{ss} = 10^\circ$ and $\theta_{ss} = 80^\circ$

signal is at $2f_{osc}$ (Fig. 3.26). Similar to the LC oscillator, phase deskew curves for both in-phase and quadrature injection are shown in Fig. 3.27. The effects of quadrature injection on jitter filtering and amplitude variations are very similar to the LC oscillator case.
3.5 Conclusion

In summary, a low power clock source that incorporates a buffer into a cross-coupled oscillator has been demonstrated. By isolating the load from the tank, the oscillator can directly drive 50-Ohm impedances or large capacitive loads with no additional buffering. A QVCO using this topology in 0.13 um digital CMOS oscillates at 20 GHz, consumes 20 mW and provides 12% tuning range with a measured phase noise of -101 dBc/Hz @ 1 MHz frequency offset. Injection-locked QVCOs are particularly useful as deskew elements in high-speed parallel links. By selectively injecting different phases of a quadrature-LC or ring VCO, variations in the ILO’s jitter tracking bandwidth are muted and phase noise can be reduced. For a fixed data rate, LC oscillators can provide lower phase noise whereas ring oscillators are preferred for variable data rates. Due to the additional VCO stages in quadrature, this technique will consume more power compared to [L. 06] and [F. 08]. The technique is demonstrated using a LC QVCO at 20 GHz while burning only 20 mW of power and providing an 8-dB improvement in phase noise. A ring oscillator deskews a 2 to 7 GHz clock while consuming 14 mW in 90 nm CMOS. These figures still compare favorably with using a complete DLL for deskewing. In addition, ILOs are more immune to supply noise and duty cycle distortion.

3.6 Appendix A - Derivation of Ring VCO constant A

In the case of a ring oscillator, the VCO transfer function is low pass. Assume the ring oscillator is implemented with \( n \) identical stages. Each stage had a dc gain of \( H_0 \) and single pole \( \omega_P \). Thus the equivalent transfer function can be written as:

\[
H(j\omega) = \frac{H_0^n}{(1 + j\frac{\omega}{\omega_P})^n}
\]  

(3.54)

Considering the positive feedback introduces 180° phase shift, the remaining phase shift required to ensure oscillation at \( \omega_0 \) is:
\[ \Phi|_{\omega=\omega_o} = \angle(H(j\omega_o)) = -n \tan^{-1}\left(\frac{\omega_o}{\omega_P}\right) = -\pi \] (3.55)

\[ \tan\left(\frac{\pi}{n}\right) = \frac{\omega_o}{\omega_P} \] (3.56)

Substituting (3.55) into (3.53):

\[ H(j\omega) = \begin{align*}
H_o^n &= \frac{n}{(1 + j \frac{\pi}{\omega_o} \tan\left(\frac{\pi}{n}\right))^n}
\end{align*} \] (3.57)

\[ \Phi = -n \tan^{-1}\left(\frac{\omega}{\omega_o} \tan\left(\frac{\pi}{n}\right)\right) \] (3.58)

Substituting this into (3.21) gives

\[ A = -\frac{\tan[n \tan^{-1}\left(\frac{\omega}{\omega_o} \tan\left(\frac{\pi}{n}\right)\right)]}{\omega_o - \omega} \] (3.59)

Adopting the approximation in (3.26) gives,

\[ A = -\frac{d \tan \Phi}{d \omega}|_{\omega=\omega_o} = \frac{n}{\omega_o} \tan\left(\frac{\pi}{n}\right) \sec^2\Phi|_{\omega=\omega_o} = \frac{n}{\omega_o} \tan\left(\frac{\pi}{n}\right) = \frac{n}{2\omega_o} \sin\left(\frac{2\pi}{n}\right) \] (3.60)

### 3.7 Appendix B - Estimation of Injection Strength

Injection strength \((K)\) of the ILO is critical for theoretical prediction of jitter tracking bandwidth. The following section describes the methods used in this thesis for estimation of injection strength for different cases.
3.7.1 Injection strength for LC ILO

Conventional QVCO uses additional differential pair $M_C$ for injection (Fig. 3.28) to provide coupling between two differential VCOs. Injection strength $K$ in this case can be simply written as $I_{inj}/I_{osc}$. However, in some cases an alternative injection point can be chosen. For example, if the current is injected directly to the inductor as shown in Fig. 3.29 deriving equivalent injection strength in this case requires more effort.

One simple way is to find equivalent current source $I_T$ to replace $I_{inj}$. It can be
Table 3.5: Verification of LC ILO lock range for \([Q = 6, \omega_o = 2\pi \times 19GHz, C_{var} = 120fF, C_{GS} = 400fF]\)

<table>
<thead>
<tr>
<th>ILO topology</th>
<th>(I_{inj}/I_{osc})</th>
<th>(K)</th>
<th>(\frac{\omega}{2Q} \sqrt{1-K^2})</th>
<th>Simulated lock range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fig.3.28</td>
<td>.05</td>
<td>.05</td>
<td>80 MHz</td>
<td>75 MHz</td>
</tr>
<tr>
<td>Fig.3.28</td>
<td>.1</td>
<td>.1</td>
<td>160 MHz</td>
<td>156 MHz</td>
</tr>
<tr>
<td>Fig.3.28</td>
<td>.2</td>
<td>.2</td>
<td>320 MHz</td>
<td>315 MHz</td>
</tr>
<tr>
<td>Fig.3.29</td>
<td>.05</td>
<td>.065</td>
<td>104 MHz</td>
<td>98 MHz</td>
</tr>
<tr>
<td>Fig.3.29</td>
<td>.1</td>
<td>.13</td>
<td>208 MHz</td>
<td>214 MHz</td>
</tr>
<tr>
<td>Fig.3.29</td>
<td>.2</td>
<td>.26</td>
<td>416 MHz</td>
<td>420 MHz</td>
</tr>
</tbody>
</table>

shown that

\[
I_T = -I_{inj}(1 + \frac{C_{var}}{C_{GS}}) \tag{3.61}
\]

Thus the magnitude of the injection strength in this case can be written as

\[
K = \frac{I_{inj}}{I_{osc}}(1 + \frac{C_{var}}{C_{GS}}) \tag{3.62}
\]

3.7.2 Injection strength for Ring ILO

Similarly in the case of a ring vco, injection strength can be defined as the ratio between injected current amplitude and free running vco’s oscillation current amplitude, \((K = \frac{I_{inj}}{I_{osc}})(\text{Fig. 3.30}). However, when used in super-harmonic injection mode, injection stage functions similar to a frequency mixer. The bottom transistor \((M_1)\) converts the injected voltage signal to a current adding to the bias current, \(I_{DC} + I_{inj}\cos(2\omega_{inj}t)\). The differential pair \(M_2\) is fully switched by the oscillator output signal \(V_{osc}\cos(2\omega_{osc}t)\).
Resulting switching functionality can be represented as:

$$S(t) = \frac{4}{\pi} \cos(\omega_{osc} t) - \frac{4}{3\pi} \cos(3\omega_{osc} t) + \text{higher harmonics}$$  \hspace{1cm} (3.63)

Output current can be written as:

$$I_{out}(t) = (I_{DC} + I_{inj}\cos(2\omega_{inj} t))(\frac{4}{\pi} \cos(\omega_{osc} t) - \frac{4}{3\pi} \cos(3\omega_{osc} t))$$  \hspace{1cm} (3.64)

Expanding the expression and keeping only the $\omega_{inj} - \omega_{osc}$ components,

$$I_{out}(t) = \frac{4I_{DC}}{\pi} \cos(\omega_{inj} - \omega_{osc}) t + \frac{2I_{inj}}{\pi} \cos(\omega_{inj} - \omega_{osc}) t - \frac{I_{inj}}{3\pi} \cos(\omega_{inj} - \omega_{osc}) t$$ \hspace{1cm} (3.65)

Notice that in this case $\omega_{inj} = 2\omega_{osc}$ and with this simplification output current can be written as

$$I_{out}(t) = \frac{4I_{DC}}{\pi} \cos(\omega_{osc} t) + \frac{2I_{inj}}{\pi} \cos(\omega_{osc} t) - \frac{2I_{inj}}{3\pi} \cos(\omega_{osc} t)$$ \hspace{1cm} (3.66)
Table 3.6: Verification of ring ILO lock range for \( n = 4, \omega_o = 2\pi \times 5GHz, I_{osc} = I_{DC} \)

<table>
<thead>
<tr>
<th>ILO topology</th>
<th>( I_{inj}/I_{osc} )</th>
<th>( K )</th>
<th>( \frac{2\omega_o}{n \sin \frac{\pi}{2}\sqrt{1-K^2}} )</th>
<th>Simulated lock range</th>
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<tbody>
<tr>
<td>Fig.3.30(b)</td>
<td>0.14</td>
<td>0.14</td>
<td>350 MHz</td>
<td>330 MHz</td>
</tr>
<tr>
<td>Fig.3.30(b)</td>
<td>0.28</td>
<td>0.28</td>
<td>700 MHz</td>
<td>705 MHz</td>
</tr>
<tr>
<td>Fig.3.30(b)</td>
<td>0.42</td>
<td>0.42</td>
<td>1150 MHz</td>
<td>1200 MHz</td>
</tr>
<tr>
<td>Fig.3.30(b)</td>
<td>0.56</td>
<td>0.56</td>
<td>1700 MHz</td>
<td>1900 MHz</td>
</tr>
<tr>
<td>Fig.3.30(c)</td>
<td>0.14</td>
<td>0.07</td>
<td>180 MHz</td>
<td>170 MHz</td>
</tr>
<tr>
<td>Fig.3.30(c)</td>
<td>0.28</td>
<td>0.14</td>
<td>360 MHz</td>
<td>375 MHz</td>
</tr>
<tr>
<td>Fig.3.30(c)</td>
<td>0.42</td>
<td>0.21</td>
<td>550 MHz</td>
<td>560 MHz</td>
</tr>
<tr>
<td>Fig.3.30(c)</td>
<td>0.56</td>
<td>0.28</td>
<td>750 MHz</td>
<td>760 MHz</td>
</tr>
</tbody>
</table>

Also note that if the oscillation amplitude is large enough to completely switch the differential stage, then \( I_{osc} = I_{DC} \). The injection strength then can be approximated as

\[
K \approx \frac{I_{inj}}{2I_{DC}}
\]  

(3.67)

For experimental results in Fig. 3.13 and 3.15 injection strength \( K \) is estimated from the lock range of the ILO. In addition, phase noise profiles of the free running VCO and locked VCO are compared to validate injection strength and jitter tracking bandwidth.
4 5-10 Gb/s Burst Mode Receiver in 90-nm CMOS

4.1 Introduction

High speed links with small AC coupling capacitances are increasing in importance. For example, wireless interconnects using either inductive or capacitive coupling between stacked dice can achieve high density [L. 05],[K. 03],[A.F07]. These interconnects also introduce spectral nulls at DC. As a result, the receiver receives a stream of positive and negative pulses corresponding to the rising and falling edges of transmitted data. Receivers which are capable of recovering NRZ signals from these narrow pulses are referred to in this work as AC coupled receivers, and are not to be confused with receivers for links with a relatively large DC blocking capacitor where the received waveform still look like an NRZ signal with some baseline wander [E. 07]. Fabrication of such interconnects are challenging due to the required alignment and heat dissipation [R. 04]. The focus of this work is to present power and area efficient I/O circuits which do not limit the interconnect density and reduce the heat that must be dissipated. One possible implementation is shown in Fig. 4.1. A shared PLL can perform frequency acquisition globally [A. 07c] and skew compensation is done individually per link.

The present status of AC coupled receivers is summarized in Table 4.1 where the power efficiency is plotted for different bit-rates. The primary focus of existing AC coupled receivers is NRZ signal recovery, and several front-ends for this purpose have been demonstrated with excellent power efficiency. However, when clock recovery is included their power efficiency significantly degrades [L. 05].

Burst mode capability is also desired for high-density AC coupled interconnects as it results in reduced power and area consumption [N.M08]. In [N.M08] no timing recovery
is performed; the receiver fully relies on matching between the data and forwarded clock path [N.M08]. This requires very accurate matching of the interconnect and stacked-die coupling. On the other hand the clock recovery techniques used in [L. 05],[K. 03] are too slow to allow burst mode operation. A timing recovery scheme which can recover a clock within several bit periods is sought. Such fast locking techniques are already employed in other wireline applications such as passive optical network (PON) systems. For example the 10 Gb/s receiver presented in [M. 05] is AC coupled and also provides fast locking. However, the 2W of power consumed in [M. 05] is not acceptable for chip-to-chip applications.

In this work we provide both NRZ recovery and fast locking with significantly reduced power (70 mW) consumption. Compared to the previous work in [M. 07] we have made several modifications: (i) We use a hysteresis latch with a variable decision threshold. This allows the receiver to be implemented with less preamp gain which translates into a 20% power savings. (ii) In this work the high-pass linear signal path introduced in [M. 07] is further leveraged to facilitate clock recovery over a broad frequency range. (Clock recovery was not considered in [M. 07].) It will be shown later that the use of this linear path results in improved jitter and lower power consumption compared with [L. 05]. (iii) Unlike [M. 05, J. 08, C. 06c], we use a half-rate ILO for clock recovery which further reduces the power consumption. Half-rate injection locking has been previously used for DC coupled channels [K. 99]. Taking advantage of the high-pass
Table 4.1: Summary of AC coupled pulse receivers

<table>
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<th></th>
<th></th>
</tr>
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<tbody>
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<td>Data</td>
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<td>3 Gb/s</td>
<td>1.23 Gb/s</td>
<td>10 Gb/s</td>
<td>11 Gb/s</td>
</tr>
<tr>
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<td>100mV</td>
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<td>40mV</td>
<td>300mV</td>
</tr>
<tr>
<td>Process</td>
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<td>0.18um</td>
<td>0.13um</td>
<td>0.13um</td>
<td>90nm</td>
</tr>
<tr>
<td></td>
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<td>(w/CDR)</td>
<td>(w/o CDR)</td>
<td>(w/ CDR)</td>
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</tr>
<tr>
<td>Application</td>
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<td>Chip-to-Chip Interconnect</td>
<td>3-D Interconnect</td>
<td>PON</td>
<td>Chip-to-Chip Interconnect</td>
</tr>
</tbody>
</table>

channel response, half-rate injection locking is here adopted for AC coupled receivers. In summary, the high pass response provided by the AC coupled channel is used to advantage for both equalization and clock recovery.

Section 4.2 will first focus on the NRZ signal recovery circuitry including experimental results. In section 4.3, burst mode timing recovery techniques will be discussed where the linear path is used to extract timing information. Some theory required to evaluate such a CDR will be derived in section 4.4. The implementation and experimental results are discussed in section 4.5.

### 4.2 NRZ Signal Recovery

NRZ signal recovery from AC coupled links is studied in, for example, [L. 05], [K. 03], [R. 04]. A simple capacitively-coupled channel is shown in Fig. 4.3. Since the coupling capacitances are small (on the order of $50 \rightarrow 500 \text{ fF}$) the time constant $RC$ is much less
than a bit period and the channel response is approximately $sRC$ over the band of interest. Hence, the transmitted NRZ signal is differentiated. On the receiver side, the channel’s differentiation can be undone by comparing the received signal to a threshold that depends upon the last bit, similar to peak detection previously employed in differentiating magnetic storage channels \cite{R. 78}. At the targeted data rates of 5-10 Gb/s, multiple lower-rate data streams can be aggregated onto each pair. The transmitter may employ either current-mode buffers or voltage-mode buffers as in \cite{L. 05}.

![Equivalent circuit of An AC Coupled link including transmitter, channel and receiver. Value of R and C are chosen such that $1/(2\pi R_{\text{term}} C_{AC}) > 0.5 f_{Bit}$ to avoid ISI](image)

**4.2.1 Hysteresis Latch (Nonlinear Path)**

The functionality described above is equivalent to decision feedback equalization (DFE)\cite{R. 78}. Unlike a conventional DFE, this can be implemented without any clock using a simple hysteresis latch as shown in Fig. 4.3(a). The decision threshold level is updated based on most-recently decoded bit, $v_{th}(n) = \beta V(n)$.

The threshold settling time $T_{V_{th}}$ varies from 60ps to 80ps for different threshold voltages which suggests that the maximum achievable data rate is 13 Gb/s. However, the output settling time $T_{V_{o}}$ is longer (120ps) which would limit the achievable data rate to 8 Gb/s. Existing techniques use cascode transistors and inductive peaking to achieve 10 Gb/s \cite{M. 05}. These techniques cannot be used in this application where area and
Figure 4.3: Hysteresis latch topology for NRZ recovery: (a) NRZ recovery with DFE (b) proposed Implementation. Device sizes are: $g_{m-in} = 10\,\text{um}$, $g_{m2} = 20\,\text{um}$, $g_{m3} = 40\,\text{um}$, $R_{in} = 170\,-\,\text{ohm}$, $R_{L1} = 100\,-\,\text{ohm}$, $R_{L2} = 160\,-\,\text{ohm}$

Figure 4.4: Threshold adjustment with $I_{tail}$ in the proposed hysteresis latch: (a) settling time of the decision threshold and output voltage

Power efficiency is critical. Thus the hysteresis latch loses some of the signal’s high frequency content while restoring the DC component of the received signal. Fortunately, this high frequency content can be recovered by adding a parallel linear path as shown in Fig. 4.5.
4.2.2 Linear Path

A linear path is added in parallel to the hysteresis latch using a broadband amplifier which has the same circuit topology as the hysteresis circuit. By swapping the feedback nodes, the feedback becomes negative instead of positive and improves the bandwidth of the linear path [S. 03a]. The transfer function of this amplifier is 2nd order, and the feedback gain $g_{mf}R_{in}$ is chosen to provide a maximally flat frequency response as evidenced by the measured frequency response of the preamp and linear amplifier shown in Fig. 4.6. Since the AC coupled channel response is inherently high pass, the linear path can provide 14 dB of boost at 8 GHz with respect to low frequency (< 200 MHz) gain (Fig. 4.6). In summary, the linear path provides better signal integrity at high frequency (e.g. alternating 1s and 0s) whereas the nonlinear path provides better signal integrity at low frequency (i.e. several consecutive 1s and 0s). By combining them we improve overall signal integrity at both low and high frequency, similar to equalization.
4.2.3 Experimental Results

A prototype front-end is implemented in 90-nm CMOS and the die photo is shown in Fig. 4.7. The benefit of the linear path is shown in measurements at 10 Gb/s in Fig. 4.8. The linear path bandwidth is set according to the data rate. The relative weight of the linear and nonlinear path in this prototype is set manually to maximize the eye opening. For verification of error free recovery, the transmitted sequence and recovered equalized sequence are captured in Fig. 4.9. Note the bits highlighted by the arrows where the linear path restores bits that would otherwise be missed by the hysteresis latch alone. The maximum achievable data rate of 13 Gb/s is limited by the hysteresis settling time which is 80 ps.
Figure 4.8: The effect of the linear path on a recovered 10 Gb/s eye diagram for $2^7 - 1$ data: (a) without linear path (b) with linear path.

4.3 Timing Recovery

NRZ signals have a spectral null at $1/T_{bit}$. To extract a clock tone the NRZ signal is passed through a nonlinearity. The extracted clock tone may then be filtered out with a bandpass filter for timing recovery. This method of clock recovery is known as ‘the nonlinear spectral line method’. Traditionally, an off-chip high Q dielectric resonator is used as the bandpass filter to eliminate high-frequency (pattern-dependent) jitter in the extracted tone [P. 92].

AC coupled channels provide a distinct advantage for burst mode clock recovery; the channel response itself filters high frequency jitter [B. 09]. Thus the CDR jitter tracking bandwidth can be extended to accommodate fast locking without a significant
Figure 4.9: Transmitted and recovered $2^7 - 1$ sequence at 12Gb/s with and without equalization captured by a pattern-locked oscilloscope. Arrows on the top indicate errors in the unequalized pattern which are corrected by equalization with the linear path.

Figure 4.10: AC coupled pulse receivers: (a) as in [L. 05] (b) as in [M. 05].

jitter penalty. However, the relatively slow settling time of the hysteresis latch output reintroduces some pattern-dependent high-frequency jitter. Hence, to take advantage of the channel response the hysteresis latch output should not be used for timing recovery. Previous methods for clock recovery in AC coupled links are shown in Fig. 4.10. Fortunately in this work, the high-frequency content in the linear path, already being used for equalization, can also be used for clock recovery, as shown in Fig. 5.6. That signal is passed through a nonlinearity and an integrated injection locked oscillator.
with moderate Q is used in place of an off-chip bandpass filter.

Fig. 4.13(a) shows the general implementation of the nonlinear spectral line method. An analog multiplier provides the required nonlinearity; three possible implementations are shown in Fig. 4.12(b-d). The first method uses a delay element and XOR gate [K. 99],[J. 08] (Fig. 4.12(b)). To support 5-10 Gb/s operation, this technique will require a broadband tunable delay element to provide a delay of $T_{bit}/2$. In the second method, the linear path output is rectified by multiplying it with the recovered NRZ signal (Fig. 4.12(c)). Finally, in the third method the output of the linear path is squared to extract the clock tone (Fig. 4.12(d)). To compare their performance we consider simulated waveforms at $V_{NRZ}$ and $V_{Slope}$. Note that all three methods generate a clock tone at 10 GHz, but their jitter performance significantly varies as shown in the eye diagrams. To obtain more insight, the jitter spectra is plotted. The peak-to-peak pattern-dependent jitter of the first and second methods are 12 ps and 14 ps respectively. Significant portions of the jitter are due to ISI on $V_{NRZ}$, mostly introduced by the finite settling time of the hysteresis latch. These ISI components appear as periodic jitter at multiples of 0.5/(pattern length) resulting in spurs on the plots of jitter spectra in Fig. 4.13. Since the ILO JTB is on the order of 100s of MHz, this jitter cannot be filtered. The peak-to-peak jitter of the third method, employed in this work, is 2.5x lower compared to other techniques because it uses only the waveform $V_{Slope}$ which has less ISI.

The implemented squaring circuit is shown in Fig. 4.14. The extracted clock ampli-
4 5-10 Gb/s Burst Mode Receiver in 90-nm CMOS

Figure 4.12: Clock recovery with nonlinear spectral line method: (a) general block diagram (b) as in [J. 08] (c) as in [J. 05] (d) this work.

...tude sets the injection strength of the ILO. Resistor $R_{com}$ is used to shift the common mode level making it compatible with the injection inputs of the ILO. The extracted clock tone is captured on-die with an oscilloscope at 5-Gb/s and shown in Fig. 4.15.

4.4 Clock Recovery Using ILO

Injection locking is functionally equivalent to a large bandwidth PLL, but can be implemented with smaller area and lower power. Existing ILO based CDRs use T-FFs [K. 99] and LC VCOs [J. 08],[J. 05]. Alternatively, ring oscillators can be used for injection locking and will be compared to LC oscillators in this work. The locking behavior of an ILO was studied in [R. 46] for small injection strengths. In the case of LC oscillators, this study was extended for large injection strengths in [L. 65]. In this work our focus is to study the transient locking behavior for both small injection and for large injection while keeping the VCO topology general as in [M. 09].

The general ILO model shown in Fig. 4.16 is adopted from [H. 99][L. 65]. The phasor diagram in Fig. 4.16 is taken with respect to the injected frequency, $\omega_{inj}$. Let the ILO’s instantaneous oscillation frequency be $\omega$. Thus, the oscillator output phasor $I_{osc} = |I_{osc}|e^{j\theta}$ rotates with an instantaneous angular frequency $\omega - \omega_{inj}$. Let $\omega_0$ be the ILO free-running frequency (i.e. the frequency at which it oscillates with no injection) and $\Delta \omega$ is the inherent frequency difference, $\Delta \omega = \omega_0 - \omega_{inj}$. The phasor $I_L$ is the vector summation of $I_{inj}$ and $I_{osc}$: $I_L = I_{osc} + I_{inj} = |I_L|e^{j(\theta-\phi)}$ where $\phi = \angle H_{VCO}$.
Figure 4.13: Simulation results comparing different timing recovery schemes in both time and frequency domain at 10 Gb/s.

is the phase response of the ILO. Finally, let $K$ be the amplitude of the injecting signal normalized to that of the ILO output, $K = |I_{inj}|/|I_{osc}|$. To study the phase tracking of the ILO, we derive the transient phase response of the VCO output starting at time $t = 0$ with an arbitrary phase difference $\theta_0$. It is shown in the appendix that this phase
Figure 4.14: Schematic of the Gilbert multiplier used for clock extraction.

Figure 4.15: Recovered NRZ signal and corresponding extracted clock tone at 5 Gb/s.

Figure 4.16: Injection locked oscillator model and corresponding phasor diagram.
difference exponentially decreases to zero and can be expressed as

$$\theta(t) \approx \theta_0 e^{-t/\tau} \quad (4.1)$$

For small injection strengths $K < 1$, time constant $\tau$ is

$$\tau = 1/\left(\sqrt{\frac{K^2}{A^2} - \Delta \omega^2}\right) \quad (4.2)$$

For large injection strengths, $K \geq 1$, $\tau$ is

$$\tau = 1/\left(\sqrt{\frac{1}{A^2} - \Delta \omega^2}\right) \quad (4.3)$$

The constant $A$ captures the VCO topology’s effect on $\tau$.

$$A \approx -\frac{d \tan \phi}{d \omega} \bigg|_{\omega = \omega_0} \quad (4.4)$$

For the parallel RLC resonant tank, it was shown in [R. 46][L. 65] that $A = \frac{2Q}{\omega_0}$ where $Q$ is the quality factor of the tank circuit. Similarly for ring oscillators it is shown in [M. 09] that $A \approx \frac{\omega_0}{\Delta \omega} \sin\left(\frac{2\pi}{n}\right)$. Here $n$ is the number of delay stages in the ring. Note that the single time constant response in (4.2) implies a first order low pass transfer function. Thus when the input injecting clock is phase modulated at a modulation frequency $w_{jitter}$, the resulting output phase modulation is related to that of the input by a stable 1st-order low pass input jitter transfer function,

$$JTF_{INPUT}(\omega_{jitter}) = \frac{1}{1 + j \omega_{jitter}/\omega_P} \quad (4.5)$$

where, $\omega_P = 1/\tau$ is also known as the jitter tracking bandwidth ($JT_B$). Jitter tolerance ($J_{TOL}$) can be obtained from the jitter transfer function as described in [B. 02] (page 330).

$$J_{TOL}(\omega_{jitter}) = |0.5 + \frac{j \omega_{jitter}/\omega_P}{j \omega_{jitter}/\omega_P}| \quad (4.6)$$
Table 4.2: Summary of ILO based CDR parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>Jitter tracking bandwidth ($\omega_p$)</td>
<td>$\sqrt{\frac{K^2}{A^2} - \Delta \omega^2}$</td>
</tr>
<tr>
<td>Phase step response ($\theta(t)$)</td>
<td>$1 - \theta_0 e^{-\omega_p t}$</td>
</tr>
<tr>
<td>Jitter transfer function ($JTF_{INPUT}$)</td>
<td>$\frac{1}{1+j\omega_{jitter}/\omega_p}$</td>
</tr>
<tr>
<td>Jitter tolerance ($J_{TOL}$)</td>
<td>$</td>
</tr>
<tr>
<td>Phase noise ($S_{out}$)</td>
<td>$\frac{\omega_p^2 S_{inj} + \omega_{jitter}^2 S_{ILO}}{\omega_p^2 + \omega_{jitter}^2}$</td>
</tr>
</tbody>
</table>

The above 1st order expressions presume a high transition density in the incoming data, such as can be provided by a line code. When the injection signal is derived from random data, in the absence of data transitions, the ILO drifts towards its natural frequency of oscillation and thus accumulates jitter. On the arrival of the next transition, the VCO frequency and phase are pulled back to the injected frequency and phase. In the presence of $L$ consecutive identical digits (CIDs) the effective injection strength is reduced by a factor $L$, with an attendant shift in the pole of $JTF_{INPUT}$.

$$\omega_p = \sqrt{\frac{K^2}{L^2 A^2} - \Delta \omega^2}$$  \hspace{1cm} (4.7)

This reduction in JTB due to CIDs has been verified experimentally. ILO theory presented in this section is summarized in Table 4.2 which can be applied to any VCO by deriving appropriate parameter $A$. 
4.5 Clock Recovery Implementation

4.5.1 LC vs Ring ILO

The expressions in Table 4.2 show how the lock time, jitter tracking and jitter tolerance can be traded off against each other. If we consider the effective $Q$ of a ring oscillator as $Q = \left( \frac{\omega_0}{2} \right) \frac{d\phi}{d\omega} \bigg|_{\omega = \omega_0}$ [B. 96], we see that for a fixed resonant frequency $\omega_0$, the effective $Q$ of a ring is proportional to $n \sin \left( \frac{2\pi}{n} \right)$ [B. 96]. This explains why more stages in a ring make it more frequency-stable and, like a high-Q LC oscillator, make it slower to track phase steps in an injecting input and give it lower JTB. In general, increasing the injection strength $K$, results in faster phase response, hence higher jitter tracking bandwidth. Thus to improve the lock time of an injection-locked LC oscillator, one can either increase the injection strength $K$ or reduce $Q$. Both approaches will result in increased power consumption. Furthermore providing the required tuning range to support 5-10 Gb/s operation is very difficult using an LC oscillator.

Figure 4.17: Comparison of ILO performance for LC vs ring VCO. The LC VCO is operating at 10 GHz, $Q=3.5$. The ring oscillator is operating at 5 GHz with $n=4$ stages: (a) lock time as a function of injection strength (b) phase noise of the free running VCO and corresponding recovered clock, $\Delta \omega = 2\pi \times 10^6$.

Ring oscillators can provide a wider tuning range and faster locking than their LC counterparts, but also have worse phase noise and higher power consumption in the 5-10 GHz range. Since the CDR will be designed with large JTB, a significant portion
of the oscillator phase noise can be filtered, but the power consumption remains a problem. To help overcome this, a half rate architecture is adopted where a 5 GHz oscillator is injected with a 10 GHz recovered clock tone. Thus, the ILO will work as an injection locked divider, which can be used to directly demux the recovered NRZ data. The theory derived above for ILOs injected near their fundamental frequency is
still applicable to half rate injection with one exception: the output referred lock range is divided by two. A critical parameter for the ring ILO is the number of stages $n$. Increasing the number of stages results in higher power consumption and longer lock time. The performance of this ring oscillator based half rate scheme is compared to LC ILO based full rate clock recovery in Fig. 4.17. For the same injection strength, $K = 0.1$, a 5 GHz 4 stage ring ILO provides 2.5x faster locking compared to a 10 GHz ($Q = 3.5$) LC ILO (Fig. 4.17(a)). The phase noise of the ILO is shaped by a 1st order high pass transfer function,

$$JT_F^{ILO}(\omega_{jitter}) = \frac{j\omega_{jitter}/\omega_P}{1+j\omega_{jitter}/\omega_P} \quad (4.8)$$

If $S_{ILO}$ is the ILO phase noise and $S_{inj}$ is the phase noise of the injected clock, then the phase noise of the recovered clock can be expressed as:

$$S_{out}(\omega_{jitter}) = |JT_F^{INPUT}(\omega_{jitter})|^2S_{inj}(\omega_{jitter}) + |JT_F^{ILO}(\omega_{jitter})|^2S_{ILO}(\omega_{jitter}) \quad (4.9)$$

Using transfer functions from equation (4.6) and (4.9), equation (4.10) can be written as:

$$S_{out}(\omega_{jitter}) = \frac{\omega_P^2S_{inj}(\omega_{jitter}) + \omega_{jitter}^2S_{ILO}(\omega_{jitter})}{\omega_P^2 + \omega_{jitter}^2} \quad (4.10)$$

Equation (4.11) is validated by simulations in Fig. 4.17(b). The phase noise of two different free-running ILOs (one ring and one LC), $S_{ILO}$, and of a much quieter injecting clock, $S_{inj}$, are obtained from transistor-level simulations. These are substituted into (11) to obtain the dashed line predictions of the phase noise under injection locking in Fig. 4.17(b). Under the same conditions, transistor level simulation results are plotted with the solid lines in Fig. 4.17(b), matching very well with the dashed line theory. Even with moderate injection strength, most of this phase noise is filtered and the effect of the ILO’s inherent phase noise on the recovered clock is insignificant except at very high offset frequencies. Note that in the case of the ring ILO, at low offset
frequencies the phase noise of the recovered clock is 6 dB lower than the reference injection. This is because the ILO is dividing the injecting clock by 2. Finally, the ring oscillator has a larger JTB and, hence, is more tolerant to jitter when injection-locked to the received data.

4.5.2 ILO Design and Implementation

A 4 stage ring oscillator is designed with stage 1 and 3 used for injection and stage 2 and 4 used to tune the free-running oscillation frequency (Fig. 4.18). The differentially tunable delay stage results in less amplitude variation over the 2 to 6 GHz frequency range compared to single ended tuning. Transmitted NRZ data, the extracted clock tone and the corresponding locked clock phases are shown in Fig. 4.18. The $n = 4$ stage ring provides an in-phase clock (Phase $0^\circ$) locked to the data edges and a quadrature clock (Phase $90^\circ$) to sample the centre of the data eye. The half rate receiver directly demultiplexes 10 Gb/s NRZ data (Fig. 4.19).

4.5.3 ILO Non-ideality

Although injection locking provides area and power efficiency, it suffers from several limitations. Firstly, although the oscillator output $V_{ILO}$ is phase locked to the equalizer output $V_{EQ}$ by injection locking, the actual sampling phase suffers additional delay through the clock buffers preceding the sampling FFs. This additional delay mismatch causes a static phase offset, $\theta_{error} = \Delta T_{clk} - \Delta T_{data}$, which is not corrected since it is outside the phase tracking loop. As a result jitter tolerance outside the tracking bandwidth is degraded:

$$J_{TOL}(\omega_{jitter}) = \left| \frac{0.5}{1 - JT_{INPUT}(\omega_{jitter})} \right| - \theta_{error} \quad (4.11)$$

Identical buffer stages were used in the clock and data paths to try to match the delay through those paths. To compensate for any remaining skew, the free-running VCO frequency is detuned away from the injection frequency, $\theta_{ss} \approx \sin^{-1}(A\Delta\omega/K)$. Doing so does reduce the JTB, but as long as the delay mismatch is kept less than 0.1 UI
by careful layout, only a small frequency offset is required and there will be negligible change in the JTB. In this prototype, under a locked condition, the ILO frequency was manually tuned to maximize timing margin. In a practical implementation this can be automated as in, for example, [F. 08] with an on-die oscilloscope. This tuning can be performed once during calibration and turned off during normal operation to avoid any significant power and area overhead.

In a high density proximity coupled application, these ILOs will be packed densely. Thus coupling between the ILOs is a major concern. In the case of a ring oscillator, coupling mainly occurs through the supply and substrate network. Fortunately, higher jitter tracking bandwidth provides better immunity to supply noise. Moreover, the VCO delay cells are implemented with current mode logic, providing good supply and substrate noise immunity compared with static CMOS logic.

4.5.4 Simulation Techniques

To evaluate the ILO’s jitter transfer characteristics two techniques are used. First, the jitter transfer function is generated from the phase noise of the free running VCO and the phase noise of the recovered clock. Using equation (4.6) the ILO jitter transfer can be written as:

\[ |JTF_{\text{input}}(\omega_{\text{jitter}})|^2 = \frac{\omega_p^2}{\omega_{\text{jitter}}^2 + \omega_p^2} = 1 - \frac{\omega_{\text{jitter}}^2}{\omega_{\text{jitter}}^2 + \omega_p^2} \] (4.12)

Since \( S_{ILO} \gg S_{inj} \) for a ring oscillator, around the cutoff frequency the output phase noise from equation (4.11) can be approximated as:

\[ S_{\text{out}}(\omega_{\text{jitter}}) \approx \frac{\omega_{\text{jitter}}^2 S_{ILO}(\omega_{\text{jitter}})}{\omega_{\text{jitter}}^2 + \omega_p^2} \] (4.13)

Combining equation (4.13) and equation (4.14), the jitter transfer function can be expressed in terms of the phase noise \( S_{ILO} \) and \( S_{\text{out}} \):

\[ |JTF_{\text{input}}(\omega_{\text{jitter}})|^2 \approx 1 - \frac{S_{\text{out}}(\omega_{\text{jitter}})}{S_{VCO}(\omega_{\text{jitter}})} \] (4.14)
This method is used to estimate the jitter transfer of the ring ILO in simulation for different injection strengths, and compared with the theoretical results of Table 4.2 and to simulations where the injected signal is sinusoidally phase modulated in Fig. 4.20. Good agreement is observed.

For burst mode applications, the lock time is an important specification which requires designers to simulate the CDR’s response to phase step. The system’s step response can also be used to estimate its jitter transfer characteristics. Estimates so obtained are shown in Fig. 4.21 and are also in good agreement with the developed theory (Fig. 4.20).

![Figure 4.20: Normalized jitter transfer function for different injection strengths with n=4 stages, an oscillation frequency of 5 GHz and an injection frequency of 10 GHz.](image1)

![Figure 4.21: Transient phase response and corresponding jitter transfer function for different injection strengths with n=4 stages, an oscillation frequency of 5 GHz and an injection frequency of 10 GHz.](image2)

With a large JTB, it is possible to generate a relatively low jitter clock from a low
power (hence, noisy) ring oscillator. Increasing the injection strength $K$ results in faster locking, higher JTB and better jitter tolerance, as illustrated in Fig. 4.20 and 4.21.

### 4.5.5 Experimental Results

For experimental verification, a complete receiver including the equalizer, half rate clock recovery and demultiplexer is implemented in 90-nm CMOS (Fig. 4.22). For testability, probe pads (with a parasitic capacitance of 25 fF each) and buffers are included at the output of the front-end, edge detector and VCO. An AC coupled channel is emulated with on-die 80 fF coupling capacitors and 50 ohm termination resistors. Probe pads with 25 fF capacitance are also included on either side of the coupling capacitors to characterize their frequency response. A schematic of the emulated channel is shown in Fig. 4.22. Excluding the probe pads and test structures, the active area of the receiver is less than 0.3mm$^2$. Experimental verification and optimization of the front-end equalizer has already been documented in section 4.2. The extracted clock tone output has also been shown in section 4.3. This section will mainly focus on clock recovery results.

![Implemented complete receiver in 90 nm CMOS.](image)

Figure 4.22: Implemented complete receiver in 90 nm CMOS.

The receiver was designed to support data rates from 5 to 10 Gb/s requiring the
The ILO to have a tuning range from 2.5 GHz to 5 GHz. The ILO has a tuning range from 2 GHz to 6 GHz as shown in Fig. 4.23(a), providing some margin for process and temperature variations. The simulated and measured lock range are shown over the ILO’s tuning range with different injection strengths, $K$, in Fig. 4.23(b). Note that the input injection frequency is twice the oscillation frequency since the VCO is used as injection locked divider. Theoretically, lock range increases with injection strength and oscillation frequency, $\omega_{lock} \propto K \omega_0$. At higher frequencies, deviation from this trend is observed due to un-accounted-for parasitics at the injection nodes. The receiver is tested with a 10 Gb/s external PRBS source at the input. At 10 Gb/s, the input was provided single-endedly to avoid any intra-pair skew in the test setup. To improve the single-ended signal integrity, the common mode node $V_{\text{com}}$ is coupled to ground with a 10 pF capacitance, but this would not be required in an application where differential inputs are always provided.

The ILO’s free running and locked spectra are shown in Fig. 4.24. The recovered clock and corresponding demuxed data are shown in Fig. 4.25 and the corresponding jitter transfer function is shown in Fig. 4.26. To study jitter accumulation during consecutive identical digits, the phase noise for both an alternating input data pattern (with at most 1 CID) and a $2^7 - 1$ PRBS input data pattern (with at most 7 CIDs) are also plotted in Fig. 4.26. Note that the measured jitter transfer function is in good agreement with theory and simulation. However, the measured phase noise of the free-running VCO and recovered clock was significantly higher compared to simulation due to supply noise not accounted for in the theoretical model. For example, the simulated recovered clock phase noise is better than -125 dBc/Hz at 1 MHz offset (Fig. 4.18) whereas the measured results in Fig. 4.27 show -120 dBc/Hz at 1 MHz offset. Similarly, the simulated ring VCO phase noise is better than -110 dBc/Hz at 30 MHz offset (figure 18) compared to -100 dBc/Hz at the same offset frequency. A burst mode test pattern comprising 10 ns of no data (consecutive 0s) followed by 5 ns of alternating data (1s and 0s) is shown along with the ILO clock output captured on an oscilloscope in Fig. 4.27. The measured lock time is less than 1.5 ns, which is as expected for the measured lock range of 900 MHz.
4.5-10 Gb/s Burst Mode Receiver in 90-nm CMOS

Figure 4.23: Measured tuning range and lock range of the implemented 5GHz 4 stage ring ILO.

Figure 4.24: Spectra of the free running and recovered clock.

4.6 Conclusion

The proposed clock recovery method is compared with previously reported burst mode receivers in Table 4.3. Note that all AC coupled receivers consume more power than their DC counterparts due to the additional circuitry required for NRZ signal recovery. The simple and inductorless implementation of the proposed architecture results in a small area of 0.3mm². Although a low power, poor phase noise ring oscillator is used as an ILO, the jitter of the recovered clock is still comparable to the existing LC VCO based CDRs.
Appendix A

4.6.1 Transient phase Response

To derive the transient phase response of an ILO we define a variable that captures the impact of oscillator topology on the injection dynamics as in [M. 09].

\[ A \approx -\frac{d\tan \Phi}{10^9} \left| \omega - \omega_c \right| \]  (4.15)
4 5-10 Gb/s Burst Mode Receiver in 90-nm CMOS

Figure 4.27: Experimental verification of lock time.

Table 4.3: Comparison of state-of-the-art burst mode clock recovery technique

<table>
<thead>
<tr>
<th></th>
<th>[M. 05]</th>
<th>[L. 05]</th>
<th>[J. 08]</th>
<th>[C. 06c]</th>
<th>[J. 05]</th>
<th>This work</th>
</tr>
</thead>
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<td>AC/DC Coupled</td>
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<td>AC coupled</td>
<td>DC Coupled</td>
<td>DC Coupled</td>
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<td>Full-rate ILO</td>
<td>Gated VCO</td>
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<td>SiGe</td>
<td>90nm</td>
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<td>Lock time</td>
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<td>50ps</td>
<td>&lt;3.2ns</td>
<td>---</td>
<td>&lt;1.5ns</td>
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<tr>
<td></td>
<td>19.6ps p-p</td>
<td>---</td>
<td>8ps p-p</td>
<td>---</td>
<td>---</td>
<td>15.5ps p-p</td>
</tr>
<tr>
<td>Receiver Power</td>
<td>1.2 W</td>
<td>117 mW</td>
<td>175 mW</td>
<td>200 mW</td>
<td>230 mW</td>
<td>70 mW</td>
</tr>
<tr>
<td>Area</td>
<td>6.25mm²</td>
<td>---</td>
<td>0.96mm²</td>
<td>3.4mm²</td>
<td>0.5mm²</td>
<td>0.3mm²</td>
</tr>
<tr>
<td>FoM(pJ/bit)</td>
<td>120</td>
<td>39</td>
<td>8.75</td>
<td>20</td>
<td>23</td>
<td>7.0</td>
</tr>
</tbody>
</table>
The analysis in [L. 65] may then be generalized resulting in the following the locking equation:

\[
\frac{d\theta}{dt} = -\frac{1}{A} \frac{K \sin \theta}{(1 + K \cos \theta)} + \Delta \omega
\]  

(4.16)

The locking equation can be solved for \( \theta(t) \) in two particular cases: small and large injection strength.

**Case I, small injection** \((K \ll 1)\)

In this particular case the locking equation (4.16) can be simplified as follows:

\[
\frac{d\theta}{\Delta \omega - \frac{K}{A} \sin \theta} = dt
\]

(4.17)

To find the transient phase response we integrate both sides. There are two possible solutions depending on the frequency difference between the injected clock tone and free running ILO frequency. First, we will consider a frequency offset small enough to keep the ILO within its lock range: \( \Delta \omega < \omega_{\text{LOCK}} \approx K/A \). In this case the integration yields:

\[
-\frac{1}{\mu} \log \left[ \frac{-\frac{K}{A} + (\Delta \omega) \sin \theta + (\mu) \cos \theta}{\Delta \omega - \frac{K \sin \theta}{A}} \right] = t
\]

(4.18)

where,

\[
\mu = \sqrt{\frac{K^2}{A^2} - \Delta \omega^2}
\]

(4.19)

To further simplify it, we assume that the frequency offset, \( \Delta \omega \) is much smaller than the lock range, i.e. \( \Delta \omega \ll \omega_{\text{LOCK}} \approx K/A \). This assumption is valid when the CDR performs frequency acquisition so that the ILO’s self-resonant frequency \( \omega_0 \) is tuned very close to the incoming data rate. With that assumption, the above equation is simplified to:
\[
\frac{1 + \cos \theta}{\sin \theta} = e^{-\left(\sqrt{\frac{K^2}{A^2} - \Delta \omega^2}\right)t}
\] (4.20)

Substituting, \(\sin(\alpha) = 2 \sin(\alpha/2) \cos(\alpha/2)\) and \(1 + \cos(\alpha) = 2 \cos^2(\alpha/2)\)

\[
\theta(t) = 2 \tan^{-1}\left(e^{-\left(\sqrt{\frac{K^2}{A^2} - \Delta \omega^2}\right)t}\right) + C \approx \theta_0 e^{-\left(\sqrt{\frac{K^2}{A^2} - \Delta \omega^2}\right)t}
\] (4.21)

where \(\theta_0\) is the initial difference between the injected clock phase and free running VCO phase. Substituting \(A = 2Q/\omega_0\) gives the same transient expression derived in [L. 65] for LC oscillators.

**Case II, large injection (K≈1)**

In this case the locking equation (4.16) is simplified as:

\[
\frac{d\theta}{\Delta \omega - \frac{1}{A} \tan(\theta/2)} = dt
\] (4.22)

Similar to the previous case, the time domain phase variation can be obtained by integrating with respect to time:

\[
\frac{A^2}{\Delta \omega^2 A^2 + 1} \left[\left(\Delta \omega\right)\theta - \frac{1}{2A} \log(\Delta \omega \cos \theta/2 - (1/A) \sin \theta/2)\right] = t
\] (4.23)

Within the lock range and for small frequency offset i.e. \(\Delta \omega \ll \omega_{\text{LOCK}} \approx K/A\), \(\theta(t)\) can be further simplified:

\[
\theta(t) = 2 \sin^{-1}[e^{-t/A}] \approx \theta_0 e^{-t/A}
\] (4.24)

In summary, for both small injection and large injection, the phase difference exponentially decreases to zero. For small injection strength the time constant is a strong function of \(K\), \(\tau = -K/A\), whereas for large injection the time constant is independent of \(K\), \(\tau = -1/A\). In [L. 65], this conclusion was derived for LC oscillators whereas in
this work we have generalized it to any VCO topology by appropriately defining $A$. 


5.4 Gb/s 6.8 mW Source Synchronous Receiver in 65-nm CMOS

5.1 Introduction

Parallel interfaces are becoming increasingly important to meet the aggregate bandwidth required in microprocessors, memory, peripheral components, network hubs, storage devices, etc. Combination of technology scaling and architectural innovation have significantly improved power efficiency of these links over the years (Fig. 5.1(a)). This summary includes both source synchronous and asynchronous links. For multilink high aggregate bandwidth interface source synchronous links are useful where their power consumption can be amortized across multiple links in the system. For example, QPI and HyperTransport include a dedicated link to carry a synchronous clock from the transmitter to receiver and shared by 5 - 20 data transceivers. As the data rate has increased to 10+ Gb/s, signal integrity issues translate to eye closure both in vertical and horizontal direction. As a result, receivers timing margin is reduced. In highspeed I/Os power supply induced jitter is considered as the main source of timing noise or jitter. Spectra of this jitter is strongly correlated to the power supply resonance caused by on-die decoupling capacitance combined with bond wire inductance. In most digital systems this resonance frequency varies between 50 MHz to 400 MHz. For example, next generation Intel core (Nehalem) supply network resonates at 300 MHz [N. 09]. Similar impedance profile is also reported in other digital systems [R.S07]. Consequently high speed I/O links are highly sensitive to jitter around this frequency range. Therefore, it is desired that the receivers have higher jitter tolerance between 100 MHz to 400 MHz. One possible solution is to achieve higher tolerance by increasing the jitter tracking bandwidth of the receiver. Unfortunately most of the state-of-the-art clock
and data recovery (CDR) unit’s tracking bandwidth is less than 10 MHz. Increasing the CDR bandwidth beyond 100 MHz can significantly increase power consumption and stress stability requirements. Instead in source synchronous receiver forwarded clock path can be used for jitter tracking as shown in Fig. 5.1(b). In these links phase error is compensated in two ways. First static phase offset is corrected by per pin phase compensation loop. Per pin deskew is done at startup [E. 00]; the optimum deskew setting is stored and the calibration circuitry turned off during normal operation. In some cases where the deskew loop is active during the normal operation, their tracking bandwidth is only in the order of KHz [E. 06]. Second, dynamic phase error is tracked by shared phase tracking loop. Jitter on the forwarded clock is correlated with jitter on the data because both shares a common design and are synchronized by the shared synthesizer. Hence, jitter tolerance is improved by retiming the data with a clock that tracks correlated jitter on the forwarded clock [K. 98]. In ideal scenario, both jitter sequence should appear at receiver side with same latency. Hence, their effect should cancel out. In reality, latency between clock and data path is not perfectly matched. Taking into account the latency mismatch, jitter transfer function (JTF) of the forwarded clock path can be written as \( e^{-(\Delta T)s} H_\Phi(s) \). Here, \( \Delta T \) is the relative skew between data and the clock path and \( H_\Phi \) is the jitter transfer function of the clock.

Figure 5.1: (a) Low power transceiver power efficiency over the years. (b) Clock forwarded receiver architecture.
Using this JTF, jitter tolerance of a forwarded clock receiver can be written as:

\[ J_{TOL}(s) = \left| \frac{5}{1 - e^{-\Delta T s}H_\Phi(s)} \right| \]  

Two existing implementations of \( H_\Phi \) are PLL (\( H_{PLL} \)) and DLL (\( H_{DLL} \)). A second order PLL transfer function can be written as \( H_{PLL} = \frac{2\zeta \omega_n s + \omega_n^2}{s^2 + 2\zeta \omega_n s + \omega_n^2} \). On the other hand DLL transfer function can be written as \( H_{DLL} = \frac{1 + s\tau / \omega_P}{1 + s/\omega_P} \). In the case of a DLL \( \omega_P = I_P / 2\pi(sC_P) \) is the pole introduced by the loop filter. JTF and jitter tolerance for these two implementations are shown in Fig. 5.2 with 5 UI and 1 UI relative skew between clock and data path. In most high speed applications PLL bandwidth is in the order of 10-30 MHz. As a result their jitter tolerance is reduced to .5 UIp around 25 MHz. Note that relative skew between clock and data path has little effect on PLL jitter tracking since high frequency jitter is always filtered. DLL on the other hand provides all pass jitter transfer with small peaking (less than 1 dB). Therefore their jitter tolerance is significantly better than PLL at 100 MHz. However, DLL’s jitter tolerance is strongly influenced by the relative skew between clock and data path. For example, 5 UI skew mismatch causes jitter tolerance reduction to 0.2 UI(peak) at 500 MHz. Given the high sensitivity to jitter around this frequency, the link performance can significantly degrade. High frequency jitter tracking with DLL in the presence of
Jitter sequence of the DLL based forwarded clock receiver with 5 UI latency mismatch. The transmitter is modulated with 100 MHz and 500 MHz sinusoid jitter.

The data and clock path jitter sequence $J_D$ and $J_C$ are defined as the phase deviation from ideal crossing points. Therefore, resultant jitter sequence can be expressed as $J_R = J_D - J_C$. To study the effect of latency mismatch we consider the effective jitter $J_R$ where clock and data path latency difference is 5 UI ($1\ UI=100\ ps$). If the transmitter side phase is modulated with 100 MHz sinusoid, $J_C$ and $J_D$ are well correlated despite the latency mismatch. Consequently resultant jitter is reduced. However, if the transmitter is modulated with 500 MHz jitter, latency causes significant phase shift between $J_D$ and $J_C$ and consequently the resultant jitter is increased. In summary, low and mid-frequency jitter which appears in-phase at the sampling clock is beneficial and should be tracked. But high frequency jitter which appears out of phase due to latency rather degrades timing margin, hence should be filtered. Recently reported results in [A. 08],[R. 10]are in good agreement with this conclusion. In [A. 08] jitter tolerance of DLL based and DLL-PLL based receivers are compared. At 10 MHz the DLL based receiver achieves higher jitter tolerance compared to PLL-DLL combination by track-
ing more correlated jitter. On the other hand, PLL based receiver in [R. 10] achieves higher timing margin by filtering 400 MHz out of phase jitter.

5.2 Background

5.2.1 Optimum Jitter Tracking

To improve jitter tolerance we replace the all pass jitter transfer function with a 1st order low pass filter where the jitter tracking bandwidth (JTB) is varied. To observe the effect of low pass filter transmitter side data signal is phase modulated with sinusoidal jitter $J_D = A \sin(\omega_j t)$. Where, $A$ is the jitter amplitude and $\omega_j$ is the jitter frequency. Forwarded clock signal is also modulated with the same sinusoid jitter with added latency $J_C = A \sin(\omega_j(t - MT))$. Where, $M$ is the skew between clock and data path and $T$ is the bit period. Jitter of the forwarded clock is shaped by a low pass filter, where the low pass jitter filter transfer function is $|H(\omega_j)| = \frac{1}{\sqrt{1 + (\omega_j / \omega_P)^2}}$. Consequently, the resultant jitter can be written as $J_R = J_D - J_C H(\omega_j)$. When normalized to the data signal jitter amplitude, the resultant jitter can be written as:

$$\frac{J_R}{J_D} = 1 - \frac{\sin(\omega_j(t - MT))}{\sin(\omega_j t)\sqrt{1 + (\omega_j / \omega_P)^2}}$$  \hspace{1cm} (5.2)

This theoretical expression of normalized jitter is plotted with behavioral simulation results in Fig. 5.4. Correlated jitter tracking is useful as long as the resultant normalized jitter is less than 1. For this behavioral simulation we phase modulated the transmitted data and clock with 200 MHz sinusoid. Similar results can be obtained for other jitter frequencies. We are interested in finding optimum jitter tracking bandwidth as a function of latency mismatch. For all three jitter frequencies (100 MHz, 200 MHz and 300 MHz)- optimum JTB continues to decrease and eventually for 10 UI or higher latency mismatch there is no benefit of jitter tracking through the forwarded clock path. For less than 1 UI latency mismatch, jitter tolerance monotonically improves with the increase of jitter tracking bandwidth. However, such latency requirement is very difficult to achieve in practical clock forwarded systems. More realistic latency mismatch
for clock forwarded link varies between 2 to 6 UI for which optimum jitter tracking bandwidth varies from 400 MHz to 25 MHz.

\[\text{Figure 5.4: (a) Normalized jitter sequence as a function of jitter tracking bandwidth (b) Optimum jitter tracking bandwidth as a function of skew mismatch between the clock and data path latency.}\]

Another important consideration is jitter amplification. In lossy, bandwidth limited channel forwarded clock jitter is amplified. To avoid jitter amplification sub-rate forwarded clock is preferred. In that case, the forwarded clock must be frequency-multiplied and aligned with the data at each receiver. In summary, the clock path in a clock forwarded transceiver should provide flexible clock multiplication, a controlled phase shift, and a JTB adjustable over 100’s of MHz to accommodate different channel losses, supply resonance, bit rates, and path delay mismatches. In this work we propose a dual phase filtering that potentially provides all the above functionalities: First the fractional rate forwarded clock is multiplied up to a full rate clock with adjustable jitter tracking from 25 MHz to 400 MHz. Each receiver receives this differential distributed clock and generate any sampling phase between 0 → 360. In addition it also provides 1st order jitter filtering to further suppress uncorrelated high frequency jitter.

### 5.2.2 Architecture Review

Source synchronous clocking can be implemented with conventional dual loop architecture with different combinations of DLL, PLL and phase interpolator. A PLL can
provide both clock multiplication and jitter filtering. Dual loop architecture can be adopted with cascaded PLLs: a shared low bandwidth PLL is used as a clock multiplying unit (CMU) and following that a local wide bandwidth PLL which generates multiphase clock required for phase interpolation [J. 07]. A superior phase noise LC VCO is normally used in the shared CMU and a low power ring oscillator is used in the local transceiver. Due to wide bandwidth, ring oscillators phase noise can be filtered up to several hundred MHz. As a result, a low jitter clock can be extracted even from a poor phase noise ring VCO. Conventional PLL is a 2nd order system with two poles contributed by the loop filter and by the VCO itself. Therefore a stabilizing zero is introduced in the loop filter. Jitter tracking bandwidth of the PLL is limited by the stability requirement which must be ensured over process corners with temperature and supply variation. When used in a clock forwarded system, its limited bandwidth filters out useful correlated jitter [A. 08].

To avoid useful jitter filtering most of the existing source synchronous links prefer DLL over PLL. For example, QPI interface implemented in [N. 09] uses DLL to generate multiple phases. These clock phases are distributed to each receiver and then interpolated to generate required sampling phase between 0 → 360. Since, atleast 4 clock phases 0,90,180,270 are distributed in this approach, clock distribution network consumes significant power. Both DLL and phase interpolator provides all pass jitter transfer, hence tracks both in-phase and out-of-phase jitter. In addition high frequency jitter such as duty cycle distortion is amplified. Therefore a DCD correction loop is often required in DLL based systems [F. 06],[A. 08]. Alternatively a phase filter can be implemented by ‘time averaging’ after the DLL which further increases power consumption and complexity. In addition DLL does not provide flexible clock multiplication, hence full rate clock needs to be forwarded.

Injection locked oscillators (ILO) are a power- and area-efficient alternative to PLLs and DLLs. In [F. 08],[K. 09] an ILO performs both jitter filtering and clock deskew by introducing a frequency offset between the ILO’s free-running frequency and the injected frequency. Note that there is no phase detector, charge pump or loop filter is required in this architecture. Therefore, excellent area and power efficiency is reported in [F. 08],[K. 09]. This simple architecture has several limitations. First, the
deskew range is limited and within the deskew range jitter tracking bandwidth varies significantly as a function of phase deskew setting. Theoretical limit of the deskew range is $\pm 90^\circ$. Maximum JTB is achieved for $0^\circ$ phase deskew setting e.g. $(\Delta \omega \approx 0)$ and minimum JTB is resulted at $90^\circ$ phase deskew e.g. $(\Delta \omega \approx \omega_P)$. Consequently, JTB varies over several hundred MHz over different deskew settings. In addition, clock multiplication is not performed.

Similar to PLL, clock multiplication can also be provided using MDLL. Unlike PLL, MDLL does not suffer from jitter accumulation since the phase error is reset to zero on by the next available reference edge. However, duty cycle distortion in MDLL is not filtered due to their all pass jitter transfer characteristics. A ILO is then used to interpolate between the coarse MDLL skew settings and filter out high frequency
periodic jitter generated in the MDLL [H. 03a]. Since only one jitter filter appears in the clock path, a low JTB is required to efficiently filter the high frequency periodic jitter, but that also filters out correlated jitter on the forwarded clock. In addition phase noise generated by the local ILO is insufficiently filtered due to lower jitter tracking bandwidth. As a result ILO phase noise dominates the recovered clock jitter. Moreover, compared to a DLL-only or ILO-only solution, the MDLL-ILO architecture consumes more power.

5.3 Proposed Architecture

Conventional dual loop architecture is implemented as a combination of two ILOs: the shared ILO provides clock multiplication and optimal jitter tracking where as the local ILO provides clock deskewing to retime the data.

5.3.1 CMU and clock distribution

Lowest power clock distribution networks employ narrow band resonant clocking. To support several data rates, a broadband transmission line based clock distribution is preferred [E. 06]. In clock forwarded architecture ondie transmission line can be used
for clock distribution. An open drain CML buffer can be used as a clock transmitter to send the clock signal over the channel and through on-die transmission line at the receiver side. CML buffer needs at least 6 mA current to achieve > 200 mV swing at the furthest receiver. This clock distribution provides a good compromise between power consumption, latency and supply noise rejection. The proposed architecture makes a simple modification to the existing clock distribution - a phase filter is implemented in the form of an injection locked ring VCO. A 3-stage ring oscillator is used as the clock multiplying ILO (MILO) where 2 stage CML inverters are used as tunable delay elements. The 3rd stage is used as clock buffer and to provide additional gain and delay required to meet the oscillation condition. Total power of the clock transmitter is now redistributed between clock tx and VCO buffer to achieve the same swing as before. The VCO is tunable from 1.7 to 4.5 GHz to support 4 Gb/s to 8 Gb/s operation. Compared to existing clock distribution, this ILO based clock distribution does not add any additional latency in the clock path. The only added power consumption in the proposed architecture is in the delay elements. Transistors $M_3$ serve as a cross-coupled

Figure 5.7: (a) Passive clock distribution in clock forwarded link (b) Proposed ILO based clock distribution. Width of $M_1$ and $M_2$ are 60um and width of $M_3$ is 30um.
common-gate clock buffer distributing clock signal across 1mm of on-die transmission line to the local injection locked oscillator (LILO). Inductor $L_1$ provides low Q bandpass filtering to reduce high frequency jitter. It is well known that injection locked oscillator is functionally equivalent to a 1st order PLL. Thus their jitter transfer function can be written as:

$$JT_{INPUT}(\omega_{jitter}) = \frac{1}{1 + j\omega_{jitter}/\omega_P} \quad (5.3)$$

where the pole of the jitter transfer function can be written as

$$\omega_P = \sqrt{\frac{K^2}{A_{VCO}^2} - \Delta\omega^2} \quad (5.4)$$

Here, $K$ is the injection strength, $A_{VCO}$ captures VCO topology dependency and $\Delta\omega$ is the frequency difference between free running VCO frequency $\omega_0$ and injected frequency $\omega_{inj}$. To accommodate clock multiplication, a subrate clock can be forwarded. If injected with a sub rate (quarter-rate or lower) clock, significant amplitude distortion and reference spurs appear at the MILO output. This problem is ameliorated by injecting a pulse train. Unlike NRZ signals, pulse trains effect the MILO output only at their transitions. As a result, amplitude distortion and frequency spurs are significantly reduced. Pulse trains are simply generated using a delay and XOR gate integrated into the clock transmitter of this prototype link (Fig. 5.7). Effective injection strength of the $n_{th}$ harmonic of the pulse train can be obtained using fourier transform:

$$K_n = \frac{2h}{n\pi} \sin \frac{n\pi d}{T} \quad (5.5)$$

for fundamental frequency, $n = 1$, it’s injection strength is expressed as

$$K_1 = \frac{2h}{\pi} \sin \frac{d\pi}{T} \quad (5.6)$$
Similarly, for the $1/N$ sub-rate forwarded clock’s strength can be expressed as

$$K_N = \frac{2h}{N\pi} \sin\frac{d\pi}{T}$$  \hspace{1cm} (5.7)

Using the expression of effective injection strength, the jitter tracking bandwidth can be written as function of pulse repetition rate, $N$, pulse duty cycle, $d/NT$.

$$\omega_p \approx \frac{2h}{AVCO N\pi} \sin\frac{d\pi}{T}$$  \hspace{1cm} (5.8)

Figure 5.8: Transmitted signal and MILO output in time and frequency domain (a) NRZ signal (b) Pulse signal

Figure 5.9: Effective injection strength of a pulse train Phase step response for different duty cycle
Here, we assume negligible frequency offset which is can be ensured with a frequency acquisition loop. The MILO JTB is set by the effective injection strength which is controlled by changing the pulse repetition rate and duty cycle thereby providing continuous adjustment of the JTB from 25MHz to 300MHz. The shared clock circuitry consumes more power than any other block in the link to ensure that even when set to a low JTB, a low phase noise clock is distributed to the LILOs.

5.3.2 Phase Interpolation with injection locking

CMU output is distributed through passive clock distribution network. This low power clock distribution technique provides better supply rejection and lower latency at the cost of smaller signal swing. Each links receiver uses this clock to compensate for the links skew with a deskew circuit. Apart from phase alignment, the deskew block also provides amplification and high frequency jitter filtering to recover high quality clock. Each receiver needs to regenerate multi-phase clock with larger swing sufficient to drive the sampling flip-flops. Existing two approaches are shown in Fig. 5.11(a – b).

In [H. 03a] both 0 and 90 degree clock phases are combined together to inject symmetrically in every stage of the the ring oscillator. By adjusting the relative strength of the injection phase interpolation can be obtained. Advantage of this method is that complete 0° → 360° phase interpolation can be obtained and JTB remains rela-
Figure 5.11: ILO based phase interpolator (a) as in [H. 03a] (b) as in [F. 06](c) this work

Figure 5.12: Implemented ILO based phase interpolator. Width of $M_2$ is 20um

tively constant over the phase interpolation range. But distributing quadrature phases ($0^\circ, 90^\circ, 180^\circ, 270^\circ$) through the die consumes significant power. Alternatively, in [F. 08] only differential phase ($0^\circ, 180^\circ$) is injected to a single point in the VCO. As a result power consumption in the clock distribution network in halved. Phase interpolation is then obtained by detuning the free running vco frequency. Major limitation of this
approach is that the pole of the JTF is a strong function of the frequency offset and hence phase deskew. As a result to obtain phase deskew greater than $\pm 45^\circ$ JTB significantly drops. In addition, compared to previous approach phase deskew range is relatively small.

To overcome the above limitations, the proposed architecture is shown in Fig. 5.11(c), where we combine the benefits of the above architectures. Instead of combining 4 phases, we inject the differential clock into the ring at two points with adjustable polarity and three possible injection strengths to select between 8 coarse deskew settings. Interpolation between these coarse settings is done by slightly detuning the LILO’s free-running frequency. Since only small frequency offsets are required to achieve $\pm 23^\circ$ phase shifts, high JTB can be maintained. The LILO’s JTB exceeds 600MHz so that the overall JTB of the clock path is determined by the MILO, independent of the phase deskew setting. As described in chapter 3, JTB and deskew both depends on frequency offset between free running frequency of the LILO and injected frequency. As a result a closed loop frequency controlling of the LILO is required to achieve high tracking bandwidth and precise deskew control. In this implementation no tracking loop is included. However, frequency tracking technique is discussed in section 6.3.

5.3.3 Phase noise filtering

Phase transfer of the shared CMU and local phase interpolator is shown in Fig. 5.13. The phase noise of the CMU output can be be written as:

$$S_{CMU}(\omega_{jitter}) = \frac{\omega_{jitter}^2 S_{ref}(\omega_{jitter}) + \omega_{jitter}^2 S_{MILO}(\omega_{jitter})}{\omega_{P1}^2 + \omega_{jitter}^2}$$  (5.9)

This CMU output is then filtered by the local phase tracking loop:

$$S_{out}(\omega_{jitter}) = \frac{\omega_{P2}^2 S_{CMU}(\omega_{jitter}) + \omega_{jitter}^2 S_{LILO}(\omega_{jitter})}{\omega_{P2}^2 + \omega_{jitter}^2}$$  (5.10)

This dual loop architecture provides several advantages. Phase tracking of the two loops can be set independently by appropriately choosing $\omega_{P1}$ and $\omega_{P2}$. Here, $\omega_{p}$ is
chosen to optimize correlated jitter tracking. From the behavioral simulations it was found that optimum JTB can vary from 25 MHz to 400 MHz. For lower jitter tracking bandwidth, MILO phase noise is not sufficiently filtered. Therefore it is critical to design the MILO with lower phase noise. As a result MILO consumes more power than any other ILO to ensure low phase noise clock generation even when the tracking bandwidth is low. Fortunately, MILO’s power will be shared by all the receivers hence does not translate to a significant power penalty. On the other hand $\omega_{PI}$ is chosen to filter out phase interpolator VCO phase noise up to 600MHz. With such high JTB very little of the LILO’s self phase noise appears in the recovered clock. As a result, LILO can be designed with lower power improving receiver power efficiency. Another advantage of high tracking bandwidth in LILO is that when used in a burst mode application, each receivers wake up time can be independently adjusted without impacting the jitter tracking. In addition jitter tracking can be adjusted during run time by simply changing the clock transmitter side code word. Very high frequency jitter due to DCD and reference spurs is attenuated by both ILOs. CML delay stages are used in both the MILO and LILO providing good supply noise immunity.
5.4 Implementation And Experimental Results

In high speed I/Os equalizers are used to improve signal integrity by compensating high frequency losses. Each receiver is implemented with an equalizer followed by demultiplexer. The purpose of the equalizer is to improve eye opening and to reduce uncorrelated pattern dependent jitter which will not be tracked by the forwarded clock path. In a relatively low loss channel, simple passive equalizer can provide this functionality with excellent power efficiency.

5.4.1 Passive Equalizer

A passive equalizer in the form of \( C - R \) highpass filter is often used to equalize FR4 traces. Implemented equalizer circuit is shown in Fig. 5.14. Transfer function of the equalizer can be written as:

\[
\frac{V_{in}}{V_{rec}} = \frac{R_2 + sCR_1R_2}{(R_1 + R_2) + sCR_1R_2} \tag{5.11}
\]

DC gain of the equalizer is \( R_2/(R_1 + R_2) \) where as the high frequency gain is 1. Thus the equalizer provides a boost of \( 1 + R_1/R_2 \). The zero and pole of the equalizer can be written as \( \omega_z = 1/CR_1 \) and \( \omega_p = 1/(C(R_1||R_2)) \). In reality, location of the pole is at lower frequency due to input capacitance, \( C_{in} \). Choice of equalizer parameters such as \( R_1, R_2, C \) is driven by the tradeoff between input termination, input time constant and maximum boost. Small \( R_1, R_2 \) degrades input matching and requires larger \( C \) (hence area) to keep the zero at the same location. Larger value of \( R \) increases input time constant. Fortunately, 1:2 demultiplexer introduces less loading compared to higher order demultiplexer. To adjust the location of the zero for different data rates and channel characteristics capacitance \( C \) can be adjusted with a switch as shown in the fig. 5.14(c). Channel responses with and without equalizer is shown in fig. 5.14(d).
Figure 5.14: (a) Implemented Passive equalizer (b) frequency response for 20-inch FR4 PCB trace with and without requalizer (c)-(d) Eye diagram without and with equalization at 10 Gb/s

Figure 5.15: Block diagram with power breakdown and implemented receiver in 65nm CMOS

5.4.2 Experimental Results

The 4-7.4Gb/s 65nm CMOS receiver prototype is tested in a QFN package and operates from a 1V supply. The area and power break down in shown in Fig. 5.15. For
this prototype only a single lane is implemented due to limited area. In practical implementation such as quick path interconnect (QPI) there will be 20 links in parallel. As a result cross-talk jitter component is not captured in this prototype. However, clock distribution network is approximately 1mm which is representative of practical implementation.

Figure 5.16: Verification of 16x clock multiplication

Figure 5.17: Phase noise of the free running VCO along with the recovered clock

The shared clock circuitry consumes 8mW, the LILO phase interpolator consumes
4.4mW and the samplers consume 2.4mW. Excluding shared clock power, each receiver consumes 6.8mW which equals 0.92pJ/bit at 7.4Gb/s. 16x clock multiplication is shown in Fig. 5.16 where the transmitter is loaded with a pattern consists of 16 1’s followed by 16 0’s. From this pattern the delay-XOR combination generates a pulse train that in frequency domain is still a pulse train spaced 250 MHz apart. The MILO locks to the tone at 4 GHz and suppresses the other tones. The reference spur is suppressed by the MILO and low Q passive resonator to -41 dBc.

The phase noise of the clock reference, MILO and LILO is shown in Fig. 5.17. As explained before, MILO free running phase noise is 10 dB better compared to LILO phase noise. Due to dual loop architecture LILO phase noise is filtered up to 1 GHz. Coarse and fine phase interpolation with the ILO is shown in Fig. 5.18. Coarse selections are set by the different injection strength whereas fine interpolation curves are generated by detuning the free running frequency of the VCO. Note that only a fraction of the lock range is used for fine interpolation. Linearity of this phase interpolator is shown in Fig. 5.19. The BER of the receiver for a $2^{31} - 1$ pattern is shown in Fig. 5.20 as a function of deskew setting over 5” FR4 interconnect. Jitter tolerance is tested at 7.4Gbps; BER is less than 10-12 with 0.45Ulpp DJ in addition
Figure 5.19: Phase output as a function of deskew setting and corresponding DNL to 1.5UIpp sinusoidal PJ at 200MHz (Fig. 5.21).

Figure 5.20: Bit error rate as a function of phase deskew at 4Gb/s and 7.4Gb/s over 10” and 5” FR4 traces respectively. BER is measured with $2^{31} - 1$ pattern. Demuxed data and recovered clock are on the right.
5.5 Conclusion

The proposed architecture is compared with state-of-the-art receivers in Table 5.1. All the architecture previously described in section 5.2 are considered in this comparison. Notice that ILO based solutions have achieved significantly better power efficiency compared to PLL or DLL based solution. However, they do not provide the complete functionality of the conventional solutions. The proposed solution combines the functionality of PLL- or DLL-based solutions without sacrificing the excellent power- and area-efficiency offered by injection locking. The high-frequency jitter tolerance achieved (1.5UI at 200MHz) is comparable to oversampling CDRs, a significant improvement over previous low-power clock forwarded receivers.

Figure 5.21: Measured jitter transfer and corresponding jitter tolerance
## Table 5.1: Comparison with state-of-the-art

<table>
<thead>
<tr>
<th></th>
<th>[R. S07]</th>
<th>[A. 08]</th>
<th>[F. 08]</th>
<th>[K. 09]</th>
<th>[H. 03a]</th>
<th>(This Work)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Architecture</strong></td>
<td>PLL-PI</td>
<td>DLL</td>
<td>ILO</td>
<td>ILO</td>
<td>MDLL-ILO</td>
<td>MILO-ILO</td>
</tr>
<tr>
<td><strong>Data Rate</strong></td>
<td>6.25Gb/s</td>
<td>5Gb/s</td>
<td>27Gb/s</td>
<td>7.2Gb/s</td>
<td>8Gb/s</td>
<td>7.4Gb/s</td>
</tr>
<tr>
<td><strong>Clock Multiplication Ratio</strong></td>
<td>16x</td>
<td>1x</td>
<td>1x</td>
<td>1x</td>
<td>1x,2x,4x,5x, 8x,10x</td>
<td>1x,2x,4x, 8x,16x</td>
</tr>
<tr>
<td><strong>Clock Frequency</strong></td>
<td>$\frac{1}{2}$-rate</td>
<td>$\frac{1}{3}$-rate</td>
<td>$\frac{1}{2}$-rate</td>
<td>$\frac{1}{3}$-rate</td>
<td>$\frac{1}{4}$-rate</td>
<td>$\frac{1}{2}$-rate</td>
</tr>
<tr>
<td><strong>Ref. Spur</strong></td>
<td>——</td>
<td>——</td>
<td>——</td>
<td>——</td>
<td>——</td>
<td>-32 dBc</td>
</tr>
<tr>
<td><strong>Clock Jitter (ps rms)</strong></td>
<td>——</td>
<td>——</td>
<td>——</td>
<td>1.4-3ps</td>
<td>1.8-6.6ps</td>
<td>1.4ps (N=1) 4ps(N=16)</td>
</tr>
<tr>
<td><strong>Jitter Tracking BW</strong></td>
<td>——</td>
<td>All pass</td>
<td>100MHz-750MHz (varies w/ phase)</td>
<td>30MHz-100MHz</td>
<td>——</td>
<td>25MHz-300MHz</td>
</tr>
<tr>
<td><strong>Jitter tolerance</strong></td>
<td>——</td>
<td>0.72UI @ 15MHz</td>
<td>0.3UI @ 100MHz</td>
<td>——</td>
<td>——</td>
<td>1.5UI@ 200MHz</td>
</tr>
<tr>
<td><strong>Technology</strong></td>
<td>90nm</td>
<td>0.13um</td>
<td>45nm</td>
<td>90nm</td>
<td>0.13um</td>
<td>65nm</td>
</tr>
<tr>
<td><strong>Area</strong></td>
<td>0.153mm$^2$</td>
<td>0.157mm$^2$</td>
<td>0.015 mm$^2$</td>
<td>0.017 mm$^2$</td>
<td>0.08mm$^2$</td>
<td>0.03 mm$^2$</td>
</tr>
<tr>
<td><strong>Rx Power</strong></td>
<td>8.2mW</td>
<td>32.25mW</td>
<td>43mW</td>
<td>4.3mW</td>
<td>33mW</td>
<td>6.8mW</td>
</tr>
<tr>
<td><strong>CMU Power</strong></td>
<td>3.6mW</td>
<td>——</td>
<td>——</td>
<td>——</td>
<td>0</td>
<td>4mW (+4mW tx)</td>
</tr>
<tr>
<td><strong>FOM (pJ/bit)</strong></td>
<td>1.31</td>
<td>6.45</td>
<td>1.6</td>
<td>0.6</td>
<td>4.125</td>
<td>0.92</td>
</tr>
</tbody>
</table>
6 Conclusion

6.1 Summary

Concepts and architectures developed in this work have been demonstrated in two common receivers for high speed I/Os: one clock forwarded and one clock embedded receiver. Both receivers have improved the state-of-the-art receiver power efficiency. They are summarized in Table 6.1. The AC coupled receiver needs pulse to NRZ conversion which consumes an additional 27 mW. Excluding this additional circuitry, it’s power efficiency is to 4.3pJ/bit, which is still higher than the clock forwarded link. Since in the clock forwarded link high frequency jitter is tracked through a common link, it’s power consumption (8 mW) is shared by all the links in the receiver and as a result their power efficiency significantly improves. However, note that forwarded clock link only tracks common mode jitter, for example, supply noise. Pattern dependent jitter such as crosstalk is not tracked by clock forwarded path. In addition, to realize the benefit of high frequency jitter tracking, latency between clock and data path should be restricted to less than 5UI. Clock embedded receivers does not suffer from these limitations due to dedicated jitter tracking for each receiver. However, this added circuitry reduces their power efficiency. To summarize, in a parallel interface where 10 to 20 links can be used, clock forwarding provides a simple power efficient jitter tracking. However, for small number of links, where overhead of clock forwarding is expensive, clock embedded receivers will be more useful.

6.2 Major Contributions

This work mainly focused on receiver architecture for $1 - D$ partial response channel. However, the clocking solution is general enough to be used in other types of channels.
Table 6.1: Summary of the low power receivers in CMOS

<table>
<thead>
<tr>
<th></th>
<th>Forwarded clock</th>
<th>Embedded clock</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>65nm CMOS</td>
<td>90nm CMOS</td>
</tr>
<tr>
<td>Data rate</td>
<td>7.4 Gb/s</td>
<td>10 Gb/s</td>
</tr>
<tr>
<td>Equalization</td>
<td>Passive Eq (0mW)</td>
<td>Hysteresis latch + Linear amp + summer (27mW)</td>
</tr>
<tr>
<td>VCO/VCDL</td>
<td>R-Load Ring VCO (4.4mW)</td>
<td>R-Load Ring VCO (6mW)</td>
</tr>
<tr>
<td>Additional</td>
<td>Shared Clock Multiplier (8mW)</td>
<td>Edge detector (20mW)</td>
</tr>
<tr>
<td>Demultiplexer</td>
<td>2.2mW</td>
<td>12mW (4 mW w/o buffer)</td>
</tr>
<tr>
<td>Total Power</td>
<td>6.8 mW + 8mW/number of Rx</td>
<td>70mW</td>
</tr>
<tr>
<td>FoM</td>
<td>1pJ/bit</td>
<td>7pJ/bit</td>
</tr>
</tbody>
</table>

such as conventional DC coupled chip to chip links. Main contributions of this work are:

- Chapter 2 introduces two novel architectures to recover NRZ signal recovery for a 1−D channel. In the first approach, using the full-rate architecture, the threshold settling and output settling are improved to achieve higher speed. In the second approach, the imposed limitation is alleviated by introducing a half-rate architecture which can potentially double the achievable data rate. Analysis, simulation and measurement results for both architectures are summarized in the following publication:


- Chapter 3 proposes a VCO with an inherent buffer that re-uses the VCO bias current and provides large driving capacity without additional power consumption. A study on injection locked oscillator for transient locking behavior, jitter
transfer and jitter tolerance characteristics with a goal to use ILO as a clock recovery unit. A theoretical framework for ILO behavior is provided in this chapter that is VCO topology-independent, so that it can be used for both LC and ring VCOs. Theory, simulation and measurement results are documented in the following publications:


C1: “20 GHz low power QVCO and De-skew techniques in 0.13um digital CMOS.” Hossain, M.; Carusone, A.C.; IEEE Custom Integrated Circuits Conference, 2008. (Best Student paper award)

• In chapter 4, a complete AC coupled receiver is implemented which utilizes the architecture developed in chapter 2 and 3. High pass channel response of an AC channel results in favorable jitter transfer, which is advantageous for high tracking bandwidth CDR. Analysis, simulation and measurement results of this concept is provided into following journal paper and conference paper:


• Chapter 5 discusses the techniques for optimum correlated jitter tracking in a clock forwarded receiver. High jitter tracking bandwidth of the ILO is utilized to achieve higher jitter tolerance. This part of the work is published in the following conference paper:

In addition to the above publications, the AC coupled receiver architecture has also been used by another researcher to facilitate frequency division communication systems for chip-to-chip links:


6.3 Future work

In this work so far it is assumed that ILO’s free frequency is tuned close to the injected clock frequency (or it’s multiple). However, in a practical system some frequency acquisition loop would be required to control the free running frequency of the ILO. One possible solution is to use a PLL with replica ILO for frequency acquisition as shown in Fig. 6.1. Functionality of approach is verified in [F. 10]. An alternative approach can be to use a DLL for frequency calibration as shown in Fig. 6.2. Note that compared to PLL, DLL provides better supply noise rejection and unconditionally stability.
6 Conclusion

Figure 6.1: Frequency acquisition with PLL and replica ILO

Figure 6.2: Frequency acquisition with DLL and replica delay element
References


6 References


6 References

