EMI Reduction in Discrete SMPS Using Programmable Gate Driver Output Resistance

by

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A thesis submitted in conformity with the requirements for the degree of Master of Applied Science
Graduate Department of Electrical and Computer Engineering
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Abstract

A gate driver IC with programmable driving strength to reduce electromagnetic interference (EMI) in SMPS is presented in this thesis. The design builds on previous segmented gate driver designs that have been used to improve light load efficiency. The presented solution is to dynamically adjust the output resistance $R_{out}$ at the arrival of each gate pulse to minimize EMI while maintaining low switching loss. Dynamically adjusting $R_{out}$ is not possible with conventional gate driver designs. Thus, a segmented gate driver is designed and fabricated in the AMS 0.35μm 40V HVCMOS process. Unlike traditional snubber circuits, the proposed method does not require extra discrete components that dissipate energy. Experimental results indicate up to a 7dBμV improvement in peak Conducted EMI (CEMI) between 20 MHz and 30 MHz and a 150μV/m improvement in peak Radiated EMI (REMI) between 88 MHz and 216 MHz.
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Chapter 1  Introduction

As discrete Switch Mode Power Supplies (SMPS) are being operated at higher frequencies, the need to reduce electromagnetic interference (EMI) is becoming critical [1]. This need arises as the maximum EMI guidelines set forth by organizations such as the American Federal Communications Commission (FCC) and the European Comité International Spécial des Perturbations Radioélectriques (CISPR), must be strictly adhered to by commercial electronics [2]. Furthermore, EMI can interfere with the operation of circuits connected to or nearby the SMPS, causing them to malfunction [3]. Nevertheless, EMI mitigation is ideally carried out without decreasing the efficiency or increasing the size or weight of the SMPS.

1.1  Discrete Low Voltage SMPS

Switch mode power supplies built using discrete components are an essential subsystem of modern commercial electronics. Not only do SMPS provide systems with a high efficiency method of converting electrical energy from one voltage level to another, they are also highly flexible and allow the designer of the system a great deal of design freedom. This freedom arises as the designer is free to mix and match discrete components as they wish in order to optimize the converter for their specific application. These optimizations may take the form of conversion ratio, load current, weight, size and even its monetary cost.

However, this flexibility does come at an expense as discrete SMPS systems cannot be switched as quickly as their integrated counterparts [4]. This limitation means that in order to meet output voltage ripple requirements, the passive components of the converter must be made larger [5], subsequently increasing the size, weight and cost of the converter. Furthermore, some SMPS enhancement techniques are unavailable to the discrete designer, such as segmentation of the output stage in order to increase light load efficiency.
1.2 EMI and EMC in SMPS

A recent trend for SMPS design is to increase the switching frequency in order to reduce the passive component size and subsequently increase energy density [6]. However, a result of this trend (and the use of SMPS in general) is that the EMI generated by these systems has become a serious problem [7]. Increased EMI degrades the electromagnetic compatibility (EMC) of devices connected to or operating close to the SMPS. In other words, the EMI generated by SMPS can render nearby devices inoperable. There are two forms of EMI that SMPS generate; conducted EMI and radiated EMI [8].

Conducted EMI is emitted by SMPS as they draw current periodically at the switching frequency from the input power source [27]. This periodic current draw causes both voltage and current distortion in other devices connected to the same power source. A fundamental characteristic of this distortion are the harmonics; much of the interference occurs at frequencies well above the switching frequency [27]. Furthermore, ringing at nodes within the SMPS can also develop into conducted EMI [9]. The FCC conducted EMI standards are defined between 150 kHz and 30 MHz [10].

Radiated EMI occurs when the SMPS generates radio waves that are emitted outward in all directions by the circuit. Radiated EMI is particularly difficult to mitigate as it can cause circuitry simply located near the SMPS to malfunction even if it is not physically connected to the SMPS in any way. The same negative effects of conducted EMI exist for radiated EMI. However, radiated EMI has the potential for severe impact on radio systems [11]. The FCC radiated EMI standards are defined for frequencies above 30MHz.

As the control circuitry of the SMPS is often directly connected to the same supply, EMI can cause malfunctions to occur in this circuitry as well. Thus, an SMPS that exhibits excessive EMI can actually cause itself to malfunction [12]. The impact of EMI can be particularly worrisome to system designers when the SMPS is to be used in mission critical applications such as medical or aerospace equipment.

1.3 Thesis Objective and Overview

The objective of this work is to reduce EMI in a synchronous buck converter without reducing efficiency and without the other penalties associated with traditional EMI reduction techniques.
In particular, this work will focus on whether or not a segmented voltage driven gate driver can be employed to reduce both conducted and radiated EMI. This work is important as conducted EMI can cause unwanted operation of devices connected to SMPS. Furthermore, many of the established EMI reduction techniques degrade the benefits of using an SMPS in the first place, such as reduced physical size and high conversion efficiency.

In order to accomplish the goal of this thesis, a segmented gate driver IC is fabricated and incorporated into a discrete buck converter system. A novel technique for operating the segmented gate driver IC is developed and experimental results are performed in order to verify that the technique reduces EMI while ensuring that efficiency is not reduced.

This thesis is organized as follows; Chapter 2 reviews the required background information, Chapter 3 discusses the proposed EMI reduction technique and the segmented gate driver design, Chapter 4 reviews the physical implementation and experimental results. Finally, conclusions and future work are discussed in Chapter 5.
Chapter 2  
Background & Research Motivation

The basic operating principles and existing EMI suppression techniques are discussed in this chapter.

2.1 The Synchronous Buck Converter

One of the most common forms of SMPS is the synchronous buck converter. Synchronous buck converters are used to convert DC electrical power to a lower DC voltage level [13]. Power conversion efficiencies above 90% can be practically realized with this topology [14]. An example of the basic synchronous buck converter is shown in Figure 2.1.

2.1.1 Basic Operation of the Synchronous Buck Converter

The buck converter operates by repeatedly connecting the switching node \((V_x)\) to either the input power source \((V_g)\) or ground using switches \(M_1\) and \(M_2\). The result of this operation is that a square wave is formed at the switching node of the converter.

![Figure 2.1 Basic Synchronous Buck Converter Topology](image-url)
The operation of the converter is strongly related to the characteristics of this switching node square wave. During continuous conduction mode (CCM), the converter is operated such that the waveforms shown in Figure 2.2 are realized [15]. During CCM, the output voltage of the converter is shown to be related to the duty cycle of the switching node voltage by (2.1) [15].

![Figure 2.2 CCM Switching Waveforms](image-url)
However, CCM only occurs when the current flowing through inductor $L$ does not become zero. If a zero inductor current does occur during the operation of the converter, the converter is said to be operating in discontinuous conduction mode (DCM) [16]. During DCM, the converter is operated such that the waveforms in Figure 2.3 are realized [16]. During DCM, the output voltage is shown to be related to duty cycle of the switching node voltage by (2.2) [16].

Figure 2.3 DCM Switching Waveforms
While (2.1) and (2.2) are first order approximations of the behavior of the buck converter, they are accurate enough that they can be used for practical control of the converter. The work in this thesis focuses on the behavior of the converter during CCM. During CCM, the transfer function of the converter from duty cycle input to the output voltage can be approximated by (2.3) [17]. Since (2.3) is a linear transfer function, the output voltage of the converter can be controlled using traditional, closed loop control system techniques [17]. Accurate control of the output voltage is an important requirement of many applications. Furthermore, (2.1) does not consider the effect of changing load current, temperature and age. These unconsidered factors may distort the output voltage but they can be corrected for using a closed loop feedback system. An example of a typical closed loop control system for the buck converter is shown below in Figure 2.4. The system shown uses a feedback loop composed of voltage divider, a PID controller and a pulse width modulator.

\[
M = \frac{V_{\text{Out}}}{V_{\text{IN}}} = D
\]  \hspace{1cm} (2.1)

\[
M = \frac{2}{1+\sqrt{1+4K/D^2}}, \ K = \frac{2L}{RT_S}
\]  \hspace{1cm} (2.2)

\[
G_{\text{VD}}(s) = \frac{G_{d0}}{1+\frac{s}{Q\omega_0}+\left(\frac{s}{\omega_0}\right)^2}
\]  \hspace{1cm} (2.3)

\[
G_{d0} = \frac{V}{D} \quad Q = R\sqrt{\frac{C}{L}} \quad \omega_0 = \frac{1}{\sqrt{LC}}
\]
2.1.2 The Synchronous Buck Converter and Dead Time

The basic operation of the buck converter discussed in in Section 2.1.1 reveals a potential problem with the power switches. As Figure 2.2 and Figure 2.3 show, switches $M_1$ and $M_2$ are enabled and disabled in a successive, recurring manner. This operation theoretically works well as only one of the switches should be enabled at any given time. However, power semiconductor switches cannot turn on and off instantaneously. This fact results in a potential situation where one switch is activated before the other one has been given sufficient time to turn off. If this situation occurs, power source $V_g$ will be shorted to ground through switches $M_1$ and $M_2$, a phenomenon known as cross conduction [18]. This is a highly undesirable occurrence as it wastes energy and could destroy the converter.

![Figure 2.4 Closed Loop Buck Converter](image-url)
Nevertheless, there is an established method for mitigating cross conduction current. This method is achieved by introducing what is known as dead-time into the gating signals of the converter [19]. An example of dead-time is as shown in Figure 2.5.

![Figure 2.5 Dead Time Gating Example](image)

Dead-time occurs when a time delay is inserted between switch transitions during which neither switch is enabled. The length of this dead-time period is essential; too short of a period will cause cross conduction and too long of a period will create a period of time where neither switch is conducting properly [19]. If MOSFET power switches are used and the dead-time period is too long, the body diode of the low side power MOSFET ($M_2$), will begin to conduct, causing power losses. The optimal dead-time period may change with the operating conditions of the converter. Adaptive dead-time techniques have been developed so that optimal conditions are always used by the converter [20].
2.2 Sources of Power Loss in Synchronous Buck Converters

The synchronous buck converter exhibits different power losses; these include switching loss, gate driver loss, gate charge loss and conduction loss.

![Digital Contoller Diagram](image)

**Figure 2.6 Digitally Controlled Synchronous Buck Converter Topology**

2.2.1 Switching Loss

Like all power MOSFETs, the high-side and low-side MOSFET switches ($M_1$ and $M_2$ respectively) do not switch on and off instantaneously. The result of this non-zero switching time is that for every cycle, there is an instantaneous power loss associated with every switch known as switching loss [21]. When a MOSFET switch is observed while it turns off, it can be easily seen how switching loss occurs. In this case, switching loss occurs because current does not immediately cease to flow through the switch as it turns off. Thus, as the forward blocking voltage of the switch begins to increase, current is still flowing through the device, causing power loss. An example of the voltage and current waveforms for $M_1$ during turn-off as well as the instantaneous power loss during the transition are shown in Figure 2.7.
From Figure 2.7 it can be seen that the switching loss can be expressed as (2.4) where $f_{sw}$ is the switching frequency, $V_{DS}$ is the drain to source voltage that is blocked in the off state, $I_L$ is the load current and $T_{ON}$ and $T_{OFF}$ are the turn on and turn off times, respectively. From (2.4) it can be seen that the switching loss scales linearly with both switching frequency and the transition times of the switches. This observation is particularly relevant as there is currently a trend to increase the switching frequency of SMPS in order to reduce passive component size. Furthermore, from (2.4) it can be seen that switching loss can be mitigated by ensuring fast transition times for the MOSFET switches.

\[
P_{\text{Switching Loss}} = f_{SW} \times V_{DS} \times I_L \times \left(\frac{T_{ON} + T_{OFF}}{2}\right)
\]  

(2.4)
2.2.2 Gate Driver Loss

Figure 2.6 shows that the gates of the power MOSFETs are driven by a pair of gate drivers. These circuits are used in order to quickly charge and discharge the large input capacitances at the gates of the MOSFETs. In typical voltage gate driver designs, the gate driver is composed of a chain of successively larger inverters. As a result, several capacitances inside the gate driver are charged and subsequently discharged every cycle. The power loss in the gate driver can be modeled as (2.5) where \( F_{SW} \) is the switching frequency, \( V_{dd} \) is the gate drive voltage, \( f \) is the inverter chain fan-out, \( N \) is the number of stages, \( C_{in} \) and \( C_{out} \) are the input and output capacitances respectively and \( P_{Static} \) represents static loss in the converter due to current leakage [22].

\[
P_{Gate\,Driver} = F_{SW} \times V_{SW}^2 \times \left( \frac{f^{N-1}}{f-1} \right) \times (C_{IN} + C_{OUT}) + P_{Static}
\]  

From (2.5) it can be seen that the gate driver loss is independent of load current and the transition times of the MOSFET, but is highly dependent on the structure of the gate driver. The characteristics of switching loss and gate drive loss have been leveraged in segmented gate driver designs in order to improve light load efficiency in discrete SMPS designs [23].

2.2.3 Gate Charge Loss

The gate charge loss of the converter arises due to the charging and discharging of the gate capacitances of the MOSFET switches that occurs with every cycle of the converter. By analyzing Figure 2.6, it can be seen that the gate charge loss can be given by (2.6) where \( C_G \) is the gate capacitance, \( V_{Gate} \) is the gate voltage and \( f_{SW} \) is the switching frequency [24].

\[
P_{Gate} = C_G \times V_G^2 \times f_{SW}
\]  

\[
C_G \propto W \times L
\]
From (2.6) and (2.7) it can be seen that gate charge loss is proportional to the width of the gate MOSFET, $W$, for a given feature size $L$.

### 2.2.4 Conduction Loss

The conduction loss of the converter arises due to parasitic resistances that are found in the converter. A common example of conduction loss is the on-resistance of the MOSFET switches [25]. Analyzing Figure 2.6 shows that the conduction loss due to the on-resistance in the MOSFET switches is given by (2.8) where $I_L$ is the load current and $R_{ON}$ is the on-resistance of the MOSFETs (assuming the high side and low side MOSFETs are identical).

\[
P = I_L^2 \times R_{ON}
\]  \hspace{1cm} (2.8)

\[
R \propto \frac{L}{W}
\]  \hspace{1cm} (2.9)

Equations (2.8) and (2.9) show that the conduction loss is inversely proportional to the width of the gate MOSFET, $W$, for a given feature size $L$. Thus, there is a tradeoff between the gate charge loss and the conduction loss of the converter. This tradeoff is leveraged in segmented output stage designs in order to improve light load efficiency in integrated SMPS designs.
2.3 FCC Electromagnetic Interference Guidelines

2.3.1 Conducted EMI FCC Guidelines

The FCC guidelines for conducted emissions are discussed in section 15.107 of the FCC standards [26]. In particular, these are the emission limits for non Class-A digital devices. These guidelines consist of the maximum emission levels that are allowed to be conducted by a device. The maximum allowed level is highly dependent on the frequency of the emission.

Table 2.1 shows these maximums and Figure 2.8 shows a graphical representation of them. The conducted EMI guidelines are only defined between 150 kHz and 30 MHz. Above 30 MHz, the emission guidelines are only defined for radiated emissions, which are described below in Section 2.3.2. No guidelines are defined for any emissions below 150 kHz. As there are no conducted emission guidelines set forth by the FCC for frequencies above 30 MHz and below 150 kHz, the work in this thesis only examines the impact on conducted emissions between 150 kHz and 30 MHz.

<table>
<thead>
<tr>
<th>Frequency of Emissions (MHz)</th>
<th>Conducted Limits (dBµV)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Quasi-Peak</td>
</tr>
<tr>
<td>0.15-5</td>
<td>66-56*</td>
</tr>
<tr>
<td>0.5-5</td>
<td>56</td>
</tr>
<tr>
<td>5-30</td>
<td>60</td>
</tr>
</tbody>
</table>

*Decreases with the logarithm of frequency
The FCC guidelines for radiated emissions are discussed in section 15.109 of the FCC standards [26]. These guidelines consist of the maximum measured values of radiated emissions that can be detected at various frequencies. Table 2.2 shows these maximums and Figure 2.9 shows a graphical representation of them. The conducted EMI guidelines are only defined above 30 MHz. Thus the work presented in this thesis only focuses on the impact of the proposed technique on radiated emissions above 30 MHz.

2.3.2 Radiated EMI FCC Guidelines

Figure 2.8 FCC Conducted EMI Guidelines (Quasi Peak)
Table 2.2 FCC Radiated EMI Guidelines

<table>
<thead>
<tr>
<th>Frequency of Emission (MHz)</th>
<th>Field Strength (µV/m)</th>
</tr>
</thead>
<tbody>
<tr>
<td>30-88</td>
<td>100</td>
</tr>
<tr>
<td>88-216</td>
<td>150</td>
</tr>
<tr>
<td>216-960</td>
<td>200</td>
</tr>
<tr>
<td>Above 960</td>
<td>500</td>
</tr>
</tbody>
</table>

![Figure 2.9 FCC Radiated EMI Guidelines](image)

2.4 Sources of EMI in the Buck Converter

2.4.1 Current Switching

The current switching of the buck converter contributes significantly to the nature of the conducted EMI spectrum. During continuous conduction mode (CCM) operation, the current drawn from the primary power supply, $I_g$, resembles what is shown in Figure 2.10 [27]. It should
be noted that while synchronous buck converters can be operated in two general modes; continuous conduction mode (CCM) and discontinuous conduction mode (DCM), EMI analysis for DCM operation will produce a similar result to CCM operation.

![Input Current Waveform, $I_g$, for CCM Operation](image)

**Figure 2.10 Input Current Waveform, $I_g$, for CCM Operation**

By analyzing Figure 2.10, the Fourier series of $I_g$ can be determined (2.10) where $D$ is the duty cycle and $I$ is the load current [27]. It is shown in (2.10) that the current switching will create conducted EMI harmonics at multiples of the switching frequency that decay inversely with increasing frequency.

\[
f(t) = DI + \sum_{k=1}^{\infty} \frac{2I}{k\pi} \times \sin(k\pi D) \times \cos(k\omega t)\]

(2.10)

2.4.2 MOSFET Gate Node Ringing

As the gate nodes of both M1 and M2 are being driven with a square wave, they have a tendency to ring at the rising and falling edge of the square wave. This ringing is the result of an interaction that occurs between the gate driver and the MOSFET gate. As shown in Figure 2.11, the output resistance of the gate driver ($R_{out}$), the parasitic inductance from the PCB trace between the gate driver IC and the power MOSFET ($L$) and the gate capacitance of the power
MOSFET \( (C_g) \), form a series RLC circuit. As \( R_{out} \) is kept low in order to minimize the transition times, this RLC circuit is often under-damped, causing ringing at \( V_g \). This ringing has a tendency to be amplified by the MOSFET switches, and subsequently appears at the switching node of the converter, causing oscillations in current draw and subsequently increases EMI [28].

![Figure 2.11 Gate Driver MOSFET RLC Circuit Formation](image)

2.5 Typical EMI Reduction Techniques

2.5.1 Input Filtering

Input filtering refers to the practice of placing a low pass filter between the primary power source of the converter and the converter itself as shown in Figure 2.12 [29]. Input filtering works by averaging the input current seen by the primary power source as demonstrated in Figure 2.13 for the L-C filter shown in Figure 2.12 and thus significantly reduces the harmonics of (2.10).

![Figure 2.12 An Example of Input Filtering](image)
While input filters are effective at eliminating conducted EMI they have two major drawbacks. First, the presence of an inductive circuit between the primary power source and converter changes the transfer characteristics of the power converter, making the converter more difficult to control [30]. Secondly, effective input filtering can require large passive components, increasing the size, weight and cost of the converter.

\[ I_g(t) \quad [A] \]
\[ Duty \ Cycle \ (D) \]
\[ Period \ (Ts) \]
\[ Time \ [s] \]

**Figure 2.13** Input Current Waveform, \( I_g \), With and Without Input Filtering

### 2.5.2 Snubber Circuits

Snubber circuits are often added to SMPS in order to reduce EMI. Snubbers operate by either dampening or clamping the current or voltage found at a particular node, eliminating the ringing, overshoot and undershoot that cause EMI [31]. A pair of snubber circuits that are commonly used to reduce EMI in buck converters is the RLD and RCD snubbers [32]. Examples of the RLD and RCD snubbers and how they are applied to the buck converter are shown in Figure 2.14 and Figure 2.15, respectively.
While snubber circuits are quite effective at eliminating EMI, they are commonly dissipative in nature [33]. In other words, they either absorb energy from the circuit or they slow down the transition times, ultimately increasing switching loss. Furthermore, snubbers require extra passive components; increasing the size, weight and cost of the converter in a similar manner to input filtering.

Figure 2.14 RLD Snubber Applied to Synchronous Buck Converter
2.5.3 Spread Spectrum Operation

Spread spectrum operation reduces EMI by taking the harmonics that results from the switching frequency of the converter and distributing them over a wide range of frequencies instead of concentrating them at the clock frequency and its harmonic multiples [34]. This behavior is achieved by dynamically varying the switching frequency of the converter in real time. An example of the impact of spread spectrum operation on conducted EMI is shown in Figure 2.16 and Figure 2.17.
Figure 2.16 Averaged EMI spectrum of the input current to the DC-DC converter with fixed frequency (Source: [35])

Figure 2.17 Averaged EMI spectrum of the input current to the DC-DC converter with the spread spectrum enabled. (Source: [35])

Spread spectrum operation lends itself better to integrated designs, where the custom analog and digital components required for a changing clock frequency can be easily and compactly implemented. Furthermore, the clock frequency of the converter cannot be spread over too large a range as the efficiency and ripple performance of the converter may begin to be affected. Also, with a digital PID controller, the location of the poles and zeroes are dependent on the clock frequency, thus with spread spectrum operation, the controllers behavior could become unpredictable [34].
2.6 Typical Gate Driver Topologies

2.6.1 Voltage Driven Gate Drivers

Voltage driven gate drivers are the simplest and most commonly used gate drivers in SMPS. These gate drivers operate by charging and discharging the gate capacitance of the MOSFETs with a constant voltage source through a series resistance [36]. A simplified example of a voltage driven gate driver is shown in Figure 2.18. An interesting characteristic of voltage driven gate drivers is that while the output resistance of the gate driver limits its maximum switching speed (as in (2.11)), it has no effect on the power consumption of the gate driver, as can be seen in eqn. (2.12).

![Simplified Voltage Driven Gate Driver Topology](image)

Figure 2.18 Simplified Voltage Driven Gate Driver Topology

\[
\Delta T = 1.6 \times R_V \times C_G \tag{2.11}
\]

\[
P_{\text{Loss}} = f_{SW} \times C_G \times V_S^2 \tag{2.12}
\]
2.6.2 Current Driven Gate Drivers

Current driven gate drivers operate by charging the gate capacitance with a constant current source [36]. These gate drivers were originally developed in order to replace voltage driven gate drivers at higher frequencies of operation [36]. A simplified example of a current driven gate driver is shown in Figure 2.19. These gate drivers are more complicated than voltage driven gate drivers and are thus less commonly used. This complexity arises as high quality current sources are difficult to produce. As long as the inequality in eqn. (2.13) holds, the power consumption (2.14) of the current driven gate driver is less than that of voltage driven gate driver for the same charge and discharge time \( \Delta t \) [36]. However, a particularly fascinating aspect of the current driven gate driver is that the current source is constantly delivering current. This situation causes a potential problem if the gate driver is operated at lower frequencies as the current source will spend much of its time wasting power over \( R_F \) instead of delivering charge to the gate. A minimum practical switching frequency is thus often exhibited in current driven gate drivers, below which their efficiency advantage over voltage driven gate drivers is negated [36].

\[
\frac{R_C + (1-2\Delta T) \times 8 \times R_F}{R_V} < 1
\]  
(2.13)

\[
P_{Loss} = f_{SW} \times C_G \times V_S^2 \times \left[ \frac{R_C}{R_V} + (1 - 2\Delta T) \left( \frac{BR_F}{R_V} \right) \right]
\]  
(2.14)
2.6.3 Resonance Driven Gate Drivers

Resonance driven gate drivers operate by transferring energy from an inductor into the gate capacitance [36]. A simplified example of a resonance driven gate driver is shown in Figure 2.20. Clamped resonance occurs when the diode $D_{clamp}$ and resistor $R_p$ are added to the circuit, full resonance occurs when these circuit elements are removed. In clamped resonance, the charge time of the gate driver is dictated by the Q factor of the circuit (2.15) as shown in Figure 2.21, but the gate voltage is clamped to voltage $V_S$. In full resonance, both the turn on time and the final gate voltage are determined by the Q factor.

$$Q = \sqrt{\frac{L_R}{C_G}}$$

(2.15)

An advantage of the resonance driven gate driver is that energy can be recovered from the circuit, eliminating some loss. However, this comes at the expense of several discrete components that must be added to the system, increasing the weight and cost.
Chapter 2 has discussed the basic buck converter topology, the fundamentals of EMI, existing EMI suppression methods and basic power MOSFET gate driver topologies. Chapter 3 discusses the proposed technique of the thesis. This technique utilizes a segmented voltage driven gate driver in order to reduce the EMI emitted by SMPS.

Figure 2.21 Normalized Charge-Interval Current and Voltage waveforms for different resonant Q values (Source: [36])
Chapter 3  Proposed EMI Reduction Technique

3.1  Effect of Rout on Switching Loss

As discussed in section 2.2.1, switching loss is a common source of energy loss within SMPS. Switching loss occurs when power MOSFETs do not instantly transition between their ON and OFF states. Furthermore, the switching loss is proportional to the turn-on and turn-off transition times of the power MOSFET ($T_{on}$ and $T_{off}$ respectively). Section 2.6.1 shows that for voltage driven gate drivers, the transition time is heavily influence by two factors; the gate capacitance of the power MOSFET ($C_g$) and the output resistance of the gate driver ($R_{out}$). Thus, for a given power MOSFET, the $T_{on}$ and $T_{off}$ times are heavily determined by the gate driver circuit. According to (2.11), a low $R_{out}$ will provide short $T_{on}$ and $T_{off}$ times whereas a large $R_{out}$ will produce longer times. Normally, a designer would try to minimize switching loss as much as possible within their monetary, size and weight budget. Thus, a gate driver with a very low $R_{out}$ would be desired so that the $T_{on}$ and $T_{off}$ times are minimized.

Experienced designers have noticed that switching loss can be controlled by dynamically adjusting $C_g$ through a process known as output stage segmentation. Output stage segmentation works by dividing the power MOSFET into a large number of parallel devices that can be enabled or disabled independently [37]. Given output stage segmentation, the effective gate capacitance of the power MOSFET can be controlled dynamically. Thus, shorter $T_{on}$ and $T_{off}$ times can be realized on demand. Output stage segmentation has been used to reduce switching loss in operating situations where switching loss has become more dominant than the conduction losses associated with a smaller output stage. An example of this situation is during light output current loading, where conduction loss becomes minimal as shown by (2.8). This technique is highly suitable for integrated designs where the complex enabling and disabling circuitry can be manufactured in a compact and cheap manner.

Work has also been done by Fomani et al. [23] where $R_{out}$ is adjusted dynamically in order to achieve a similar effect as output stage segmentation. This approach is better suited for discrete designs as the required circuitry can be easily contained within the gate driver IC.
3.2 The Effect of $R_{out}$ on Electromagnetic Interference

As shown in Figure 3.1, the output resistance of the gate driver ($R_{out}$), the parasitic inductance from the PCB trace between the gate driver IC and the power MOSFET ($L$) and the gate capacitance of the power MOSFET ($C_g$), form a series $RLC$ circuit [28]. An analysis of the $RLC$ circuit is shown from (3.1) to (3.4). If the system is under damped, the amount of ringing that the circuit exhibits for a step input is determined by the dampening ratio ($\zeta$). By controlling $R_{out}$, the amount of ringing that occurs can be controlled as $\zeta$ is linearly related to $R_{out}$. Furthermore, the system will likely be under damped as $R_{out}$ is often set very low by the system designer in order to produce practical levels of switching loss. However, in order to reduce the amount of ringing, $R_{out}$ must be kept high. Furthermore, an increase in $R_{out}$ will result in less overshoot and undershoot being exhibited at the gate node.

\[
\frac{V_G}{V_i} = \frac{1}{1 + R_{out}C_g s + LC_g s^2} \quad (3.1)
\]

\[
\omega_0 = \frac{1}{\sqrt{LC_g}} \quad (3.2)
\]
$$\omega_{OSC} = \omega_0 \sqrt{1 - \zeta^2}$$

$$\omega_{OSC} \approx \omega_0$$ \hspace{1cm} (3.3)

$$\omega_{OSC} \approx \frac{1}{\sqrt{LC_g}}$$

$$\zeta = \frac{R_{out}}{2} \sqrt{\frac{C_g}{L}}$$ \hspace{1cm} (3.4)

Reducing ringing at the gate nodes of power MOSFETSs is important as ringing at these nodes may result in oscillations in the current drawn by the converter, subsequently producing EMI. The reason that this phenomenon could occur is that during the transition of the power MOSFET, the device will spend a small amount of time in saturation mode and will behave as a voltage controlled current source. Thus, any oscillations in voltage at the gate of the power MOSFET will be translated into oscillations in current that are injected directly into the input power supply of the SMPS.
3.3 Dynamic $R_{out}$ Operation

The observation in sections 3.1 and 3.2 suggest that there is a tradeoff between EMI generated by an SMPS and the efficiency of the overall converter. Looking at the mechanisms behind this tradeoff indicates that the output resistance of the gate driver, $R_{out}$, plays an important role. A low value for $R_{out}$ provides a low amount of switching loss for the converter and thus improves efficiency. However, a high value for $R_{out}$ will reduce EMI. Essentially, a low value of $R_{out}$ provides short switching times but encourages ringing whereas a high $R_{out}$ provides long switching times but reduces ringing. As traditional voltage driven gate drivers have a static $R_{out}$, a system designer is constrained by this tradeoff. They must pick a gate driver for their system that sufficiently inhibits switching loss but at the same time does not encourage excessive ringing.

The work presented in this thesis seeks to break this EMI-efficiency tradeoff and provide the designer with a new design tool. In order to perform this task, a new voltage driven gate driver is presented. In this structure, the output resistance, $R_{out}$ is not static but instead can be adjusted dynamically. With this approach, the gate drive can be operated in the manner shown in Figure 3.2.

![Figure 3.2 Gate Driver IC Timing Diagram](image-url)
With this operation, the output resistance of the gate driver is held low during output transitions but is held high after the transition has passed. Through this operation, a short transition time is guaranteed but any oscillations of the gate node that follow the transitions will be damped by the higher output resistance of the gate driver. Thus, the tradeoff between EMI and efficiency can be broken at the expense of a more complex gate driver circuit.

At first glance, it could be easily surmised that in order to maximize the benefits of this approach the ideal maximum $R_{out}$ value and the ideal minimum $R_{out}$ resistance value ($R_{outh}$ and $R_{outl}$ respectively) would be infinite and zero respectively. There are however reasons why this arrangement is not possible. Firstly, it would be impossible to produce a practical device with a zero value for $R_{out}$; all known room temperature materials exhibit non-zero electrical resistance. A gate driver with a very large $R_{outh}$ value that is effectively infinite is possible to construct. However, any leakage current at the gate of the MOSFET would steadily discharge the gate, causing significant conduction losses in the MOSFET. Thus, $R_{outh}$ must be selected to be a finite value.

### 3.4 Switching Characteristics

The proposed switching waveform shown in Figure 3.2 uses two variables to define the operation of the gate driver; $T_{\text{post}}$ and $T_{\text{pre}}$. $T_{\text{post}}$ is defined as the time after the transition that $R_{out}$ remains low. $T_{\text{pre}}$ is defined as the time before the transition that $R_{out}$ becomes low. This characterization has been used as a simplified approach and does not incorporate the possibility of using more than two values for $R_{out}$. Additionally, the same $T_{\text{post}}$ and $T_{\text{pre}}$ values are used for both the rising and falling edges of the gate driver pulse. Nevertheless, despite these simplifications, the characterization does provide enough control over the system in order to explore the behavior of the proposed technique.

$T_{\text{post}}$ and $T_{\text{pre}}$ must be selected such that they break the tradeoff between switching loss and EMI while at the same time not interfering with the normal operation of the converter. Furthermore, the values are only specific to a particular converter design. Changing the MOSFETs used in the SMPS or voltage levels of the system will likely require new values for $T_{\text{post}}$ and $T_{\text{pre}}$. 
3.5 Gate Driver Topology

In order to implement the segmented gate driver required by the algorithm outlined above, a gate driver with the topology used in [23] was designed and fabricated using the AMS 0.35um 40V process. With this design, the gate driver consists of seven identical driver segments, connected in parallel as shown in Figure 3.3. Each segment has two inputs ($V_{in}$ and $Enable$) and a single output ($V_{out}$). All of the $V_{in}$ lines are tied together and all of the output lines are tied together. Thus, each segment is supplied the same input waveform and drives the same load. The enable signals are used to control the behavior of the individual segments. When an enable signal is brought low, the output of the segment is forced into a high impedance state. The enable lines are connected together in such a way as to create three distinct groups; a group of four segments, a group of two segments and a single segment on its own. With this arrangement, the number of segments that are enabled may be controlled from zero to seven with a minimal number of digital control inputs.

![Proposed Gate Driver Topology](image.png)

Figure 3.3 Proposed Gate Driver Topology
3.6 Segment Design

Each of the seven gate driver segments are designed as shown in Figure 3.4. The segments are designed such that shoot-through current in the final stage is minimized and they can be digitally enabled or disabled independently.

The enable signals are used to control the behavior of the individual segments. When the enable signal is brought low, the segment is forced into a high impedance state [23]. Thus, a disabled segment provides no conduction path to source or sink current from adjacent segments. A disabled segment therefore increases the $R_{out}$ of the overall gate driver [23]. With this approach, $R_{out}$ can be adjusted to seven distinct values, as described by (3.5) where $r_{out}$ is the output resistance of an individual driver segment and $N$ is the number of segments that has been enabled.

![Figure 3.4 Topology of an individual gate driver segment](image)

$$R_{out} = \frac{r_{out}}{N} \tag{3.5}$$
Chapter 4 Implementation and Experimental Results

4.1 IC Implementation

In order to test the proposed gate drive technique, a segmented gate driver IC was designed and fabricated by A. Fomani, a former MASc student in our group for efficiency study. The design was fabricated using the AMS 0.35µm 40V process. A micrograph of the resulting die is as shown in Figure 4.1. This IC contains two gate driver circuits; one for each of the MOSFETs used in a synchronous buck converter. The overall die size is 2mm × 1.5mm. Digital input signals are located near the top of the die and the power signals and output signals are located near the bottom of the die.

Each gate driver is composed of seven gate driver segments. The enable signals for each gate driver are arranged as discussed in Chapter 3. Both gate drivers have independent enable signals, which allows for their output resistances to be controlled independently.

![Figure 4.1 Micrograph of Gate Driver IC](image-url)
The output resistance, $R_{out}$, of the gate driver was measured in order to verify that the intended operation of the gate driver predicted by (3.5) was correct. These output resistance measurements are shown in Table 4.1.

<table>
<thead>
<tr>
<th></th>
<th>Pull Up (Ω)</th>
<th>Pull Down (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Min. $R_{out}$</strong></td>
<td>1.80</td>
<td>0.65</td>
</tr>
<tr>
<td><strong>Max. $R_{out}$</strong></td>
<td>13.00</td>
<td>4.50</td>
</tr>
</tbody>
</table>

Table 4.1 Measured Gate Driver Output Resistance

### 4.2 Discrete System Implementation

The gate driver IC discussed in section 4.1 was mounted in a 24-CFP ceramic, surface mount package. The packaged gate driver was subsequently incorporated into a discrete synchronous buck converter of the topology shown in Figure 4.2. The system utilizes two International Rectifier IRF8707GTRPBF power MOSFETs (data sheet can be found in Appendix A) for $M_1$ and $M_2$ with 9.3 nC gate charge at 5 V and on-resistance of 9.3 mΩ when $V_{GS} = 10$V. Gate drive voltages of 10 V were used to drive $M_1$ and $M_2$. A Susumu PCMC135T-1R0MF inductor with an inductance of 1 µH was used as the output inductance $L_1$. A surface mount ceramic capacitor with a capacitance of 20 µF was used as the output capacitance $C_1$. The bootstrapping circuit (composed of a diode and capacitor, $D_1$ and $C_2$) was used to provide the voltage required to turn on the high-side power MOSFET $M_1$. A Diodes Inc. SD103BWS-7-F Schottky diode was utilized for $D_1$, it has a rated maximum average current of 350 mA and a forward voltage drop of 600 mV when conducting 200mA of current. A 22 µF ceramic capacitor was used for $C_2$. 
Most commercial SMPS operate with a closed loop control system that continually monitors the output voltage of the circuit and adjusts the operation of the converter in order to guarantee that the output voltage is constant and stable. An example of this type of control is shown below in Figure 4.3. A tightly controlled output voltage was not required for the experiments contained in this thesis and thus the control loop was left open (as shown in Figure 4.4) in order to simply the work. A result of this design decision is that the duty cycle of the converter needs to be adjusted manually for every experiment.
The system described above was implemented on a two-layer FR4 PCB. The design of the top and bottom copper layers are as shown in Figure 4.5. The assembled PCB is as shown in Figure 4.6. Power was supplied to and removed from the converter using Emerson Network Power Connectivity Solutions 108-0740-001 banana plug receptacles. The digital signals driving the gate driver IC were supplied with an Altera Cyclone II FPGA DE2 Development Board. The DE2 board allowed for manual control of the duty cycle, dead time, $T_{post}$ and $T_{pre}$ values. The Altera DE2 board was connected to the converter via a 40pin header connection.
Figure 4.5 Top and Bottom Layers of Synchronous Converter PCB Design
Figure 4.6 Synchronous Buck Converter PCB Implementation
4.3 Gating Signal Generation

In order to generate the gating pulses for the system, a digital pulse width modulator (DPWM) was employed using the Altera Cyclone II FPGA on the DE2 board. The only requirements of the DPWM were that it should be capable of driving the converter with pulse width modulated signals of at least 1MHz and with an accuracy of at least 1ns for dead-times and dynamic output resistance adjustments. The 1 ns resolution requirement was selected as this value would be an order of magnitude lower than the expected rise time and fall times of the MOSFET gate nodes which were expected to be around 10 ns. Two common forms of DPWM are the counter based DPWM and the delay line based DPWM. The hybrid DPWM is another topology that can be used to combine the benefits of both approaches and was selected for this project.

The counter based DPWM approach is discussed in [38]. The approach uses a digital counter and a digital comparator as shown in Figure 4.7. The counter based DPWM has several benefits, including; an area that is logarithmically related to its bit size and a very linear operation. However, the counter based DPWM has two major drawbacks. First, the energy consumed by the counter based DPWM increases with the required precisions of the DPWM. This phenomenon occurs as greater precision requires that the DPWM be driven with a greater clock frequency, increasing dynamic power loss. Secondly, the precision of the counter based DPWM is limited for FPGA implementations as the maximum clock frequency of an FPGA is much lower than that of a fully integrated ASIC design. For the Cyclone II FPGA, the maximum clock frequency is rated at 500MHz [39], limiting the accuracy to 2 ns, lower than the project requirement of 1 ns.

The delay line based DPWM is discussed in [40]. This approach uses a tapped delay line and a multiplexer as shown in Figure 4.8. The delay line based DPWM has several benefits including less power consumption than the counter based DPWM as the circuit exhibits precision that depends on the minimum element delay in the delay line and not the switching frequency. However, delay line based DPWMs have a severe drawback in that their occupied area is linearly related to their bit size, consuming considerable area when a highly accurate DPWM is required. Furthermore, the linearity of the delay line based DPWM can be highly degraded if there is poor matching between delay elements.
An often employed solution to the tradeoffs between the counter based and delay line based DPWMs is the hybrid DPWM [41]. The hybrid DPWM essentially works by combining the counter based and delay line based DPWM approaches. In order to meet the accuracy requirements of this project a hybrid DPWM similar to the one shown in Figure 4.9 was employed. With this topology, the (N-1) most significant bits of the pulse width modulation are determined by the digital counter and the least significant bit is supplied by the delay line. This arrangement allows the DPWM to achieve an accuracy of 1 ns without requiring the counter to
be operated at a frequency greater than the 500 MHz limit of the FPGA. The delay element was implemented using Altera “lcell” modules.

![Diagram of Digital Counter and Duty Cycle](image)

**Figure 4.9 Hybrid DPWM Topology**

However, the hybrid DPWM used for this project operates in a slightly more complex manner than the general topology presented in Figure 4.9. This complexity occurs as the DPWM is required to create the output resistance control signals for the proposed technique. These signals must be generated in addition to the complementary pulse width modulated signals with controllable dead time that are required for basic buck converter operation. In order to characterize this extension of the topology, a sub circuit known as the “Hybrid Comparator” or “HCompare” module is defined as shown in Figure 4.10. The HCompare module produces a PWM signal with a duty cycle controlled by DataIn and synchronized to a 500 MHz external counter but exhibits an accuracy of 1 ns. Eight HCompare modules were incorporated into the hybrid DPWM as shown in Figure 4.11.
The augmented Hybrid DPWM circuit shown in Figure 4.11 was implemented on the DE2 using Verilog HDL code. The $DC$ variable refers to the Duty Cycle command provided to the DPWM, the $DTn$ variable refers to the negative edge dead time command provided to the DPWM, the $DTp$ variable refers to the positive edge dead time command provided to the DPWM and $T_{pre}$ and $T_{post}$ are the output resistance control variables defined in Section 0. The “Digital Logic” block is composed of static logic elements that combine the signals from the HCompare modules and produces the gating signals and the output resistance control signals.
4.4 Measurement of Conducted EMI and Efficiency

In order to perform efficiency and conducted EMI measurements, the converter discussed in sections 4.2 and 4.3 was modified as shown in Figure 4.12. The conditions under which the system was tested are presented in Table 4.2.
Figure 4.12 Circuit Diagram of Experimental Test Setup

Table 4.2 Operating Conditions for Testing

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{in}$</td>
<td>10 V</td>
</tr>
<tr>
<td>$V_{out}$</td>
<td>1.2 V</td>
</tr>
<tr>
<td>$C$</td>
<td>20 µF</td>
</tr>
<tr>
<td>$L$</td>
<td>1 µH</td>
</tr>
<tr>
<td>$I_{out}$</td>
<td>2 A</td>
</tr>
<tr>
<td>$f_{sw}$</td>
<td>1 MHz</td>
</tr>
</tbody>
</table>
4.4.1 Measurement of Conducted EMI

Conducted EMI was measured using a similar technique to [34]. With this technique, a Tektronix TCPA300 current probe measures the common mode current flowing between the 10V supply and the converter. The signal from the current probe is then amplified using a Tektronix TCP312 current probe amplifier and the signal is supplied to an HP8591E spectrum analyzer. With this setup, the spectrum of the current drawn from the primary power supply can be measured between 150 kHz and 30 MHz, the FCC frequency range of interest for conducted EMI. The system can perform conducted EMI measurements at frequencies up to 100 MHz. The 100 MHz limitation arises as this is the TCPA300 current probe’s maximum bandwidth. With this topology, the spectrum analyzer presents spectrum data with dBµA units. In order to convert these units to dBµV, (4.1) must be used [42]. However (4.1) simplifies to (4.2) as the transfer impedance ($Z_t$) is equivalent to 1 for the Tektronix current probe system that was used.

$$dB\mu V = dB\mu A + 20 \times \log(Z_t)$$  \hspace{1cm} (4.1)

$$dB\mu V = dB\mu A$$  \hspace{1cm} (4.2)

4.4.2 Measurement of Efficiency

Efficiency of the system ($\eta$) was determined by measuring the exact output and input voltages ($V_{out}$ and $V_{in}$ respectively) using voltmeters, measuring the input and output currents using ammeters ($I_{out}$ and $I_{in}$ respectively) and applying equation (4.3). The power consumption of the FPGA was ignored as the digital circuits that it contains could be easily migrated to an ASIC implementation where their power consumption would be drastically reduced.

$$\eta = \frac{I_{out} \times V_{out}}{I_{in} \times V_{in}}$$  \hspace{1cm} (4.3)
4.5 Measurement of Radiated EMI

In order to perform radiated EMI measurements, the converter discussed in sections 4.2 and 4.3 was placed in an RF shielded anechoic chamber. Radiated emissions were then detected using a simple dipole antenna and were analyzed using a HP8591E spectrum analyzer with a resolution bandwidth of 1 kHz. Figure 4.14 and Figure 4.15 show the test setup that was used to perform the radiated EMI tests. The resonant frequency of the dipole antenna was set to be 88 MHz. The resonant frequency was selected as 88 MHz is the boundary frequency between the two lowest FCC radiated emissions ranges (30 MHz to 88 MHz and 88 MHz to 216 MHz). Thus, this resonant frequency allowed for measurements within both of these EMI frequency ranges. Furthermore, both of these frequency ranges are close to the measured gate ringing frequency of approximately 70 MHz. Given (4.4), the dipole antenna was constructed with a structure shown in Figure 4.13 and a length \( L \) of 1.625 m [43]. For simplicity, the gain of the antenna and cabling connecting it to the spectrum analyzer was neglected. Thus, to convert the dB\( \mu \)V reading of the spectrum analyzer to the \( \mu \)V/m units required by the FCC radiated emission standards, (4.5) was employed [42]. Furthermore, the height of the antenna \( (H) \) was selected to be 1.4 m in accordance with the guidelines set forth by [44].

\[
L = \frac{143 \times 10^6}{F} \quad (4.4)
\]

\[
[\mu \text{V/m}] = 10^{(([\text{dB}\mu \text{V}])/20)} \quad (4.5)
\]

![Figure 4.13 Radiated EMI Dipole Antenna Structure](image)
Figure 4.14 Radiated EMI Test Setup (Side View)

Figure 4.15 Radiated EMI Test Setup (Top View)
4.6 Determining the Effects of $T_{pre}$ and $T_{post}$

The conducted EMI (as discussed in 4.4.1) and the efficiency of the converter (as discussed in 4.4.2) were measured while the timing parameters $T_{pre}$ and $T_{post}$ were adjusted. This operation was performed in order to observe the effects that these parameters exert over the system. With this testing, the optimal values for $T_{pre}$ and $T_{post}$ were extracted. For the tests in this section, the conducted EMI was measured between 30 MHz and 100 MHz, which is above the FCC conducted EMI range of 150 kHz to 30 MHz. This approach was taken as it was observed that the greatest reduction in conducted EMI occurred at the same frequency as the gate node ringing which was observed to be approximately 70 MHz and the goal of this phase of testing was to find the values of $T_{pre}$ and $T_{post}$ that reduce ringing the most.

4.6.1 The Effects of the $T_{pre}$ Variable

Figure 4.16 shows the improvement in peak conducted EMI as a function of the $T_{pre}$ variable. In this graph, improvement is measured as the difference in peak conducted EMI between the proposed technique and the low output resistance mode.
The low output resistance mode being defined as the mode when all gate drive segments are constantly enabled, lowering the gate drive resistance as much as possible. For this measurement, $T_{post}$ was set at 10 ns and all dead-time values were selected to be 8 ns. From this graph it can be seen that beyond a minimum value of approximately 3 ns, the value of $T_{pre}$ has little bearing on the conducted EMI of the converter.

Figure 4.17 shows the converter efficiency as a function of the $T_{pre}$ variable. As can be seen in this graph, the effect that $T_{pre}$ has on the efficiency of the converter is negligible. When $T_{pre}$ is varied from 0 ns to over 20 ns, the efficiency of the converter varies by less than 0.5% for values of $T_{pre}$ above 3 ns. Thus, $T_{pre}$ has little effect on the overall efficiency of the converter above a magnitude of 3 ns.

![Figure 4.17 Converter Efficiency VS Tpre](image)

From the analysis of Figure 4.16 and Figure 4.17, it can be concluded that the value of $T_{pre}$ only needs to satisfy two requirements. First, the value of $T_{pre}$ must be sufficiently large that that it does not inhibit conducted EMI reduction. Second, the value of $T_{pre}$ must be sufficiently small...
such that it does not interfere with the normal operation of the converter. Given these requirements and the data from Figure 4.16 and Figure 4.17, $T_{pre}$ was selected to have the value of 5 ns. This selection is larger than the minimum $T_{pre}$ determined by analyzing Figure 4.16 but not so large that it inhibits operation of the converter.

4.6.2 The Effects of the $T_{post}$ Variable

Figure 4.18 shows the improvement in peak conducted EMI as a function of the $T_{post}$ variable. In this graph, improvement is measured as the difference in peak conducted EMI between the proposed technique and the low output resistance mode. The low output resistance mode being defined as the mode when all gate drive segments are constantly enabled, lowering the gate drive resistance as much as possible. For these measurements, $T_{pre}$ was set as 5 ns and all dead time values were selected as 8 ns. As shown in Figure 4.18, the improvement in conducted EMI is reduced for very high (over 10 ns) values of $T_{post}$. This result makes sense as large values of $T_{post}$ will mean that the output resistance is held low long after the gate transition has passed and ringing at the gate node is not dampened.

![Figure 4.18 Improvement in Conducted EMI VS Tpost](image-url)
Figure 4.19 shows the efficiency of the converter as a function of $T_{post}$. From this graph it can be seen that the efficiency of the converter decreases slightly for low values of $T_{post}$ but that $T_{post}$ has a diminished influence on efficiency when its value exceeds approximately 10 ns. This observation makes sense as low values of $T_{post}$ should cause the converter to function identical to the case where the output resistance is held constantly high and the switching loss is increased, causing power loss. Furthermore, large values of $T_{post}$ cause the converter to function identical to the case where the output resistance is held constantly low.

![Converter Efficiency VS Tpost]

**Figure 4.19 Converter Efficiency VS Tpost**

Given the data of Figure 4.18 and Figure 4.19, a value of 8 ns was selected for $T_{post}$. This particular value was selected as this value causes a significant reduction in ringing while not reducing the efficiency of the converter. Furthermore, the value of 8 ns matches the rise time and fall time of the gate nodes when the output resistance of the gate drivers is set to the lowest possible value (only one segment enabled), which was measured to be approximately 8 ns. Thus, the $T_{post}$ value has been selected to be just long enough that the entire gate node transition occurs during the low output resistance period.
4.7 Voltage Waveforms

In order to determine the effect that the proposed technique has on ringing within the system, voltage waveforms for the high side gate, low side gate and the switching node of the converter were measured. These measurements were performed using a Tektronix MSO 4034 oscilloscope. These particular voltage waveforms were monitored as it is intended for the proposed technique to directly control the ringing of these nodes in order to produce a reduction in EMI without degrading efficiency. Thus, for the theory of the presented technique to be validated, it must be confirmed that the effects on EMI and efficiency result from changes in the behavior of these voltage waveforms.

4.7.1 Voltage Waveform Measurement Strategy

In order to observe the proposed technique, measurements were organized into three tests, each test having a particular gate drive output resistance. During this testing, \( T_{post} \), \( T_{pre} \) and the maximum/minimum resistance values were identical for both the rising and falling edge of the gate driver. Furthermore, these variables were identical for both high side and low side gate drivers.

During the first test, the output resistance of the gate drivers was set to be constantly high. This operation was achieved by only activating one of the seven segments of both gate drivers. By performing this experiment, a situation where switching loss is significant but conducted EMI is reduced can be examined.

During the second test, the output resistance of the gate drivers was set to be constantly low. This operation was achieved by activating all of the seven segments of both gate drivers. By performing this experiment, a situation where switching loss is reduced but conducted EMI is significant can be examined.

During the third test, the output resistance of the drivers was operated using the proposed technique. The low output resistance setting was achieved by activating all seven segments of the gate drivers. The high output resistance setting was achieved by activating one of the seven segments of the gate drivers. Values for \( T_{post} \) and \( T_{pre} \) were set using the information shown in
Section 4.6. The previous two experiments provided a baseline set of measurements, against which results from this experiment could be compared. In particular, it needed to be determined if the proposed technique achieved the conducted EMI spectrum of the high output resistance mode while maintaining the efficiency of the low output resistance mode.

4.7.2 Voltage Waveform Measurements

In order to measure the effects of the presented technique, the voltage waveforms were measured under the three operating conditions outlined in 4.7.1. The voltage waveform measurements for the high side gate node, low side gate node and the switching node of the converter for high gate drive output resistance and low gate drive output resistance are shown in Figure 4.20 and Figure 4.21 respectively.

When the converter is operated with a high gate driver output resistance it can be seen that the rise times and fall times of the low side and high side gate nodes are approximately 40 ns. Overshoot of 8 V for the high side gate node and 0 V for the low side gate node is observed. Furthermore, undershoot of 8 V for the high side gate node and 4 V for the low side gate node is observed.

When the converter is operated with a low gate driver output resistance it can be seen that the rise times and fall times of the low side and high side gate nodes are approximately 8 ns. Overshoot of 16 V for the high side gate node and 8 V for the low side gate node is observed. Furthermore, undershoot of 16 V for the high side gate node and 6 V for the low side gate node is observed.

During the low output resistance mode, a decrease in rise time of 32 ns is observed relative to the high output resistance mode. However, a significant increase in the overshoot and undershoot of the gate nodes is also observed for the low output resistance mode, increasing the ringing at these nodes. Furthermore, the increase in gate node ringing exhibited by the low output resistance mode is causing an increase in ringing at the switching node as well. This observation confirms the theory outlined in Section 0 that there is a tradeoff between gate node ringing and the transition times of the power switches.
Figure 4.20 Voltage Measurements For High Output Resistance (One Segment Enabled)

Figure 4.21 Voltage Measurements For Low Output Resistance (All Segments Enabled)
Figure 4.22 shows the voltage waveforms of the converter during operation of the proposed technique. $T_{post}$ was selected as 8 ns and $T_{pre}$ was selected as 5 ns. For this graph, the rise times and fall times of the gate nodes were measured to be approximately 8 ns. Overshoot of 4 V for the high side gate node and 6 V for the low side gate node is observed. Furthermore, undershoot 16 V for the high side gate node and 0.5V for the low side gate node is observed.

These observations indicate that the proposed technique is reducing gate node ringing during the rising edge of the high side gate and the falling edge of the low side gate node. However, the technique is not effectively dampening the ringing that occurs at the falling edge of the high side gate node. Thus, despite the inability to eliminate all the ringing at the gate node, the proposed technique is reducing some ringing without introducing longer transition times.
4.8 Conducted EMI Spectrum and Efficiency Measurements

In order to measure the effects of the presented technique, the conducted EMI spectrum of the converter is measured under the three operating conditions outlined in 4.7.1. The conducted EMI spectrums of the converter for high gate drive output resistance and low gate drive output resistance are shown in Figure 4.23 and Figure 4.24 respectively.

When the converter is operated with a high gate driver output resistance it can be seen that the conducted EMI spectrum between 20 MHz and 30 MHz has a peak magnitude of 28 dBµV. When the converter is operated with a low gate driver output resistance it can be seen that the conducted EMI spectrum between 20 MHz and 30 MHz has a peak magnitude of 30 dBµV.

These measurements clearly show that the reduction in ringing that occurs when the gate drive resistance is increased causes a reduction in the conducted EMI emitted by the converter. This observation validates the theory presented in section 3.2 that the ringing at the gate node contributes to the conducted EMI of the converter.

Table 4.3 shows the efficiency of the converter for the three operating conditions. Looking at the efficiency for the high output resistance and low output resistance modes, it can be seen that an increased output resistance does diminish the efficiency of the converter by 2.3%. This observation validates the theory outlined in section 3.1 concerning the effects of increased MOSFET transition times and switching loss.
Figure 4.23 Conducted EMI Spectrum for High Output Resistance (One Segment Enabled)

Figure 4.24 Conducted EMI Spectrum for Low Output Resistance (All Segments Enabled)
Figure 4.25 shows the conducted EMI spectrum of the converter during operation of the proposed technique. $T_{post}$ was selected as 8 ns and $T_{pre}$ was selected as 5 ns. From this graph it can be seen that the conducted EMI spectrum between 20 MHz and 30 MHz has a peak magnitude of 23 dBµV. Thus, there is an improvement of 7 dBµV between 20 MHz and 30 MHz relative to the low output resistance mode. Furthermore, there is an improvement of 5 dBµV relative to the high output resistance mode. This result indicates that the proposed technique inhibits gate node ringing even more effectively than an increased gate driver output resistance. The efficiency of the converter when operating using the proposed technique was 76.5 %. Thus, the proposed technique provided an improvement in conducted EMI without a significant reduction in converter efficiency.

![Conducted EMI Spectrum for Proposed Technique](image)

**Table 4.3 Converter Efficiency for Different Modes of Operation**

<table>
<thead>
<tr>
<th>Operation Mode</th>
<th>Converter Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>High Output Resistance</td>
<td>74.3 %</td>
</tr>
<tr>
<td>Low Output Resistance</td>
<td>76.6 %</td>
</tr>
<tr>
<td>Adjustable Driving Strength</td>
<td>76.5 %</td>
</tr>
</tbody>
</table>
4.9 Radiated EMI Measurements

In order to fully measure the effects of the presented technique, the radiated EMI spectrum of the converter is measured under the three operating conditions outlined in 4.7.1. Specifically, the spectrum from 88 MHz to 216 MHz was measured as this is the only FCC defined radiated EMI frequency range that the proposed technique was found to have influenced. The radiated EMI spectrums of the converter for low gate drive output resistance and high gate drive output resistance are shown in Figure 4.27 and Figure 4.28 respectively.

Additionally, the radiated EMI spectrum of the anechoic chamber was measured while the converter was not in operation, the results of which are shown in Figure 4.26. A small amount of RF interference is leaking in the chamber between the frequencies of 88 MHz and 110 MHz. This observation makes sense as broadcast FM radio uses the frequencies of 87.5 MHz to 108 MHz and the anechoic chamber in use was situated only 2 km from the CN Tower, which supports several very strong FM transmitters.

When the converter is operated with a low gate drive output resistance it can be seen that the radiated EMI spectrum between 88 MHz and 216 MHz has a peak magnitude of 700 µV/m. When the converter is operated with a high gate driver output resistance it can be seen that the conducted EMI spectrum between 88 MHz and 216 MHz has a peak magnitude of 285 µV/m.

It is also observed that while the peak radiated EMI occurs near 90 MHz a secondary occurrence of radiated EMI was observed near 135 MHz. When the converter is operated with low gate driver output resistance it can be seen that the radiated EMI spectrum near 135 MHz has a peak magnitude of 94 µV/m. When the converter is operated with a high gate driver output resistance it can be seen that the conducted EMI spectrum near 135 MHz has a peak magnitude of 45 µV/m.

These measurements clearly show that the reduction in ringing that occurs when the gate drive resistance is increased causes a reduction in the radiated EMI emitted by the converter. This observation validates the theory presented in section 3.2 that the ringing at the gate node contributes to the radiated EMI of the converter.
Figure 4.26 Ambient Radiated EMI Spectrum

Figure 4.27 Radiated EMI Spectrum for Low Output Resistance (All Segments Enabled)
Figure 4.28 Radiated EMI Spectrum for High Output Resistance (One Segment Enabled)

Figure 4.29 Radiated EMI Spectrum for Proposed Technique
Figure 4.29 shows the radiated EMI spectrum of the converter during operation of the proposed technique. $T_{\text{post}}$ was selected as 8 ns and $T_{\text{pre}}$ was selected as 5 ns. From this graph it can be seen that the radiated EMI spectrum between 88 MHz and 216 MHz has a peak magnitude of 550 µV/m. Thus, there is an improvement of 150 µV/m between 88 MHz and 216 MHz relative to the low output resistance mode. Furthermore, a radiated EMI measurement of 40 µV/m was observed near 135 MHz. This measurement indicates an improvement in radiated EMI of 54 µV/m near 135 MHz relative to low output resistance operation. Thus, the proposed technique provided an improvement in radiated EMI in addition to conducted EMI without a significant reduction in converter efficiency.
Chapter 5  Conclusions and Future Work

A segmented gate driver technique is presented in this work with goal of reducing electromagnetic interference. The overall design of the gate driver and the experimental results of the work are presented in this section.

5.1 Thesis Summary

Switch mode power supplies built using discrete components are an essential subsystem of modern commercial electronics. As discrete SMPS are being operated at higher frequencies, the need to reduce EMI is becoming critical. Reducing EMI is important to system designers as excess EMI can cause devices connected to the SMPS or even simply located nearby to malfunction. Periodic current draw and ringing at nodes within the SMPS contribute heavily to EMI.

In this thesis, a segmented gate driving technique is developed and shown to reduce conducted and radiated EMI in a discrete synchronous buck converter without a significant reduction in efficiency. This operation is achieved by leveraging the fact that segmentation of the gate driver means that the output resistance of the gate driver can be dynamically adjusted on the fly. With this ability, the output resistance of the gate driver can be set low during a transition to reduce switching loss and then set high after the transition has passed in order to dampen any ringing that may occur at the gate node. Thus, the tradeoff between switching loss and EMI resulting from gate node ringing can be eliminated.

The technique was verified by incorporating a segmented gate driver IC into a discrete buck converter system. An improvement in CEMI of 7dBμV between 20 MHz and 30 MHz and an improvement in REMI of 150 uV/m between 88 MHz and 216 MHz was realized at an output load of 2 A.
5.2 Future Work

The suppression of EMI in an affordable and elegant manner is a highly desired commercial goal. As such, work on this topic will continue into the foreseeable future. Future work on this project can be summarized into four distinct approaches.

1. The impact on EMI of using more than two settings for $R_{out}$ should be examined. The current approach has only investigated the effects of switching the gate driver between a single low and single high $R_{out}$ value, thus utilizing only two settings for the output resistance. Future work should investigate whether or not using intermediate values for $R_{out}$ has any positive impact on EMI or efficiency. This operation will likely require a redefinition of the gate driver switching waveform beyond the simple variables of $T_{pre}$ and $T_{post}$.

2. The impact of using a larger number of segments should be investigated. The current IC used for testing has only seven segments. Thus, the ratio between the largest and the smallest $R_{out}$ values is limited to a factor of seven. Future work should involve fabricating a new gate driver IC with a larger number of gate driver segments, perhaps 100 or even 1000 segments. This level of segmentation will likely not increase the die size of the gate driver by much but will allow a greater ratio between the smallest and largest output resistances that the gate driver can be set to.

3. The suitability of the presented technique for insulated gate bipolar transistors (IGBTs) should be examined. IGBTs are becoming increasingly common in high voltage systems (500 V and above). Future work should investigate whether or not the technique presented has the ability to reduce EMI when used with IGBT devices instead of power MOSFETs. This work will require a new segmented gate driver IC capable of driving the larger gate capacitances inherent to modern commercial IGBT devices.
References


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Appendix A  MOSFET Data Sheet

International Rectifier

IRF8707GPbF
HEXFET® Power MOSFET

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$</td>
<td>30</td>
<td>V</td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>±20</td>
<td></td>
</tr>
<tr>
<td>$I_{D} @ T_{J} = 25^\circ C$</td>
<td>11</td>
<td>A</td>
</tr>
<tr>
<td>$I_{D} @ T_{J} = 70^\circ C$</td>
<td>9.1</td>
<td></td>
</tr>
<tr>
<td>$I_{PD}$</td>
<td>183</td>
<td></td>
</tr>
<tr>
<td>$P_{D} @ T_{J} = 25^\circ C$</td>
<td>2.5</td>
<td>W</td>
</tr>
<tr>
<td>$P_{D} @ T_{J} = 70^\circ C$</td>
<td>1.6</td>
<td></td>
</tr>
<tr>
<td>$T_{J}$</td>
<td>-55 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>

Thermal Resistance

<table>
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<tr>
<th>Parameter</th>
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<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{ja}$</td>
<td>—</td>
<td>20</td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{ja}$</td>
<td>—</td>
<td>50</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

Notes 1 through 5 are on page 9
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**Static @ T_j = 25°C (unless otherwise specified)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}^{max}$ Breakdown Voltage</td>
<td>20</td>
<td></td>
<td></td>
<td>V</td>
<td>$V_{DS} = 9V, I_{DS} = 0.15mA$</td>
</tr>
<tr>
<td>$\Delta V_{DS}^{max}/\Delta T_j$</td>
<td>0.022</td>
<td></td>
<td></td>
<td>V/°C</td>
<td>Reference to 25°C, $I_{DS} = 1mA$</td>
</tr>
<tr>
<td>$R_{DS(on)}$ Static Drain-to-Source Resistance</td>
<td>9.3</td>
<td>11.9</td>
<td></td>
<td>mΩ</td>
<td></td>
</tr>
<tr>
<td>$V_{GS(th)}$ Gate Threshold Voltage</td>
<td>1.35</td>
<td>1.60</td>
<td>2.35</td>
<td>V</td>
<td>$V_{GS(th), I_{D} = 25µA}$</td>
</tr>
<tr>
<td>$\Delta V_{GS(th)}$ Gate Threshold Voltage</td>
<td>-5.6</td>
<td></td>
<td></td>
<td>mV/°C</td>
<td>$V_{GS(th), I_{D} = 25µA}$</td>
</tr>
<tr>
<td>$i_{ds}$ Drain-to-Source Leakage Current</td>
<td>1.0</td>
<td></td>
<td>150</td>
<td>µA</td>
<td>$V_{DS} = 24V, V_{GS} = 0V$</td>
</tr>
<tr>
<td>$I_{oss}$ Gate-to-Source Forward Leakage</td>
<td>100</td>
<td></td>
<td></td>
<td>nA</td>
<td>$V_{DS} = 20V$</td>
</tr>
<tr>
<td>$I_{oss}$ Gate-to-Source Reverse Leakage</td>
<td>-100</td>
<td></td>
<td></td>
<td>nA</td>
<td>$V_{DS} = -20V$</td>
</tr>
<tr>
<td>$g_{fs}$ Forward Transconductance</td>
<td>25</td>
<td></td>
<td></td>
<td>S</td>
<td>$V_{DS} = 15V, I_{D} = 0.8A$</td>
</tr>
<tr>
<td>$Q_{th}$ Total Gate Charge</td>
<td>6.2</td>
<td>9.3</td>
<td></td>
<td>nC</td>
<td>$V_{GS} = 16V, V_{DS} = 0V$</td>
</tr>
<tr>
<td>$Q_{ph}$ Pre-βth Gate-to-Source Charge</td>
<td>1.4</td>
<td></td>
<td></td>
<td>nC</td>
<td>$V_{GS} = 15V$</td>
</tr>
<tr>
<td>$Q_{poh}$ Post-βth Gate-to-Source Charge</td>
<td>0.7</td>
<td></td>
<td></td>
<td>nC</td>
<td>$V_{GS} = 4.5V$</td>
</tr>
<tr>
<td>$Q_{gd}$ Gate-to-Drain Charge</td>
<td>2.2</td>
<td></td>
<td></td>
<td>nC</td>
<td>$I_{D} = 0.8A$</td>
</tr>
<tr>
<td>$Q_{oss}$ Gate Charge Overdrive</td>
<td>1.9</td>
<td></td>
<td></td>
<td>nC</td>
<td>See Figs. 15 &amp; 16</td>
</tr>
<tr>
<td>$Q_{ss}$ Switch Charge ($Q_{oss} + Q_{gd}$)</td>
<td>2.9</td>
<td></td>
<td></td>
<td>nC</td>
<td></td>
</tr>
<tr>
<td>$C_{iss}$ Output Charge</td>
<td>3.7</td>
<td></td>
<td></td>
<td>nC</td>
<td>$V_{GS} = 16V, V_{DS} = 0V$</td>
</tr>
<tr>
<td>$r_{f}$ Gate Resistance</td>
<td>2.2</td>
<td>3.7</td>
<td></td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>$t_{on}$ Turn-On Delay Time</td>
<td>6.7</td>
<td></td>
<td></td>
<td>ns</td>
<td>$V_{GS} = 15V, V_{DS} = 4.5V$</td>
</tr>
<tr>
<td>$t_{off}$ Turn-Off Delay Time</td>
<td>7.9</td>
<td></td>
<td></td>
<td>ns</td>
<td>$I_{D} = 0.8A$</td>
</tr>
<tr>
<td>$t_{r}$ Fall Time</td>
<td>4.4</td>
<td></td>
<td></td>
<td>ns</td>
<td>See Fig. 16</td>
</tr>
<tr>
<td>$C_{iss}$ Input Capacitance</td>
<td>760</td>
<td></td>
<td></td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>$C_{iss}$ Output Capacitance</td>
<td>170</td>
<td></td>
<td></td>
<td>pF</td>
<td>$V_{DS} = 15V$</td>
</tr>
<tr>
<td>$C_{oss}$ Reverse Transfer Capacitance</td>
<td>82</td>
<td></td>
<td></td>
<td>pF</td>
<td>$f = 1.0MHz$</td>
</tr>
</tbody>
</table>

### Avalanche Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E_{ak}$ Single Pulse Avalanche Energy</td>
<td>65</td>
<td></td>
<td>µJ</td>
</tr>
<tr>
<td>$I_{ak}$ Avalanche Current</td>
<td>8.5</td>
<td></td>
<td>A</td>
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### Diode Characteristics

<table>
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<tr>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Units</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{D}$ Continuous Source Current (Body Diode)</td>
<td></td>
<td></td>
<td>3.1</td>
<td>A</td>
<td>MOSFET symbol showing the integral reverse p-n diode</td>
</tr>
<tr>
<td>$I_{su}$ Pulsed Source Current (Body Diode)</td>
<td></td>
<td></td>
<td>8.8</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>$V_{DO}$ Diode Forward Voltage</td>
<td></td>
<td>1.0</td>
<td></td>
<td>V</td>
<td>$T_j = 25°C, I_{D} = 0.8A, V_{DS} = 0V$</td>
</tr>
<tr>
<td>$I_{d}$ Reverse Recovery Time</td>
<td>12</td>
<td>18</td>
<td></td>
<td>ns</td>
<td>$T_j = 25°C, I_{D} = 0.8A, V_{DS} = 15V$</td>
</tr>
<tr>
<td>$Q_{d}$ Reverse Recovery Charge</td>
<td>13</td>
<td>20</td>
<td></td>
<td>nC</td>
<td>$dV/dt = 300µV/A$</td>
</tr>
<tr>
<td>$I_{F}$ Forward Turn-On Time</td>
<td></td>
<td></td>
<td></td>
<td>A</td>
<td>Intermittent turn-on time is negligible turn-on is dominated by LSI delay</td>
</tr>
</tbody>
</table>

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**Fig 1.** Typical Output Characteristics

**Fig 2.** Typical Output Characteristics

**Fig 3.** Typical Transfer Characteristics

**Fig 4.** Normalized On-Resistance vs. Temperature

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Fig 9. Maximum Drain Current vs. Ambient Temperature

Fig 10. Threshold Voltage vs. Temperature

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient
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Fig 12. On-Resistance vs. Gate Voltage

Fig 13. Maximum Avalanche Energy vs. Drain Current

Fig 14. Unclamped Inductive Test Circuit and Waveform

Fig 15. Gate Charge Test Circuit

Fig 16. Gate Charge Waveform
**Fig 17.** Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

**Fig 18a.** Switching Time Test Circuit

*V_{DS} = 5V for Logic Level Devices*

**Fig 18b.** Switching Time Waveforms

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SO-8 Package Outline
(Mosfet & Fetky)
Dimensions are shown in millimeters (inches)

SO-8 Part Marking Information

Example this is an IRF8707GPbF

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/
IRF8707GPbF

SO-8 Tape and Reel

Dimensions are shown in millimeters (inches)

NOTES:
1. CONTROLLING DIMENSIONS: MILLIMETERS
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)
3. OUTLINE CONFORMS TO EIA-445 & EIA-441

Notes:
1. Repetitive rating; pulse width limited by max. junction temperature.
2. Stirling TΩ = 25°C, L = 1.3mH, RΩ = 25Ω, IR = ± 8.8A.
3. Pulse width ≤ 400μs; duty cycle ≤ 2%.
4. When mounted on 1 inch square copper board.
5. RΩ is measured at TΩ of approximately 90°C.

Note: For the most current drawing please refer to IR's website at http://www.irf.com/package

Data and specifications subject to change without notice.

This product has been designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

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