INTERACTIVE FLEXIBLE SWITCH MODE POWER SUPPLIES FOR REDUCING VOLUME AND IMPROVING EFFICIENCY

by

S M Ahsanuzzaman

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Graduate Department of Electrical and Computer Engineering

University of Toronto

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ABSTRACT

Interactive Flexible Switch Mode Power Supplies for Reducing Volume and Improving Efficiency

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Graduate Department of Electrical and Computer Engineering

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The purpose of this thesis is to introduce a family of interactive Switch Mode Power Supplies (SMPS) for reducing the overall volume of the conventional converter topologies in low-to-medium power (up to 60W) applications. As shown in this thesis, the interaction between power supplies and electronic devices can be incorporated with emerging digital controllers for SMPS, to implement flexible converter topologies. These flexible topologies dynamically change the converter configuration, based on the load requirement, to provide near ideal transient response and/or improved efficiency over a wide range of operating conditions. This interaction relaxes the energy storage requirement for the converter reactive components and results in a low volume implementation. The interaction with the SMPS can be between the electronic load and the power supply or different conversion stages of a multi-stage converter. The effectiveness of the introduced family of SMPS is verified on digitally controlled dc-dc and ac-dc converter topologies.
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Chapter 1

Introduction

The subjects of this thesis are interactive flexible converter topologies for digitally controlled switch mode power supplies (SMPS) providing up to 60 W. As demonstrated here, the interaction between the power supply and electronic load or between different stages of multi-stage topologies can be utilized to implement flexible converters, which dynamically change their configuration depending on the conditions in the circuit. This interaction can be incorporated in emerging digitally controlled power supplies [1]-[5]. These flexible power supplies have far superior dynamic performance and increased power conversion efficiency compared to conventional topologies. In many emerging applications the physical limitations of the converter become the bottle-neck in improving dynamic response and, consequently, in minimizing bulky and expensive reactive components. This thesis primarily focuses on different approaches that result in effective reduction of converter reactive components. Moreover, the thesis shows how this interaction can further be utilized to achieve attractive features, such as dynamic efficiency optimization.

1.1 SMPS in AC-DC and DC-DC Power Conversions

In numerous modern electronic devices, consuming power from a fraction of watt to several hundreds of watts, switch mode power supplies (SMPS) are primarily used for energy conversion from one voltage level to another. Compared to linear power supplies, SMPS are more attractive due to their reduced cost, smaller dimensions and higher energy conversion efficiencies. SMPS are used in various electronic devices, ranging from portable electronics such as mobile phones,
digital cameras, and laptop computers to home appliances, lighting equipment, automotive devices, and so on. This thesis focuses on modern portable applications where SMPS are widely used as both ac-dc and dc-dc converters. In portable applications ac-dc converters are usually used as front stage energy converters, such as battery chargers; whereas dc-dc converters are used to provide power to different components requiring different supply voltage levels from the same battery source.

The primary focus of this thesis is to introduce interactive flexible converter designs for dc-dc converters ranging from low-to-mid power levels. The targeted applications include power supplies for computer processors, memories, and digital signal processors (DSPs), as point of load converters. The interactive approach is then extended to a typical ac-dc portable application, where the converter charges the battery while providing power factor correction for universal ac input, i.e. utility line voltage from 90 V\text{rms} to 260 V\text{rms}.

A switch-mode power supply (SMPS) typically consists of a power stage (converter), also known as the output stage, and the controller. The power stage includes switching elements, such as power mosfets and diodes, and reactive components, such as inductors and capacitors. Traditionally, the controller was usually implemented in an analog manner, but in recent years, digital and/or mixed-signal implementations emerged as a viable alternative. Out of all different control approaches, the most common method is known as voltage-mode control that employs pulse-width modulation (PWM) [6]. In the voltage-mode control the output voltage of the converter is compared with a set reference voltage to generate the error signal [Fig.1.1]. This error signal is then used to determine the duty ratio of the gate driving pulses. In the current programmed mode (CPM) control approach, which is also widely accepted, the inductor current
information is incorporated in the controller to achieve simultaneous control of the converter current.

![Diagram of a buck converter with typical analog controller](image)

**Fig.1.1: A buck converter with typical analog controller**

### 1.2 Digital Control of Switch Mode Power Supplies

Even though digital controllers for ac-dc and dc-dc converters are used in numerous applications today, analog controllers predominate in low power applications. This is due to the fact that analog controllers are simple to design, require low silicon area and have low power consumption. As shown in [6], a typical voltage-mode analog controller consisting of a subtractor, proportional-integral-derivative (PID) regulator, and an analog pulse-width modulator (PWM) can be implemented using 20 to 30 transistors and a few passive components. They are capable of providing tight output voltage regulation and in many applications, satisfactory dynamic response. However, analog controllers have some major design limitations. These
include poor portability when transferring from one CMOS process to another. They often cannot be integrated on the same die as the digital processors or FPGA due to process variations. On the other hand, digital controllers consist of digital circuits described in a hardware-description language (HDL) such as Verilog or VHDL and can be re-synthesized for different process technologies. Fig.1.2 shows the system level diagram of a typical digital controller based converter architecture.

Fig.1.2: A buck converter with a typical digital controller

Apart from the already mentioned advantages, digital control is the enabling technology to implement more sophisticated user defined custom control actions, which in many cases cannot be achieved easily in analog controllers. These include advanced control algorithms shown in [7]–[12]. The primary motivation behind such advanced control actions is to improve the converter dynamic performance. The following subsection explains how the dynamic performance is related to the size of the converter output stage.
1.3 Dynamic Response and Size of Output Filter

The dynamic response of the converter, often called the transient response, is one of the major design constraints in modern power supplies. This is due to the fact that modern electronic devices can tolerate only a small voltage deviation at their supply voltage during sudden change of the load current. Once the load current is changed, the converter current, typically the average current through the inductor, needs to change to meet the new load requirement. It takes a certain time, depending on converter topology and the operating conditions. During this transition, the converter energy storage components, such as output filter capacitor, need to provide the difference in the load currents. Hence, the energy requirement during the largest load transient for a given application determines the size of the output filter capacitor. Slower dynamic response requires more energy to be transferred from the filter capacitor and results in much bulkier components increasing the overall size and cost of the power supply.

1.4 Thesis Objective

This thesis presents several design implementations to demonstrate the advantages of interactive flexible SMPS for reducing volume of conventional converter topologies. All of these designs have the common element of modifying converter topology and incorporating a certain level of communication between the converter and electronic load to minimize the overall volume. To achieve this primary goal, two different approaches are investigated.

The first approach illustrates how flexible converter topologies can improve the converter dynamic response beyond the physical limitation of the conventional converter topologies. For this approach, two solutions for different groups of SMPS are demonstrated. The first solution is
for point of load converters (PoL), where the converter directly supplies a load. Here, the load-
interactive converter topology utilizes the information of an upcoming change in the load current
to reduce the amount of energy taken from the output capacitor during transients. The second
solution targets multi-stage topologies, where a series connection of converters between the
unregulated source and the load exist. Here in addition to improving response, dynamic
efficiency optimization is achieved.

The second approach is based on inductor core biasing. In steady stage, the biasing reduces the
inductor core flux density, creating the possibility of reducing size of the bulky inductor. During
transients, the biasing results in saturation of the core, minimizing the effective inductance value
to improve transient response.

1.5 Thesis Overview

This thesis is organized as follows: Chapter 2 gives an overview of previous art and research
motivation for the research presented in this work. Recent relevant research publications and
their shortcomings are also discussed in this section. Chapter 3 proposes a load-interactive
flexible converter topology to reduce the size of the bulky converter output filter. Chapter 4
presents the inductor core biasing technique to further reduce the overall converter volume.
Chapter 5 discusses how interaction between different converter stages can significantly reduce
the intermediate energy storage components. Chapter 6 illustrates how the enhanced interaction
with the converter can result in additional attractive features such as efficiency optimization, and
variable frequency operation.
Chapter 2

Previous Art and Research Motivation

Numerous recent publications [13-20] show various methods for achieving fast dynamic response and consequent reduction of the energy storage capacitor at the output of the converter. Advanced control actions during transients, implemented in both analog and digital manners, are proposed to achieve virtually the fastest dynamic response in various conventional converter topologies. Among them the time optimal [17]-[18] and minimum deviation [20] controllers are arguably the most practical solutions.

2.1 Time Optimal Control

Time optimal control algorithms [17]-[18] recover to steady state from load transients in the fastest possible time. The main motivation is to reduce the converter energy storage requirement during transients, creating a possibility to reduce the bulky output capacitor. Although different implementations of the time optimal control are proposed, they share the same principle of recovering from the transients in a single on/off switching cycle in a buck [Fig.2.1] or buck based converter topology. As shown in Fig.2.1, in a typical time-optimal controller implementation a PID or PI controller is used during steady-state to regulate the output voltage. Once the transient occurs the Fast Transient Control block, implementing a time optimal control algorithm, takes the control role to recover from the transient.
Fig. 2.2 shows the waveforms for inductor current and output capacitor voltage of a buck converter during a light-to-heavy load transient. Once the time optimal block takes control, it detects the valley point, where the converter current matches with the new load current. Based on the valley point of the output voltage, the controller calculates the lost capacitor charge. From the charge value appropriate on and off times of the switch are calculated so that inductor current is brought to the new steady stage. After this, the PID operation is resumed.
Despite its superior transient response compared to conventional solutions, the time optimal controller raises some practical implementation issues. First, the implementation inherently requires the buck inductor to be rated for a much larger current, due to the current overshoot. This increases requirements for the inductor core or number of windings, increasing the total inductor volume. Second, any inaccuracy and delays in detecting the valley point might cause wrong calculations of on/off times. This results in a sub-optimal response, possibility of creating a second transient or, in the worst case, instability. Third, although different implementations have been proposed for time optimal control, they are mostly limited to buck or buck derived topologies and all of them require rigorous calculations to find optimal on/off time.
2.2 Minimum Deviation Controller

Minimum deviation control [20] is a practical solution to reduce the output capacitor volume. Minimum deviation control was introduced to address the major design issues of the time optimal control, i.e. inductor current overshoot and demanding calculations. The idea here is similar to time optimal control in the sense that minimum deviation control tries to reduce the energy taken from the output capacitor during transients as well. However, it does not try to recover from the transients in the shortest possible time or a single on/off switching sequence. It rather tries to use multiple switching cycles to recover the transient to prevent causing inductor current overshoot. However, it effectively limits the maximum voltage deviation up to the same level as the time optimal control, resulting in reduction of output capacitance. Fig. 2.3 shows the waveforms for a minimum deviation control.

![Waveforms to illustrate minimum deviation controller response](image)

**Fig.2.3:** Waveforms to illustrate minimum deviation controller response
The principle of operation is similar to that of the time optimal control. During the steady state operation the PID or PI controller regulates the output voltage. Once the transient is detected the minimum deviation algorithm takes the control role until the valley point is reached. After reaching the valley point, the PID resumes its operation to bring the output voltage back to the desired level. The advantage here is that the inductor current overshoot is completely eliminated, even though the settling time of the output voltage is increased compared to time optimal control. Since the maximum output voltage deviation is same in both time optimal and minimum deviation control, they result in same volume reduction of the output capacitor.

### 2.3 Challenges for Further Improvement

The time optimal and minimum deviation control algorithms have pushed the transient response to a certain point where only the converter topology and operating condition are the limiting factor in reducing the volume of the reactive components. This can be seen from Figs. 2.2 and 2.3, where the inductor current of the converter is at a maximum slew-rate. For a buck converter the slew rate is limited by the inductance value and the input and output voltages. As a result, the fastest dynamic response that can be achieved with the advanced control algorithms, are only constrained by the physical limitations of the conventional converter topologies. The physical limitation has become the bottle-neck for further improving dynamic performance and consequent, volume reduction. The motivation of this thesis is to overcome the challenge of the physical limitation of the conventional converter topologies, by introducing interactive flexible converters.
2.4 Digital Controllers Implementing Flexible Topologies

Since digital control is relatively recent trend in implementing low-to-medium power SMPS, the primary focus of most research works was to achieve comparable performance as the analog counterparts. In this thesis it has been shown that, apart from implementing advanced control actions, digital controllers can also be used to overcome limitations of the existing converter topologies by dynamically changing their structures. This concept is named flexible topology because, unlike conventional converter systems, the physical configuration of the converter can be optimized based on specific load requirement or converter operating conditions. As shown in this thesis this approach can result in significant volume reduction compared to the state of the art conventional converter based solutions.

2.5 Dynamic Efficiency Optimization

Dynamic efficiency optimization is an attractive feature for portable applications to maximize the battery life. In these applications need for a low volume converter implementation often motivates designing of high frequency switching converters. However, this results in higher switching losses and limits the maximum operating frequency to maintain satisfactory conversion efficiency. Although both conduction and switching losses are major contributors of reducing overall conversion efficiency, switching loss becomes dominant at lighter load conditions. Since many modern portable devices are operated in idle mode most of their life time, achieving high efficiency at light load condition is crucial. Chapter 6 of this thesis presents a practical solution for variable frequency operation to improve the efficiency. Incorporated in multistage interactive converters, this can significantly improve the efficiency of the downstream converter.
Chapter 3

Load Interactive Converter with Minimized Output Filter Capacitance

The chapter introduces a concept of load-interactive digitally controlled point-of-load (POL) dc-dc converters where the size of the output filter capacitor can be minimized based on enhanced load-related communication between the digital load and the converter controller. Based on the information about upcoming load changes, the inductor current of the dc-dc converter is adjusted such that the converter output current matches the new load, thus minimizing the energy storage requirements for the output filter capacitor. The effectiveness of this approach is verified on a digitally controlled 3.3 V/30 W experimental prototype, where the dc-dc converter is a steered-inductor non-inverting buck-boost. Transient response results show that, compared to standard converters with near-time optimal control, the new system has about three times smaller voltage deviation, allowing for a significant reduction in the output capacitor size.

3.1 Design Overview

In recent years, advanced “power aware” digital chipsets have been introduced in devices such as cell phones, computers, and other electronic equipment having a large portion of digital hardware. These digital loads communicate with power supplies and, to a certain extent, regulate their operation to reduce the overall power consumption [21]-[24]. Examples include dynamic/adaptive voltage scaling (DVS/AVS) and adaptive body biasing (ABB) techniques, where the supply voltage of the digital signal processors is dynamically changed, depending on
the processing load, to minimize dynamic and static power consumption [21]-[26]. Also, the latest Intel chipset, provide the switched-mode power supply (SMPS) with an indication of the current demand it expects over a period of time [27], so that this information can be used for phase shading to improve efficiency of multi-phase SMPS, as shown in [11]. Methods that dynamically perform efficiency optimization of a segmented power stage based on the prediction of the load current from a digital signal stream processed by the electronic load have also been shown [28]. So far, communication between the digital load and the SMPS has mostly been motivated by power savings. Furthermore, inductor current feed-forward approach, utilizing the information of the load current, is demonstrated to improve the transient response of dc-ac converters [84] and dc-dc converters [85].

![DC-DC Converter Diagram](image)

Fig.3.1: Digital Controller with modified buck-boost converter
The objective of this chapter is to show how this communication can further be utilized to minimize the overall size of the SMPS, by dramatically reducing bulky and costly energy storage output filter capacitors. The system of Fig.3.1 consists of a modified non-inverting buck-boost converter, i.e. steered-inductor buck-boost, a digital controller, and a communication block providing load current information.

The modified buck-boost converter has an additional switch $SW_5$, for current steering [29], which, as it will be shown here, provides dramatic improvements of transient response in both buck and boost modes. It should be noted that the non-inverting buck boost is a common stage in numerous battery powered applications (e.g. [31]), so compared to those systems, no additional switches or conduction losses are introduced.

To provide the load current information, i.e. pre-load command, a block similar to those implemented in the latest generation of Intel processors [27] is used. Based on the pre-load command, during heavy-to-light load transients, the power stage is reconfigured, to steer the inductor current away from the output capacitor into the source. Similarly, the load information is used during the light-to-heavy transient to ramp up the inductor current to the upcoming load value before the transient occurs.

### 3.2 Principle of Operation

In a point-of-load (POL) dc-dc converter, the bulky output filter capacitor is sized based on the energy storage required to supply current during large step-load transients. This capacitor value is usually significantly larger than the value required to meet the output voltage ripple
specification. The latency in the inductor current change, i.e. its limited slew rate, compared to that of the load is the major factor in determining the value of the output filter capacitance.

The converter of Fig. 3.1 is a modification of the steered-inductor topology proposed in [29]. This topology also resembles the conventional non-inverting buck boost [6], except for an addition of SW5. This switch allows flexible and bidirectional control over the slope of the inductor current, which, in conjunction with the load information communicated by the load, as described in the following subsections, is a key element in providing dramatic improvements in the dynamic response. In the buck mode, SW4 is on, SW3 is off at all times while SW1 and SW2 change their states at the switching rate. When operating as a boost, SW1 is on, SW2 is off at all times and switches SW3 and SW4 are active.

It should be noted that constant operation in buck-boost mode is also possible. During steady state buck-boost operation, SW1 and SW3 would conduct instantaneously followed by the conduction of SW2 and SW4. However, it is avoided in steady state operation to minimize the number of active switching components operating at switching frequency and, consequently, to reduce the switching losses. Furthermore, in the buck mode, the rms current and consequently, the conduction losses, are also reduced.

3.2.1 Light-to-Heavy Load Transient Improvement

When operating as a conventional buck, the rate of change of the inductor current during a light-to-heavy load transient is limited by:

\[
\frac{di_L}{dt} = \frac{V_g - V_{out}}{L}
\]  

(3.1)
where $V_g$ is the input voltage, $V_{out}$ is the output voltage and $L$ is the converter inductance. As a result, during a sudden light-to-heavy load change, the output capacitor initially discharges providing the difference between the load and output currents, until the inductor current reaches the load value.

In the boost mode, when the input voltage is relatively low (compared to that of the output), the slope of the inductor current during a light-to-heavy load transient is limited by

$$\frac{di_L}{dt} = \frac{V_g}{L}$$

which causes a latency in the following of the load current. Moreover, to respond to a load transient, a fast acting controller initially disconnects the inductor from the load, leaving the output capacitor to provide all the current. In a properly designed SMPS, this capacitor is usually selected to be large enough, so that the charge lost during transients does not significantly affect the output voltage.

In the system introduced here, the converter switches in the steering/boost mode of operation, based on a pre-load command. In this mode $SW_1$ and $SW_3$ are conducting to increase the inductor
current. In some cases, this action is periodically replaced with the conduction of switches $SW_1$ and $SW_4$ to maintain the output voltage regulation, as described in the following section. During the steering/boost mode, the controller increases the inductor current to the load level prior to the load change, such that, ideally, at the transient instant, the two currents are matched. This results in a minimum amount of charge exchange with capacitor. As shown in Fig.3.2, during the pre-charge phase, the inductor current is charged at the maximum instantaneous rate equal to $V_g/L$.

3.2.2 Heavy-to-Light Load Transient Improvement

During a heavy-to-light load transient the inductor current slew rate of the buck converter is limited by:

$$\frac{di_L}{dt} = \frac{-V_{out}}{L}$$  \hspace{1cm} (3.3)

In modern low power devices, where the output voltage of the converter is often very low (0.8-1.2V) [30], this low voltage severely slows down recovery from heavy-to-light load transients causing the output voltage overshoots. To minimize the overshoots, in a conventional converter, the output filter capacitor must be oversized.

In a traditional boost the situation is similar; the slope of the inductor current, limited by

$$\frac{di_L}{dt} = \frac{V_g - V_{out}}{L}$$  \hspace{1cm} (3.4)
causing the capacitor overcharge. This is a significant problem when the difference between the input and output voltage of the converter is small, which is often the case in numerous portable applications, where a non-inverting buck-boost is used to slightly boost the battery voltage [32].

Unlike the light-to-heavy load transient operation that requires charging up the inductor current prior to the load transient, the heavy-to-light load operation is performed at the point when the actual load transition occurs. At that instant, the controller closes $SW_2$ and $SW_5$, as shown in Fig.3.3, to discharge the inductor current to the new steady state value while driving the current back to the source. It can be seen that this action not only disconnects the inductor from the capacitor and prevents overcharging but, in the buck mode, also changes the current slew rate to a significantly higher value:

$$\frac{di_L}{dt} = \frac{-V_g}{L}$$  \hspace{1cm} (3.5)
In this case, the pre-load command supplies the controller with the information about the new steady state current value, which is used to determine the point when the regular buck or boost operation could resume.

### 3.3 Practical Implementation

The controller architecture, shown in Fig.3.1, incorporates a PID compensator that is used for steady-state voltage regulation with a block named *mode control logic*. The mode control logic is a finite state machine (FSM), which chooses different operating modes for the converter, depending on the pre-load information and the conditions in the circuit.

Fig.3.4: State flow diagram of the mode control logic
The state transitions of the FSM are shown in Fig. 3.4. During the steady state, a modified PID controller operates the converter as a buck or a boost, depending on the input and output voltages (as in [9]). Once the ‘Pre-Load’ command is received, the mode control logic determines the required steer-inductor current action. In the case of a light-to-heavy load transient, steering/boost is activated prior to the occurrence of the load step, to achieve the required inductor current. Once the desired current is reached, the FSM generates the ‘Done Signal’ to inform the load that the power consumption can be increased. In the case of the heavy-to-light load transient, $SW_2$ and $SW_5$ are turned on to steer the inductor current back to the source $V_g$.

Fig. 3.5 demonstrates the operation of the mode control logic. The logic governs the inductor current steering after receiving the ‘Pre-Load’ command during steady state. Once the operation is completed the “Done Signal” is created to inform the load that the inductor current has reached the new requested value. It can also be seen that for the changes of load from a very light to a heavy value (as shown in Fig. 3.5) the steer operation reduces to a single switching action, where only $SW_1$ and $SW_3$ are turned on until the desired current is reached. Such simplified operation is possible as long as the inductor current can be charged to the new steady state value before a significant change of the capacitor voltage due to the load transient occurs. Otherwise, a more advanced control action is required, as described in the following subsection.

3.3.1 Preventing Significant Capacitor Discharge during Inductor Current Steering

As shown in Figs. 3.2 and 3.3, during the inductor current steering, the output capacitor is not connected to the inductor. As a result, it discharges through the load that causes a voltage drop. When the load change is significant, this voltage drop cannot be neglected. In order to minimize
this variation, a threshold for the maximum allowable voltage dip is set, the output is monitored, and a periodic switching between steering and boost operation is activated accordingly.

![Fig.3.5: Gating signals for different modes of operation.](image)

The operation in this mode is illustrated in Fig.3.6. In the case of light-to-heavy load transient, if the output voltage drops below the threshold ($V_{out} < V_{Threshold}$), the mode control logic momentarily stops the steer operation to charge up the output capacitor back to the desired level by turning on $SW_1$ and $SW_4$. After the voltage is recovered, the logic reestablishes the steering through $SW_1$ and $SW_3$. This allows increasing the inductor current while maintaining the output voltage. Similarly, during a heavy-to-light load transient in order to prevent capacitor discharging beyond the threshold the steer operation is periodically paused and the output capacitor is charged by the inductor by turning off $SW_3$ and turning on $SW_4$ (Fig.3.4).
Fig. 3.6: The converter operation as a boost converter during light-to-heavy load transient.
3.4 Experimental System and Results

To verify the operation of the system shown in Fig.3.1 an experimental system was built. The 30-W, 3.3-V, 500 kHz power stage is designed for the input voltage ranging between 1.5V and 12V. To compare the performance, a time optimal controller capable of recovering output voltage through a single on-off action, similar to [7], was developed as well.

The experimental results presented in Figs.3.7 to 3.10 show comparisons of the transient responses of both converters and verify superior performance of the load-interactive steered-inductor topology. The waveforms show the comparison for the case when the converter is operating as a buck with a 10V input and 3.3 V output. Fig.3.11 and 3.12 show the converter switching in steer and boost operation mode.

Fig.3.7 shows the transient response of the time-optimal controller to a 6.5A light-to-heavy load transient. The gating signals of $SW_1$ and $SW_2$ depict the action of the time-optimal control during the transient. Fig.3.8 shows the response of the load-interactive system. It can be seen that the new system has less than one half of the voltage undershoot for the same load step. Moreover, unlike the time optimal controller, the load-interactive system exposes the inductor to a much smaller peak current preventing possible saturation. The pre-load command that informs the converter prior to the occurrence of the load step is also shown. Based on the pre-load command $SW_1$ and $SW_3$ are turned on, to charge up the inductor to the desired level. Once the desired current is achieved the regular PID operation is resumed and it continues until the next pre-load command is received.
Fig. 3.7: The light-to-heavy load transient of the time-optimal controller—Ch1: output converter voltage (100mV/div); Ch2: inductor current (3.5A/div).

Fig. 3.8: The light-to-heavy load transient of the proposed load-interactive controller—Ch1: output converter voltage (100mV/div); Ch2: inductor current (3.5A/div).
Figs. 3.9 and 3.10 show the transient responses of the time-optimal controller and that of the proposed load-interactive converter to a 6.5A heavy-to-light load step, respectively. A similar improvement to that for the light-to-heavy transient case can be observed. The waveforms of Fig. 3.10 also experimentally verify the operation described in Section II. It can be seen that the steer inductor operation during the heavy-to-light load transient is performed at the point of the actual load step. The digital gating signals of $SW_2$ and $SW_3$ indicate that the inductor current is driven back to the source until it reaches the desired value.

Fig. 3.9: The heavy-to-light load transient of the time-optimal controller—Ch1: output converter voltage (100mV/div); Ch2: inductor current (3.5A/div).
Fig. 3.10: The heavy-to-light load transient of the proposed load-interactive controller—Ch1: output converter voltage (100mV/div); Ch2: inductor current (3.5A/div).

Figs. 3.11 and 3.12 show the converter operation in steer and boost mode, due to the output voltage drop below threshold voltage. In Fig. 3.11 it is shown that the inductor current level achieved is below the desired load current level due this operation. Nevertheless, this operation brings the inductor current close to the desired level, while maintaining the output voltage in the acceptable range. Fig. 3.12 zooms into this operation to show the boost-converter-like switching. As this operation is taking place during buck mode, when $SW_1$ and $SW_4$ conduct to restore the output voltage, the inductor current increases with a slope ($V_g - V_{out}/L$) which is lower than the slope during the steer operation ($V_g/L$).
Fig. 3.11: Steer and Boost mode of operation—Ch1: output converter voltage (100mV/div); Ch2: inductor current (5A/div).

Fig. 3.12: Boost converter like switching during steer and boost operation—Ch1: output converter voltage (100mV/div); Ch2: inductor current (5A/div).
3.5 Summary

A load interactive flexible digitally controlled dc-dc converter with minimized output filter capacitor is introduced in this chapter. It is shown that by using a modified buck-boost converter, named steered inductor buck-boost, and by improving communication between the converter and its digital load the size of the output capacitor can be drastically reduced. Based on the information about the load current, the inductor current is steered into or out of the capacitor, at a much higher slew rate compared to the conventional designs, minimizing the current provided by the capacitor during load transients. Theoretically, the newly proposed system opens a possibility of designing dc-dc converters such that the output filter capacitor is selected only based on the maximum allowable switching ripple, thus drastically reducing the overall size of the dc-dc converters.
Chapter 4

Adaptive Inductor Core Biasing to Reduce Magnetic Core

This chapter introduces a digitally-controlled buck converter with adaptive core biasing that allows for minimization of the output capacitor as well as of the inductor core. The improved performances are obtained through adaptive relocation of the converter operating point on the B-H curve of the inductor core, with the help of a digitally controlled low-power biasing circuit and an extra inductor winding. During transients, the point is set in the saturation region, so the inductance is drastically reduced. As a result the inductor current slew rate and, consequently, load transient response are improved allowing output capacitor reduction. The biasing is also used to reduce flux density allowing the core volume minimization. Experimental verifications with a 3.3 V, 30 W, 500 kHz prototype show that the adaptive biasing system has about two times smaller voltage deviation than the conventional buck allowing for proportional reduction in the output capacitance and for about 40% reduction in the magnetic core size.

4.1 Design Overview

In numerous electronic devices the output filter components of dc-dc converters are among the main contributors to their overall size and weight [33]. The output filter inductor is usually sized based on its current rating and maximum allowable ripple [6], where the amount of the current passing through the inductor is usually limited by the maximum flux density of the magnetic core [34]. As described in the previous chapter, the size of the other energy storage element (the
output capacitor) is usually determined based on the transient performance of the converter, i.e. voltage deviation during the maximum load change, rather than on the ripple criteria [35], [36].

To minimize the output capacitor without compromising the inductor current ripple, a number of solutions for improving charging current slew rate during transients have been proposed [13]-[16],[37] in addition to the system presented in the previous chapter. These include 3-level converters [13], use of auxiliary inductors [14], [37] or resistors [15], and current steering [16]. The proposed solutions drastically minimize the size of the output capacitor but, at the same time introduce additional components in the current conduction path or paths increasing the conduction losses and partially offsetting capacitor reduction advantages.

Fig.4.1: Digitally-controlled buck converter with adaptive inductor biasing.
The main goal of this chapter is to introduce a buck converter with a complementary controller of Fig.4.1 that allows minimization of both the output capacitor and the inductor core without introducing extra components into the current conduction path. These advantages are achieved through adaptive biasing of the inductor core using a low-power auxiliary circuit. During transients the biasing circuit is used to saturate the inductor core, reducing the inductance value and, consequently, drastically improving transient response. In steady state the biasing circuit is used to reduce the flux density, allowing for significant reduction of core size. This reduction also creates a possibility for on-chip integration of the inductors with increased current rating, compared to existing solutions, in which relatively small core volume is among the main constraint [38].

The following section provides the system description and explains the principle of operation. Practical implementation is discussed in Section 4.3. Section 4.4 presents experimental results verifying proper operation of the inductor core biasing system introduced in this chapter.

### 4.2 System Description and Principle of Operation

In the conventional design of power converters, the inductor needs to meet the steady state current ripple constraint under all operating conditions [6]. The inductor core is designed such that it stays well below saturation for the rated maximum current of the converter. This is to guarantee that the current ripple stays within the constraint for heavier load conditions.

The approach shown here allows core biasing. The power supply of Fig.4.1 is a simple modification of a mixed-signal current programmed mode (CPM) controlled buck converter [39],
[40]. Here the outer voltage loop is digital and it sets the current reference for the analog control loop, through a digital-to-analog converter (DAC). An extra inductor winding and a low-power biasing circuit are added to the system. The biasing circuit is controlled by the signal $i_c[n]$, which is inherently available digital equivalent of the inductor current reference. The voltage loop also contains an analog-to-digital converter (ADC) and a proximity-time optimal compensator [17]-[19], [41] that provides recovery from transients in the virtually fastest possible time, through a single on-off switching action.

As explained in the following subsections, the biasing module adaptively changes the location of the operating point on the inductor B-H curve. This allows the core to saturate during transients, decreasing the inductance value, $L$ and, hence, improving the transient response. The adaptive biasing also minimizes the magnetic core by reducing the flux density inside the core.

### 4.2.1 Light-to-Heavy Load Transient Improvement

To explain the operation of the converter, simplified inductor B-H curves and inductor current waveform during transient of Figs.4.2 and 4.3 can be used. In conventional converters, light load operation sets the inductor core well into the linear region of the B-H curve (point A, Fig.4.2.b). During light-to-heavy load transients the rate of change of the inductor current of the buck converter is limited by:

$$\frac{d}{dt} i = \frac{V_g - V_{out}}{L}, \quad (4.1)$$
where $V_g$ and $V_{out}$ are the input and output voltages of the converter, respectively. The inductance, $L$ is proportional to the slope of the curve around the operating point. As the load and, consequently, the inductor current increase, the operating point travels along the B-H curve through the linear region. During this transient the inductance is mostly constant and as shown in Fig.4.2, the inductor slew rate is approximately the same as in the steady state.

In the system introduced here a biasing winding is used to adaptively relocate the position of the operating point on the B-H curve. The adaptive biasing is demonstrated in Fig.4.3. At light loads, the operating point is relocated close to the top knee of the B-H curve (point 1). This relocation

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Fig.4.2: (a) Inductor current of a conventional buck during a light-to-heavy load transient. (b) Corresponding B-H curve with load transient trajectories; where $L$ is inductance, $l_{core}$ is core length, $N$ is number of turns in the winding and $\Delta i_L$ is the change of load current.
allows a light-to-heavy load transient to push the core into saturation, i.e. to move from point 1 to 2, drastically reducing the inductance value. As a result, the inductor current slew rate is increased and the transient performance improved. The operating point is relocated by providing

![Diagram](image)

**Fig.4.3: Relocation of the operating point on B-H curve through adaptive core biasing**

a positive dc current to the biasing winding of the core (Figs.4.1 and 4.4) therefore, increasing the flux density. Once the transient is completed, the biasing circuit brings the operating point back to the linear region (point 3, close to the bottom knee point), where the inductance is larger, to maintain a low current ripple.

4.2.2 Heavy-to-Light Load Transient Improvement
During a heavy-to-light load transient, the inductor current slew rate of the buck converter is limited by:

\[
\frac{d i_L}{d t} = -\frac{V_{out}}{L}
\]

(4.2)

Similar to the previous operation, at heavy loads the operating point on the B-H curve is relocated to improve the current slew rate and consequently, heavy-to-light load transient response. In this case the biasing circuit brings the operating point close to the bottom knee of the B-H curve (point 3 of Fig. 4.3) so that a sudden drop in the inductor current \(i_L(t)\) pushes the

Fig. 4.4: Simplified diagram of the inductor with biasing windings
core into saturation. This moves the operating point from 3 to 4. In this way the inductance value is reduced and the current slew rate is increased. The core stays in this low inductance mode until the optimal controller recovers the voltage. After the transient is completed, the biasing circuit brings the operating point back to the linear region of the B-H curve (point 1), increasing inductance.

4.2.3 Ripple Current Reduction using Biasing

In addition to the increase of the slew rate and consequent output capacitor reduction, the biasing also allows inductor core reduction. As described previously, for heavy loads the biasing is applied such that flux of the opposite direction from that created by $i_L(t)$ is established. This effectively means that the net flux through the core, i.e. flux density, is reduced and that the cross-sectional area of the core can be reduced as well. As it is shown in the experimental section of this chapter, the biasing allows up to 40% reduction in the core size depending on the core geometry. This feature is well suited for on-chip integration of the inductors with semiconductor components of low-power supplies where the limited dimension of the magnetic materials is among the main obstacles in increasing the current rating of the integrated solutions [38].

4.3 Practical Implementation

The key elements of the adaptive biasing converter are the low-power biasing circuit and the inductor with biasing core. In this section their practical implementation is described. The biasing circuit of Fig.4.5 is designed with having overall system efficiency in mind. To minimize the requirements for the biasing current and, at the same time, maximize its effect on the core flux density, a biasing winding with a significantly larger number of turns than that of the main
inductor is used. The biasing current is provided through a structure consisting of a digital-to-analog converter (DAC) and an H-bridge. The DAC operates as a voltage source whose output value is regulated such that the desired biasing current is achieved. The H-bridge is used to change the polarity of the biasing current. As described in the previous section, the polarity of the current depends on the operating conditions and, in this implementation, is changed with the polarity control block. Both the DAC and the polarity control block receive the control signals from the mapping circuit, which transfers the current control loop reference signal $i_c[n]$ (Fig. 4.1) into a digital value proportional to the biasing current $i_{bias}[n]$.

4.3.1 Inductor with Biasing Winding

As described in the previous subsection, in this implementation a biasing winding with a larger number of turns than that of the main inductor $L$ is used to minimize power consumption. However, if implemented as shown in Fig. 4.4, the larger number of turns can cause a large reflected voltage spike from the main winding affecting the circuit operation. To reduce this problem the inductor is designed so that a partial cancellation of the flux caused by the main

Fig. 4.5: Low-power biasing circuit
inductor winding is achieved. The implementation is shown in Fig. 4.6. The biasing winding is a simple addition to the widely used E-core inductor [42]. Here, the biasing windings are placed across side legs [43], [44] of the core and the main inductor is wound across the centre leg, as in conventional implementations. As shown in Fig. 4.6, the number of turns on the side legs is different and the right leg has twice as many turns. Here the biasing is performed such that during transients the right leg of the core is most saturated. The flux lines also show that, in this configuration the main winding partially cancels the flux of the biasing winding through one leg and contributes to the flux of the other leg, resulting in net reflected voltage that is a 1/3 of the straightforward design shown in Fig. 4.4. A larger cancellation of the reflected voltage is possible but it comes at the cost of a significant increase in power consumption of the biasing circuit.

Fig. 4.6: Implementation of the inductor with biasing winding.
4.3.2 Loss in Magnetic Core due to Bias Winding

There are two major loss mechanisms [34] associated with the time-varying fluxes due to the bias winding. The first is the ohmic $I^2R$ loss, which is associated with the induced currents in the core material. According to Faraday’s law time-varying magnetic fields give rise to electric fields, and that induces currents in the core material, i.e. *eddy current*. This induced current creates a demagnetizing effect in the core and requires increased current in the bias winding to counteract.

The second loss mechanism is due to the hysteresis loop of the magnetic material [34]. In a magnetic circuit like Fig. 4.4, a time-varying excitation results in cyclic variation in the magnetic material described by a hysteresis loop. Each time the magnetic material goes through the excitation cycle, the energy input can be calculated by multiplying the area of the hysteresis loop and the volume of the core.

The injected current in the bias winding allows reducing the flux density in the core, allowing reduction in the core volume. This in return reduces the core loss and partially offsets the power consumption in the bias winding.
4.4 Experimental System and Results

Based on diagrams of Figs. 4.1, 4.5, and 4.6, a 10 V - to - 3.3 V, 500 kHz experimental prototype was built. Even though the maximum inductor current of the adaptive biasing buck is about 10A, an off-shelf E-core inductor with core saturation at 4A was used. For the controller, an FPGA evaluation board and discrete components were used. The inductor was modified by placing biasing winding on the side legs of the core, as described in the previous section. To verify the advantages of the introduced concept, the performance of the system with and without influence of the biasing circuit are compared in Figs.4.7 and 4.8. The results show that with the adaptive biasing transient performance is improved and results in a 1.6 times smaller output voltage deviation allowing for equivalent reduction in the output capacitor value.

Fig.4.7: The light-to-heavy load transient without core biasing– Ch1: output converter voltage (50mV/div); Ch2: inductor current (1A/div).
In order to show the ability to reduce the steady state current ripple, hence allowing larger than rated current for the core, a very large load step (9A) was performed on the same core. As Fig.4.9 shows this large load step pushes the core deep into saturation, drastically increasing the ripple compared to lighter load operation. Fig.4.10 shows how the biasing reduces the ripple back to normal operating condition. As the bias current is injected, the ripple is reduced by half indicating reduction in flux density and, consequently, allowing core size reduction.
Fig. 4.9: 9A load step without core biasing—Ch1: output converter voltage (100mV/div); Ch2: inductor current (5A/div).

Fig. 4.10: Inductor ripple reduction using biasing—Ch3: Bias current (5A/div); Ch4: current ripple 2A/div.
4.5 Summary

A buck converter with adaptive core biasing of the magnetic core that reduces the size of reactive components without introducing extra switches, i.e. losses, in the main current conduction path is introduced in this chapter. The core biasing is performed with an extra winding, by dynamic relocation of the operating point on the B-H curve of the inductor, based on inherently available information in the control loop of a mixed-signal current programmed controller. To minimize the problem of a high reflected voltage, an implementation of the winding based on a simple modification of an E-core based inductor is shown. The experimental results verify that the adaptive biasing system can be implemented with a smaller capacitor and an inductor with a smaller core size than those of the conventional buck converter.
Chapter 5

Programmable-Output PFC Rectifier with Minimized Bus Capacitance

This chapter introduces a digitally-controlled 2-stage single-phase rectifier with power factor correction (PFC) that is well suited for emerging low-power applications requiring programmable supply voltage. The rectifier is a modification of a flyback-buck cascaded configuration where the intermediate energy storage capacitor is replaced by a non-symmetric capacitive divider with independent control of tap voltages. The voltages are dynamically controlled through a single secondary winding, such that the optimized efficiency and reduced size of the downstream stage are achieved without sacrificing dynamic response. Results obtained with a 30W universal-input experimental prototype confirm fast transient response during efficiency optimization, operation with a near unity power factor, and about a 50% reduction in the flyback capacitor value, as compared to single-stage solutions.

5.1 Design Overview

Single-phase rectifiers with power factor correction (PFC) providing power up to approximately 100 W are widely used as chargers for mobile devices or dedicated supplies. The applications include personal computers, consumer electronics, telecommunication devices, and avionics equipments. In addition to providing close to unity power factor (PF) and low total harmonic
distortion (THD), emerging standards and applications also require programmable output voltage. For example, the IEEE-UPAMD standard [45], which defines a connection between a charger (adapter) and supplied mobile device, defines a communication link that sets up required output voltage level as well as voltage transition times. Similarly, in adaptive voltage bus system [46], a programmable dc bus voltage is changed quickly based on the load requirements.

A number of single-phase ac-dc solutions with power factor correction have been proposed [47-51]. Generally, they can be divided into single [52-55] and two-stage [56] systems. In a typical low power application, where the cost is a dominant factor, single stage solutions employing a flyback converter [57] are frequently used. This is mostly due to the controller and system simplicity as well as due to the existence of galvanic isolation. However, these systems usually suffer from voltage regulation problems [58] and require a bulky output capacitor to compensate for low frequency line harmonics in the output voltage [59]. More complex two-stage solutions have better voltage regulation [56]. There, the first stage provides ac-dc rectification and the second dc-dc step-down stage keeps the output voltage well regulated [56]. In these systems, the intermediate voltage between the two stages is usually selected based on output voltage and design tradeoffs between the converter efficiency and dynamic response [60]. In general, by reducing the difference between the input and output voltages the efficiency of the downstream stage can be improved. However, this improvement comes at the expense of the dynamic response and, larger output capacitance value. In the ac-dc applications with programmable output voltage that require fast transient response this tradeoff is a serious concern.

The primary objective of this chapter is to present the simple flyback-based two-stage solution of Fig.5.1 that is well suited for emerging ac-dc applications requiring programmable output
voltage. The converter operates with a relatively small flyback capacitor, has tight output voltage regulation, and provides fast transient response while operating at the optimized efficiency point.

Fig.5.1: Programmable-output PFC rectifier and complementary digital controller.

The following section gives the system description and explains the principle of operation of the proposed converter architecture. A practical implementation is discussed in Section 5.3 and Section 5.4 presents experimental results verifying the proper operation of the implemented power supply.

5.2 System Description and Principle of Operation

The system in Fig.5.1 is a 2-stage converter, where the first stage is a modified flyback converter and second stage is a conventional buck with an extra switch, \( SW_6 \). The flyback is modified such
that the output capacitor is replaced with a non-symmetric capacitive divider of a smaller equivalent capacitance, where the voltages of the two capacitors are independently regulated. The divider centre tap voltage $v_{bus}(t)$, i.e. bus voltage, is the input of the buck during regular steady-state operation. This voltage is allowed to have relatively large ripple at twice the line frequency, to minimize the capacitor ($C_{bus}$). As described below, the dc value of the bus voltage is dynamically adjusted, based on the desired output voltage level, such that the efficiency is maximized. The top capacitor of the divider is used during transients to improve the dynamic response, i.e. to step up inductor current slew rate. Both stages are regulated with a digital controller that has two interactive control loops. The front-end controller regulates operation of the flyback converter such that close to unity factor is achieved and, at the same time, regulates the average values of divider tap voltages, based on information from efficiency optimization block. The controller of the buck provides tight output voltage regulation and fast dynamic response. During transients the buck controller employs a minimum deviation control algorithm [20], recovering the current in a single on-off switching cycle with minimum possible output voltage deviation.

5.2.1 Programmable Intermediate Bus Voltage for Efficiency Optimization

The efficiency of a 2-stage converters with a wide range of operating conditions can be optimized by changing the voltage difference between the intermediate bus voltage and the output voltage, as demonstrated in [60]. This optimizes the sum of converter conduction and switching losses depending on the output power level of the converter. For the optimum efficiency, this results in much lower than maximum intermediate bus voltage, due to significant reduction of switching losses. This reduction of voltage difference reduces component stress on
the second stage dc-dc converter and results in lower inductor ripple, allowing possible reduction of the inductor size [61]. Hence, to optimize the efficiency and at the same time to minimize the value of the buck inductor while maintaining a constant ripple, the intermediate bus voltage is dynamically changed based on the operating condition.

5.2.2 Improving Dynamic Performance of the Downstream Stage

The reduction of the input voltage described in the previous subsection optimizes efficiency of the downstream buck stage but, at the same time, degrades dynamic performance and consequently increases the requirements for the output capacitor value. A larger output capacitor is required even though the buck inductor is reduced. This is due to even larger drop in the inductor current slew rate during light-to-heavy load transients, resulting in a slower charging of the output capacitor.

Fig. 5.2: Reduction in inductor size vs. inductor current slew rate for a 5V buck converter which bus voltage changes between 5.5 V and 10 V.
This can be demonstrated by the example depicted in Fig.5.2 showing maximum possible reduction in the inductance and, for the reduced inductance value, the drop in the inductor current slew rate. The results are shown for a 10 V- to - 5 V rated buck converter, as its supply voltage changes between the output, i.e. 5V, and the maximum rated value. The diagrams are obtained from simple equations [6] for the inductor current ripple and current slew rate during a light-to-heavy load transient.

In order to improve transient, a second capacitor, $C_{\text{top}}$ of Fig.5.1, is incorporated in the design. This capacitor is charged at a higher voltage than the bus voltage and used during light-to-heavy load transients, to improve the inductor current slew rate. As described in the following section the average voltage value of this capacitor is regulated independently of the bus voltage, with the modified flyback converter. It should be noted that the value of this capacitor is much smaller than that of $C_{\text{bus}}$ (Fig.5.1) allowing for cost-effective implementation. This is because the $C_{\text{top}}$ only provides energy during transients and is not used to supply the difference between the time varying input and constant output power [6]. The following calculation, along with Fig.5.3, shows how the size of $C_{\text{top}}$ is selected to improve the transient response of the second stage.

Charge transferred from $C_{\text{top}}$ to output capacitor, $C$ during a $\Delta i$ step transient can be calculated as:

$$\Delta Q = \frac{1}{2} \times T_c \times \Delta i$$  \hspace{1cm} (5.1)

Where the time to reach the new steady stage current value:

$$T_c = \frac{\Delta i}{V_{\text{top}} + V_{\text{bus}} - V_{\text{out}}} \hspace{1cm} (5.2)$$
where $V_{top}$ and $V_{bus}$ are the top and bus capacitor voltages, respectively and $V_{out}$ is the output voltage. $L$ is the value of the inductor. Substituting (5.2) in (5.1) we get,

$$\Delta Q = \frac{1}{2} \frac{L \cdot \Delta i^2}{V_{top} + V_{bus} - V_{out}}$$

(5.3)

Now since the top capacitor, $C_{top}$ is sized much smaller than the bus capacitor, $C_{bus}$; if the voltage drop due to this charge transfer is $\Delta V$, we can assume that the entire drop occurs across the top capacitor. Hence, the top capacitor can be calculated as:

$$C_{top} = \frac{1}{2} \cdot \frac{L \cdot \Delta i^2}{(V_{top} + V_{bus} - V_{out}) \cdot \Delta V}$$

(5.4)

The large difference in the capacitor values is used to implement practically independent control of the output voltages, as described in the following section.

Fig.5.3: Charge transfer from $C_{top}$ during transients.
5.3 Practical Implementation

In the system of Fig. 5.1, a PI compensator regulates the intermediate bus voltage \( v_{bus}(t) \) and a dual-mode compensator to regulates the output voltage \( v_{out}(t) \). Two analog-to-digital converters (ADC) are utilized to sample the outputs of the two stages and to compare them with the corresponding references. The load information, which can be obtained through inductor current measurement, estimation [62], or directly from the load, sets the reference for the output voltage based on the load requirement. The reference for the bus voltage is selected such that optimum efficiency is achieved for the given operating condition. For achieving a high power factor, the flyback converter is operated at the boundary conduction mode (BCM), similar to the system presented in [63]. As shown there, the BCM operation minimizes current stress and results in a relatively low electromagnetic interference. Fig. 5.4 shows the current waveforms on the primary side \( i_{primary} \), secondary side \( i_{secondary} \) and the input current \( i_{in} \). As explained in the following subsection, ADC\(_1\) is utilized in controlling both voltages of the capacitive divider, i.e. the bus voltage, \( v_{bus}(t) \) and the voltage across \( C_{top} \) capacitor, \( v_{top}(t) \). The fast transient control block utilizes charge stored at \( C_{top} \) by momentarily turning \( SW_6 \) on during transients to improve the inductor current slew rate in the second stage.

5.3.1 Dual Output Control through Flyback Secondary Winding

To provide voltages for both taps of the capacitive divider a flyback transformer with two secondary windings could be used [6]. However such a solution suffers from the cross-regulation problem [64] that affects the output voltage regulation and requires a custom flyback transformer design. To eliminate this problem and simplify system implementation, a simple method for providing two independent voltages is developed. Here, both divider taps are controlled from the
same secondary winding of the flyback converter. As shown in Fig.5.5, when $SW_2$ is on, the secondary winding current (Fig.5.4) charges the bottom capacitor. During this time the body diode of $SW_3$ is reversed biased. In this case $ADC_1$ samples the voltage stored at the bus capacitor, i.e. $v_{bus}(t)$.
Similarly, as Fig. 5.6 shows, by turning on $SW_3$ the series connection of both capacitors is charged. In this case the ADC$_1$ samples the sum of voltages stored across both capacitors. Since as described in the previous section, the top capacitor is much smaller than the bottom one, the voltages across them are not changed equally. The voltage of the smaller, i.e. top, capacitor is primarily affected, allowing the two capacitor voltages to be controlled independently. This is performed over a portion of one switching period, as described with timing diagrams of Figs. 5.7 and 5.8.

![Fig. 5.6: Charging of the top capacitor.](image)

Fig. 5.6 shows the conventional operation, i.e. boundary conduction mode, without charging of the top capacitor, where the total inductor current is used to supply the bottom capacitor. Fig. 5.8 illustrates the switching cycle, where a portion of the secondary conduction period is used to charge up $C_{top}$. This is shown as charge $Q_{-C_{top}}$ when $SW_3$ is on. Since a portion of the charge is given to $C_{top}$, the controller increases the on-time, in the following cycle, for $SW_1$ ($\Delta d$ in Fig. 5.7), to maintain steady bus voltage.
Fig. 5.7: Timing diagram of bus capacitor charging.

Fig. 5.8: Timing diagram of top capacitor charging.
5.3.2 Increased Conduction Loss and Light Load Efficiency Improvement

Compared to a conventional flyback, the proposed first stage converter has an extra switch ($SW_2$) in the conduction path. But since the switch and the diode are rated for a half the voltage now, the increase in the conduction loss in minimized. This is due to the fact that the channel length, hence the on resistance, of a semiconductor device is proportional to the component rating. Similarly addition of $SW_6$ will now require blocking in both directions for $SW_4$. As a result, $SW_4$ needs to be replaced by two switches in series with half the voltage rating, as shown in Fig.5.1. The size of the $SW_3$ and $SW_6$ can be much smaller compared to other switches as the rms current through them is much smaller. Furthermore, during light load operation, in order to improve the efficiency of the converter only $SW_3$ and $SW_6$ can be used to regulate the output voltage.

5.4 Experimental System and Results

To verify the operation of the system shown in Fig. 5.1 an experimental prototype was built. The universal input, 2-stage 30-W ac-dc converter with power factor correction and programmable bus and output voltages was designed. Switching frequency of the first stage varies between 50 kHz to 200 kHz, depending on the operating condition, and the second stage operates with 500 kHz fixed switching frequency.

Figs.5.9 and 5.10 show steady-state operation of the system. The power factor of the input current waveform of Fig.5.9 is about 0.98 and stays in 0.95-0.99 range over all operating conditions.
Fig. 5.9: Input voltage and current waveform of the proposed converter—Ch1: input voltage (50V/div); Ch2: input current (100 mA/div).

Fig. 5.10 shows regulation of the bus voltage and the output voltage regulations. Even though a 600 µF bus capacitor is used, which is at least 50% smaller than that of state of the art single phase solutions [59], [65], the output voltage is well-regulated. As mentioned before, this is achieved by allowing bus voltage to contain a relatively high ripple of 1.5V_p-p at twice the line frequency. However, the output voltage of the converter shows tight regulation with 20mV ripple at 2V output voltage across 220 µF output capacitor.
Fig. 5.10: Regulation of Bus Voltage and Output Voltage – Ch1: Bus voltage (500mV/div); Ch2: Output voltage (20mV/div).

Fig. 5.11 shows a step response of the top capacitor to demonstrate independent charging. As the figure illustrates, once the reference for the top capacitor is updated, the capacitor is charged to 8V in 150ms without affecting the bus voltage, i.e. the voltage across the bottom capacitor.

Fig. 5.12 shows the transient response comparison between the introduced converter architecture and a conventional downstream buck stage. For the proposed architecture case, the bus voltage was regulated at 4V, to minimize switching losses of the downstream converter, and the top capacitor was charged to 8V. On the other hand, the conventional buck was operating with a fixed 12V input voltage. As the waveform shows, both result in similar voltage deviation during the transients. In other words, the proposed architecture allows efficiency optimization without sacrificing the transient response. For 2V output and 4V bus voltage the efficiency of the second
stage is measured to be 87% for 4A output current, compared to 81% efficiency for 12V fixed
bus voltage. In case of smaller loads this improvement is expected to be greater due to reduction
of more dominant switching losses.

![Graph showing voltage levels](image)

**Fig.5.11: Charging of Top Capacitor – Ch1: Bus + Top Cap voltage (5V/div); Ch2: Bus voltage (2V/div); Ch3: Change reference for Top Cap.**

### 5.5 Summary

A single-phase rectifier with power factor correction well suited for emerging applications
requiring quickly changing programmable voltage is introduced. The 2-stage solution is a
modification of flyback-buck topology where a non-symmetric capacitive divider with
practically independent control of two tap voltages is used. The centre tap, i.e. bus voltage, is
adaptively regulated such that the efficiency of the downstream stage is optimized. The top capacitor of the divider, with a much smaller value than that of the bottom one, is used to increase current slew rate during transients canceling negative effects of the efficiency optimization. A practically independent regulation of the divider voltages is performed with a single secondary winding, eliminating the need for a custom flyback inductor design, as well as cross-regulation problem existing in two winding solutions. The regulation is based on the current steering and utilization of a large difference in the divider capacitance values. Experimental results confirm system advantages and proper operation.

Fig. 5.12: Transient response comparison – Ch1: Programmable $v_{bus}$ and $v_{top}$ (100mV/div); Ch2: Buck with 12V $V_{in}$ (100mV/div); Ch3: Inductor current (2A/div); Ch4: $V_x$ node voltage (10V/div)
Chapter 6

Adaptive Switching Frequency Scaling for Improving Efficiency

This chapter introduces a practical system for improving efficiency of low power dc-dc converters regulated by digital voltage-mode PWM controllers that can be used as the downstream stage of the previously presented topology. Depending on the input voltage, the controller adaptively changes the switching frequency, thus minimizing related losses while maintaining tight output voltage regulation. For interactive 2-stage converter presented in previous chapter, the switching frequency of the downstream stage is selected based on the intermediate bus voltage to maximize the efficiency. The implementation described in this chapter also constrains electromagnetic interference (EMI) caused by the variable frequency operation. The presented architecture, whose key new element is all-digital adaptive clock and spread spectrum generator, can be implemented in the latest CMOS technologies and, as such, is well-suited for on-chip integration in portable battery-powered applications.

The effectiveness of the system is verified with a 2.1 V/5 W buck prototype, where the input voltage ranges between 2.75 V and 5.5 V. The results show that, for an adaptive frequency regulation in the range between 780 kHz and 2 MHz, loss reduction of up to 18% is achieved.

6.1 Design Overview

In modern portable battery powered electronic devices, the efficiency of the switch mode power supplies (SMPS) is one of the main concerns because it directly translates into battery life [66].
As shown in [66]-[69] batteries have a wide variation in voltage output depending on their charge level. The battery is usually connected to a fixed switching frequency SMPS providing a constant output voltage [67]-[70]. The output filter of such a supply is often oversized. The capacitor is usually sized based on the energy storage requirement during large load transients [35],[36], and the inductor is selected so that, for a given frequency, its steady-state ripple requirement is satisfied for the full range of input voltages, including the worst case. For a buck converter, the worst case corresponds to the largest input voltage. Such sizing provides tight output voltage regulation, but also results in a sub-optimal operation, from the efficiency point of view, for virtually all inputs except for the worst case. In other words, since the ripple for other input voltages is smaller than the allowable, the converter operates at a larger than the minimal possible frequency increasing switching losses.

As shown in chapter 5, for 2-stage interactive converters the intermediate bus voltage is selected to maximize the efficiency of the second stage. The switching loss of the downstream stage is depended on the difference between the intermediate bus voltage and the output voltage, and the switching frequency of the downstream stage. As a result variable frequency operation based on the intermediate bus voltage maximizes the efficiency of the downstream stage.

Conventional analog hysteretic controllers inherently providing constant current or voltage ripple [71] are not the preferable solution. This is mostly due to the variable frequency of operation causing EMI problems and incompatibility for on-chip integration in the latest CMOS technologies, primarily dedicated to digital systems. While the EMI problems in numerous applications have been resolved, with spread spectrum mitigation techniques [72],[73], the on-chip integration with digital systems providing numerous benefits [74] remains a challenge. This
is due to difficulties [75] in analog implementation of comparators, which need to be fast and accurate. On the other side, the digital hysteretic controller proposed in [76], operates at a fixed frequency not offering proposed efficiency improvement. Constant voltage ripple based hysteretic solutions [77] are challenging to implement, since they require sensing of very small output variations. On the other hand, constant current ripple designs [78] require current sensing introducing additional losses. Constant off-time controllers [79] also inherently provide constant ripple operation. However, this advantage comes only with buck-based topologies.

Frequency variations of the constant ripple controllers often raise EMI issues and, hence, mitigation techniques such as spread spectrum [72], [73] are applied. In low-power supplies most of these are implemented in an analog manner.

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Fig.6.1: Adaptive switching frequency PWM controller regulating operation of a buck converter.
This chapter introduces practical digital controller architecture of Fig. 6.1 that minimizes losses by adaptively changing the switching frequency, depending on the input voltage. To compensate for the variable frequency operation, not preferable in the targeted noise-sensitive applications, the controller employs adaptive EMI cancelation, using the key new element, named all-digital clock divider and spread spectrum generator.

### 6.2 Principle of Operation

The controller architecture of Fig. 6.1 is designed around a digital PWM architecture [11], [16], [5], [20], proven to be well suited for a full integration in the latest CMOS technologies [5], [20]. In this case, the clock frequency of the digital pulse-width modulator (DPWM) and, consequently, the switching frequency of the converter are changed using the clock divider and spread spectrum generator block from the figure. Input voltage dependent control signal $f_{sw,f}[n]$ adaptively changes the fundamental frequency of the clock signal, as well as its spectrum. This means that the switching frequency $f_{sw}$ is formed of two components, i.e. $f_{sw} = f_{sw,f} + f_{ss}$. The fundamental component $f_{sw,f}$, is determined by the current ripple amplitude. The second component minimizing EMI, $f_{ss}$ is created by the spread spectrum part of the generator.

To eliminate the input voltage measurement, the fundamental component resulting in a constant current ripple, for buck and boost converters, respectively, is selected as

$$f_{sw,f} = \frac{V_{out}(1 - D)}{2L \times \Delta i_L} = k_R \cdot D'$$ \hspace{1cm} \text{[Buck]} \quad (6.1)$$

$$f_{sw,f} = \frac{V_{out}}{2L \times \Delta i_L} D(1 - D) = k_R \cdot D \cdot D'$$ \hspace{1cm} \text{[Boost]} \quad (6.2)$$
where, $\Delta i_L$ is the ripple amplitude, $L$ is the output filter inductance, $V_o$ is the output voltage, and $D$ is the steady-state duty ratio value. In the system of Fig.6.1, this equation is implemented with a simple multiplier providing the control signal for the clock generator and having a control input $k_R[n]$ for regulating the ripple amplitude. The maximum allowable current ripple depends on the input and output voltages as well as on the width of the frequency side bands introduced by the spread-spectrum generator, increasing the current ripple and thus the steady-state voltage ripple. The variable inductor current ripple does not have a significant effect on the output capacitor. In modern SMPS the output capacitors are sized based on more stringent requirement regarding energy storage capability during transients. Hence, from the charge ripple perspective, they are oversized and this portion of ripple is usually negligible [6].

To avoid potential slower dynamic response caused by operation at lower clock frequency, the controller employs an optimal response circuit [20].

### 6.3 Practical Implementation

The key new element of the presented architecture is the *clock and spread spectrum generator*. To generate spread spectrum, usually mixed-signal solutions based on analog circuit modifying the frequency of a voltage controlled oscillator (VCO) are usually used [80]. This principle is implemented in [81] to create a variable spectrum of a ring-oscillator based digital pulse-width modulator (DPWM). On the other hand, an all-digital solution based on modifying resolution of a counter based DPWM [82], as authors explained, results in voltage regulation problems.

A digital architecture suitable for implementation in the latest CMOS technologies, providing variable switching frequency and EMI mitigation, without the above mentioned problems is presented in the following subsection.
6.3.1 All-digital clock divider and spread spectrum generator

The all-digital clock divider and spread spectrum generator, generating both variable fundamental frequency and spread-spectrum frequency components, is shown in Fig.6.2. Unlike conventional spread-spectrum implementations, utilizing a constant-frequency master clock, the proposed solution modifies the master clock frequency based on both the input voltage and desired spread spectrum bandwidth.

The operation of the generator can be described through the diagram of Fig.6.2 and corresponding waveforms of Fig.6.3. The DPWM clk signal is generated by a combined ring oscillator and $2^m$:1 multiplexer. The multiplexer selects the location, i.e. cell, where the pulse propagating through the $2^m$-cell ring oscillator is transmitted to the output. Selection of the active input is performed with a wraparound adder producing digital signal $\text{sel}[n]=\text{sel}[n-1] + k[n]$, 

![Diagram of the all-digital clock divider and spread spectrum generator.](image)

Fig.6.2: All-digital clock divider and spread spectrum generator.
where $k[n]$ is a variable depending on $f_{sw} = f_{sw,f} + f_{ss}$.

As seen in Fig.6.3, showing waveforms of a 64-cell generator, the lowest frequency is produced when $k[n]=0$. The pulse propagating through the ring-oscillator is transmitted through the first multiplexer input, $in_0$, resulting in a clock with a $64T_d$ period, where $T_d$ is propagation time of each ring oscillator cell. For different values of $k[n]$, the active multiplexer input changes resulting in faster frequencies. For $k[n] = 30$ (decimal), assuming $sel[0]=0$, the wraparound adder increments the active multiplexer input by 30 (i.e. such that the multiplexer input select pattern becomes 0, 30, 60, 26, 56,..,) resulting in a clock signal with a $30T_d$ period.

It can be seen that the frequency of the clock changes as $f_{clk} = 1/(kT_d)$ and $2^m$ discrete period steps can be obtained. Since the clock frequency is inversely proportional to the control signal $k[n]$, a mapping circuit is used to convert an input $f_{sw}[n]$ into the corresponding control value.

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Fig.6.3: Key waveforms of 64-cell clock generator. Top two: for $k[n] = 0$; Bottom: for $k[n] = 30$. 
6.3.1.1 Simplified design for the clock divider module

A simplified clock divider and spread spectrum generator module is proposed in Fig. 6.4, improving the monotonicity of the ring oscillator and reducing area requirement for possible IC implementation. The simplified implementation uses only two delay cells and an enable input to generate the desired clock frequency. The enable input is generated by a set of shift registers. The shift register performs division-by-2 operation each time the pulse is circled back through the ring oscillator, until the quotient of the division becomes zero, while the output of the remainder block selects the mux output. Once the quotient is zero the enable input is driven high, generating a clk pulse. At this point, the wraparound adder updates the value of sel[n] for the next cycle and the process is repeated.

Fig. 6.4: Simplified clock divider and spread spectrum generator.
6.3.2 Programmable spread-spectrum generation

To create a spread-spectrum modulating signal $f_{ss}[n]$ a pseudo-random number generator (PRNG) based on a linear feedback shift register [83] is modified such that its numbers range can be adaptively changed.

Figure 6.5 shows the modified PRNG that can create up to $2^p-1$ different $f_{ss}[n]$ numbers in a pseudo random fashion. This generator is triggered by the rising edge of the pulse-width modulated signal $c(t)$ (Figs. 6.1 and 6.2) and changes its value after each switching cycle. The range of the numbers produced by the generator is selected depending on the value of the fundamental frequency signal $f_{sw-f}$. For lower frequencies the $f_{ss}$ range decreases keeping the ratio between the maximum $f_{ss}$ variation and $f_{sw-f}$ constant, limiting the degradation of the inductor ripple. The variation of the frequency range is performed by changing the number of the shift register in the feedback loop, using a demultiplexer controlled by most significant bits of $f_{sw-f}$.

![Fig.6.5: PRNG based on variable-length shift register.](image-url)
6.4 Experimental System and Results

To verify operation of the system shown in Fig.6.1, an FPGA-based controller prototype was created. It controls operation of a 1.8 V, 5 W buck converter. The input voltage of the system is varied between 2.75V and 5.5V emulating behavior of a Li-ion battery cell.

6.4.1 Functional verification

To test the ability of the system to keep the ripple at a constant level, the spread spectrum block is temporarily disabled. Fig.6.6 shows response of the system for sudden variations of the input voltage. The results confirm that the new architecture provides tight control of the current ripple amplitude while adaptively changing the switching frequency depending on the input voltage.

Fig.6.6: Response of the adaptive switching frequency controller for sudden variations of the input voltage. Ch.1: output voltage of the converter (50 mv/div); Ch.2: inductor current (1A/div); Ch.3: switching node voltage of the buck converter (5V/div); D13: voltage transient control signal (digital signal). The time scale is 2 μs/div.
Figs. 6.7 and 6.8 show input current spectrum measurements for the converter operating in steady state at frequency of 780 KHz before and after the activation of the spread spectrum circuit, respectively. It can be seen that the spread spectrum circuit effectively reduces the low-frequency fundamental component mitigating potential EMI problem. Fig 6.9 shows the inductor current waveform when the read-spectrum module is enabled.

Fig. 6.7: Input current conducted EMI for fixed frequency. FFT operation performed with Y-axis: 5db/div, X-axis: 500 KHz/div.

Fig. 6.8: Input current conducted EMI for Spread Spectrum. FFT operation performed with Y-axis: 5db/div, X-axis: 500 KHz/div.
6.4.2 Efficiency Improvement

Figs. 6.10 and 6.11 compare the converter efficiency when the system operates at a constant switching frequency of 2 MHz and when the switching frequency is adaptively varied based on the input voltage. The results are shown for two different output load conditions. It can be seen that the adaptive frequency controller results in an up to 2% efficiency improvement, translating into a larger than 18% reduction of the total losses.

Finally, Fig. 6.12 shows the efficiency comparison over the wide range of load currents for an input voltage of 2.75 V. The switching frequency was scaled down to 780 KHz from 2 MHz. The efficiency improvement is around 2% over the entire range of load currents. This observation makes the proposed solution very attractive for portable applications where as the lithium-ion
battery discharges, resulting in reduction in input voltage, the efficiency of the converter increases over the entire range of load conditions.

Fig. 6.10: Efficiency comparison for fixed frequency and variable frequency operation for 500 mA load current.

Fig. 6.11: Efficiency comparison for fixed frequency and variable frequency operation for 1.25 A load current.
An adaptive frequency all-digital controller architecture improving efficiency of dc-dc supplies is presented. The architecture well suited for on-chip integration in the latest CMOS technologies allowing utilization of digital implementation advantages. Depending on the input voltage, the controller adaptively changes the switching frequency reducing losses while minimizing EMI problems related to the variable frequency operation. The key controller element is novel clock divider and spread spectrum generator allowing dual modulation of the clock generator, depending both on the spread spectrum and input voltage requirements. Experimental results prove the effectiveness of the system.
Chapter 7
Conclusions and Future Work

The interactive flexible switch-mode power supplies, discussed in this thesis, significantly reduce output filter volume compared to conventional converter topologies. This reduction is demonstrated on several designs. The common element for all of them is that, the advantages are achieved by modifying the conventional converters and incorporating a certain level of communication between the power stage and its load.

7.1 Load Interactive Converters

In this system, based on the information about the load current, the inductor current of a modified non-inverting buck-boost is steered into or out of the capacitor, at a much higher slew rate compared to the conventional designs. Thus, the current provided by the capacitor during load transients is minimized. Theoretically, the newly proposed system opens a possibility of designing dc-dc converters such that the output filter capacitor is selected only based on the maximum allowable switching ripple, thus drastically reducing the overall size of the dc-dc converters.

7.2 Inductor Core Biasing

Inductor core biasing concept presented in this thesis is another approach to utilize the information of the load to minimize both the inductor core and the output capacitance. A buck
A converter with adaptive core biasing of the magnetic core that reduces the size of reactive components without introducing extra switches, i.e. losses, in the main current conduction path is introduced. The core biasing is performed with an extra winding, by dynamic relocation of the operating point on the B-H curve of the inductor, based on inherently available information in the control loop of a mixed-signal current programmed controller. To minimize the problem of a high reflected voltage, an implementation of the winding based on a simple modification of an E-core based inductor is shown. The experimental results verify that the adaptive biasing system can be implemented with a smaller capacitor and an inductor with a smaller core size than those of the conventional buck converter.

### 7.3 Programmable-Output PFC Rectifier

A single-phase rectifier with power factor correction well suited for emerging applications requiring quickly changing programmable voltage is presented here. The 2-stage solution is a modification of flyback-buck topology where a non-symmetric capacitive divider with practically independent control of two tap voltages is used. The centre tap, i.e. bus voltage, is adaptively regulated such that the efficiency of the downstream stage is optimized. The top capacitor of the divider, with a much smaller value than that of the bottom one, is used to increase current slew rate during transients canceling negative effects of the efficiency optimization. A practically independent regulation of the divider voltages is performed with a single secondary winding, eliminating the need for a custom flyback inductor design, as well as cross-regulation problem existing in two winding solutions. Also, in the thesis a frequency adaptive downstream stage for further improving efficiency of the system is proposed.
7.4 Adaptive Frequency Scaling

An adaptive frequency all-digital controller architecture improving efficiency of dc-dc supplies is presented. The architecture well suited for on-chip integration in the latest CMOS technologies allowing utilization of digital implementation advantages. Depending on the input voltage, the controller adaptively changes the switching frequency reducing losses while minimizing EMI problems related to the variable frequency operation. The key controller element is novel clock divider and spread spectrum generator allowing dual modulation of the clock generator, depending both on the spread spectrum and input voltage requirements. Experimental results prove the effectiveness of the system.

7.5 Future Work

The load interactive converter topologies presented in this thesis can be practically implemented in systems where the information of the load behavior is inherently available. Although in many emerging applications this is the case, a more attractive feature would be to incorporate a prediction or fast transient detection based load interactive current estimation. The core biasing concept to improve the transient response of the converter is successfully demonstrated through the experimental results conducted on a widely used E-Core [42] structure. The primary motivation of these experiments were to proof the concept, rather than addressing practical issues such as power consumption in the bias winding or the optimum core structure to achieve maximum core size reduction. Further research related to this topic would create the opportunity to address those concerns.
References


