ELECTRICAL PROPERTIES AND BAND DIAGRAM OF InSb-InAs NANOWIRE TYPE-III HETEROJUNCTIONS

by

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Abstract

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The electrical properties of nanowire-based $n$-InSb-$n$-InAs heterojunctions grown by chemical beam epitaxy were investigated both theoretically and experimentally. This heterostructure presented a type-III band alignment with the band bendings at 0.12 eV for InAs side and 0.16 – 0.21 eV in InSb. Analysis of the temperature dependent current voltage characteristics showed that the current through the heterojunction is caused mostly by generation-recombination processes in the InSb and at the heterointerface. Due to the partially overlapping valence band of InSb and the conduction band of InAs, the second process was fast and activationless. Theoretical analysis showed that, depending on the heterojunction parameters, the flux of non-equilibrium minority carriers may have a different direction, explaining the experimentally observed non-monotonic coordinate dependence of the electron beam induced current at the vicinity of heterointerface.
Dedication

To My Parents and Eva
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Chapter 1

Introduction

1.1 Overview

Semiconductor materials form the basic constituents of modern integrated circuits. Most of the devices used to process analog signals, perform logic operation and store digital information are made of silicon. Apart from the main stream silicon technology, there is another branch where compound semiconductor homostructures and heterostructures are used for application in interaction with light, high speed devices, and gas sensing. A bird’s eye perspective on the landscape of fabrication, characterization, and potential technological applications is included to serve as an introduction to semiconductor nanowires (NWs).

Examples of light interacting devices are photodiodes and light emitting diodes. Depending on the wavelength, different band gap materials are used such as InGaN for blue and green range [1]. Using semiconductor heterostructures for laser, first proposed by Kroemer [2], allows confinement of carriers which makes room temperature lasing possible. The bandgap of the active region can also be tuned by taking advantage of the quantum size effects in quantum well heterostructures.

Perhaps the most well known heterosystem is the AlGaAs/GaAs heterointerface. The
modulation-doped [3] AlGaAs/GaAs quantum wells have exceptionally high electron mobility at cryogenic temperatures [4]. Applications of such structure include high electron mobility transistors (HEMTs) which is used in radio-frequency (rf) and microwave circuits [5]. Development in GaN HEMT implies it is of high potential for high power rf application [6].

Semiconductor gas sensors, such as SnO$_2$, ZnO, and In$_2$O$_3$ [7, 8, 9], recognize a target gas through a gas-solid interaction which induces an electronic change of oxide surface and transduces the surface phenomenon into an electrical resistance change of the sensor. They can be used in precise and rapid detection, alerting, and monitoring of toxic gases. Depending on the type of target gases and background, the sensitivity of these sensors is typically in the range of parts per million (ppm) [10].

Recent development in growth of semiconductor nanowires through metal-catalyzed vapour-liquid-solid (VLS) method has expanded the catalog of application of compound semiconductors. This method, which was first demonstrated by Wagner and Ellis [11], is noteworthy for their applicability to a wide variety of materials [12], and sophisticated control over geometry, composition and accurate placement of large numbers of nanowires [13].

1.2 Semiconductor Nanowires

Semiconductor nanowires have attracted considerable worldwide research efforts [14]. They are 1-D or quasi 1-D structure if the diameter is small enough. Thus far, researchers have not only demonstrated the above mentioned applications with semiconductor nanowires [14] [15] [16], but also utilized nanowires for quantum computing applications [17]. Approaches to fabricate these nanostructure can be classified into two main categories: “top-down” and “bottom-up”. Nanowires fabricated through top-down method are achieved by etching or oxidizing [18] from a bulk substrate. This method is
similar to the main stream silicon CMOS fabrication technique except the device structures are different. One disadvantage is the surface of semiconductor that often degraded during the wet or dry etching processes. Moreover, doping of nanowires sometimes required ion implantation which can introduce defect into these nanostructures. In this thesis, we will only consider the bottom-up approach.

The bottom-up approach has several advantages which are summarized as followed.

- **No etch damage:** As mentioned previously, top-down approach can introduce defect and surface roughness to the nanowire. This not only affect the lifetime of carriers but also introduce uncertainty to the structure. On the other hand, bottom-up approach does not have this problem. As long as the growth parameters are tuned properly, nanowires can have very smooth surface.

- **Different types of substrate:** Many groups have demonstrated growth of nanowires on different type of substrates. For example, InAs nanowires on GaAs substrates and even on elemental semiconductor substrate such as Silicon and Germanium \cite{19, 20}. Controlled growth of compound semiconductor nanowires on Silicon substrates is extremely attractive for sources and detectors in nanowire-based Silicon-integrated photonics \cite{21}.

- **Controlled size, geometry and location:** The diameter of a nanowire is mostly determined by the size of the gold catalyst. Wu et al. has demonstrated the growth of nanowire with diameter down to as small as 3 nm \cite{22} with an overall length typically ranges from hundreds of nanometers to a few microns. Location of the wire can be controlled in a similar manner since nucleation only occurs at sites of metal catalysts. Thus, one can employ top-down lithographic processes to define the location of catalysts permitting control over the exact location of nanowire growth \cite{23} instead of building devices from randomly dispersed nanostructures.

- **Composition of nanowires:** Different from top-down approach where the com-
position of the wire is pre-determined by the starting material, bottom-up approach allows changes of composition during the growth by simply modulated the precursors. This opens up the possibility to grow both novel radial and axial heterostructure [24]. Doping of nanowires can also be achieved without damaging the nanostructure. Björk et al. [25] has demonstrated the ability to alter between InAs and InP every few tenths of nanometer over the entire nanowire.

- **Greater strain tolerance:** One constraint for growing heterostructure is the lattice mismatch between two materials. In planar structure, the defect-free epitaxial growth can only be achieved between material with similar lattice constant. The GaAs/AlGaAs system only have $\sim 0.1\%$ in lattice mismatch [26]. With lattice mismatch greater than a few %, defects like dislocations and stacking faults will emerge at the vicinity heterointerface which can serve as recombination cites for carriers. On the other hand, nanowire geometry allows greater strain accommodation enabling growth of defect-free heterojunction (HJ) between large lattice mismatch semiconductors [27].

### 1.3 Motivation and Objectives

Among the great variety of semiconductor heterojunctions studied and used in device application, there is a small group of so-called type-III HJs with an unusual band diagram and physical properties. These HJs are formed by a pair of semiconductors with noticeably different electron affinity $\chi$ such that the conduction band of one semiconductor partially overlaps the valence band of the other one. For a long time, this type of HJ, first investigated several decades ago [28], was exemplified by GaSb-InAs, since other possible combinations suffer from strong lattice mismatch, and prevented the realization of sufficient quality material.

Developments in epitaxial growth of nanowires opened up the possibility of expand-
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ing the choice of materials for growing defect-free type-III heterostructures. An example is the InSb-InAs heterostructure with a lattice mismatch $\sim 7\%$. The InSb-InAs system has the smallest bandgap and highest electron mobility among III-V semiconductor compounds and is of potential interest for application in high speed field effect transistors [29, 30], infrared optoelectronic devices [25, 29, 31], resonant tunneling diodes [32], thermoelectric devices [29], microwave [33] and Terahertz (THz) [34] detectors. However, in these studies the basic current mechanisms through this heteropair still remain unexplored.

Thus in this thesis, we collaborate with Laboratorio NEST (National Enterprise for nanoScience and nanoTechnology) to investigate the band structure, the current mechanisms, and minority carriers for this InSb-InAs NW heterojunction.

1.4 Thesis Outline

The thesis is organized into five chapters. Chapter 1 will continue with the necessary background and theory included in this thesis, including the band structure of type-III heterojunction, current voltage relationship, potential in quasi-classical limit, and theory for electron beam induced current. Experimental setups and methods will be introduce in Chapter 2 which goes over the growth of nanowire heterostructure, device fabrication, current voltage characteristic (CVC) and electron beam induced current (EBIC) setup. The theoretical analysis of band structure, experimental CVC result and theoretical treatment of CVC are discussed in Chapter 3. Chapter 4 investigate the properties of minority carriers using technique of EBIC. The temperature dependent carrier diffusion length is also studied. Finally, we summarize main conclusions of this thesis and propose some future works of this project.
1.5 Background

1.5.1 Nanowire Growth - VLS process

Vapor-Liquid-Solid process is one of the most popular processes for nanowire growth according to ISI Web of Knowledge [35]. Among this process, there are different kinds of growing techniques such as chemical vapor deposition [36, 37], laser ablation [38], supercritical fluid solution phase [39], metalorganic chemical vapor deposition [40, 41, 42], molecular beam epitaxy [43, 44], and chemical beam epitaxy (CBE) [45, 46]. Each has its own advantages and disadvantages, but the basic mechanisms are the same. In this section, the basic VLS mechanism will be discussed serving as background for nanowire growth described in Sec. 2.1 where the detail growth condition for InSb-InAs NWs will be introduced.

VLS is a bottom-up approach where precursors in vapor phase incorporated with liquid catalyst nanoparticle, often Au, on a substrate heated to an appropriate temperature. When the liquid catalyst absorbs vapor phase precursors and reaches a supersaturation level, solidification of precursors occurs at interface between the catalyst and the substrate, resulting in nanowire growth. This process is shown schematically as in Figure 1.1 starting with liquid metal droplets exposed to flux of precursors to nanowire growth. Depending on the growing condition and time, the overall length of a nanowire can easily reach hundreds of nanometer to a few micron.

1.5.2 Heterojunction

When two different semiconductor materials are used to form a junction, the junction is so called a semiconductor heterojunction. Before we turn to this topic, let us begin by examining the formation of energy band diagram of a homojunction such as pn junction.

Shown in Figure 1.2 a familiar example of formation of a pn junction. In Figure 1.2a, we begin with a charge neutral p-type semiconductor (left) and another neutral n-type
Figure 1.1: The schematic shows the VLS mechanism for nanowire growth. Starting from left to right, metal droplet sitting on substrate was heated to liquid phase and followed by collection of vapor phase precursors. And finally, when supersaturation level was reached, precipitation of precursors began at interface between catalyst and substrate and hence the nanowire growth.

semiconductor (right). Before they are in contact, there are separate Fermi levels for the $n$- and $p$-type semiconductor. After placing them in contact, electrons flow from the region with higher Fermi level to the region with lower Fermi level. As a result of this flow, a space-charge layer builds up and a built-in potential (band bending) results as depicted in Figure 1.2).

Figure 1.2: Illustration of the formation of a $pn$ junction (a) before contact and (b) after contact

Now, let us consider the case for abrupt heterojunction such that the semiconductor changes abruptly from a narrow-bandgap material to a wide-bandgap material (The
graded heterojunction is beyond the scope of this thesis). In this case, we can have three possible band alignments as shown in Figure 1.3.

![Figure 1.3: Three possible band alignments for heterojunction: (a) straddling (type-I), (b) staggered (type-II), and (c) broken gap (type-III).](image)

In type-I HJ, the band gaps of one material entirely overlaps that of the other. The famous GaAs/AlGaAs heterosystem belongs to this group. The definition for type-II HJ are $E_v^1 > E_v^2$ and $\Delta E_c < E_g^1$. The term $\Delta E_c$ is conduction band offset which is defined as

$$
\Delta E_c = \chi_2 - \chi_1
$$

where $\chi$ is the electron affinity. An example for this type of HJ is InAs/Al$_{0.4}$Ga$_{0.6}$Sb. For the situation of $\Delta E_c > E_g^1$, it represents the band alignment for type-III HJ (some authors have name this type of HJ as type-II misaligned). The InAs/GaSb system is one example for this HJ, and in this thesis, the heterostructure investigated also belongs to this group. A detail type-III heterostructure band diagram before contact is shown in Figure 1.4a. The example shown here is an $nN$ isotype HJ where both semiconductors have $n$-type conductivity. After placing them in contact, similar to $pn$ junction, electrons flow from the semiconductor with higher Fermi level to the one with lower Fermi level (left to right) until a potential barrier for stopping the flow is established. Such band alignment is presented in Figure 1.4b. Because the conduction band of one material lies lower than the valence band of the other one, this interface is sometimes referred
to as semimetalic. The exactly value of the band bending will depend on the material parameters. We will return to this subject for InSb-InAs band alignment in Sec. 3.3 using the theory discussed in Sec. 1.5.3.

The mechanism for carriers to overcome the barrier is a temperature dependent process which is similar to that of a rectifying metal-semiconductor contact or Schottky barrier. Thus, it can be described on the basis of thermionic emission of carriers over the barrier \[ j = A^* T^2 \exp \left( -\frac{\Delta_i}{kT} \right) \] (1.2) where \( A^* \) is the Richardson constant, and \( \Delta_i \) is effective barrier height. The value of effective barrier height can be obtained from temperature dependent current voltage measurement. Even though the exact expression still need to include the effects of diffusion and tunneling as well as the difference in effective mass, the general form of the current voltage relation is still similar to that of a Schottky barrier diode.

1.5.3 Potential in Quasi-classical limit

It is essential to understand the band alignment of a heterojunction before we can investigate the carriers transport behaviour. However, unlike the depletion layers which exist in almost all the HJs and is described by the elementary Schottky model [48], accumulation or inversion layers that may exist in InSb-InAs heterointerface, are treated differently. A theory developed by Shik et al. [49] initially to formulate the accumulation layer in InAs-GaSb heterojunction is adapted here for this thesis.

Let us consider a single electron layer formed by a band bending near semiconductor surface or interface as shown by the yellow shaded area in Figure 1.4b. Such a layer represents a 1-D potential well \( V(z) \) for electrons and the energy spectrum contains both continuous and discrete components,

\[ E = E_i + \frac{p_x^2 + p_y^2}{2m} \] (1.3)
Figure 1.4: Band diagrams of type-III HJ (a) before contact and (b) after contact where \( \zeta \) is the Fermi level.
where \( E_i \) are the energy levels in potential well, \( V(z) \). The layer we assumed here can either be accumulation or inversion. Also, we consider the case as non-heavily doped semiconductor such that the Fermi level, \( \zeta \), in the bulk lies near or below the conduction band edge.

To calculate this layer, one must solve Poisson and Schrödinger equations self-consistently,

\[
\frac{d^2 \tilde{V}}{d\tilde{z}^2} = -4 \sum_{i=1}^{N} (\tilde{\zeta} - \tilde{E}_i) \Theta(\zeta - E_i)|\psi_i|^2; \quad (1.4)
\]

\[
-\frac{1}{2} \frac{d^2 \psi_i}{d\tilde{z}^2} + \tilde{V}\psi_i = \tilde{E}_i \psi_i. \quad (1.5)
\]

If \( V(z) \) is a deep potential well such that the total number of bound states \( N >> 1 \) (quasi-classical limit), then the summation in Eq. 1.4 can be replaced with integral which converts it into the Thomas-Fermi equation,

\[
\frac{d^2 \tilde{V}}{d\tilde{z}^2} = -8\sqrt{2} \frac{\sqrt{\pi}}{3\pi} (\tilde{\zeta} - \tilde{V})^{3/2}. \quad (1.6)
\]

Now if we let the boundary conditions such that the potential at the interface \( V(0) \) and the electric field \( F = \frac{dV}{dz} \) in the point where \( V = \zeta \) (or \( F = \zeta \)) to be some given values, the implicit solution of Eq. 1.6 is given by the expression

\[
\int_{\tilde{\zeta} - \tilde{V}}^{\tilde{\zeta} - V(0)} \frac{du}{\sqrt{\frac{32\sqrt{2}}{15\pi} u^{5/2} + F}\zeta} = \tilde{z}. \quad (1.7)
\]

The theory describe above is used in calculating the band diagram of InSb-InAs NW HJ in Sec. 3.3.
1.5.4 Current Voltage Characteristics for Type-III Heterojunction

For anisotype HJ, CVC is dominated by the generation-recombination processes. However, for system like InAs-GaSb (type-III), these processes may have principal distinction from the ordinary p-n junction or type-I HJ [49]. The most important fact is electrons and holes are not separated by band gap but may coexist at the same energy level. This means generation of electron-hole pairs is an activation-less process and the HJ will not give huge asymmetry in CVC when temperature is lowered.

For the mechanism of current flow in such system, consider some electrons in conduction band of InAs with energy \(0 < E < \Delta E_c - E_{g1}\) where \(E = 0\) corresponds to the band edge. When electrons reach the heterointerface, they can either reflect back or transmit into valence band of GaSb with transmission probability \(T\). If transmission did occur, this process is similar to recombination between an electron in InAs and a hole in GaSb. The transmission probability, \(T\), results from the admixture of electron states to the states of valence band in GaSb, and light hole states to the states of conduction band in InAs where the admixture is proportional to the carrier energy measured from the corresponding band gap. Therefore, transmission probability is a function of \(E\) and will vanish at \(E = 0\) and \(E = \Delta E_c - E_{g1}\). A detail derivation to determine \(T(E)\) quantitatively by solving the exact multi-band quantum mechanical problem in envelope function approximation was given in Ref.[50] and has the following expression

\[
T = 2 \sqrt{\frac{E(\Delta E_c - E_{g1} - E)}{E_{g1}E_{g2}}}. \tag{1.8}
\]

Now we know the transmission probability, the electron flux density from InAs into GaSb, or the interface recombination rate can be calculated [49]

\[
R(E) = \frac{2E^{3/2}(\Delta E_c - E_{g1} - E)^{1/2}m_2}{\pi^2\hbar^3 E_{g1}^{1/2} E_{g2}^{1/2}} \tag{1.9}
\]

At equilibrium, this recombination flux is compensated by a generation process, but
under the condition of applied bias, there will be net current through the heterointerface

\[ j = e \int_0^{\Delta E_c - E_{g1}} R(E) [f_1(E) - f_2(E)] dE, \]

(1.10)

where \( f_i \) is the Fermi function with the chemical potential \( \zeta_i \).

The mechanism for current flow described here is for InAs-GaSb system, but it can also be applied to InSb-InAs HJ (See Sec. 3.5) since these two systems have similar band alignment.

### 1.5.5 Electron Beam Induced Current

Electron beam induced current is a technique stems from scanning electron microscopy which can reveal the built-in potential and extract minority carriers diffusion length, \( L \). This technique can be used in both scanning electron microscope (SEM) and scanning transmission electron microscope (STEM), but due to the difficulty in sample preparation for STEM, EBIC measurements are mostly performed with SEM [51]. To understand the image formation mechanism, we need to first discuss the working principle of SEM. A SEM consists essentially of two cathode ray tubes (CRTs). One CRT controls the focused electron beam to bombard the sample of interest. The effects of this bombardment are sensed by a suitable detector. In the case for regular SEM image, it will be a secondary electron detector. This signal is then fed to the second CRT, or display CRT. Since both CRTs are controlled by a single scan generator, their scans are synchronized and the image of the specimen is built up point by point on display CRT. A schematic of the SEM is shown in Figure [1.5] (Modern SEM might not have the display CRT but the working principle is same).

Similarly, an EBIC image can be constructed by connecting the display CRT to the specimen via a current preamplifier. In this case, the image represents the current collected at each point of the sample. EBIC signal arises only when built-in potential is presented in the sample. When high energy electron beam hits a sample of semiconductor,
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Figure 1.5: Schematic representation of the scanning electron microscope.

electron hole pairs (ehps) may be created. The number of ehps, $N_{ehp}$, created by a single electron with energy $E$ is described by

$$N_{ehp} = \frac{E}{E_{ehp}} \left(1 - \frac{\gamma E_{bs}}{E}\right)$$  \hspace{1cm} (1.11)

where $E_{ehp}$ is the average energy required to create one ehp, $\gamma$ is the backscattering coefficient, and $E_{bs}$ is the mean energy of the backscattered electrons [52]. Typically, this number is in the range of $100 \sim 1000$ [53]. If there is no built-in potential at the vicinity of created ehps, these ehps will recombine and give no EBIC signal. On the other hand, if the ehps are created within the built-in potential ($p$-$n$ junction or Schottky barrier), these ehps will be separated by the electric field and contribute to EBIC signal. For ehps generated near the built-in field, if the diffusion length of minority carriers is large enough to diffuse into the junction, they will contribute to EBIC signal. By measuring the variation of current and the distance from the junction, the property of minority carrier diffusion length can be extracted through the expression [54]

$$I_{EBIC} = I_{max} \exp \left(-\frac{x}{L}\right).$$  \hspace{1cm} (1.12)

We will revisit this subject in Chapter 4 where the EBIC technique is applied to InSb-InAs NW HJ.
Chapter 2

Experimental Methods

This chapter is intended to serve as background for nanowire growth, device fabrication and measurement system setups. In this thesis, the nanowires were grown by our collaborator, Laboratorio NEST, in Pisa, Italy. While the device fabrication and characterization were performed in Centre for Advanced Nanotechnology at University of Toronto.

2.1 Nanowire Growth

InSb-InAs heterojunction nanowires are grown on InAs(111)B through Au-assisted growth with CBE system, Riber Compact-21. Au nanoparticles were realized by thermal dewetting of 0.1 nm thick Au film which was deposited by thermal evaporation in a separate system and then transferred to CBE system [55]. In the CBE chamber, the substrate was heated to 500°C under tertiarybutylarsine (TBA) flow for 20 minutes to remove the surface oxide and dewet the Au film into nanoparticles of diameter around 50 nm.

The InAs segment was grown for 60 minutes at a temperature of 420°C with line pressures of 0.3 and 2.0 Torr for trimethylindium (TMI) and TBA respectively. To initiate growth of InSb segment, the group-V precursor was abruptly switched from
TBA to tert-dimethylaminoantimony (TDMASb) with a line pressure of 1.0 Torr while the TMI flux and substrate temperature remained the same. The InSb segment was grown another 60 minutes before the termination of growth.

InSb-InAs nanowires were characterized by SEM as shown in Figure 2.1a while the chemical composition of both segments, InAs and InSb, were confirmed with energy dispersive X-ray spectroscopy (EDX). From the SEM image, the InSb segment has a slightly larger diameter which maybe due to the change of solubility of Au catalyst when precursor was switched to TDMASb. On average, InAs segment has a diameter of 50 nm and 1 µm in length; while for InSb section, the diameter is 70 nm with an average length of 250 nm.

The crystal structures of nanowire heterostructure were investigated with transmission electron microscope (TEM). High resolution TEM (HRTEM) image shown in Figure 2.1b was obtained along [110] InSb zone axis with the associated fast Fourier transforms (FFT) of region enclosed by white square presented in Figure 2.1c. The FFT indicated that InAs (blue) segment crystallized in wurtzite (WZ) phase and InSb (red) in zincblende (ZB) phase. From the HRTEM analysis, this HJ appeared to be an abrupt junction with a defect-free InSb segment and a few stacking faults in InAs which confirmed the quality of the InSb-InAs nanowire heterostructure.

The InSb-InAs NWs growth and electron microscopy analysis were performed by our collaborators, Dr. Daniele Ercolani et al., from Laboratorio NEST in Pisa, Italy.

2.2 Device Fabrication

2.2.1 Nanowires Transfer

Single InSb-InAs NW devices fabrication start with cutting a small piece of heavily doped p⁺ silicon wafer (approximately 12 mm by 12 mm) with resistivity, ρ, ranges from 0.002 ~ 0.005 Ω cm and capped with 100 nm thick thermally grown SiO₂. The
Figure 2.1: (a) SEM image of InSb-InAs nanowire growth substrate. The bottom segment is InAs and the top segment corresponds to InSb. The scale bar is equal to 1 µm. (b) HRTEM image of the nanowire along [110]_{\text{InSb}} zone axis. (c) The associated FFT of the interfacial region suggesting InAs (blue) crystallized in WZ phase and InSb (red) in ZB phase
Chapter 2. Experimental Methods

A combination of heavily doped Si wafer and dielectric allow us to gate NWs through global backgate. This small piece of wafer, or substrate, was first patterned with electron beam lithography (EBL) system to define metallic markers for positioning the NWs. After the lift-off, the substrate was dipped in N-Methyl-Pyrrolidinone organic stripper at 60°C for 15 minutes. This step was to remove the residual resist from the lift-off step and then followed by immersion in heated (120°C) acetone and isopropanol (IPA) each for 2 minutes. Finally, the substrate was rinsed with de-ionized (DI) water and blown dry with nitrogen. These procedures ensure a clean substrate surface before transferring NWs which is crucial for NW adhesion and performance according to our experience.

After obtaining a clean substrate with metallic markers, NWs transferring was achieved by putting NWs growth sample upside down on the pre-prepared substrate and gently touched the back of growth sample with a tweezers. Depending on the desired density of NWs, the force applied to the back of growth sample may be adjusted. To prevent NWs from moving during spin-coating or handling, the substrate was baked at 120°C for 15 minutes.

2.2.2 Locating Nanowire and Forming Ohmic Contacts

To locate NWs, the substrate was loaded into a EBL system (DSM 940 and RAITH Elphy Plus) and the coordinates of the selected wires were recorded with respect to the pre-defined metallic markers (trilateration). Prior to exposure, the target substrate was removed from EBL chamber and spin-coated with Poly-Methyl-Methacrylate (PMMA)-based resist followed by soft baking at 170°C for 90 seconds. This is to reduce the remaining solvent content in the resist. Depending on the feature size, different thickness of resist was used. In this thesis, I used 200 nm for the sample I fabricated. Sometimes a copolymer underlayer, which provides a retrograde resist profile, was used to enhance the lift-off process. The exposure process was performed with 25 keV electrons and the beam current and spot size are related to the finesse of the structure. During this process,
patterns transferred onto the sample included source/drain electrodes on the top of NWs, the 200 × 200 µm wirebonding pads, and 10 µm wide traces connecting the electrodes and pads. Afterward, sample was developed in methyl-isobutyl-ketone (MIBK) and IPA (1:3) for 40 seconds and was rinsed with IPA to terminate the development. To remove residual resist on exposed regions, the sample was loaded into a homemade oxygen plasma system with the plasma ignited for 10 seconds at 100 mbar of oxygen. This plasma was generated by a commercial McCarroll cavity (Opthos Instruments) operating at 2.45 GHz.

Prior to metal deposition, the native oxide on the exposed region InSb-InAs NWs must be removed in order to ensure good ohmic contacts. This was done by dipping the sample into a solution of DI water and 0.3% by weight of ammonium polysulfide for 8 minutes to remove the oxide and passivate the surface with sulfur atoms. After the passivation, the sample was cleaned with DI water, blown dry and quickly loaded into a home-built thermal e-beam hybrid evaporation system. This system is equipped with thermal source (MDC Vacuum model Re-vap 900) for Au deposition and e-beam sources (Oxford Applied Instruments model EGN4) for Ti deposition. It is also specially designed for high speed pumping and is capable of reaching a vacuum level of $3 \times 10^{-7}$ mbar within 40 minutes which minimized the re-oxidization of the NWs surface. For the metal deposition, a 10 nm Ti was deposited first to ensure good adhesion to SiO$_2$ surface and followed by 120 nm of Au. The final step was lift-off which was performed by immersing the sample in acetone and followed by cleaning processes described in Section 2.2.1. A schematic of the entire processes is shown in Figure 2.2. Figure 2.3c shows the closeup SEM image of one NW device. The InSb and InAs segments are indicated in the image along with the HJ and Au catalyst. Although it is hard to identify, the InSb segment has a slightly larger diameter than InAs segment.
Figure 2.2: This schematic outlines the main steps in device fabrication. Starting from top left to bottom right, InSb-InAs NWs heterostructure was first mechanically transferred onto Si substrate with 100 nm of SiO$_2$ and followed by spin coating of PMMA. The third step indicates the electrodes were defined by EBL system and developed. The NWs were then subject to (NH$_4$)$_2$S$_x$ passivation to remove native oxide and terminate the surface with sulfur atoms. The fifth step was to deposit 10 nm of Ti and 120 nm of Au and finally lift off of unnecessary metal.
2.2.3 Wire Bonding

To make electrical connection between NWs and measurement system, wire bonding was required. The processed sample was first diced into smaller piece for fitting into the chip carrier. The chip carrier used throughout this thesis is 28 pin leadless chip carrier (LCC). LCC is chosen over other conventional package such as dual in-line (DIL) because it is more robust and easier for thermal anchoring in cryogenic application. To secure the sample, indium bonding was applied which is achieved through placing a tiny piece of indium between LCC and back of sample and heated to 160°C. Indium was preferred not only of its electrical conductivity for gating NW devices but also again for its thermal conductivity in low temperature measurement.

Figure 2.3a shows the as fabricated sample with square bonding pads viewed through optical microscope. Wire bonder (KS 4526) was used for connecting gold wire between bonding pads and LCC as shown in Figure 2.3b. To avoid leakage current, often caused by damaging the SiO₂ dielectric layer during bonding process, the proper bonding wedge and parameters were used. Also, the spacing of square bonding pad was specially designed to further minimize this effect.

Once the NW devices were wire bonded, they were subjected to electrostatic discharge (ESD) damage. It is crucial to maintain proper grounding and shielding to protect the devices. This was done by using ESD safe tools when handling with the sample. A conductive box was used for storing the sample.
Figure 2.3: (a) The fabricated device viewed under optical microscope. The scale bar in the image is equal to 200 µm. (b) Sample substrate was attached to LCC and wire bonded. (c) Closeup SEM image of a NW device. The InSb and InAs segments are as indicated along with HJ and Au catalyst. The scale bar is equal to 1 µm.
2.3 Measurement Setup

2.3.1 Current Voltage Characteristic

First part of the measurement involved determining current voltage characteristic of the NW devices. The experiment was performed in a closed cycle He cryostat (Advanced Research System model ARS DE 202) with a temperature range from 10 to 350 K. A temperature controller (LakeShore 330) monitored and adjusted the temperature through a feedback loop between heater and sensor. A special design copper carrier holder, as shown in Figure 2.4a, in conjunction with a copper top plate are used to host and secure the LCC. The whole sample holder is made of oxygen-free copper to maximize thermal conductivity. Twelve twisted pair of wires are used for connection between sample holder and vacuum electrical feedthrough. On the other end of the feedthrough, air side, the cable is connected to a switch box. The purpose of the switch box is to protect the NW devices when they are not connected to measurement circuit or when making adjustment on instruments such as changing the gain on a current preamplifier. Such adjustment, in most of the instruments, will create a sharp voltage peak and can vaporize NW easily. To avoid this issue, NW devices are connected to a 1 MΩ resistor when making these adjustments.

The CVC measurement was performed with Keithley 4200 Semiconductor Characteristic System which can supply voltage with precision of 100 µV and record current in picoamp range. An image of the entire setup is shown in Figure 2.4b. The schematic of the measurement circuit is shown in Figure 2.4c with one end of the NW connected to voltage output and the other end to picoammeter. Depending on the type of measurements, the global back gate is employed where applicable. The entire setup is carefully constructed to minimize the effect of ground loop in order to obtain the cleanest signal.
Figure 2.4: (a) The image shows the copper carrier holder for hosting the LCC with a temperature attached near the sample and (b) instruments used for CVC experiment including cryostat, picoammeter, and switch box. In (c), a schematic of the measurement circuit is shown with one end of the wire connected to voltage supply and the other end to picoammeter.
2.3.2 Electron Beam Induced Current

To investigate the minority carriers and local electrical field distribution near the heterointerface, the technique of EBIC was employed. EBIC is a special technique in electron microscopy and in this case, I used Philips SEM 525 for this part of experiment. Before the actual measurement, a series of upgrades and modification were made to the microscope, such as re-designed sample stage to host LCC and incorporated a home-made liquid nitrogen cryostat for low temperature measurement. The most crucial change was to modify the vacuum system for higher brightness LaB$_6$ cathode instead of tungsten. If the beam current is too small, higher gain will be needed but it will compromise the bandwidth of the current preamplifier. If that was the case, the scan rate will be limited and the issue of sample drifting might arise. Other type of cathode, such as Schottky, gives even higher brightness but it requires ultra high vacuum and different gun geometry.

EBIC setup is composed of a current preamplifier (SR570), a signal buffer, and a switch box similar to the one in CVC setup. Also, an electrical vacuum feedthrough was used for wiring NW devices to current preamplifier. The output of the current preamplifier goes to the signal buffer and is then sent to the scan generator of the SEM. The total capacitance of the measurement circuit is estimated to be $\sim 200$ pF which is low enough for EBIC measurement. A picture of the above described setup is shown in Figure 2.5a and Figure 2.5b. A faraday cup which is used to monitor the beam current is also placed right beside the sample as shown in Figure 2.5c. Accelerating voltage is selected on the basis to prevent charging the SiO$_2$ dielectric layer, and this is possible where electrons has less than $\sim 9$ keV, thus will not have sufficient energy to penetrate through oxide layer. On the other extreme, a too high accelerating voltage might damage the wire. Therefore, the accelerating voltage used in the experiment was set to 10 keV and the setting for beam size was 20 nm in diameter, giving a beam current of 150 pA. The same setting with tungsten filament will only give 30 pA in beam current and larger beam size.
A sample of silicon P-i-N nanowire diode (Figure 2.6a) was loaded into the chamber for testing the EBIC setup before the actual experiment. This top-down NW device was designed to have a junction near the center of the wire. The EBIC image of the device is shown in Figure 2.6c. From the image, the location of the junction is confirmed suggesting the EBIC apparatus is working as expected. Two other NW devices with similar configuration had been tested and gave similar results.
Figure 2.5: The setup of the EBIC apparatus. (a) Electron microscope used in this experiment including the feedthrough, current preamplifier, and signal buffer. Inside the main chamber (b), it shows the copper LCC holder, the cryostat and (c) the closeup picture of the sample holder with a temperature diode placing right beside the sample along with a faraday cup.
Figure 2.6: SEM image (a) of the Si P-i-N nanowire device. In (c), the EBIC image is presented and the white region represents the location of the junction. The zoom-in images are presented in (b) and (d). The twisted look of the NW in (b) is caused by charging due to the thick dielectric layer.
Chapter 3

Current Voltage Characteristic of InSb-InAs Nanowire

3.1 Introduction

As mentioned in Sec. 1.3, the InSb-InAs NW HJ can be a potential candidate for future high speed electronic devices, far-infrared detectors, or even terahertz radiation detectors. However, the basic character of this heteropair still remain unknown and the purpose of this chapter is to resolve its band alignment and current voltage characteristic.

In this chapter, the carrier concentrations in InSb and InAs segments are determined separately to provide necessary data for band diagram calculation. Then the band diagram of this heteropair is discussed in Sec. 3.3. This gives us some important background before we start analyzing the CVC data. Sec. 3.4 gives the experimental data of the CVC measurement and also the calculation for effective barrier height seen by carriers. The CVC is then formulated in Sec. 3.5 in which the mechanisms for current flow are caused mostly by generation-recombination processes in the InSb and at the heterointerface. Because of the partially overlapping valence band of InSb and the conduction band of InAs, the second process is fast and activationless. Sec. 3.6 shows the carrier concentration can
be tuned through gating the wire. In terms of device application, this demonstrates that
the performance of the NW can be adjusted to match the desired application.

3.2 Carrier Density

To begin with, the carrier concentrations in each of the segments, InSb and InAs, were
determined. This was achieved by putting four electrodes on a InSb-InAs HJ NW with
two electrodes on the InSb segment and the remaining two on InAs. A room temperature
field effect transistor (FET) measurement was performed on the InAs segment by mea-
suring the current as a function of gate voltage, $V_{gate}$, at a fix source-drain bias, $V_{SD}$. 
This measurement is shown in Figure 3.1. The measurement reveals a $n$-type conductivity
in InAs segment. The carrier density is then estimated from the total charge, $Q$, in
the InAs segment \[56]: $Q = CV_{th}$, where $C$ is the capacitance and $V_{th}$ is the threshold
voltage. The capacitance has the relation

$$C = \frac{2\pi \varepsilon \varepsilon_o L}{ln(2h/r)}, \quad (3.1)$$

where $\varepsilon$ is dielectric constant, $h$ is the thickness of the SiO$_2$, $L$ is the length, and $r$ is the
radius of the wire. The electron density, $n = Q/(e\pi r^2 L)$ is found to be at the level of
$3 \times 10^{17}$ cm$^{-3}$. This number confirms with most other InAs nanowire reported by other
groups \[57 \ 58\]. During the growth, no intentional doping was carried out. Although
these NWs were not intentionally doped during the growth, this n-type behaviour raised
from surface fixed charges and possible local imbalance in stoichiometry \[59\].

The InSb segment also shows $n$-type behaviour, but similar FET measurement for
this segment gives unwarranted result. This maybe due to the small band gap in InSb
which may result in the contribution of intrinsic carriers to the measured data \[60\]. Thus,
the carrier concentration in InSb segment, estimated with its resistivity 0.2 $\Omega$ cm, has
a value of $n_1 = 10^{16} - 10^{17}$ cm$^{-3}$. From this measurement, both segments show $n$-type
conductivity suggesting an isotype character of the heterojunction.
Figure 3.1: FET measurement for calculating carrier density in InAs segment with a constant source-drain bias of 10 mV at room temperature.

### 3.3 Band diagram

Due to the anomalously high value of the electron affinity in InAs, $\chi_2 = 4.9$ eV, the band diagram of InSb-InAs $n$-$n$ heterojunction has a special form. For InSb, the electron affinity, $\chi_1$, is 4.59 eV and the conduction band offset is $\Delta E_c = \chi_2 - \chi_1 = 0.31$ eV. This exceeds the band gap of InSb, $E_g1 = 0.17$ eV (at $T = 300$ K) and it represents a type-III HJ (or type-II misaligned) where the conduction band of InAs partially overlaps the valence band of InSb as shown in figure 3.2a. In the figure, the valence band of InAs is not shown because it does not participate in carrier transport. In the calculation given below, we measure Fermi level, $\zeta_2$, from the conduction band edge in bulk InAs (that is at $x \to \infty$), and Fermi level in InSb, $\zeta_1$, is measured from the conduction band edge in InSb at $x \to -\infty$. The $x$-axis is directed along the NW with $x = 0$ at the heterointerface. In this notation, both Fermi levels are the constants determined exclusively by the corresponding doping levels.
Calculations of the HJ band diagram require knowledge of the basic parameters of contacting semiconductors, such as band gaps, electron affinities, and carrier effective masses. Such parameters for InSb are well known but those for InAs NWs crystallized in wurtzite phase may differ from corresponding values for bulk InAs which has a zincblende crystalline structure. Unfortunately, there is few information on this account. For instance, the experimental data \[61\] and theoretical calculations \[62\] indicate that the effective mass of electrons in InAs NWs, \(m_{n2}\), is approximately 2 times more than that in bulk InAs, so that in our future calculations we will assume \(m_{n2} = 0.045m_0\). However, for \(\chi_2\), according to Ref. \[63\], no reliable data are available, so that the above-mentioned value from bulk InAs will be used. It is unlikely that the real \(\chi_2\) differs from this value by more than the difference in bandgaps between the zincblende and wurtzite InAs, which, according to different authors \[62\] \[64\] \[65\], lies in the interval 0.04-0.055 eV. Such variations will not undermine the inequality \(\Delta E_c > E_{g1}\), resulting in the type-III band alignment of Figure 3.2 a, and hence all qualitative consideration given below.

The exact shape of the band diagram and the band bendings \(V_1\) and \(V_2\) are determined by three charged layers: (1) the depletion layer of donors in InSb, (2) the electron accumulation layer in InAs, and (3) the hole inversion layer in InSb, if it exists. For calculating the profile of the accumulation layer in the InAs, we use the quasi-classical formula for a degenerate electron gas described in Sec. 1.5.3. Let \(V(x) < 0\) be the electrostatic energy profile for electrons with \(V(x) = 0\) at \(x \rightarrow -\infty\) and \(V(x) = -V_1 - V_2\) at \(x \rightarrow \infty\). If \(x_\zeta\) is the point where the Fermi level \(\zeta_2\) crosses the conduction band edge \((V(x_\zeta) = \zeta_2)\) then for \(0 < x < x_\zeta\) the profile \(V(x)\) is determined from the equation

\[
\int_{\zeta_2 - V}^{\zeta_2 + V_2} \frac{du}{\sqrt{\frac{32\sqrt{2}e^2m_{n2}^{3/2}}{15\pi\hbar^3\varepsilon_2} u^{5/2} + e^2E^2(x_\zeta)}} = x.
\]

(3.2)

Here \(\varepsilon_2\) and \(m_{n2}\) are the dielectric constant and the electron effective mass in InAs, \(E(x) = -\frac{1}{e} \frac{dV}{dx}\) is the local contact electric field. For the electric field at the interface,
Figure 3.2: The band diagram of InSb-InAs type-III heterojunction (a) in equilibrium, (b) at reverse bias, and (c) at forward bias. The x axis is directed along the NW with \( x = 0 \) at the heterointerface. The dashed areas show the accumulation layer in InAs and the inversion layer in InSb (if it exists). The valence band of InAs, not participating in the carrier transport, is not shown.
Chapter 3. Current Voltage Characteristic of InSb-InAs Nanowire

$E_2(0)$, Eq. (3.2) gives:

$$E_2(0) = \sqrt{\frac{32\sqrt{2}m_{n2}^{3/2}}{15\pi\hbar^2\varepsilon_2}} (V_2 + \zeta_2)^{5/2} + E^2(x_\zeta). \quad (3.3)$$

If $\zeta_2 \approx 0$, so that $x_\zeta \to \infty$ and $E(x_\zeta) \to 0$, Eq. (3.2) simplifies and gives the explicit formula for $V(x)$ at $x > 0$:

$$V(x) = -\left[ V_2^{-1/4} + x \sqrt{\frac{2\sqrt{2}e^2m_{n2}^{3/2}}{15\pi\hbar^2\varepsilon_2}} \right]^{-4}. \quad (3.4)$$

The doping level of the InAs $n_2 \approx 3 \times 10^{17}$ cm$^{-3}$ (see Sec. 3.2) has the same order of magnitude as the effective density of states in the conduction band of InAs at room temperature ($8.7 \times 10^{16}$ cm$^{-3}$ [66]), so that the assumption $\zeta_2 \approx 0$ seems quite reasonable.

Now let us consider the potential profile in InSb. In our energy scale, the edge of InSb valence band at the interface is $\Delta E_c - E_{g1} - V_2$. Then at $\zeta_2 > \Delta E_c - E_{g1} - V_2$ the inversion layer in InSb is absent and the whole contact potential, $V_1$, drops at the depletion layer creating the electric field $E_1(0) = \frac{2\sqrt{2}\pi n_1 V_1}{\sqrt{\varepsilon_1}}$ at the interface where $n_1$ and $\varepsilon_1$ are the doping level and the dielectric constant in InSb. At $\zeta_2 < \Delta E_c - E_{g1} - V_2$ the energy differences at the depletion and inversion layers are, respectively, $\zeta_2 - \Delta E_c + E_{g1} + V_1 + V_2$ and $\Delta E_c - E_{g1} - \zeta_2 - V_2$. The potential profile in the inversion layer can be described by a formula similar to Eq. (3.2) with $m_{n2}$ replaced by the effective mass of holes in InSb $m_{p1}$, corresponding changes of the integration limits, and $E(x_\zeta)$ replaced by the field of depletion layer $\frac{2\sqrt{2}\pi n_1(\zeta_2 - \Delta E_c + E_{g1} + V_1 + V_2)}{\sqrt{\varepsilon_1}}$. This finally gives the surface electric field in InSb $E_1(0)$, which, together with Eq. (3.3) and the continuity of electric induction, gives the basic equation

$$\frac{\varepsilon_2}{\varepsilon_1} \left( \frac{m_{n2}}{m_{p1}} \right)^{3/2} V_2^{5/2} = \left( \Delta E_c - E_{g1} - V_2 - \zeta_2 \right)^{5/2} \Theta (\Delta E_c - E_{g1} - V_2 - \zeta_2)$$

$$+ \frac{15\pi^2 n_1}{4\sqrt{2}m_{p1}^{3/2}} \min \left\{ V_1; V_1 + V_2 + \zeta_2 - \Delta E_c + E_{g1} \right\} \quad (3.5)$$

where $\Theta(x)$ is the unit step function. Along with the condition of equilibrium

$$V_1 + V_2 = \Delta E_c + \zeta_1 - \zeta_2, \quad (3.6)$$
Eq. (3.5) allows us to determinate of the values $V_1$, $V_2$ and hence the whole band diagram of the HJ.

We can calculate the equilibrium HJ band diagram at the room temperature for two different values of $n_1$, $10^{16}$ and $10^{17}$ cm$^{-3}$, with the parameters characterizing InSb and InAs, $E_{g1} = 0.17$ eV, $\Delta E_c = 0.31$ eV, $m_{p1} = 0.43m_0$, $m_{n2} = 0.045m_0$, $\varepsilon_1 = 17.9$, $\varepsilon_2 = 14.6$ and assuming $n_2 = 3 \times 10^{17}$ cm$^{-3}$. From Eqs. (3.5) and (3.6) we get the values of the band bendings which are shown in Table 3.1. It can be seen that in both cases, an inversion layer in the InSb does present. Due to the high density of states in this layer, the change in $n_1$ and hence in $\zeta_1$, causes a noticeable variation of $V_1$, but the influence on band bending in InAs, $V_2$, is much smaller.

Table 3.1: Corresponding values of band bending for two different electron concentrations in InSb.

<table>
<thead>
<tr>
<th>$n_1$ (cm$^{-3}$)</th>
<th>$V_1$ (eV)</th>
<th>$V_2$ (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$10^{16}$</td>
<td>0.16</td>
<td>0.11</td>
</tr>
<tr>
<td>$10^{17}$</td>
<td>0.21</td>
<td>0.12</td>
</tr>
</tbody>
</table>

3.4 Experimental CVC

Despite the isotype character, the CVC of InSb-InAs nanowire still had an asymmetric rectifying behaviour. Figure 3.3a shows the CVC of the device from 170 K to 250 K. Even though the terms “forward” and “reverse” bias are not as straightforward as for an anisotype junction, let us still use them assuming by “forward” the voltage polarity corresponding to lower differential resistance of the heterojunction. In our case, this is realized by applying positive potential to the InAs segment. From the figure, the CVC become linear at large positive bias with differential resistance $R_0 \simeq 180$ kΩ which is almost independent of temperature and is characterizing the resistance of the NW
outside the heterojunction. After subtracting the voltage drop at $R_0$, we can obtain the characteristic of the heterojunction itself which is shown in Figure 3.3b.

To determine the potential barriers in the HJ, the main mechanisms for overcoming them, and the evolution of the band diagram with applied bias, we measured the temperature dependence of the current at each CVC point from 170 K to 250 K, and found the corresponding effective activation energy as present in Figure 3.4. Arrhenius relation $j \sim \exp \left( -\frac{\Delta^+}{kT} \right)$ similar to Eq. 1.2 is used for extracting the activation energy. The term $T^2$ is dropped here because the exact mechanisms for overcoming the barrier may not have $T^2$ relation. A separated construction of the activation energy plot with $T^2$ term included (data not shown) also gives similar result. Figure 3.4b gives the example of obtaining each point on the plot at selected applied voltages.

The basic experimental dependencies of the CVC revealed by Figure 3.4a can be summarized as follows.

1. The CVC is strongly asymmetric with the lower resistance (forward) branch corresponding to a positive voltage on the InAs.

2. The mechanism for overcoming the barriers is temperature dependent with activation energy being maximal at $U \simeq 0$.

3. At negative bias, $U < -0.2V$, the CVC saturates and has the activation energy of $\simeq 0.14$ eV.

4. Finally, at positive bias, $U > 0.1V$, the CVC can be approximated by the expression $j \sim \exp \left( -\frac{\Delta^+}{kT} \right) \exp \left( \frac{eU}{\eta kT} \right)$ with the activation energy $\Delta^+ \simeq 0.2$ eV and the “non-ideality coefficient”, $\eta \simeq 5$. The non-ideality coefficient is obtained from the inverse of the slope indicated in Figure 3.4a.
Figure 3.3: CVC of the InSb-InAs HJ (a) before the correction from 170K to 250K and (b) after subtracting the voltage drop, R₀
Figure 3.4: (a) The voltage dependence of the effective activation energy of current. (b) Examples of obtaining each point on the plot at selected applied voltages.
3.5 Theoretical CVC

The current through the HJ discussed in previous section is now discussed theoretically as a function of the applied bias $U$ (where $U > 0$ corresponds to the positive potential applied to InAs segment). Since both semiconductors have n-type conductivity, there is always the possibility of a monopolar drift-diffusion current provided by electrons overcoming the potential barrier in the conduction band equal to $V_1$ for the forward bias and $\Delta E_c - V_2$ for the reverse bias. However, for the band diagram of Figure 3.2a containing the contact between accumulation and inversion layers at the HJ, there is also a possible alternative current mechanism including two consecutive generation-recombination processes. One of which occurs at the heterointerface and the other in the space charge layer or the quasineutral region of InSb.

To estimate the relative role of these two mechanisms and find the correct expression for the whole CVC, we characterize the biased HJ by three chemical potential quasi-levels: $\zeta_1$ and $\zeta_2$ describing electrons in InSb and InAs respectively and $\zeta_3$ describing holes in InSb, if an inversion layer exists. The first two levels are coupled by the requirement $\zeta_1 - \zeta_2 = eU$. If the current through the HJ has a monopolar character, then the generation-recombination current through the interface is negligible and quasi-levels of the inversion and accumulation layers coincide, which in our notations means $\zeta_2 = \zeta_3 + \Delta E_c - V_1 - V_2$. In this case, the band diagram of the biased HJ is described with the same equations, Eqs. (3.5) and (3.6), where in the right side of Eq. (3.6), the term $-eU$ should be added. As indicated in Sec. 3.3 due to the high density of states in the accumulation layer, the band bending $V_2$ is practically independent of $\zeta_1$ or, in our case, of the applied voltage $U$. This is why the biased band diagrams, shown in Figure 3.2(b) and 3.2(c), have identical band bending in $V_2$ as in Figure 3.2(a). It means that the forward branch of the CVC should have the character of $\exp \left( \frac{eU}{kT} \right) - 1$ while the reverse one saturates and has a temperature dependence with activation energy $\simeq 0.2$ eV. However, both of these features contradict with the experimental data described in section 3.4, which indicates that the
current through the HJ is governed, to a great extent, by the generation-recombination processes.

Thus for \( U < 0 \), we have the following current mechanism. The interband thermal generation creates electron-hole pairs in the InSb, which are separated by the contact electric field. Electrons go to the external contact, while holes approach the heterointerface and recombine with the electrons coming from the bulk of the InAs and providing the continuity of current in the circuit. For \( U > 0 \), the recombination and generation processes change places. The volume and interface generation-recombination act in series and should be characterized by the same resulting current, \( j \). This condition of current continuity determines the value of the quasi-level, \( \zeta_3 \).

For a more detailed analysis, we describe the volume recombination in terms of a single recombination level with binding energy \( E_i \), concentration \( M \) and capture coefficients \( \gamma_n, \gamma_p \), so that the corresponding current density is given by the classical Sah-Noyce-Shockley model [67]:

\[
j = \gamma_n \gamma_p M N_c N_e \exp \left( -\frac{E_{g1}}{kT} \right) \left[ \exp \left( \frac{\zeta_1 - \zeta_3}{kT} \right) - 1 \right] \times \int dx \frac{\gamma_p N_e \left[ \exp \left( \frac{V^*(x) - \zeta_3 - E_{g2}}{kT} \right) + \exp \left( \frac{E_{g2} - E_{g1}}{kT} \right) \right] + \gamma_n N_c \left[ \exp \left( \frac{\zeta_1 - V^*(x)}{kT} \right) + \exp \left( \frac{-E_{g1}}{kT} \right) \right]}{\gamma_p N_e \left[ \exp \left( \frac{V^*(x) - \zeta_3 - E_{g2}}{kT} \right) + \exp \left( \frac{E_{g2} - E_{g1}}{kT} \right) \right]} \right]
\]

where \( V^*(x) = V(x) + V_1 + V_2 \) is the potential profile in InSb. In contrast to the equation for a simple p-n junction, the quasi-level \( \zeta_3 \) in equation (3.7) is not equal to \( \zeta_1 - eU \) but should be determined self-consistently. The theoretical expression for the generation-recombination current at the type-III heterojunction derived in Sec. 1.5.4 can be written in the form

\[
j = \frac{e(\Delta E_c - E_{g1})^3 m_n}{8\pi \hbar^3 (E_{g1} E_{g2})^{3/2}} F(\zeta_2, \zeta_3)
\]

where the function \( F \) vanishes at \( \zeta_2 = \zeta_3 \) and tends to \( \pm 1 \) at large \( |\zeta_2 - \zeta_3| \). For the InSb-InAs system, the prefactor before \( F \) is on the order of \( 10^7 \) A/cm\(^2\). The expressions, equation (3.7) and (3.8), determine the unknown values of \( \zeta_3 \) and \( j \) (that is the CVC).
For large negative $U$, by analogy with the theory of $p$-$n$ junctions, we can neglect the first terms in square brackets in the denominator of Eq. 3.7 describing the concentration of free electrons and holes, which makes the integrand independent of the unknown potential profile $V^*(x)$. The resulting expression for $j$ contains an exponentially small activation factor and is less than the prefactor before $F$ in Eq. 3.8. This means that $F(\zeta_2, \zeta_3) \ll 1$, which can only be realized at very small $\zeta_2 - \zeta_3$. This allows us to replace $\zeta_3$ in Eq. (3.7) by $\zeta_2 - \Delta E_c + V_1 + V_2$, so that $\exp\left(\frac{\zeta_1 - \zeta_4}{kT}\right)$ in Eq. (3.7) becomes equal to $\exp\left(\frac{eU}{kT}\right)$, and can be neglected. As a result, for large reverse bias we obtain the same result as for a homojunction in InSb: the current saturates at the value

$$j_s \propto \exp\left[-\frac{\max\{E_i; E_{g1} - E_i\}}{kT}\right]$$

having activation energy in the interval $\{E_{g1}/2; E_{g1}\}$ depending on the position of the recombination centers in the bandgap. The experimental value of 0.14 eV (see Sec. 3.4) belongs exactly to this interval.

For very small $|U|$, the numerator in Eq. (3.7) is proportional to $\zeta_1 - \zeta_3$ while in the denominator we can assume $\zeta_1 = \zeta_3$ and use for $V^*(x)$ the equilibrium expression obtained in Section 3.3. The presence of the earlier ignored coordinate-dependent terms describing free carriers in the denominator of Eq. (3.7) changes the temperature dependence of the current, as compared to Eq. (3.9). To elucidate the character of this change, we perform numerical calculations on Eq. (3.7) assuming $\gamma_p N_v \simeq \gamma_n N_c$. The main contribution to the integral is given by those $x$ where the Fermi level is close to the midgap, that is in the depletion layer, which makes the exact shape of the inversion layer irrelevant and allows us to replace $V(x)$ by the quadratic Schottky potential. The results for $V_1 = 1.2E_{g1}$ (which for InSb corresponds to $V_1 = 0.21$ eV given in Table 3.1) and two different $E_i$ are given in Fig. 3.5. It is seen that the observed activation energy (the slope of the curves) for $U \simeq 0$ is larger than that for the saturation current at large negative $U$ (Eq. (3.9)), in agreement with the experimental data of Fig. 3.3. A qualitative explanation of this change in the activation energy is most clear for $E_i = E_{g1}/2$. In this symmetric case, the
Figure 3.5: Temperature dependence of the generation-recombination current at zero bias (1) and large reverse bias (2). Solid curves correspond to $E_i = 0.5E_{g1}$, dashed curves to $E_i = 0.4E_{g1}$.
activation energy for reverse bias (see Eq. (3.3)) is $E_g/2$. At the same time, the free-carrier terms in the denominator of Eq. (3.7), which were ignored for reverse bias but become important at $U \simeq 0$, are different for electrons and holes, and bring asymmetry similar to the deviation of $E_i$ from $E_g/2$, and cause an increase in the effective activation energy of the current.

For positive $U$, the total contact potential $V_1 + V_2$ will decreases with $U$ in accordance with the law $V_1 + V_2 = \Delta E_c - eU$ (see Eq. (3.6)). If $V_2$ remains almost independent of $U$ and $\zeta_3$ coincides with $\zeta_2$, then Eq. (3.7) gives the the standard Sah-Noyce-Shockley CVC with the “non-ideality coefficient” $\eta = 2$: $j \propto \exp \left( -\frac{eU}{2kT} \right)$. Normally, non-ideality factors between 1 and 2 are results of competition between carrier drift-diffusion and generation recombination processes. Larger values of $\eta$ observed experimentally could be attributed to three factors missed in our calculations. Firstly, calculations show that at positive $U$ the inversion layer in InSb disappears, and the accumulation layer in InAs with its much lower density of states (due to $m_n \ll m_p$) can no longer provide pinning the Fermi level, so that the voltage drop $U$ will be divided between $V_1$ and $V_2$. Secondly, the dependence of the surface generation Eq. (3.8) on the difference $\zeta_3 - \zeta_2$ is rather weak and, to provide equality of this expression to the exponentially growing Eq. (3.7), $\zeta_3$ may become to differ noticeably from $\zeta_2$ thus making the difference $\zeta_1 - \zeta_3$ in Eq. (3.7) less than $eU$. Thirdly, the barriers for recombining carriers, described by the coordinate-dependent terms in Eq. (3.7), can be partially overcome by tunneling, especially by electrons with their very small effective mass ($m_n \approx 0.014m_0$). In fact, researchers have reported $\eta = 5 \sim 7$ in devices with trap-assisted tunneling and carrier leakage \cite{68, 69, 70, 71}. All these factors weaken the $j$ vs $U$ dependence, increasing $\eta$. 
3.6 Back Gate

As shown in Figure 2.4c, the NW device has a global back gate which allows us to control the carrier concentration in the wire. In terms of device application, this provide an extra parameter for tuning the characteristic. Figure 3.6a shows how the breakdown voltages were shifted for different gate biases, $V_{bg}$, at 300 K. In each set of the measurement, the data have been slightly shifted ($+1 \mu A$) in such a way that the breakdown is represented by the downward spikes. The possibility to control the breakdown voltages can represent a useful tool to improve the diode efficiency in rectifying electrical signals with large intensities.

An activation energy plot similar to Figure 3.4 has been constructed and is shown in Figure 3.6b. In this case, the bias voltage was held constant at 0.1 V (applied to InAs segment) with the gate bias swept from -6 V to +6 V and temperature from 170 K to 250 K. From the plot, the activation energy is 0.2 eV at zero gate bias which coincides the data in Sec. 3.4 confirming the reliability of the measurement. As the gate bias move toward negative potential, electrons are depleted from InSb-InAs HJ and thus increased in the activation energy. On the other extreme, the activation energy can be lower by populating the structure with electron with positive gate bias.
Figure 3.6: (a) The CVC measurement at different gate biases for $T = 300$ K. The data have been shifted by $+1 \mu A$ in order to show the breakdown voltages which are represented by the downward spikes. (b) Activation energy plot versus the gate bias.
3.7 Conclusion

Current voltage characteristic of a InSb-InAs NW HJ is investigated thoroughly by extracting firstly the carrier density in each of the segment. The values turn out to be a $n$-$n$ isotype HJ with $3 \times 10^{17}$ cm$^{-3}$ in InAs and $10^{16} - 10^{17}$ cm$^{-3}$ in InSb. With these data, the band diagram is then discussed in detail to show that this heteropair represents a type-III alignment as well as the existence of an inversion layer of hole near the heterointerface and the amount of band bending ranging from $0.16 - 0.21$ eV. Experimental CVC data shows the mechanism for overcoming the barrier is temperature dependent with the maximum activation energy equals to $\sim 0.2$ eV. A detail analysis of the CVC suggests that the current through the HJ, to a great extent, is governed by the generation-recombination processes. One of which is in the InSb and the second one is at the heterointerface which is fast and activationless. The non-ideality factor was expected to be 2 but the experimental data gives a value of 5. There are a few possibilities of this deviation such as the tunneling through the barrier, unpinning of Fermi level, and surface generation. Lastly, a gated CVC measured was performed to show the ability to tune the breakdown region of the device showing a potential for application in different field.
Chapter 4

Electron Beam Induced Current on InSb-InAs Nanowire

4.1 Introduction

Carrier diffusion length and lifetime are two important parameters that tell us the quality of the diode. One way to extract these parameters is through the technique of electron beam induced current. Compare to other techniques, EBIC offer the best resolution which is desired for investigating structure like nanowire \(^{72}\). Moreover, through this technique, the exact location of the built-in electric field can be revealed. This is a crucial information since we can place local side gate right beside the heterointerface to couple radiation into the wire \(^{73}\).

The setup of this technique is described in detail in Sec. 2.3.2 and the experimental results (Sec. 4.3) give an unusual EBIC profile which has never been reported before. This interesting phenomenon is associated with motion of minority carriers and we come up with a theory to formulate these carriers in Sec. 4.4. The conventional EBIC theory assumes the generation volume is greater than the diffusion length. However, for the case of nanowire, the generation volume will be close to the size of beam size and we take
Chapter 4. Electron Beam Induced Current on InSb-InAs Nanowire

this into account and derived new theory for nanostructures in Sec. 4.5. To start, we will begin with data processing techniques (Chapter 4.2) to obtain the cleanest EBIC signal before further analysis.

4.2 Data Processing

Among all different types of noise, ground loop is one of the most notorious noise for high sensitivity measurement. For EBIC measurement, most of the high frequency noise will be filtered by the current preamplifier because of its low bandwidth \( \sim 1 \text{ kHz} \) (for 1 nA/V gain setting). On the other hand, the frequency for ground loop noise is only at 60 Hz or the resonance of it which will be picked up and amplified. One way to solve this problem is through isolating the entire measurement system like what we did for the CVC setup. However, the case for EBIC setup is somewhat different. The EBIC apparatus cannot be isolated from SEM since the output of current preamplifier is fed to the scan generator in order to create EBIC image. Thus, one must troubleshoot the entire microscope in order to remove the ground loop.

Another way to bypass this issue is through data processing. An EBIC image with ground loop noise is shown in Figure 4.1a. The periodic strips across the entire image are caused by ground loop. Fortunately, since they have periodic nature, we can perform a Fast Fourier Transform (FFT) as shown in Figure 4.1b to remove the 60 Hz noise and all its resonance by blocking the vertical straight lines. Once all the lines are removed, another FFT will restore the image without ground loop noise as shown in Figure 4.2b. Similarly, the line scan profile of EBIC signal, which is recorded by oscilloscope for higher resolution, is also treated with this method to remove all the ground loop noises.
Figure 4.1: (a) The EBIC image of the InSb-InAs NW HJ with noise caused by ground loop and (b) its corresponding FFT.
4.3 EBIC Experiment

The same InSb-InAs NW device, in which the CVC measurement was performed, was then investigated using EBIC technique. Figure 4.2b shows the EBIC image of this NW device at 100 K without external bias. Room temperature image was also obtained but the image quality is much better in terms of signal contrast at lower temperature. This maybe due to the reduction in penetration depth at lower temperature which allows a single primary electron to generate more electron hole pairs within the wire.

To show the relative location of the heterointerface, the SEM image of the device is given again in Figure 4.2a which was taken simultaneously with EBIC image. A higher resolution SEM image taken with S-4500 (Figure 2.3) shows the change in nanowire diameter clearly which corresponds to the location of heterointerface. Thus, by comparing these images, it is easy to notice that the current reaches its maximum near the heterojunction.

Line scans of EBIC signal along the NW are depicted in Figure 4.3 for both 100 K and 300 K measurements. From the EBIC image, the two contacts, top (bright - positive current) and bottom (dark - negative current), can be seen clearly. This contrast on the electrodes arises from the direct absorption of the primary electron beam and their consequent current generation. Sometimes, is is called resistive EBIC (REBIC) [74]. In our setup, when electrons reach the current preamplifier via the lower electrode, contrast will be dark and bright for carriers reaching the amplifier through upper electrode. The REBIC current is only a fraction of the beam current (150 pA) which is shown by the horizontal dashed lines in Figure 4.3. This fraction, collected by the upper electrode, is in the range of 30 ~ 40%. For the lower electrode, the contact peak is partially overlapped with the signal from the NW and cannot be measured separately. However, it is still in a good agreement with the results of 2-D Monte-Carlo simulation using the Casino v3.2 program [75], confirming that the contacts of our composition and thickness absorb most of the 10 keV electrons. A capture of the simulation is shown in Figure 4.4.
Figure 4.2: (a) Secondary electron image of the InSb-InAs NW device and (b) its EBIC image at 100 K. The scale bar in both pictures is equal to 1 micron. The dashed coordinate axis shows the direction of scan resulting in the EBIC profile.
Figure 4.3: Line scans of NW at 100 K and 300 K. $x = 0$ corresponds to the InSb-InAs interface. Horizontal dashed lines give for comparison the current in the electron beam.
When the electron beam is focused on the NW, only a minor part of the beam current is absorbed by the NW. Most of the electrons just penetrate through the wire and oxide into Si substrate. The large EBIC signal for $-0.2 \mu m < x < 0.9 \mu m$, in some regions even exceeding the beam current, is explained only by the multiple electron-hole pair generation by high energy electrons, which is typically characterized by the quantum yield of $100 \sim 1000$ per primary electron in conventional structure [53]. In nanowire, primary electrons will just penetrate the structure resulting in a much lower quantum yield. The most remarkable EBIC feature, seen directly in Figure 4.3, is the change of signal sign in the vicinity of the junction, in contrast to EBIC in homo- and most heterojunctions, where the properties of EBIC are described by the simple theory of a photodiode (see, e.g., Holt and Joy [76]). The latter predicts that the current always has the same sign, corresponding to the reverse current of the junction, and its dependence on the beam position is a single-maximum curve with the width equal to the sum of the minority carrier diffusion lengths in $n$- and $p$- regions. An example will be the test sample depicted in Figure 2.6c. In a double heterostructure, a non-monotonic EBIC profile was reported by A. Gustafsson et al. [77] but no sign change was observed. This phenomenon also showed up in the EBIC images of two other InSb-InAs NW devices. The unusual properties of the InSb-InAs NW heterojunction are connected with the specific band diagram of this system as mentioned in previously.

4.4 EBIC Theory

To understand this unusual phenomena of the EBIC profile, we will have to look into the behaviour of minority carriers in more detail. To start, we will discuss non-equilibrium phenomena including the interband photocurrent and EBIC in the InSb-InAs NW HJ with the band diagram shown in Fig. 3.2a. Characteristic features of these phenomena caused by generation of electron-hole pairs followed by their separation in the contact
Figure 4.4: Monte-Carlo simulation of the 10 keV electron beam penetrating the layer composites in our device structure. Most of the primary electrons stop within the gold layer confirming the contact peaks in EBIC line scan profile is direct absorption of electron beam.

field, are governed by the behaviour of the minority carriers (holes).

Let us begin with the properties of non-equilibrium holes in InAs. Contrary to the case for the depletion layers, where the diffusion drift motion of minority carriers is always directed towards the contact, such motion in the accumulation layers may have a different direction, as determined by the two competing factors. On the one hand, the InSb valence band represents a potential well for the holes in the InAs and thus attracts them. On the other hand, to be captured by this well or to recombine at the interface, holes should overcome the repulsive electric field forming from the potential barrier $V_2$. To find the resulting distribution of the hole concentration $p(x)$ in the InAs (at $x > 0$) and the current of non-equilibrium holes, we must solve the continuity equation for holes, containing the terms describing drift in the electric field, $E(x) = -\frac{1}{e} \frac{dV}{dx}$, recombination, and diffusion. For $V(x)$ given by Eq. 3.4, as well as for other potential profiles except for the unrealistic case $E = \text{const}(x)$, this problem cannot be solved analytically. However,
accumulation layers with their high carrier concentration have a rather small width \( l \), satisfying the condition \( l \ll L_{\nu 2} \) where \( L_{\nu 2} = \sqrt{D_{\nu 2}\tau_{\nu 2}} \) is the diffusion length, \( D_{\nu 2} \) is the diffusion coefficient, and \( \tau_{\nu 2} \) is the lifetime of holes in InAs. This allows us to ignore recombination processes at \( 0 < x < l \) which reduces the continuity equation in this region to the requirement of current continuity: 
\[
-eD_{\nu 2} \frac{dp(x)}{dx} + \frac{dp(x)}{dx} = j = \text{const}(x).
\]
The general solution of this differential equation is
\[
p(x) = \begin{cases} 
C - \frac{j}{eD_{\nu 2}} \int_0^x \exp \left[ \frac{V(x') - V_2}{kT} \right] dx' \exp \left[ \frac{V_2 - V(x)}{kT} \right] & \text{for } 0 < x < l \end{cases}
\]
(4.1)

From the boundary condition \( p(0) = 0 \) corresponding to a fast drop of the holes reaching the interface into the potential well in the InSb valence band, we get \( C = 0 \). By differentiating Eq. (4.1) and assuming \( x = l \) where \( l \) is the border of space charge region \( (V(l) = 0) \), we obtain the relationship between \( p \) and \( \frac{dp}{dx} \) at \( x = l \). For \( V_2 \gg kT \) the main contribution to the integral in Eq. (4.1) is given by small \( x \) where \( V(x) \simeq V_2 - eE_2(0)x \) with \( E_2(0) = -\frac{1}{e} \frac{dv}{dx}(0) \) being the electric field at the interface. This finally gives
\[
p(l) = \frac{kT}{eE_2(0)} \exp \left( \frac{V_2}{kT} \right) \frac{dp}{dx}(l).
\]
(4.2)

We note that our calculations and their final result Eq. (4.2) are valid for an arbitrary \( V(x) \) and not restricted to the particular quasiclassical expression Eq. (3.4).

Outside the space charge region, at \( x > l \), the motion of non-equilibrium holes has a purely diffusive character and \( p(x) \sim \exp \left( \pm \frac{x}{L_{\nu 2}} \right) \). In our case \( l \ll L_{\nu 2} \) we can replace \( l \) in Eq. (4.2) by 0 and consider this condition as the boundary condition to the diffusion equation. If the non-equilibrium holes are created by light with the uniform generation rate \( G \), then the corresponding distribution of the hole concentration is
\[
p(x) = G\tau_{\nu 2} \left[ 1 - \frac{\exp \left( -\frac{x}{L_{\nu 2}} \right)}{1 + \frac{kT}{eE_2(0)L_{\nu 2}} \exp \left( \frac{V_2}{kT} \right)} \right].
\]
(4.3)

This expression can be used for theoretical analysis of photoelectric phenomena in our HJ.
The situation is different under conditions of EBIC when the carrier generation occurs in a narrow region determined by the diameter of electron beam, which is typically much less than \( L_{p2} \), so that we can write the generation term in the form \( G(x) = g\delta(x - x_0) \). In this case the general solution in the region \( 0 < x < x_0 \) is \( p(x) = A\exp\left(\frac{x}{L_{p2}}\right) + B\exp\left(-\frac{x}{L_{p2}}\right) \) and in the region \( x > x_0 \), \( p(x) = C\exp\left(-\frac{x}{L_{p2}}\right) \). The matching conditions at \( x = x_0 \) represent the continuity of \( p(x) \) and the continuity of hole flux given by \( A\exp\left(\frac{x_0}{L_{p2}}\right) + (C - B)\exp\left(-\frac{x_0}{L_{p2}}\right) = \frac{g_{p2}}{D_{p2}} \). Together with the condition Eq. (4.2) at \( x = 0 \), this gives the photocurrent density in the external circuit, computed as the difference of hole fluxes right and left from the plane \( x = x_0 \):

\[
\begin{align*}
    j_p &= -eg\exp\left(\frac{V_2}{kT}\right) - \frac{eE_2(0)L_{p2}}{kT} \exp\left(-\frac{2x_0}{L_{p2}}\right) \\
    \text{Eq. (4.4)}
\end{align*}
\]

As in Sec. 3.5, a positive sign of \( j_p \) corresponds to the motion of holes from right to left in Fig. 3.2a. It is seen that the EBIC may have different sign depending on the relationship between the parameters \( V_2 \) and \( E_2(0) \), characterizing the accumulation layer, and the diffusion length \( L_{p2} \). For the particular model case of triangular potential \( V(x) \) a similar result has been earlier obtained in [78]. It differs from Eq. (4.4) by terms of the order 

\[
\frac{kT}{eE_2(0)L_{p2}} < \frac{V_2}{eE_2(0)L_{p2}} = \frac{l}{L_{p2}} \ll 1.
\]

When light or electron beam are absorbed in InSb, the resulting non-equilibrium holes move towards the interface and recombine there with electrons from InAs providing continuity of the current through the HJ, which in this case has always negative sign and is given by the same formulae as that in a Schottky diode [79] from InSb with similar parameter and the barrier height \( V_1 \).

The theory presented above allows us to explain the observed EBIC profile in previous section. According to Eq. (4.4), the sign of EBIC depends on the combination \( \exp\left(\frac{V_2}{kT}\right) - \frac{eE_2(0)L_{p2}}{kT} \). For \( V_2 \simeq 0.12 \text{ eV} \) (see Table 3.1), Eq. (3.3) gives \( E_2(0) \simeq 150 \text{ kV/cm} \) and the given combination becomes negative (and hence \( j_p \) positive) at \( L_{p2} > 100 \text{ nm} \). The real value of \( L_{p2} \) in the experimental samples can be determined from the dependence of \( j_p \) on the position of electron beam \( x_0 \). By comparison the curves in Fig. 4.3 with Eq. (4.4),
$L_{p2}$ was found to vary from 300 to 500 nm (see Sec. 4.5 for detail), which corresponds to a positive sign for the EBIC. For $x_0 < 0$, that is in the depletion layer of InSb, $j_p$ should be negative, as in ordinary Schottky diodes, so that the observed change in the EBIC sign, is well explained.

### 4.5 Diffusion Length

One of the most attractive features about EBIC is the determination of small minority carrier diffusion length which cannot be extracted by common optical excitation method. We see from Eq. 4.4 that moving the electron beam away from the junction results in the exponential drop of EBIC with the characteristic length determined by $L$, which is similar to an ordinary $p$-$n$ junction. This allows us to determine the value of $L$ by measuring the spatial variation of the EBIC signal right of the main maximum in Figure 4.3, that is in the InAs segment but not too close to the second maximum where the signal is influenced by the contact.

The same procedure was repeated at different temperatures and the result of temperature dependence of $L$ is presented in Figure 4.5a as well as the semi-log plot for line scans in Figure 4.5b at selected temperatures. The data shows the diffusion length increases from 300 nm at 300 K and approaches to 500 nm at 100 K. Our data has comparable value and similar temperature dependence in the interval from 100 K to 300 K with the diffusion length in InAs observed in Ref. [80]. To be more precise, Dupuy et al. measured the ambipolar diffusion length which in n-type samples must be close to the hole diffusion length. The temperature dependence of $L$ can be attributed to the drop in mobility caused by phonon scattering. For phonon scattering, the mobility in different InAs structures must have a universal value, varying in the interval 100 to 400 cm$^2$ V$^{-1}$ s$^{-1}$ [66]. This allow us to estimate the hole lifetime which is in the order of $4 \cdot 10^{-10}$ s in our sample.
Figure 4.5: (a) The diffusion length of holes in n-InAs vs. temperature (square) compared to the similar data from Dupuy et al. (Triangle). (b) EBIC line scan at selected temperature.
4.6 Conclusion

In summary, EBIC image of InSb-InAs NW HJ gives unusual result in which the sign of EBIC current changes in the vicinity of heterointerface. This is attributed to the special form of band alignment and the motion of holes in InAs segment. The sign of current is determined by two competing potentials, one created by valence band of InSb and the other one from the band bending $V_2$. According to the theoretical calculation, the EBIC current in InAs segment will become positive when diffusion length of hole is greater than 100 nm. From our experimental data along with the derived theory for diffusion length extraction in nanostructure, we measured diffusion length to be in a range of 300 nm to 500 nm depending on the temperature proving the correctness of our theory. On the other hand, the motion of holes in InSb is much simpler and can be formulated with Schottky barrier. The minority carrier diffusion length in InSb cannot be extracted because its signal partially overlapped with contact electrode.
Chapter 5

Conclusion

This thesis presents a set of experiments that advances the understanding of critical issues such as mechanisms of current flow, band alignment, and behaviour of minority carriers in InSb-InAs nanowire heterostructures.

We began by investigating the current voltage characteristic of these chemical beam epitaxy grown nanowires. From the FET measurement, carrier density in each of the segment was extracted where in InAs it was at $3 \times 10^{17}$ cm$^{-3}$ and $10^{16} - 10^{17}$ cm$^{-3}$ for InSb segment. The band diagram in this heterostructure presented a type-III band alignment with the calculated band bending values at 0.12 eV for InAs side and 0.16 – 0.21 eV in InSb. Temperature dependent CVC measurement gave a barrier height of 0.2 eV and non-ideality coefficient of 5. This large non-ideality coefficient may contribute by carrier tunneling through the barrier. To a great extent, the current through the heterojunction was governed by the generation-recombination processes. One of them was in InSb and the second one occurred at heterointerface which was a fast and activationless process. We also showed the versatility of this nanowire heterojunction through gated measurement.

The second set of experiments involved technique of electron beam induced current to study behaviours of minority carriers in InAs. EBIC image of InSb-InAs nanowire gave unusual result where the sign of EBIC current reversed in the vicinity of heterointerface.
This was attributed to two competing potentials. One of which was created by valence band of InSb and the other one formed from the band bending in InAs. Our theoretical calculation showed this change of sign will occur for diffusion length of holes in InAs greater than 100 nm. From the temperature dependent EBIC measurement, we obtained diffusion length to be in a range of 300 nm at 300 K to 500 nm at 100 K. On the other hand, the motion of holes in InSb was much simpler and can be formulated with Schottky barrier.

In this thesis, the gated measurement was only slightly explored. In order to facilitate the application of this heterojunction, areas like theoretical formulation of gated CVC and gated EBIC measurement should be explored. Introduction of far infrared radiation to excite the carriers in either InSb alone or the entire nanowire during EBIC experiment can further reveal the behaviour of minority carriers. Hole diffusion length in InSb segment was never studied because its EBIC signal partially overlapped with contact. Nevertheless, this thesis still provided preliminary results on electrical properties of InSb-InAs nanowire type-III heterojunction.
Bibliography


Appendix A

Contributions

A.1 Peer Reviewed Publications


A.2 Publications Related But Not Included