Analytical Modelling of Carrier Depletion
Silicon-on-Insulator Optical Modulation Diodes

by

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Graduate Department of Electrical and Computer Engineering
University of Toronto

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Abstract

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We derive an analytical model for the depletion capacitance of silicon-on-insulator (SOI) optical modulation diodes. This model accurately describes the parasitic fringe capacitances due to a lateral $pn$ junction and can be extended to other geometries, such as vertical and interleaved junctions. Analytical results show excellent agreement with numerical simulations. The model is used to identify the waveguide slab to rib height ratio as a key geometric scaling parameter for the modulation efficiency and bandwidth for lateral diodes. We characterise the fringe capacitance as a parasitic effect that leads to a decrease of about 20% in modulation bandwidth of typical SOI diodes without a corresponding increase in modulation efficiency. From the scaling relations, the most effective way to increase the modulation bandwidth is to reduce the series resistance of the diode. In the light of our analysis, we propose high-speed and low power microdisk structures for future SOI modulators.
Acknowledgements

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List of Frequently Used Symbols and Abbrevations

\( n_{\text{eff}} \)  
Effective index of waveguide

\( \Delta n_{\text{eff}} \)  
Effective index change per volt

\( f_{3\text{dB}} \)  
3 dB electrical bandwidth

\( C_{\text{Dep}} \)  
Total depletion capacitance of a \( pn \) junction

\( C_{\parallel} \)  
Capacitance of an infinite parallel plate conductor pair

\( C_f \)  
Fringe capacitance associated with a finite parallel plate conductor pair

\( C_{\text{CPSt},b} \)  
Capacitance of the top/bottom half of a coplanar stripline

\( R_{p,n} \)  
Resistance of the \( p/n \) doped regions

\( V_{pp} \)  
Peak-to-peak modulation voltage

\( V_{\text{bias}} \)  
Bias voltage

\( V_j \)  
Built-in potential of a \( pn \) junction

\( N_{A,D} \)  
Acceptor/donor doping concentration

\( n/p \)  
Electron/hole carrier density

\( n^{++}/p^{++} \)  
Electron/hole carrier density of the degenerately doped regions

\( h_{\text{rib}} \)  
Rib height of the waveguide

\( h_{\text{slab}} \)  
Slab height of the waveguide

\( w_{\text{rib}} \)  
Width of the rib waveguide

\( w_{\text{slab}} \)  
Distance from rib waveguide edge to \( p^{++}/n^{++} \) doped region

\( w_D \)  
Depletion width of a 1D \( pn \) junction

\( \phi \)  
Electrostatic potential

\( \varepsilon_{\text{top},\text{bottom}} \)  
Relative permittivity of the top/bottom waveguide cladding material

\( \varepsilon_{\text{Si}} \)  
Relative permittivity of silicon
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\varepsilon_0$</td>
<td>Vacuum permittivity</td>
</tr>
<tr>
<td>$q$</td>
<td>Fundamental electron charge</td>
</tr>
<tr>
<td>$\lambda$</td>
<td>Operational optical wavelength 1550 nm</td>
</tr>
<tr>
<td>$\omega$</td>
<td>Angular modulation frequency</td>
</tr>
<tr>
<td>$K(k)$</td>
<td>Complete elliptic integral of the first kind</td>
</tr>
<tr>
<td>$B(\omega)$</td>
<td>Frequency normalized susceptance</td>
</tr>
<tr>
<td>$R_{\text{disk}}$</td>
<td>Radius of microdisk</td>
</tr>
<tr>
<td>$R_{\text{wg}}$</td>
<td>Radius of microring</td>
</tr>
<tr>
<td>$Q$</td>
<td>Quality factor of microring/disk</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
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<tbody>
<tr>
<td>SOI</td>
<td>Silicon-on-insulator</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary metal-oxide semiconductor</td>
</tr>
<tr>
<td>DRAM</td>
<td>Dynamic random-access memory</td>
</tr>
<tr>
<td>WDM</td>
<td>Wavelength division multiplexing</td>
</tr>
<tr>
<td>TIA</td>
<td>Transimpedance amplifier</td>
</tr>
<tr>
<td>MZI</td>
<td>Mach-Zehnder interferometer</td>
</tr>
<tr>
<td>VLSI</td>
<td>Very large scale integrated</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal-oxide-semiconductor field-effect transistor</td>
</tr>
<tr>
<td>FEM</td>
<td>Finite element method</td>
</tr>
<tr>
<td>PECVD</td>
<td>Plasma-enhanced chemical vapor deposition</td>
</tr>
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</table>
Chapter 1

Introduction

Microelectronic industry is primarily based on the complementary metal-oxide-semiconductor (CMOS) technology, which facilitates the integration of a large number (> billions) of transistors together with several layers of copper-based electrical interconnects on a single silicon chip [1]. The performance of a microelectronic chip can be enhanced by increasing the transistor clock-frequency and/or by increasing data capacity of the chip. This is achieved by increasing the instruction complexity and parallelism using multi-threaded and/or multicore architectures [2]. The transistor clock-frequency is fast approaching its fundamental limits with the downscaling of transistor gate lengths to only a few nano-meters [2,3]. On the other hand, the multi-threaded and multicore approaches face a fundamental chip-to-chip input/output data bottleneck due to the inefficient copper interconnections. This is because the loss, the latency, and the cross-talk noise in the copper interconnects increase dramatically at data rates higher than a few gigabits per second (Gbit/s) [4,5].

Optical interconnects have been proposed to replace electrical interconnects at various scales: from fibre optical links spanning over kilometers to on-chip optical links which can be only a few milimeters or even a few micrometers in length [6–8]. The feasibility of a point-to-point communication link is assessed based on the distance-bandwidth product, energy per communicated bit and the deployment costs [9]. Fig. 1.1 (taken from [9]) illustrates the trend in the deployment of optical interconnects over electrical interconnects over the years. Following this trend, at the chip-to-chip communication level, the switch from copper to optical interconnects becomes

1
feasible when the distance × bandwidth is about 1 Tb/s × cm, which corresponds to the bandwidth density and interconnect length requirements for the next generation chip-to-chip communications.

![Figure 1.1: Roadmap for the introduction of optical interconnections over electrical interconnections in the past few decades. Link distance vs. link bandwidth and the cost per Gbit/s is shown (taken from [9]).](image)

Photonics based on the silicon-on-insulator (SOI) platform is currently the most attractive candidate for the deployment of photonic interconnects at the chip scale [4, 5]. The high refractive index between silicon (Si) and its oxide (SiO$_2$) allows the tight confinement of light inside the silicon optical waveguides. This makes device footprint small enough for the photonic devices to be integrated on-chip, beside other electronic circuitry. Furthermore, due to its potential compatibility with the mature CMOS processes, silicon photonics is also the most economical solution with the highest yields in fabrication compared to other photonic platforms [10].

The “macro-chip” architecture, proposed by Oracle, is a future multi-core processor employing on-chip silicon photonic interconnects [2]. The macro-chip consists of an array of dynamic random-access memory (DRAM) processors linked together by wavelength division multiplexed (WDM) silicon optical links (Fig. 1.2, taken from [2]). A typical optical link in this architecture is shown in Fig. 1.3 (taken from [9]).
optical circuit consists of on-chip optical waveguides and devices such as modulators, multiplexers and demultiplexers, and detectors.

Figure 1.2: The macro-chip concept, proposed by Oracle. DRAM and microprocessors are bridged by silicon photonic links (taken from [9]).

Figure 1.3: Schematic of a silicon photonic link. The shaded area represents the on-chip component of the link. Not shown are the limiting amplifier stages and the clock and data recovery circuits that may follow the transimpedance amplifier (TIA) of the receiver (taken from [2]).

The macro-chip architecture is predicted to achieve aggregate input/output communication data rates in the scale of a terabit per second (Tbit/s), if the optical circuits and the electronic driver circuits can meet the low-power and high speed requirements [9,11]. Therefore, a significant amount of research in the past decade has been directed towards the design of photonic components on the SOI platform.
1.1 SOI Optical Modulators

A critical component in an integrated optical link is the electro-optic modulator - the device that is responsible for the conversion of electrical signals into optical signals. Until recently, optical modulators were mainly limited to (1) III-V semiconductor [12] and (2) Lithium niobate (LiNbO$_3$) material [13] platforms, where, respectively, changes in light absorption properties or the changes in refractive index of the material to an applied electric field is used for light modulation. However, both of these effects are extremely inefficient in silicon: (1) silicon is transparent at the 1.55 µm optical communication wavelength and (2) the second order susceptibility ($\chi^{(2)}$), required for electro-optic effects, of silicon is zero as a result the inversion symmetry of the lattice [14].

Electrically controlled optical modulation in silicon is realized by utilizing the free carrier plasma dispersion effect [17]. This mechanism changes the refractive index of

![Figure 1.4: Schematics of (a) a MZI modulator [15] and (b) a ring modulator [16]. The Si optical waveguide sections with the $pn$ diode phase shifters are shown.](image)
silicon upon the injection or the depletion of carriers into/from the material. As shown in Fig. 1.4, silicon optical modulator would typically consists of an interferometor (eg. Mach-Zehnder interferometer (MZI) [18]) or a resonantor (eg. a microring [16], a race-track [19, 20] or a microdisk [21]) waveguide structure with phase shifting elements. The optical waveguides would have built-in \( pn \) junctions for carrier injection or depletion.

The \( pn \) junction plays a crucial part in the modulator’s performance. The modulation efficiency, which is the achievable modulation depth per volt, and the maximum modulation rate are both determined on the \( pn \) junction. Fig. 1.5 shows three popular \( pn \) junction geometries in SOI waveguides: (1) lateral (2) vertical and (3) interleaved.

\[ \text{undoped} \]

Figure 1.5: Popular doping arrangements for defining a \( pn \) diode in a Si optical waveguide structure. (a) Lateral \( pn \) junction (b) Vertical \( pn \) junction and (c) Interdigitated or interleaved \( pn \) junction.

To be compatible with high-speed CMOS electronics, it is desired that the next generation of optical modulators will (1) operate at speeds exceeding 50 Gbit/s, (2) consume less than 10 fJ of energy per bit, (3) operate with drive voltages under 2 V, and (4) maintain footprint sizes under \( 10^3 \mu m^2 \) [9, 11]. Carrier injection through a \( pn \) junction is a slow process, and can only reach modulation bandwidths of a few GHz at most [22, 23]. Hence, carrier depletion in \( pn \) diodes is the common method for light modulation in SOI waveguides [11]. Therefore, the focus of this thesis will
be the carrier depletion type SOI modulators.

The past few years have seen remarkable developments of high-speed and low-power carrier depletion SOI modulators. The characteristics of a few of the state-of-the-art carrier depletion modulators are detailed in Table 1.1. Important performance metrics such as modulation speed, extinction ratio, energy consumption per bit, peak-to-peak modulation voltage ($V_{pp}$), bias voltage ($V_{bias}$) and the footprint size (area efficiency), have been summarized.

Table 1.1: State-of-the-art carrier depletion SOI modulators.

<table>
<thead>
<tr>
<th>Device Structure</th>
<th>Bit rate (Gbits/s)</th>
<th>Energy per bit (fJ/bit)</th>
<th>Extinction Ratio (dB)</th>
<th>$V_{pp}$ (V)</th>
<th>$V_{bias}$ (V)</th>
<th>Device footprint ($\mu m^2$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MZI (lateral) [24]</td>
<td>20</td>
<td>200</td>
<td>3.7</td>
<td>0.63</td>
<td>0</td>
<td>$\sim 10^4$</td>
</tr>
<tr>
<td>MZI (lateral) [25]</td>
<td>50</td>
<td>-</td>
<td>5.56</td>
<td>7</td>
<td>-5</td>
<td>$\sim 10^4$</td>
</tr>
<tr>
<td>MZI (interleaved) [26]</td>
<td>40</td>
<td>$4.1 \times 10^3$</td>
<td>7</td>
<td>7</td>
<td>-3.5</td>
<td>$\sim 10^3$</td>
</tr>
<tr>
<td>Microring (lateral) [27]</td>
<td>40</td>
<td>-</td>
<td>7</td>
<td>2</td>
<td>-1</td>
<td>$\sim 50$</td>
</tr>
<tr>
<td>Microring (interleaved) [28]</td>
<td>44</td>
<td>300</td>
<td>3.45</td>
<td>3</td>
<td>-3</td>
<td>$\sim 10^2$</td>
</tr>
<tr>
<td>Microdisk (vertical) [29]</td>
<td>12.5</td>
<td>3</td>
<td>3.2</td>
<td>1</td>
<td>-3.5</td>
<td>$\sim 10$</td>
</tr>
</tbody>
</table>

Majority of the modulators shown in Table 1.1 are capable of operating near 50 Gbit/s speeds. However, most of them still exceed the required energy efficiency, drive voltage and the footprint size for monolithic CMOS integration [9, 11]. The microdisk modulator in [29] have been demonstrated to meet all the other criteria.
for CMOS integration except for the desired modulation speed. The progress of the SOI modulators and the emerging photonic-electronic integrated circuits suggest that the state-of-the-art devices are fast approaching the required level of maturity for monolithic integration with very large scale integrated (VLSI) electronics.

1.2 Equivalent Models for SOI Optical Modulators

As photonics-enabled microelectronic chips emerge [5], much like the macro-chip architectures discussed previously, it is necessary to co-design active photonic circuits beside VLSI electronics. This requires design tools that rapidly and accurately compute the characteristics of device elements.

Equivalent circuit models are essential for the design of VLSI microelectronic circuits. Analytical and semi-analytical circuit models are commonly found for electronic devices (e.g., models for pn junctions [30], short channel and double gate MOSFETs [31, 32] and FinFETs [33]). These models help evaluate a technology, develop compact models for large scale circuit simulations, and understand the impact of physical effects on the device operation [34]. In the electronic circuits community, these models are developed and maintained to the standards specified by the Compact Model Council [35]. Because of the simplicity and the economical advantages, these models are used by various companies involved in the micro electronic industry. For example foundries, fabless companies, integrated manufacturers and electronic design automation companies such as Agilent, Ansys, and Cadence [33,35].

Similar to VLSI electronics, deployment of on-chip optical interconnects would require a large number of optical components to be integrated on-chip. For example, the macro-chip discussed earlier (Fig. 1.2) would have several hundreds of optical links (Fig. 1.3) each consisting of several modulators, detectors and tunable filters; all of which would have to be integrated alongside the VLSI electronics. From a designer’s perspective, the availability of equivalent circuit models will help by reducing the simulation times and by providing a higher level of abstraction for design
at the circuits level, much like the design of electronic circuits. However, analytical circuit models, similar to those for electronic devices, have been far less common for integrated optoelectronic devices.

Therefore, before advancing carrier depletion modulators and other SOI optoelectronic components to higher levels of integration densities with microelectronics circuitry, it is necessary to develop equivalent circuit models that can accurately represent the opto-electronic devices within the surrounding electronic circuits. Although the important device parameters (e.g., depletion capacitance, series resistance) can be extracted from numerical simulations, analytical descriptions are desired since they offer insights into the operation and scaling of the device. Especially for opto-electronic devices, simple scaling is challenging, since different structural features contribute to both the electrical and the optical performance of the device.

Currently, models of optical modulation diodes have largely been semi-empirical [36–38]. An analytical model for lateral SOI optical modulation diodes has not been shown to date and the precise dimensional scaling effects of the \( p \bar{m} \) junction are unclear.

### 1.3 Thesis Objectives

In this thesis\(^1\)\(^,\)\(^2\) we present the first analytical model of the depletion capacitance and depletion region of lateral SOI modulation diodes in waveguides. The model is combined with the free carrier dispersion index change in silicon to quantify the trade-offs between the intrinsic diode modulation bandwidth and modulation efficiency. The key feature of this model is the description of the fringing electric fields and fringe capacitances, resulting in accurate expressions for the small-signal modulation bandwidth and carrier density response. Because of the scaling of the capacitance with optical waveguide geometry, it is shown that the most effective way to optimize the modulation diode is to reduce the series resistance. We further our discussion

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by proposing microdisk modulators as a method of structurally reducing the series resistance. We also discuss how the concepts developed in this thesis can be extended to vertical and interleaved diode geometries.

The results presented in this thesis have purposely excluded the effects of electrical contacts, because their design depends specifically on the modulator type (e.g., Mach-Zehnder interferometer, rings, disks, or gratings/photonic crystals) and the fabrication process. Examples of electrode designs can be found in [36, 41, 42]. The objective of the work presented is to provide a generic model for SOI carrier-depletion modulation diodes that can be incorporated with specific electrode models for a variety of device simulations.

Such a circuit model could be the first step in paving the path for future high density integration of electronic and photonic devices on chip by enabling the use of powerful VLSI design tools that already exist for electronic chip design.

1.4 Organization of the Thesis

The work presented in this thesis is organized as follows.

In Chapter 2, we begin by outlining the numerical simulation of the optical modulation diodes. We discuss the simulations in the electrical and the optical domain.

In Chapter 3, we derive a fully analytical model for the 2D shape of the depletion region and obtain accurate expressions for the depletion capacitance of the lateral SOI modulation diode. We compare our results with the numerical results and find excellent agreement between the two.

In Chapter 4, we further our analysis by using the calculated capacitances from Chapter 3 in a small-signal model of the $pn$ diode. First, we obtain accurate analytical expression for the modulation bandwidth. We then express the modulation efficiency by using analytical carrier density profiles from Chapter 3 in optical simulations. We study the effects of the fringe electric fields on the modulation bandwidth and efficiency. We close this chapter by outlining a generic procedure for the optimized
SOI modulation diode design.

The first half of Chapter 5 is devoted to show that our analytical results can be validated against measured experimental data. We then discuss the future directions for analytical modelling of optoelectronic devices. In the second half of Chapter 5, we propose microdisk modulators to improve the performance of the SOI optical modulators.

Chapter 6 is the closing chapter outlining the work presented throughout this thesis.
Chapter 2

Numerical Simulations of SOI Modulation Diodes

In this chapter, we outline the simulation of the SOI modulation diodes and the calculation of the small signal diode parameters by the use of numerical methods. Simulations of an electro-optic modulator incorporate device simulations in both the electrical and optical domains. Electrical simulation determines the carrier density modulation inside the device in response to an applied voltage signal. The optical simulation would then determine the modulation efficiency ($\Delta n_{\text{eff}}$, the effective index change per volt of the guided mode) of the waveguide based on the carrier density response evaluated by the electrical simulation. Synopsys Sentaurus [43] software is used to perform electrical device simulations and Comsol Multiphysics [44] software is used for optical simulations. Both software tools use the finite element method (FEM).

2.1 Simulation Structure and Parameters

Fig. 2.1 shows the generic $pn$ diode cross-section in context of the SOI waveguide structure studied in this thesis. The critical waveguide dimensions are labelled. For simplicity, we define all the doping profiles to be constant. The $pn$ junction is taken to be abrupt, meaning that the charge concentrations change abruptly between dif-
ferently doped sections. Unless otherwise stated, the parameters in Table 2.1 are assumed for the calculations. These parameters correspond to typical values found in foundry processes of SOI modulation diodes.

Figure 2.1: Cross-section of the waveguide and $pn$ diode geometry.

Table 2.1: Default diode parameters used in calculations.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Carrier concentration in $p/n$ regions ($N_{A,D}$)</td>
<td>$5 \times 10^{17}$ cm$^{-3}$</td>
</tr>
<tr>
<td>Carrier concentration in $p^{++}/n^{++}$ regions</td>
<td>$10^{20}$ cm$^{-3}$</td>
</tr>
<tr>
<td>$h_{rib}$</td>
<td>250 nm</td>
</tr>
<tr>
<td>$h_{slab}$</td>
<td>100 nm</td>
</tr>
<tr>
<td>$w_{rib}$</td>
<td>450 nm</td>
</tr>
<tr>
<td>$w_{slab}$</td>
<td>800 nm</td>
</tr>
<tr>
<td>Bias voltage ($V_{bias}$)</td>
<td>-0.3 V</td>
</tr>
<tr>
<td>Relative permittivity of the top and bottom claddings $\varepsilon_{top,bottom}$</td>
<td>3.9 (radio frequencies), 2.13 (optical frequencies); SiO$_2$</td>
</tr>
<tr>
<td>Relative permittivity of silicon $\varepsilon_{Si}$</td>
<td>11.7 (radio frequencies), 12.11 (optical frequencies)</td>
</tr>
<tr>
<td>Operating wavelength</td>
<td>1550 nm</td>
</tr>
</tbody>
</table>
2.2 Electronic Device Simulations

The modulation diode waveguide cross section shown in Fig. 2.1 corresponds to the structure simulated in Sentaurus. Electrical contacts, modeled as zero resistance contacts (shown in pink color in Fig. 2.1) directly contact the heavily doped $n^{++}/p^{++}$ sections. Physics models for doping dependent Shockley-Read-Hall recombination, mobility, high-field saturation and bandgap narrowing were included to the simulation for the accurate representation of device physics in the SOI platform.

Several methods of time domain simulations corresponding to steady-state or DC, small-signal and transient signal simulations are supported by Sentaurus. Carrier concentration throughout the simulated diode cross-section can be extracted in DC, small-signal or transient simulations at any given time. Fig. 2.2 shows the time variation of the average hole concentration at the edge of the depletion region to an applied transient voltage pulse.

Figure 2.2: Time variation of the average hole concentration at the edge of the depletion region with an applied voltage pulse.
For the majority of this thesis, we are concerned with the calculation of the small-signal parameters for the optical modulation diodes. Sentaurus computes the small-signal parameters by performing a Y-matrix (admittance-matrix) analysis on the 2-port modulation diode (circuit schematic shown in Fig. 2.3 with ports $p, n$) and measuring the small current changes ($\delta i$) to small voltage changes ($\delta v$).

Figure 2.3: Circuit diagram for Y-matrix analysis for the $pn$ modulation diode.

The Y-matrix for Fig. 2.3 can be written as follows:

$$
\delta i = Y(\omega) \cdot \delta v, \quad (2.1a)
$$

$$
\delta i = (G(\omega) + j\omega B(\omega))\delta v, \quad (2.1b)
$$

$$
\begin{bmatrix}
i(p) \\
i(n)
\end{bmatrix} = \begin{bmatrix}
g(p, p) & g(p, n) \\
g(n, p) & g(n, n)
\end{bmatrix} + j\omega \begin{bmatrix}
b(p, p) & b(p, n) \\
b(n, p) & b(n, n)
\end{bmatrix} \cdot \begin{bmatrix}
v(p) \\
v(n)
\end{bmatrix}. \quad (2.1c)
$$

$G(\omega)$ refers to conductance and $\omega B(\omega)$ is the susceptance. In Eq. (2.1c), $g(p, n)$ represents the in-phase current response to a small voltage change and $b(p, n)$ represents the out-phase current response to a small voltage. $b(p, n)$ also corresponds to the $p$-to-$n$ capacitance. The $f_{3dB}$ value, which corresponds to the $RC$ time constant, is found at the point where $B(\omega)$ is half of its DC value.
2.3 Optical Device Simulations

Simulations in the optical domain are carried out by feeding the carrier density profiles, \( n(x, y) \) and \( p(x, y) \), and the changes for small-signal modulation, \( \Delta n(x, y) \) and \( \Delta p(x, y) \), calculated from Sentaurus into Comsol Multiphysics. The latter is used to calculate the effective mode index (\( n_{\text{eff}} \)) and the change in \( n_{\text{eff}} \) per volt (\( \Delta n_{\text{eff}} \)) of the modulator waveguide structure. Since Sentaurus and Comsol are two separate software packages, we first save the carrier concentration data from the Sentaurus simulation grid, which is rectangular. The saved data is then imported to Comsol and linearly interpolated to the Comsol’s triangular mesh.

The change in the refractive index (\( \Delta n_{\text{Si}} \)) of silicon and the change in the absorption coefficient (\( \Delta \alpha_{\text{Si}} \)) of silicon as a result of the change in the carrier concentration is described by the plasma dispersion equations [11,17],

\[
\Delta n_{\text{Si}} = \Delta n_e + \Delta n_h = - \left[ 8.8 \times 10^{-22} \times \Delta n + 8.5 \times 10^{-18} \times (\Delta p)^{0.8} \right], \tag{2.2a}
\]

\[
\Delta \alpha_{\text{Si}} = \Delta \alpha_e + \Delta \alpha_h = 8.5 \times 10^{-18} \times \Delta n + 6.0 \times 10^{-18} \times \Delta p. \tag{2.2b}
\]

In Eqs. (2.2a) and (2.2b), \( \Delta n \) and \( \Delta p \) are the change in the electron and hole concentrations expressed in units of cm\(^{-3}\). \( \Delta n_{e,h} \) and \( \Delta \alpha_{e,h} \) are the change in the refractive index and the absorption coefficient of silicon as a result of electron or hole density changes. Eqs. (2.2a) and (2.2b) are programmed into Comsol, which modifies the the refractive index of silicon in the optical simulation domain, \( n_{\text{Si}}(x, y) \), accordingly.

Fig. 2.4 shows the normalised electric field intensity of the guided mode calculated using Comsol. \( \Delta n_{\text{eff}} \), calculated by applying a transient voltage pulse (similar to Fig. 2.2) is shown in Fig. 2.5. Similarly, the optical response for a small signal input (\( \delta v \)) at the terminals can be computed by feeding the appropriate carrier density concentrations obtained from a small-signal Sentaurus simulation.
Chapter 2. Numerical Simulations of SOI Modulation Diodes

Figure 2.4: Normalized electric field intensity of the fundamental waveguided mode calculated from Comsol Multiphysics software.

Figure 2.5: Time variation of the change in the effective mode index $\Delta n_{\text{eff}}$ with the applied voltage. The applied voltage pulse is equivalent to that shown in Fig. 2.2.
2.4 Summary

Summarizing this chapter, we have outlined the numerical simulation process of an SOI optical modulator. This involves simulations in the electrical domain which produces the carrier density modulation effects in the waveguide as a result of an applied electrical signal at the input of the modulator. The optical simulation is then used to evaluate the modulation in the optical signal as a result of the applied electrical signal.
Chapter 3

Analytical Model for Depletion Capacitance

Device level simulations that we have outlined in the previous chapter are not feasible for the design and simulation of complex circuits with thousands of devices due to the excessive requirements placed on computational resources. Compact analytical models of electronic devices, much like the one that we shall present in this chapter, capture device physics in mathematical form allowing the device performance to be evaluated in a fraction of seconds. Therefore, they have become essential for the design of large-scale integrated circuits. In this chapter\(^1,\)\(^2\), we shall derive an accurate analytical model for describing the depletion region and the capacitance \((C_{Dep})\) of the carrier-depletion SOI optical modulation diode. The spatial charge distribution inside semiconductor devices are described by the Poisson’s equation,

\[
\nabla^2 \phi = -\frac{\rho}{\varepsilon_0 \varepsilon_r},
\]

where \(\phi\) is the electrostatic potential, \(\rho\) is the charge density, \(\varepsilon_0\) is the vacuum permittivity and \(\varepsilon_r\) is the relative dielectric constant of the medium. While electronic simulation softwares \([43,45]\) solve Poisson’s equation using numerical methods, an an-

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alytic description of the device requires the Poisson’s equation to be solved with the appropriate boundary conditions. We start our analysis by looking at the 1D solution of the Poisson’s equation, which is widely used in the study of \( pn \) junctions. However, due to the modification of the shape of the depletion region from the fringing electric fields at the edge of the diode, this solution is not accurate to be used with optical modulation diodes. Hence, in Section 3.2, we develop an analytic solution in 2D for the shape of the depletion region using a conformal mapping technique. Approximating the 2D shape with a parallel plate and coplanar strip capacitors, we then obtain accurate analytical expressions for \( C_{Dep} \) of the optical modulation diodes. Our results show excellent agreement with numerical simulations. We also show how our analytical results may be extended to describe vertical and interdigitated \( pn \) diode designs (Section 3.4).

### 3.1 1D Diode Model

It is common practice in electronic device calculations to approximate \( pn \) junctions with a 1D analytical solution. A closed form of the Poisson’s equation is obtained by considering boundary conditions: \( \phi \) is constant and the electric field strength \( (-\nabla \phi) \) is zero at the two edges of the depletion region. The width of the depletion region, \( w_D \), is then found to be [46],

\[
w_D = w_{Dp} + w_{Dn} = \left[ \frac{2\varepsilon_0 \varepsilon_S}{q} \left( \frac{N_A + N_D}{N_A N_D} \right) \left( V_j - V_{bias} - 2 \frac{k_B T}{q} \right) \right]^{1/2},
\]

(3.2)

where \( w_{Dp,n} \) are the depletion widths in the \( p \) and \( n \) sides, \( k_B \) is the Boltzmann constant, \( q \) is the fundamental electron charge, \( T \) is the ambient temperature, \( V_j \approx (k_B T/q) \ln(N_D N_A/n_i^2) \) is the built-in potential of the junction, and \( n_i \) is the intrinsic carrier density of silicon. We have neglected the resistance outside the depletion region and assumed that the potential difference between the \( p \) and \( n \) side depletion boundaries is equal to \( (V_{bias} - V_j) \). The term \( 2 \frac{k_B T}{q} \) in Eq. (3.2) is a result of consid-
Chapter 3. Analytical Model for Depletion Capacitance

20

ering the majority carrier distribution tails at the edge of the depletion region [46]. This term is usually neglected by the majority of the electronic device textbooks [47]. However, if the depletion width is small ($w_{Dn,p} < 50 \text{ nm}$) and if $V_{\text{bias}}$ is sufficiently small, which is the case for many optical modulation diodes, $\frac{k_BT}{q}$ cannot be neglected. The depletion capacitance calculated using the 1D model would take the form of capacitance of a pair of infinite parallel plates ($C_{||}$).

To account for graded doping profiles, Eq. (3.2) can be modified to obtain $w_{Dp,n}$ near the centre of the diode using the standard procedure (e.g., [46]).

3.2 Shape of the Depletion Region

In reality, the shape of the depletion region of an optical modulation diode is significantly different from that approximated by the 1D model. Fig. 3.1(a) shows the electric field intensity in the vicinity of the $pn$ junction captured from a device simulation. The shape of the depletion region and the electric field distribution near the depletion region is sketched in Fig. 3.1(b). As a result of the fringing electric fields at the top and bottom of the diode, the width of the depletion region is widened.

![Diagram](image)

Figure 3.1: (a) Normalised electric field intensity at the $pn$ junction and in the surrounding cladding area. (captured from Synopsis Sentaurus Device simulation). (b) Schematic representation of the shape of the depletion region and the associated electric fields.
along the vertical dimension away from the center of the diode [48]. This widening has been experimentally observed using scanning capacitance microscopy [49–51]. For the doping conditions given in Table 2.1, the widening of the depletion region at the edges is about 10 nm, which is more than 25% of the depletion width at the center \( w_D \). Therefore, an accurate analytical description of the shape of the depletion region is required to account for the effects of the fringing electric fields, which can be significant.

To determine the shape of the depletion region, we have to solve the Poisson’s (Eq. (3.1)) in 2D near the top and the bottom surfaces of the diode. Typical analytical approaches for electronic device models do not apply here since the geometric boundaries of the depletion region are not known a priori [52–54]. For example, when addressing the inverse-narrow-width- effects in MOSFETs, fringing electric fields at the MOSFET channel edges are bound by the gate and edges of the source and drain making the area under consideration geometrically well defined [48]. However, for the \( pn \) diode, the boundary conditions of the 2D depletion region remain similar to the 1D case (i.e \( \phi \) is constant and the electric field strength \( -\nabla \phi \) is zero along the boundaries of the depletion region). The general solution to Eq. (3.1) is the sum of a particular and the homogeneous solution. For the particular solution, we use the results from the 1D analysis of the junction using Eq. (3.2). This assumption means that the effect of the fringing fields on the center depletion width is minimal. As we shall show, given the height of the waveguide \( h_{rb} \) is large enough, \( w_D \) is a good approximation for the center depletion width. The finite height of the diode only acts as a perturbation to the depletion region.

To find the homogeneous solution, which is the solution to the Laplace’s equation \((\nabla^2 \phi = 0)\), we adapt the conformal mapping technique detailed in [55,56]. Conformal mapping transforms the problem defined in the \( x-y \) plane \((z = x + iy)\) to an another plane defined by \( \phi - \psi \) \((w = f(z) = \phi + i\psi)\). The functions \( \phi(x,y) \) and \( \psi(x,y) \) also satisfies the Laplace’s equation and can be interpreted as potential and field (flux) lines. The coordinate system \( \phi - \psi \) is chosen such that the equipotential and the field
lines form a rectangular (or polar, depending on the preference) grid which simplifies the analysis of the initially complex 2D system defined in the $x - y$ plane [57]. For example, Fig. 3.2 illustrates how the analysis of the fringing electric field lines between two finite parallel conductor plates (finite parallel plate capacitor) is simplified by conformal mapping between the $x - y$ and the $\phi - \psi$ planes. Conformal mapping has been widely used in the for solving 2D electrostatic problems such as coplanar strip-lines [58], parasitic effects of on-chip copper interconnects [59] and fringing fields effects of semiconductor devices such as MOSFETs [48, 54].

![Conformal transformation](image)

**Figure 3.2:** Conformal transformation between the $z = x + iy$ and $w = \phi + i\psi$ planes for a parallel plate capacitor. The constant electric field and the constant potential lines are shown with dashed lines (Figure taken from [57]).

Our problem, which is to analytically evaluate the shape of the $pn$ junction depletion region, is further simplified by noting the analogy between the electrostatic problems and problems concerning frictionless and irrotational fluid flow. The electrostatic potential is alike the velocity potential, the electric field is alike the streamline function and the dielectric constant similar to the fluid density [55, 56, 60]. For example, the conformal mapping analysis of fluid flow in to a rectangular channel is similar to the analysis of a finite plate capacitor [60]. Similarly, we note that the conformal mapping technique used to analyse the fluid flow out of a two-dimensional orifice can be used to analyse our problem [56, 60]. The shape function rendered from this analysis is known as the “$\pi/2$ Borda profile,” which is used in the following analysis to characterise the 2D shape of the depletion region of the $pn$ modulation diode [60].
As shown in Fig. 3.3, we divide the diode along $y = -h_{rib}/2$ and treat the top and bottom halves as semi-infinite sections, which is a good approximation for $h_{rib} \gtrsim 160$ nm. Since the conformal mapping cannot rigorously account for discontinuity in the dielectric constant, we assume that each half of the diode is in a homogeneous material with a dielectric constant of $\varepsilon_{top,bottom}$. Physically, this assumption implies that the fringe fields are contained nearly in its entirety in the cladding.

![Figure 3.3: Depletion region boundaries for the top half of the diode in the simplified transformation domain. The depletion boundaries are described by Eq. (3.3).](image)

The resultant shape $x_{p,n}$ for the $p, n$ sides of the depletion region for the top half of the diode is given by the following expressions, which are parameterized in $\theta$,

\[
\begin{align*}
    x_p &= \left( \frac{2w_{Dp}(\varepsilon_{top})}{\pi} + w_{Dp} \right) - \frac{4w_{Dp}(\varepsilon_{top})}{\pi} \sin^2 \left( \frac{\theta}{2} \right) \\
    x_n &= \frac{4w_{Dn}(\varepsilon_{top})}{\pi} \sin^2 \left( \frac{\theta}{2} \right) - \left( \frac{2w_{Dn}(\varepsilon_{top})}{\pi} + w_{Dn} \right) \\
    y &= \frac{2w_{Dn}(\varepsilon_{top})}{\pi} \left\{ \ln \left[ \tan \left( \frac{\pi}{4} + \frac{\theta}{2} \right) \right] - \sin \theta \right\}
\end{align*}
\]

where $w_{Dp,n}(\varepsilon_{top})$ is the depletion width of the diode calculated using $\varepsilon_{top}$. Fig. 3.3 illustrates the shape of the depletion region embodied by Eq. (3.3). The depletion region of the bottom half of the diode can also be calculated similarly. The complete depletion region is constructed by joining the top and the bottom halves along the vertical center at $y = -h_{rib}/2$. 
By considering Eq. (3.3) at the edges (when $\theta = 0$), we find $t_{p,n} = 2w_{Dp,n}(\epsilon_{top, bottom})/\pi$. We would use $t_{p,n}$ and $w_{Dp,n}$ calculated in this section and the previous section to obtain accurate expressions for the depletion capacitance in the next section.

### 3.2.1 Comparison with Simulations

The analytical method detailed in this chapter produces an excellent approximation to the shape of the depletion region for diodes with typical waveguide heights. Analytically and numerically computed shapes of the depletion region near the top edge of the p-side of the diode for different top cladding materials are shown in Fig. 3.4.

For typical SOI waveguide dimensions, the depletion width at the vertical center of the diode is nearly equal to the result from the 1D model. With a SiO$_2$ cladding and $w_D \sim 50$ nm, we find that the center depletion widths given by Eq. (3.3) are within 1% of the depletion widths $w_{Dn,p}$ given by Eq. (3.2), when $h_{rib} > 160$ nm. Near the surface of the diode, the depletion region is about 50% wider than $w_{Dn,p}$.

![Figure 3.4: Comparison between depletion region boundary near the top edge of p-side of the diode calculated from FEM simulations (dots) and the analytical model (solid lines) for diodes with different upper cladding dielectrics. In the numerical simulations, we find the depletion edge by locating the points where the majority carrier concentration has dropped to $\sim$60% of $N_{A,D}$.](image-url)
3.3 Capacitance of the pn Modulation Diode

By modifying the shape of the depletion region at the top and bottom edges, fringing electric fields contribute significantly to the capacitance of a modulation diode. Therefore, use of a 1D pn diode model, which would result in a depletion capacitance with the form of a pair of infinite parallel plates \( (C_{\parallel}) \), would not accurately model the capacitance of the pn modulation diode. 1D approximation is only accurate for sufficiently thick waveguides \( (h_{rib} > 500 \text{ nm}) \), the field at the center is much stronger than the fringing electric fields and the capacitance due to fringing electric fields is significantly smaller than \( C_{\parallel} \) [61]. As we shall show, for typical SOI modulation diodes with \( h_{rib} \sim 250 \text{ nm} \) and a SiO\(_2\) cladding, the fringe capacitance is non-negligible and is about 20% of \( C_{\parallel} \).

Fringe capacitance depends on the doping, the diode geometry, and the cladding dielectric constant. Therefore, an accurate description of the fringe capacitance is important for the determination of the diode capacitance.

For most cases that use conformal mapping techniques to evaluate the static electric field distribution, it becomes straightforward to calculate the device capacitance in the conformally mapped space [56]. However, as we have mentioned in the previous section, conformal mapping cannot account for the discontinuity in the dielectric (from Si to SiO\(_2\)) at the edges of the diode. Hence, calculation of capacitance in the conformal space becomes tedious. Therefore, to simplify the calculation of depletion capacitance, we separate the static electric field into the contributions shown in Fig. 3.5 (right side): a parallel plate capacitor with its fringing electric fields, and the fringing electric fields caused by the wider depletion regions near the top and bottom surfaces. Hence, the depletion capacitance, \( C_{Dep} \), can be written as a sum of 4 capacitances: (1) \( C_{\parallel} \), the ideal depletion capacitance from a 1D model of the pn diode, (2) \( C_f \), the fringe capacitance due to the charges at the center of the diode, (3) \( C_{CPS_t} \) and (4) \( C_{CPS_b} \), the fringe capacitances due to extended depletion widths \( t_{p,n} \) at the top and bottom surfaces of the waveguide, respectively.

Using \( w_D \) (the center depletion region width) and \( t_{p,n} \) calculated from Eqs. (3.2)
and (3.3) in the previous sections, we can now find $C_\parallel$, $C_f$ and $C_{CPSt,b}$ (Fig. 3.5). $C_\parallel$ is the ideal capacitance of two parallel conductor plates of height $h_{rib}$ separated by $w_D$. We take $C_f$ to be the fringe capacitance associated with the electric field lines terminating on the outer surfaces of these parallel plates. The expression for $C_f$ is given in [62, 63]. For $C_{CPSt,b}$, the capacitances due to the wider depletion widths at the top and bottom surfaces of the diode, we model the charge distribution as co-planar strips with widths $t_{p,n}$ separated by a gap of $w_D$. From Eq. (3.3), we find $t_{p,n} = 2w_{Dp,n}(\varepsilon_{top,bottom})/\pi$. Therefore, the per-unit length depletion capacitance is

$$C_{Dep} = C_\parallel + C_f + C_{CPSt} + C_{CPSt,b},$$ (3.4a)

$$C_\parallel = \varepsilon_0\varepsilon_{Si} \frac{h_{rib}}{w_D},$$ (3.4b)

$$C_f = \varepsilon_0 \left( \frac{\varepsilon_{top} + \varepsilon_{bottom}}{2\pi} \right) \ln \left( 2\pi \frac{h_{rib}}{w_D} \right),$$ (3.4c)

$$C_{CPSt,b} = \varepsilon_0\varepsilon_{top,bottom} \frac{K(\bar{k})}{K(k)},$$ (3.4d)

where $K(k)$ is the complete elliptic integral of the first kind, $k = \sqrt{\frac{w_D(w_D + t_n + t_p)}{(w_D + t_n)(w_D + t_p)}}$, and $\bar{k} = \sqrt{1 - k^2}$ [64].
### 3.3.1 Comparison of $C_{Dep}$ with Simulations

Comparing our analytical expression for $C_{Dep}$ with full 2D FEM device simulations using Synopsys Sentaurus Device shows they are in excellent agreement. In Sentaurus Device, $C_{Dep}$ is taken to be the DC value of the frequency normalized small-signal susceptance, $B(\omega)$ (see Chapter 2), of the device biased at a voltage of $V_{bias}$. Fig. 3.6 compares $C_{Dep}$ for several upper cladding materials. In all cases, the differences between the analytical expression and device simulation are less than 2%.

![Comparison between depletion capacitance calculated from FEM simulations (solid lines) and the analytical model (dashed lines) for diodes with different upper cladding dielectrics and a lower cladding of SiO$_2$. The capacitance without the fringe field contribution ($C_{||}$) is shown in green. $C_{||}$ was calculated from Sentaurus Device.](image)

Fig. 3.6: Comparison between depletion capacitance calculated from FEM simulations (solid lines) and the analytical model (dashed lines) for diodes with different upper cladding dielectrics and a lower cladding of SiO$_2$. The capacitance without the fringe field contribution ($C_{||}$) is shown in green. $C_{||}$ was calculated from Sentaurus Device.

Fig. 3.7 (a) compares $C_{Dep}$ for $V_{bias}$ ranging from -2 V to +0.3 V, and the differences between the results are less than 4%. Fig. 3.7 (b) shows that excellent agreement between the analytical and simulation results also exists in asymmetrical diodes, where $N_A$ is varied between $5\times10^{16}$ cm$^{-3}$ and $1\times10^{18}$ cm$^{-3}$. The green curves in Fig. 3.6 and Figs. 3.7 (a) and (b), which show only $C_{||}$, indicate that the fringe effects are major contribution to the total diode capacitance $C_{Dep}$ ($C_{||}$ was
Figure 3.7: Comparison between depletion capacitance calculated from FEM simulations (solid lines) and the analytical model (dashed lines) for (a) different bias voltages from -2 V to +0.3 V and (b) different doping concentrations in the p-side of the diode. n-side doping is kept at a constant value of \(5 \times 10^{17}\) cm\(^{-3}\). The capacitance without the fringe field contribution \((C_{\|})\) is shown in green. \(C_{\|}\) was calculated from Sentaurus Device.
computed from FEM simulations with cladding dielectric constant set to zero). The fringe capacitance can be as large as $C_{||}$ for thin waveguides.

Summarizing this section, we have shown that our analytical expressions give capacitance characteristics and depletion region shape with excellent agreement with full electron device simulations.

### 3.4 Vertical and Interdigitated Diodes

In this section, we briefly discuss the extension of the capacitance model developed in Section 3.3 to other $pn$ junction geometries.

For vertical $pn$ diodes in microdisks as demonstrated in [21], the shape of the depletion region is accurately described by rotating Eq. (3.3) by 90°. For vertical junctions in ridge waveguides as in the MZI modulator in [65], our analytical model is not as accurate because $C_{||}$ in Eq. (3.4b) is a poor approximation due to the complex shape of the depletion region at the center of the waveguide. An accurate expression for $C_{||}$ is necessary for a fully analytical model. Nonetheless, Eqs. (3.4c) and (3.4d) yield a fringe capacitance $C_f + C_{CPS_t} + C_{CPS_b}$ with a reasonable accuracy (within 5% of simulated value when $h_{rib} \gtrsim 150 \text{ nm}$).

To use the analytical model for interdigitated $pn$ junctions [66], $C_{||}$ should be calculated by applying Eq. (3.4b) to the doped rib and slab sections that constitute each $pn$ junction. Then, Eqs. (3.4c) and (3.4d) are used to calculate the fringe capacitances where the depletion region is exposed to the cladding oxide at the top, bottom, and sides of the waveguide. Eqs. (3.4c) and (3.4d) are also used with $\varepsilon_{top, bottom} = \varepsilon_{Si}$ to approximate the capacitances at the two ends of the diode where one type of dopant is terminated before the other and the depletion region is exposed to undoped silicon. We find that the calculated value of the capacitance is within 5% of the simulated result when $h_{rib} \gtrsim 150 \text{ nm}$.
3.5 Summary

In this chapter we have presented an analytical calculation of the shape of the depletion region of a lateral SOI modulation diode by solving the Poisson’s equation in 2D using a conformal mapping technique. We have approximated the depletion shape with a parallel plate capacitor and a pair of coplanar striplines to accurately calculate $C_{Dep}$ of the modulator. Our results show excellent agreement when compared to numerical results, where the difference between the two is less than 5% for all the tested cases. We also discussed how the concepts developed in this chapter can be extend to obtain analytical expressions for the capacitance of vertical and interleaved $pn$ junctions.
Chapter 4

Modulation Bandwidth and Efficiency

In this chapter\(^1,2\), the expressions for \(C_{Dep}\) developed in Chapter 2 are used with the small-signal model to study the scaling of the modulation efficiency (\(\Delta n_{eff}\), the effective index change per volt) and the 3 dB modulation bandwidth (\(f_{3dB}\)) of the diode with the waveguide dimensions. \(\Delta n_{eff}\) is related to \(V_\pi L\), a commonly used parameter for figure of merit, by \(V_\pi L = \lambda/(2\Delta n_{eff})\). We identify the \(h_{slab}/h_{rib}\) ratio as a key scaling parameter of the device, and a specific value of \(h_{slab}/h_{rib}\) generally optimizes the modulation bandwidth and efficiency.

In Section 4.5, we examine the effects of the fringe capacitance on \(f_{3dB}\) and \(\Delta n_{eff}\) of the modulator and show that fringe capacitance is a parasitic effect. Several techniques to reduce the fringe capacitance is then discussed. In Section 4.6, it is proposed that the best method of increasing \(f_{3dB}\) without affecting \(\Delta n_{eff}\) is by reducing the \(w_{slab}\) parameter (the distance to the \(n^{++}, p^{++}\) sections from the edge of the waveguide as illustrated in Fig. 2.1). In the light of this discussion, a generic design procedure for the carrier depletion modulators is outlined in Section 4.7.

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4.1 Small-signal model

The small-signal model of the diode with the capacitances calculated in Section 3.3 is illustrated in Fig. 4.1.

\[ R_{p,n} = \frac{w_{slab}}{qN_{A,D}\mu_{p,n}h_{slab}L_{diode}} + \frac{w_{rib}/2 - w_{Dp,n}}{qN_{A,D}\mu_{p,n}h_{rib}L_{diode}}, \] (4.1)

where \( \mu_{p,n} \) is the mobility of \( p, n \)-doped silicon calculated according to [67] and \( L_{diode} \) is the length of the diode. Since the resistance due to \( h_{slab} \) is typically much larger than the resistance due to \( h_{rib} \), the contribution of \( h_{rib} \) to \( R_{p,n} \) can be neglected in Eq. (4.1). Typically, the waveguide width, \( w_{rib} \), is restricted to \( \sim 400 - 600 \) nm to maintain optical confinement and the single-mode waveguide condition. \( N_{A,D} \) is in the range of \( 5\times10^{16} \) cm\(^{-3} \) to \( 1\times10^{18} \) cm\(^{-3} \) depending on the desired \( \Delta n_{eff} \) and the tolerable optical loss. Changes to \( N_{A,D} \) or \( w_{rib} \) within these limits would not significantly change the \( f_{3dB} \) or \( \Delta n_{eff} \) results to follow.
4.2 Dimensional Scaling of the 3 dB Modulation Bandwidth

As it was detailed in Chapter 2, in Sentaurus Device, \( f_{3dB} \) is obtained by performing a small-signal AC simulation and computing the susceptance \( \omega B(\omega) \) over a range of frequencies. Here, \( f_{3dB} \) is the frequency when the frequency normalized susceptance, \( B(\omega) \), is half of its DC value. Analytically, from Eqs. (3.4) and (4.1), the expression for the \( f_{3dB} \) of the diode is,

\[
f_{3dB} = \frac{1}{2\pi(R_n + R_p)C_{D_{eq}}L_{diode}} = \frac{A}{2\pi}\left(\frac{h_{slab}}{h_{rib}}\right)\left[\frac{\varepsilon_0\varepsilon_{Si}}{w_D} + \left(\frac{C_f + C_{CPSl} + C_{CPSb}}{h_{rib}}\right)\right]^{-1},
\]

(4.2)

where \( A = \frac{q}{w_{slab}}\left(\frac{\mu_p\mu_n N_A N_D}{\mu_p N_A + \mu_n N_D}\right) \). Fig. 4.2 (a) shows \( f_{3dB} \) decreases with increasing \( h_{rib} \) for a specific \( h_{slab} \) and the good agreement between the analytical expressions and simulations.

More generally, Eq. (4.2) shows that \( f_{3dB} \) is primarily determined by the ratio, \( h_{slab}/h_{rib} \). \( C_{CPSl} \) and \( C_{CPSb} \) are independent of \( h_{rib} \). For \( h_{rib} > 250 \text{ nm} \), \( C_f \) is also approximately constant. Therefore, the term \( (C_f + C_{CPSl} + C_{CPSb})/h_{rib} \) only has a small dependence on \( h_{rib} \) for \( h_{rib} > 250 \text{ nm} \), and \( f_{3dB} \) scales approximately linearly with the ratio \( h_{slab}/h_{rib} \). This is illustrated by Fig. 4.2 (b), where the variation of \( f_{3dB} \) with \( h_{slab}/h_{rib} \), calculated directly using FEM simulations, is shown for a range of rib heights.
Figure 4.2: (a) $f_{3dB}$ calculated from FEM simulation (solid line) and from the analytical model developed (dashed line). (b) $f_{3dB}$ as a function of $h_{slab}/h_{rib}$ for several values of $h_{rib}$ calculated from FEM simulations.
4.3 Dimensional Scaling of the Effective Index Modulation

In Chapter 2, we discussed the numerical simulation of $\Delta n_{eff}$ by feeding the carrier density profiles from Sentaurus into Comsol Multiphysics. Similarly, here, we calculate $\Delta n_{eff}$ by feeding the analytically calculated carrier concentration profiles $(n(x, y), p(x, y))$ and their low-frequency small-signal responses $(\Delta n(x, y), \Delta p(x, y))$ into an COMSOL Multiphysics.

We use Eq. (3.3) to obtain $p(x, y)$ and $n(x, y)$, and we construct $\Delta p(x, y)$ and $\Delta n(x, y)$ from the modulation of the depletion width near the vertical center of the diode, $dw_{Dp,n}/dV$. The carrier density modulation due to the majority carrier tails penetrating the depletion region is negligible; thus, its effect on index modulation is negligible. Hence, it is here assumed that the free carrier concentration is: (1) zero in the depletion region, and (2) equal to $N_{A,D}$ in the $p,n$ regions on either side of the depletion boundary. In this case, modulation of the depletion width is,

$$
\frac{dw_{Dp,n}}{dV} \approx \frac{C_{Dep}}{h_{rib}N_{A,D}} = \frac{1}{N_{A,D}} \left[ \frac{\varepsilon_0 \varepsilon_{Si}}{w_D} + \frac{C_f + C_{CPSb} + C_{CPSb}}{h_{rib}} \right],
$$

(4.3)

where $V$ is the amplitude of the applied small-signal voltage.

$\Delta n_{eff}$ depends on $dw_{Dp,n}/dV$ and the optical mode overlap with the depletion region. Figure 4.3 (a) shows that $\Delta n_{eff}$ increases with increasing $h_{rib}$ for a specific $h_{slab}$. It also shows good agreement between the analytical expressions and simulations, indicating that the spatial distributions of the charges are accurately described by Eq. (3.3).

From the arguments for the $h_{slab}/h_{rib}$ scaling in section 4.2, $dw_{Dp,n}/dV$ is also nearly independent of $h_{rib}$ for $h_{rib} \gtrsim 250$ nm. The optical mode confinement increases with decreasing $h_{slab}$. Also, the confinement becomes nearly independent of $h_{rib}$ when $h_{rib} \gtrsim 300$ nm as the confinement approaches a maximum. Therefore, as shown in Fig. 4.3 (b), $\Delta n_{eff}$ tends to decrease with increasing $h_{slab}/h_{rib}$.
Figure 4.3: (a) $\Delta n_{\text{eff}}$ calculated from FEM simulation (solid line) and from the analytical model (dashed line). (b) $\Delta n_{\text{eff}}$ as a function of $h_{\text{slab}}/h_{\text{rib}}$ for several values of $h_{\text{rib}}$ calculated from FEM simulations.
4.4 Optimal dimensions

As evidenced by Figs. 4.2(b) and 4.3(b), $f_{3dB}$ and $\Delta n_{eff}$ depend oppositely on $h_{slab}/h_{rib}$. We define $\Delta n_{eff} \times f_{3dB}$ as a figure of merit, akin to the gain-bandwidth product used for filters. Considering $\Delta n_{eff} \times f_{3dB}$, we find that an optimum value is $h_{slab}/h_{rib} \approx 0.6$ regardless of the rib height (Fig. 4.4). The figure of merit is maximized for rib heights in the range of 250 - 300 nm, which are typical in state of the art SOI photonic devices.

![Figure 4.4](image)

Figure 4.4: $\Delta n_{eff} \times f_{3dB}$ as a function of $h_{slab}/h_{rib}$ for a range of $h_{rib}$ values. Calculated from FEM simulations. $\Delta n_{eff} \times f_{3dB}$ is optimized for $h_{slab}/h_{rib} \approx 0.6$ regardless of the rib height when $h_{rib} > 200$nm.

4.5 Effects of Fringing Electric Fields

According to the analytical model developed in Chapter 3 and the numerical simulations, fringing electric fields can have a non-negligible impact on the diode capacitance and the depletion region, hence, on the modulation efficiency and on the modulation bandwidth. The fringe fields cause the carrier density modulation to occur further
from the lateral center of the diode at the top and bottom sides, while the optical intensity is highest at the center of the diode. Therefore, fringe capacitance only slightly contributes to the increase of $\Delta n_{eff}$, but more significantly contributes to the decrease in $f_{3dB}$ and increase in the energy consumed per bit, which is given by $\frac{1}{4}C_{Dep}V^2$. Fig. 4.5 shows the increase in capacitance due to fringe fields ($C_{Dep} - C_{||}$) as a fraction of $C_{||}$ and the corresponding percentage increase in $\Delta n_{eff}$ and decrease in $f_{3dB}$.

![Figure 4.5: Fractional increase in $C_{Dep}$ relative to $C_{||}$ due to fringing fields and the resultant fractional increase in $\Delta n_{eff}$ and decrease in $f_{3dB}$. $\epsilon_r$ values used for calculations at radio frequencies are $\epsilon_{air} = 1$, $\epsilon_{SiN_4} = 7.5$ and $\epsilon_{SiCOH} = 2.8$. At optical frequencies $\epsilon_{air} = 1$, $\epsilon_{SiN_4} = 4$ and $\epsilon_{SiCOH} = 2.13$.](image)

The percentage increase in $\Delta n_{eff}$ is smaller than the increase in capacitance and the decrease in $f_{3dB}$. Thus, the fringe capacitance, $(C_f + C_{CPSt} + C_{CPSb})$, is a parasitic effect.

However, the fringe capacitance does not vary strongly with the geometry, doping, bias, and cladding dielectrics; thus, this intrinsic parasitic effect is difficult to mitigate. First, a higher $h_{rib}$ increases the relative magnitude of $C_{||}$ relative to the fringe capacitance, but results in only modest $f_{3dB}$ gains of approximately 2 - 3 GHz at a
Figure 4.6: (a) $f_{3dB}$ and (b) $\Delta n_{eff}$ for diodes with different cladding dielectrics for the geometry shown in Fig. 4.5. $\varepsilon_r$ values used for calculations at radio frequencies are $\varepsilon_{air} = 1$, $\varepsilon_{Si_3N_4} = 7.5$ and $\varepsilon_{SiCOH} = 2.8$. At optical frequencies $\varepsilon_{air} = 1$, $\varepsilon_{Si_3N_4} = 4$ and $\varepsilon_{SiCOH} = 2.13$. 
fixed ratio of $h_{\text{slab}}/h_{\text{rib}}$ (Fig. 4.6(a)). The drawback of a larger $C_{||}$ is a larger energy consumption for the modulation, because $\Delta n_{\text{eff}}$ is not increased (Fig. 4.6(b)). Second, changing $V_{\text{bias}}$ within the range of -2 V to 0 V only produces a minute reduction of $(C_f + C_{\text{CPSt}} + C_{\text{CPSb}})/C_{||}$ of 5%. Third, reducing $N_{A,D}$ near the top and bottom surfaces of the diode only reduces $(C_f + C_{\text{CPSt}} + C_{\text{CPSb}})/C_{||}$ by less than 1%, whereas increasing $N_{A,D}$ produces a few GHz of gain in $f_{3\text{dB}}$. Finally, as shown in Fig. 4.6(a) and (b), by lowering $\varepsilon_{\text{top, bottom}}$ using low-k dielectrics, the improvements in $f_{3\text{dB}}$ and $\Delta n_{\text{eff}}$ are also found to be incremental. Using SiCOH ($\varepsilon_r = 2.8$) [68] as the upper and even lower cladding yields a gain of only $\sim$3 GHz over SiO$_2$. Replacing the upper cladding with air also yields a 3 GHz improvement. A gain of $\sim$6 GHz (not shown in Fig. 4.6(a)) is expected if air is used as the top and the lower cladding, which may be implemented with localized substrate removal [69]. If the cladding material has a low refractive index at optical wavelengths, they can increase the optical confinement to improve the modulation efficiency (Fig. 4.6(b)). Because SiCOH has a similar refractive index as SiO$_2$ at $\lambda = 1.55$ µm, it has a similar $\Delta n_{\text{eff}}$.

### 4.6 Improving the Modulation Response

Sections 4.2 and 4.3 and 4.5 of this chapter demonstrate that the modulation bandwidth and efficiency of the diodes are constrained: (1) $f_{3\text{dB}}$ and $\Delta n_{\text{eff}}$ have opposite dependences on $h_{\text{slab}}/h_{\text{rib}}$, and (2) substantial improvements to $\Delta n_{\text{eff}}$ and $f_{3\text{dB}}$ by reducing the fringe capacitance are challenging. Therefore, the most effective way to increase $f_{3\text{dB}}$ without sacrificing $\Delta n_{\text{eff}}$ is to reduce the series resistance, $R_{p,n}$, by decreasing $w_{\text{slab}}$ in Fig. 2.1. For the waveguide widths considered, $\Delta n_{\text{eff}}$ is largely independent of $w_{\text{slab}}$.

Typically, as in the calculations presented in this thesis so far, $w_{\text{slab}} \gtrsim 700$ nm to limit the optical losses due to the $p^{++}/n^{++}$ sections [70, 71]. Fig. 4.7(a) shows that $f_{3\text{dB}}$ can be increased by over 35 GHz when $h_{\text{slab}}/h_{\text{rib}} < 0.4$ and $w_{\text{slab}}$ is reduced such that the excess optical loss from the $p^{++}/n^{++}$ sections is 1 dB/cm. For $h_{\text{slab}}/h_{\text{rib}} = 0.2,$
Figure 4.7: Variation of (a) $f_{3\text{dB}}$ and (b) $\Delta n_{\text{eff}} \times f_{3\text{dB}}$ as a function of $h_{\text{slab}}/h_{\text{rib}}$ for $w_{\text{slab}} = 800 \text{ nm}$ and $w_{\text{slab}}$ for 1 dB/cm excess loss due to the $p^{++}/n^{++}$ sections. (For $0.2 \leq h_{\text{slab}}/h_{\text{rib}} \leq 0.6$, $w_{\text{slab}}$ was $183 \text{ nm} \leq w_{\text{slab}} \leq 548 \text{ nm}$ to obtain 1dB/cm excess loss).
$w_{slab}$ can be reduced below 200 nm, resulting in an increase in $f_{3dB}$ of over 35 GHz compared to when $w_{slab}= 800$ nm. Here, it is assumed that the contribution to the series resistance from the metal vias and contacts is negligible when compared to the resistance of the thin silicon slab section. This assumption is confirmed by the data provided by fabrication facilities [72] and from recent literature [18,36,42]. Fig. 4.7(b) compares the $\Delta n_{eff} \times f_{3dB}$ values for the two cases of $w_{slab}$. The optimum value of $h_{slab}/h_{rib}$ for the reduced $w_{slab}$ values is about 0.4, where the corresponding $f_{3dB}$ is approximately 80 GHz.

The results show that reducing $w_{slab}$ is a highly effective way to increase $f_{3dB}$. In practice, the challenge is to precisely control $w_{slab}$ and prevent the diffusion of dopants into the waveguide during annealing processes [70].

### 4.7 Design Procedure for Lateral Carrier Depletion Modulators

This section provides a simple procedure to design lateral depletion modulation diodes. Table 4.1 summarizes the dependences of the lateral diode parameters on the waveguide geometry. For the typical diode structure we have studied, $f_{3dB}$ is limited to $\sim 65$ GHz at the optimum $\Delta n_{eff} \times f_{3dB}$ (See Fig. 4.4). Since high-speed SOI modulators demonstrated to date with 40 - 50 GHz bandwidths have comparable dimensions, they may be close to this fundamental modulation rate limit [18,66,73]. Recent demonstrations of modulation at and beyond 40 GHz have relied on increasing $h_{slab}/h_{rib}$ [18,66,74]. However, the results of this thesis show that the gain in $f_{3dB}$ is achieved at a penalty in $\Delta n_{eff}$. In contrast, reducing $h_{slab}/h_{rib}$ increases $\Delta n_{eff}$, which can reduce the drive voltage and energy consumption at the cost of bandwidth. Low voltage and ultra-low energy SOI microring modulators have been demonstrated this way [38,75].

Given these trade-offs, the design process of depletion modulation diodes to achieve a specific $f_{3dB}$ can be straight-forward. In the arguments to follow, it is assumed...
Table 4.1: Summary of the dependence of the diode parameters on waveguide dimensions.

<table>
<thead>
<tr>
<th>Diode Parameter</th>
<th>Approximate Dimension Dependence</th>
</tr>
</thead>
<tbody>
<tr>
<td>Depletion capacitance ($C_{Dep}$)</td>
<td>increases with $h_{rib}$</td>
</tr>
<tr>
<td>Bandwidth ($f_{3dB}$)</td>
<td>increases with $\frac{h_{slab}}{h_{rib}w_{slab}}$</td>
</tr>
<tr>
<td>Modulation efficiency ($\Delta n_{eff}$)</td>
<td>decreases with $\frac{h_{slab}}{h_{rib}}$</td>
</tr>
</tbody>
</table>

that $h_{rib}$ is between 250 nm and 350 nm for the high confinement type of single-mode SOI waveguides and $V_{bias}$, $N_{A,D}$, and $h_{rib}$ are specified. $N_{A,D}$ should be chosen considering the required $\Delta n_{eff}$ (or $V_{\pi}L$) and the tolerable per-length absorption loss. An optimized doping profile would have very high doping concentrations at the center of the diode to increase $\Delta n_{eff}$ and relatively low doping concentrations further away from the junction to reduce the absorption losses [38, 66, 74, 76, 77]. An asymmetric diode (i.e., $N_D > N_A$ and/or $pn$ junction is located away from the center of the waveguide) can further improve $\Delta n_{eff}$ [18]. However, the choice of doping profiles is ultimately determined by the choice of the foundry and its fabrication process.

First, $w_{rib}$ should be chosen to maximize the mode overlap with the depletion region and to reduce the sensitivity to sidewall scattering losses. In this range of $h_{rib}$, regardless of the eventual value of $h_{slab}$, the mode overlap is maximized around $w_{rib} \sim 400$ nm. Next, $C_{Dep}$ should be calculated using Eq. (3.4) or with simulations to find the upper-bound for $R_{p,n}$ required to reach the desired $f_{3dB}$. $R_{p,n}$ is proportional to $w_{slab}/h_{slab}$ (Eq. (4.1)). The geometry with the smallest $h_{slab}$ and the associated smallest $w_{slab}$ (as limited by the tolerable optical loss or fabrication process) results in the diode with the highest $\Delta n_{eff}$ that satisfies the $f_{3dB}$ requirement.
4.8 Summary

In this chapter we have used our analytical results for $C_{Dep}$ from Chapter 3 with the small-signal model of the modulator’s $pn$ junction to obtain analytical/semi-analytical expressions for $f_{3dB}$ and $\Delta n_{eff}$. The analytical results show excellent agreement when compared with numerical results. We have identified $h_{slab}/h_{rib}$ as a key scaling parameter of the diode contributing to $C_{dep}$ and shown that $f_{3dB}$ and $\Delta n_{eff}$ have opposite dependences. Therefore, because of the trade-off between $f_{3dB}$ and $\Delta n_{eff}$, the optimum value of the figure-of-merit parameter, $\Delta n_{eff} \times f_{3dB}$ is reached when $h_{slab}/h_{rib} \sim 0.6$, regardless of $h_{rib}$.

We have also discussed the significant parasitic effects of the fringe capacitances on $f_{3dB}$ and $\Delta n_{eff}$. We investigated methods of reducing the parasitic fringe effects by lowering $\epsilon_r$ of the cladding. However, only small gains in $f_{3dB}$ and $\Delta n_{eff}$ were observed, proving that it is difficult to mitigate the parasitic effects of fringing electric fields.

Finally, we proposed to reduce $R_{p,n}$ as the most suitable method of increasing the $f_{3dB}$ of the modulator without affecting $\Delta n_{eff}$. We showed that the $w_{slab}$ of the modulator can be reduced to be in the range of $200 \text{ nm} < w_{slab} < 500 \text{ nm}$, while maintaining the additional loss due to $n^{++}/p^{++}$ regions under 1 dB, to obtain significant gains in $f_{3dB}$. Based on this, we outlined a general procedure for the optimal design of the lateral $pn$ junction modulator.
Chapter 5

Experiments and Future Work

In the previous chapters, we have developed a fully analytical model for the depletion capacitance of the SOI modulator and obtained excellent agreement with the numerical simulations. We have also shown good agreement of the $f_{3dB}$ and the $\Delta n_{eff}$ values obtained using the analytical model and the numerical results. Thus, we have shown that the analytical model can be used in the design and development of modulation diodes in the place of numerical simulations, which can be quite complicated and computationally intensive.

In this chapter, we first compare our analytical results with the experimental values of $C_{Dep}$ and $\Delta n_{eff}$ presented for the MZI modulator by Yu and co-workers [66]. We discuss the future research directions for further development and verification of compact, analytical models for SOI modulation diodes. Then we propose high-speed microdisk modulator structures based on the analysis presented in Chapter 4. We further extend the results to show how a vertical junction microdisk minimizes the adverse effects of a high $R_{p,n}$ value while increasing $\Delta n_{eff}$. Efficient single-mode coupling to a SOI microdisk is experimentally demonstrated to motivate the use of microdisk modulators. We finally discuss the future prospects of microdisk modulators.
5.1 Comparison of the analytical results with measurements

Direct comparison of analytical results with experimental data available in the literature can be complicated due to many reasons. The analytical model that we have presented in this thesis only describes the $pn$ diode and waveguide section of the SOI modulator. The modulator performance is also affected by the metal vias and contacts. These parasitic effects depend largely on the fabrication process and the contact design of the modulator (e.g., lumped electrode [73], travelling wave electrode [24]). Usually, the junction capacitance ($C_{Dep}$) is determined by fitting a small-signal model with the measured frequency response [28]. However, to extract the intrinsic properties of the $pn$ junction, ideally, results should be compared with reference structures that only consists of vias and contacts [24].

Here, we compare the $C_{Dep}$ from our analytical model with the measured $C_{Dep}$ presented in [66] for a MZI optical modulator with a lateral $pn$ junction. A 3D schematic of the modulator is shown in Fig. 5.1 [left side]. Fig. 5.1 [right side] illustrates the doping profiles used. The doping conditions produce an average doping concentration of $N_{A,D} = 1 \times 10^{18}$ cm$^{-3}$ in the $p,n$ regions. As illustrated in Fig. 5.1 [right side], the authors have chosen to separate the doping profiles by $d = 40$ nm to optimize $\Delta n_{eff}$. We account for this separation between the doping profiles by...
using the analytical results for the depletion width of a pin diode with a 40 nm wide $i$ region, for the calculation of the center depletion width $w_D$ [46,47].

The values obtained for $C_{Dep}$ from the measurements in [66] and from the analytical model are shown in Fig. 5.2. The analytical results show excellent agreement with the measured data. Difference between analytical and the measured data is less than 3%. The capacitance given by the parallel plate approximation ($C ||$) is also shown in Fig. 5.2 (green). The difference between measured values and $C ||$ is about 20%.

![Figure 5.2: Comparison between the measured values (taken from [66]) and the analytical results for $C_{Dep}$ vs. $V_{bias}$ of the MZI modulator presented in [66].](image)

In Fig. 5.3, we compare the analytical results for $\Delta n_{eff}$ for the same device with the measured values presented in [66]. The analytical results show good agreement with the measured values in low reverse bias regime, $-3 \text{ V} < V_{bias} < 0 \text{ V}$. The difference between the two is less than 5% in this regime. However, for larger reverse bias values, $V_{bias} < -4 \text{ V}$, the model deviates from the measured results. We attribute this mismatch to the non uniform doping profiles created in the waveguide as a result of the lateral straggling of the ions during the ion implantation and thermal annealing procedures. We have not taken this effect in to account in the analytical model.
Figure 5.3: Comparison between the measured values (taken from [66]) and the analytical results for $\Delta n_{eff}$ vs. $V_{bias}$ of the MZI modulator presented in [66].

5.1.1 Future work on equivalent modelling

In this section, we have compared $C_{Dep}$ and $\Delta n_{eff}$ calculated from our analytical model with the measured data presented in [66] and have shown that the agreement between the two is reasonable. Therefore, our analytical model is well suited for modelling the depletion region of the lateral SOI modulation diode. However, a complete analytical model of the device would have to take the effect of the metal contacts, which as we have mentioned before, would differ depending on the modulators electrode configuration and the fabrication process. For example, in [36] an analytical model for the travelling wave electrode MZI modulator have been developed. Our model can be integrated to such electrode models in the future for complete evaluation of the device performance.

Furthermore, the analytical model has to be further evaluated against a wide range of experimental data, preferably for devices fabricated through different foundry
processes. The model might have to be modified, especially for the calculation of the depletion widths $w_{Dp,n}$, to account for the dopant variations due to the lateral straggling of the ions (for example, using models for linearly graded doping profiles [46,76]).

In Chapter 3, we have briefly outlined how the concepts used in the analytical model for the lateral $pn$ junction can be used to obtain similar models for vertical and interleaved $pn$ junctions. The idea of compact modelling can be extended to other active optoelectronic devices such as $pin$ phase shifters and photodetectors.

5.2 Towards microdisk modulators

In Chapter 4, we have shown that $f_{3dB}$ and $\Delta n_{eff}$ have opposite dependences on the geometry scaling parameter, $h_{slab}/h_{rib}$ of the rib waveguide. Thus, we have proposed that the most effective way of increasing $f_{3dB}$ is by reducing the series resistance, $R_{p,n}$ of the device. The highest contribution to $R_{p,n}$ is from the thin, lightly doped $w_{slab}$ sections (see Fig. 2.1). As it will be discussed later, a microdisk structure can effectively reduce $R_{p,n}$ by about 50% to yield improvements of a similar scale in the modulators frequency response. However, the use of microdisk modulators in the literature is rare [29], mainly because of the difficulty in single mode coupling and the difficulty in defining efficient $pn$ junctions (e.g., vertical junctions) in these type of modulators. Therefore, in this section, we propose and compare two novel microdisk modulators with a (1) lateral junction and a (2) vertical junction to a commonly found microring type modulator in terms of $C_{Dep}$, $f_{3dB}$ and $\Delta n_{eff}$.

5.2.1 Microdisk modulators with lateral and vertical $pn$ junctions

The cross-section schematics of the two microdisk modulators, with laterally and vertically oriented $pn$ junctions, and the microring modulator is shown in Figs. 5.4 (a), (b) and (c) respectively. The key device parameters are shown. The waveguide
Figure 5.4: Cross-section schematics of (a) a lateral $pn$ junction microdisk (b) a vertical $pn$ junction microdisk and (c) a lateral $pn$ junction microring modulator. Important device parameters are shown.

height, $h_{rib}$, is 220 nm and the slab height, $h_{slab}$ is 90 nm to be compatible with the IME silicon photonics platform [70]. We have used the same doping levels shown in Table. 2.1 (i.e $N_{A,D} = 5 \times 10^{17} \text{ cm}^{-3}$). The radius of all three structures is taken to be 10 $\mu$m, as a smaller radius can increase the resistance between the silicon and the contact metal inside the microring/disk by reducing the contact area at the silicon-metal interface.

The normalized electric field intensity of the fundamental TE mode of the microdisk is shown in Fig. 5.5. The optical mode is well confined near the edge of the microdisk and the field penetration into slab region is significantly lower compared to a microring mode. Because of this, heavily doped $n^{++}$ region outside the disk can
be brought closer to the disk, 400 nm in this case, without introducing additional losses. For the same reason, the $p^{++}$ region inside the disk is moved away from the edge of the disk, to 2 $\mu$m, to minimize its overlap with the optical mode. However, the increase in $R_p$ by lengthening the 220 nm $p$ doped region to the left of the $pn$ junction is much less than the decrease in $R_n$ by reducing the thin slab region to the right of the junction. As we shall see, the overall series resistance, $R_p + R_n$, of the microdisk device is reduced to almost half of the $R_p + R_n$ value of a microring device. The free-carrier induced loss from the holes is less than that from the electrons [11]. Hence, the microdisk structures in Fig. 5.4(a) and (b) are doped $p$ type towards the center of the microdisk to minimize the losses.

![Normalized electric field intensity profile of the fundamental TE mode of the 10 $\mu$m microdisk.](image)

The microring waveguide structure studied here (Fig. 5.4(c)) is much similar to the waveguide studied so far in this thesis (see Fig. 2.1 and Table 2.1); however, we have chosen $w_{rib} = 500$ nm and $h_{rib} = 220$ nm.

For simplicity, the $pn$ junction is located at the center of the microring waveguide in Fig. 5.4(c). For the lateral junction microdisk (Fig. 5.4(a)), the junction is located 500 nm away from the edge of the microdisk, which is approximately the center of the optical mode. The vertical $pn$ junction in the microdisk in Fig. 5.4(b) extends 600 nm into the microdisk covering most of the optical mode. In the calculations to
follow, there is still room for slight improvements in $\Delta n_{eff}$ by optimizing the location of the junction.

### 5.2.2 $f_{3dB}$ and $\Delta n_{eff}$ of microdisk modulators

The normalized frequency response obtained from Sentaurus simulation for the three devices at $V_{bias} = -1$ V is shown in Fig. 5.6. $B(\omega)$ is the frequency normalized susceptance, which can be expressed as $B(\omega) = \frac{C_{Dep}}{1 + \omega^2 (R_p + R_n)^2 C_{Dep}^2}$ using the small-signal model of the $pn$ junction (Fig. 4.1).

![Normalized frequency response for the microdisk and the microring structures.](image)

Figure 5.6: Normalized frequency response for the microdisk and the microring structures. The $f_{3dB}$ values are found at the points where the dashed line intersects with the curves.

Table 5.1 compares the the microdisk and microring devices in terms of their $C_{Dep}$, $f_{3dB}$ and $\Delta n_{eff}$. As expected, $f_{3dB}$ of the lateral junction microdisk is found to be greater than 100 GHz, where $f_{3dB}$ of the microring modulator is around 57 GHz (Fig. 5.6). Since they both have a small-signal capacitance of 2.9 pF/cm, the gain in $f_{3dB}$ is due to the lowered $R_{p,n}$ value of the microdisk. However, the lateral junction microdisk has a $\Delta n_{eff} = 4.5 \times 10^{-5}$ V$^{-1}$ (i.e., $V_\pi L = 1.722$ Vcm), which is about $0.65 \times$ that of the microring modulator. This is because the microdisk mode is far
less confined than the microring mode, the mode volume of the microdisk mode being almost twice the size of that of the microring mode. For the disk with the vertical junction, \( f_{3dB} = 30 \text{ GHz} \), much lower than the \( f_{3dB} \) of the ring. However, \( R_{p,n} \) value of this device is still much lower than that of the microring device. The lower value of \( f_{3dB} \) is because the \( C_{Dep} \) of this device is 7.5 pF/cm, almost \( 2.5 \times \) the \( C_{Dep} \) of other two lateral junction devices due to the large the \( pn \) junction. As a result, the vertical junction yields a much larger \( \Delta n_{eff} \) of \( 10.4 \times 10^{-5} \text{ V}^{-1} \) (i.e., \( V_r L = 0.745 \text{ Vcm} \)) because the junction overlaps the disk mode almost entirely.

Table 5.1: Comparison of microring and microdisk modulators

<table>
<thead>
<tr>
<th>Device type</th>
<th>( C_{Dep} ) (pF/cm)</th>
<th>( f_{3dB} ) (GHz)</th>
<th>( \Delta n_{eff} ) (V(^{-1}))</th>
<th>Loss (dB/cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>microdisk - lateral</td>
<td>2.9</td>
<td>&gt;100</td>
<td>( 4.5 \times 10^{-5} )</td>
<td>12.3</td>
</tr>
<tr>
<td>(Fig. 5.4 (a))</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>microdisk - vertical</td>
<td>7.5</td>
<td>30</td>
<td>( 10.4 \times 10^{-5} )</td>
<td>7.9</td>
</tr>
<tr>
<td>(Fig. 5.4 (b))</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>microring (Fig. 5.4</td>
<td>2.9</td>
<td>57</td>
<td>( 6.9 \times 10^{-5} )</td>
<td>12</td>
</tr>
<tr>
<td>(c))</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*All the devices are biased at -1 V.

We have shown that the microdisk modulators can be designed to have either a (1) large \( f_{3dB} \) value using a lateral \( pn \) junction or (2) large \( \Delta n_{eff} \) with a reasonable \( f_{3dB} \) using a vertical \( pn \) junction, when compared to microring modulators of similar radius and doping.

Although we have shown modulator structures with large 3 dB bandwidths in the electrical domain (\( f_{3dB} \)), ultimately, the modulation bandwidth of the microring/disk modulators is also limited by the photon cavity life time of the resonant structure [75]. The 3 dB modulation bandwidth, \( f_{3dB-total} \), determined by \( f_{3dB} \) and the photon cavity
lifetime $\tau$, can be calculated by,

$$\frac{1}{f_{3dB-total}^2} = (2\pi\tau)^2 + \frac{1}{f_{3dB}^2},$$

(5.1)

where, $\tau = \frac{\lambda Q}{2\pi c}$, and $Q$ is the quality factor of the microring/disk [75]. The $f_{3dB-total}$ calculated according to Eq. (5.1), for the microring/disk modulators shown in Fig. 5.4, is plotted in Fig. 5.7 as function of $Q$-factor. The bandwidth limited by the $Q$-factor alone is shown in black-dashed lines. From Fig. 5.7, it is evidenced that the large $f_{3dB}$ of the lateral $pn$ junction modulators are masked by the $Q$-factor limited bandwidth. Furthermore, the low $\Delta n_{eff}$ of the lateral structures would not be able to produce the required modulation depths at lower values of $Q$ ($< 10^4$). On the other hand, the vertical junction microdisk with a $Q$-factor of about 7,000-10,000 can be expected to reach $f_{3dB-total}$ of about 20 GHz. They should have good modulation efficiencies because of the high $\Delta n_{eff}$.

The main difference between the vertical junction microdisk structure that we have proposed in this section and the microdisk modulators demonstrated by Watts
and co-workers [21, 29] is the presence of the slab region in our structure. Because of the orientation of the electrodes in [21, 29], the $pn$ junction spans across the entire microdisk, while the optical mode is concentrated to a region of 1 $\mu$m close to the perimeter of the disk (see Fig. 5.5). The presence of the slab in the device proposed here allows us to define the $pn$ junction just long enough to increase the overlap with the optical mode and hence optimize the useful $C_{Dep}$ for optical modulation. Therefore, while the modulator presented in [29] operated at 12.5 Gbit/s, with an energy consumption of 3 fJ/bit, we expect our device to reach $f_{3dB-total}$ of above 20 GHz, with a similar energy per bit value.

### 5.2.3 Single mode coupling to microdisk modulators

As we have mentioned before, it is difficult to efficiently couple light into the fundamental mode of a microdisk resonator. The microdisk supports multiple transverse modes. The light scattering at the bus waveguide and the disk can cause a significant proportion of the coupled light to excite higher order modes. However, using a “pulley-coupled” structure [78], where the bus waveguide is curved around the microdisk, we have demonstrated efficient coupling to the fundamental disk mode on the SOI platform.

Fig. 5.8 [left side] illustrates the more commonly found point-coupling and Fig. 5.8 [right side] the pulley-coupling geometries. Key parameters are shown in the figures. The phase matching condition for the pulley-coupled disk is reached when $n_{wg}R_{wg} = n_{disk}R_{disk}$, where $n_{wg}$ and $n_{disk}$ are the mode indices of the curved waveguide and the disk and $R_{disk}$ and $R_{wg}$ are the radii of the waveguide and the disk. In effect, this is matching the phase velocity of the waveguided mode with that of the disk mode. Therefore, even a slight mismatch can decouple the two structures significantly by increasing the phase walk-off between the two modes. The length of the pulley-coupler is given by $2R_{wg}\theta$.

Point-coupled and a pulley-coupled microdisks with were fabricated in SOI (220 nm thick Si on a 3 $\mu$m thick oxide layer). We have used the standard electron-
beam lithography process at the University of Washington Microfabrication Facility [79]. The devices were etched leaving a Si slab region with a height of 90 nm and the fabricated devices were clad with a plasma-enhanced chemical vapor deposited (PECVD) oxide to mimic standard IME foundry fabrication process.

Fig. 5.9 compares the transmission spectra of a point-coupled and a pulley-coupled microdisk ($R_{\text{disk}} = 20 \, \mu\text{m}$ and $\theta = \pi/4$). While the point-coupled microdisk exhibits significant coupling to a higher order mode, the pulley-coupled disk only couples to the fundamental mode.

![Figure 5.8: Point-coupled [left side] and pulley-coupled [right side] microdisks.](image)

![Figure 5.9: Transmission spectrum for the point-coupled (blue) and the pulley-coupled (red) microdisk devices ($R_{\text{disk}} = 20 \, \mu\text{m}$).](image)
5.2.4 Future work on microdisk resonators

In this section, we have investigated microdisk modulators as an alternative to the widely used microring modulators. We have shown that microdisk modulators with a slab region can reduce the large $R_{p,n}$ of SOI modulation diode and increase $f_{3dB}$. We have also demonstrated efficient single-mode coupling to a microdisk on the 220 nm thick SOI platform.

As a first step we have completed designing microdisk modulators with lateral $pm$ junctions through the CMC-IME process [80]. Vertical $pm$ junctions were not available. However, foundries are now in the process of developing vertical $pm$ junctions that are similar to that of the modulator we have proposed in this section (Fig. 5.4(c)) [81]. Therefore, further work can be directed towards the development of vertical junction microdisk modulators. Incorporating high-speed $pm$ junctions (with reduced $R_{p,n}$) in coupling-modulated microdisks may help mitigate the bandwidth limitations due to the photon cavity lifetime of the resonator [82]. We believe such modulators will meet the high-speed and low-power performance requirements of the next generation on-chip electro-optical modulators.
Chapter 6

Conclusions

6.1 Achievements of this thesis

In this thesis, we have presented the first analytical model of the depletion region and the depletion capacitance of lateral SOI modulation diodes. We have presented analytical/semianalytical expressions for the 3 dB roll-off frequency and the modulation efficiency. We have studied how the performance of the modulation diode is scaled with key parameters of the optical waveguide.

The shape of the depletion region at the edge of an optical modulator is widened as a result of the fringing electric fields from the depletion region that extend into the cladding. This widening is significant (typically about 25% of the total depletion width) and increases the depletion capacitance of the device. We have used a conformal mapping technique to obtain the shape of the depletion region by solving the Poisson’s equation in 2D. The shape obtained by our analysis is also known by the name “π/2 Borda profile” in hydrodynamics and closely matched numerically simulated results.

To calculate the depletion capacitance, $C_{Dep}$, we have approximated the 2D depletion shape by a pair of parallel plate conductors and a pair of coplanar waveguides, of which the capacitance is readily calculated using existing formulae. We have found excellent agreement upon comparison of analytically obtained results for $C_{Dep}$ with the
results from full 2D FEM simulations. The difference between the two methods is less than 5% for a cases with different waveguide dimensions, doping and bias conditions. The key feature of our analytical model is its accuracy in calculating the capacitance due to the fringing electric fields, which can be typically as large as 20% of $C_{Dep}$.

We have then used the analytical $C_{Dep}$ with the analytically calculated diode series resistance, $R_{pn}$, to obtain the small-signal model and the modulation bandwidth, $f_{3dB}$. The analytical model of the depletion region was then combined with the free carrier dispersion index change to quantify the modulation efficiency, $\Delta n_{eff}$. The results, for $f_{3dB}$ and $\Delta n_{eff}$, closely matched the simulations.

The slab height ($h_{Slab}$) and rib height ($h_{rib}$) of the optical waveguide play an important part in the design of the optical modulator. We have quantified the effects of the scaling of $h_{slab}/h_{rib}$ on the diode performance and have found a trade-off between $f_{3dB}$ and $\Delta n_{eff}$ with the scaling. Optimum value for the figure-of-merit parameter $\Delta n_{eff} \times f_{3dB}$, is obtained when $h_{slab}/h_{rib} \sim 0.6$, regardless of the value of $h_{rib}$.

As a result of the fringing electric fields, a large percentage of $f_{3dB}$ is lost in return for a small gain in $\Delta n_{eff}$. Hence, we have characterized the fringe capacitance as a parasitic effect. Small gains in $f_{3dB}$ can be obtained by replacing the cladding, usually SiO$_2$, with a material with a lower dielectric coefficient.

In light of our analysis of $f_{3dB}$, $\Delta n_{eff}$, and fringe capacitance effects, we find that the most effective method of increasing $f_{3dB}$ without affecting $\Delta n_{eff}$ is by reducing the $w_{slab}$ parameter (the distance to the $n^{++}, p^{++}$ sections from the edge of the waveguide). This is equivalent to reducing $R_{p,n}$, of which the highest contribution is from the thin lightly doped slab regions. Depending the value of the scaling parameter $h_{slab}/h_{rib}$, typically, $w_{slab}$ can be reduced to be in the range of 200 nm to 500 nm without introducing additional losses due to the mode overlap with the $n^{++}/p^{++}$ regions. This reduction of $w_{slab}$ can contribute to significant gains in $f_{3dB}$ up to 35 GHz.
6.2 Future work

The work presented in this thesis can direct future research efforts in two main directions. Firstly, further work on development, numerical and experimental verification of analytical models of optoelectronic devices is required before active photonic circuits can reach large-scale integration densities. Secondly, starting from physical insights gained from the analytical models, work could be directed towards the optimization and performance enhancement of the SOI modulation diodes.

As we have thoroughly compared our analytical results with numerical simulations, the next step would be to verify the analytical results with measurements. As a first step, we have compared our results for $C_{Depl}$ and $\Delta n_{eff}$ with those presented in [66] in this thesis. For the complete evaluation of the device performance, the effects of the metal contacts has to be taken into account. Our model can be easily integrated into existing models particular electrode configurations [36, 41, 42]. As we have outlined in this thesis, concepts used in the derivation of the model for the lateral $pn$ junction can be extended to describe vertical and interleaved $pn$ diode modulators. Further work could be on the development of circuit models for other active optoelectronic devices such as $pin$ phase shifter elements and photodetectors.

In this thesis, we showed microdisk modulators can improve the modulation bandwidth by lowering $R_{p,n}$, and increase the modulation efficiency by using vertical junctions. We also demonstrated efficient single-mode coupling to the microdisk devices on the SOI platform. As a first step, we have designed microdisk modulators with lateral $pn$ junctions. Future work on microdisk resonators can be first directed towards realizing the vertical junction modulators proposed in this thesis. Research into coupling modulation of these devices may yield further performance enhancements. As the modulation bandwidths reach above 60 GHz, further improvements would require developments in CMOS integrated driver circuitry. We envision that the analytical circuit models of SOI modulators would be invaluable for research and development of the CMOS driver circuits.
Bibliography


M. J. Kumar, S. K. Gupta, and V. Venkataraman, “Compact modeling of the effects of parasitic internal fringe capacitance on the threshold voltage of high-


