REAL-TIME SIMULATION OF MODULAR MULTILEVEL CONVERTERS

by

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Graduate Department of Electrical and Computer Engineering
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Abstract

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This thesis presents the real-time simulation of a realistic-size Modular Multilevel Converter (MMC) based High-Voltage Direct Current (HVDC) transmission system. Based on the concept of time-varying Thevenin equivalent, a computationally efficient model of the MMC is developed and deployed on an FPGA platform.

The salient features of the developed MMC model are: (i) The decoupling of the solutions of the MMC model and the of the rest of the system, (ii) it provides an equivalent representation of the full MMC, (iii) it is suitable for parallel implementation.

The model is used as part of the simulation of the 401-level France/Spain MMC-HVDC link between, in which 2 separate MMCs are included, showing the expandability of the designed system to larger DC grid scenarios. Hardware in the loop (HIL) testing capabilities of the system are also demonstrated with the addition of an external controller to the simulation system.
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Chapter 1

Introduction

1.1 Statement of Problem

Traditionally, bulk electric high-voltage transmission systems have been based on alternating current. This is a sensible choice, as this is how power is generated and large loads are operated. This can also be justified by the relative simplicity of AC transformers, which allow high voltage transmission, reducing losses. There are, however, several advantages to using direct current for high-voltage transmission. They include: lower transmission losses, the capacity to transfer more power over the same right of way and the ability to interconnect systems that are not synchronized or use different frequencies. Substations designed to transfer between AC and DC systems are required at each end of an high-voltage direct current (HVDC) transmission line. These converter stations provide additional controls to the transmission system which can help improve its stability.

These advantages, however, can be negated by the costs associated with building and operating the converter stations as well as the losses created by the switching elements required to invert or rectify the power at each end of the DC line. Traditional 3-phase converter systems, either the current-sourced converters (CSC) (based on thyristors) or the voltage-sourced converter (VSC) (based on Insulated Gate Bipolar Transistors (IGBTs)), present limitations.

CSCs require large quantities of reactive power during operation, they cannot control real and reactive power independently and generate low frequency harmonics that require expensive filters.

Conventional 2-level VSCs generate large high frequency harmonics and cause higher losses compared to CSCs due to the fast switching of the IGBTs during operation. They also require a large number of switches connected in series, providing multiple failure points.

In recent years, a new configuration of IGBT based VSC, the modular multilevel converter (MMC), has been commercially developed and presents multiple advantages over previous types of converters. Amongst them, one can note:

1. Modularity & Scalability

2. Lower switching frequency of the individual levels, compared to conventional VSCs, to obtain the same waveform properties, at lower losses

3. Improved reliability as the converter can function even when some switches or modules fail or experience problems
4. Very high number of levels are possible, further increasing efficiency (by reducing the switching frequencies of the individual switches for the same equivalent switching frequency) and availability

5. Significant reduction of the magnitude of the harmonics generated, reducing and possibly eliminating the need for filter banks

6. No reliance on a large inductance to force current continuity during switching, as is required for commutation of CSCs. In some cases, the requirements for expensive transformers is removed.

All the advantages of the modular multilevel converter make it an attractive option and may help alleviate the drawbacks of conventional converters in modern transmission systems.

Work was performed and published on the simulation and control of MMCs over the last few years [1–20], but much still remains to be understood and tested in terms of dynamic performance, especially for converters configured with a large number of modules, before this type of converter can be fully deployed in large scale applications.

The goal of this thesis is to develop a model and perform studies on the dynamic operation of the of the MMC converter in the Real-Time Digital Simulator (RTDS). Studies can and have been performed with off-line simulators, but there are some drawbacks to this method:

1. Off-line simulators do not allow for Hardware in the Loop (HIL) testing.

2. The large number of modules (up to several thousands per converter) makes simulation run times extremely long. This has led to the development of simplified models [16–18].

3. Several processes are required for the correct operation of the MMC, such as sorting of the capacitor voltages, which can be updated on every cycle in an off-line simulation, but may not be possible to perform at these speeds in real-time.

4. Off-line simulators may not correctly represent some potential real-life issues such as, quantization errors, communication and transmission delays.

The limitations in computing power for the off-line simulators are present in real-time simulations as well, and it will not be a trivial task to overcome them. The MMC modules will be simulated using a high-speed FPGA, to allow for fast computation of all module voltages. This FPGA will require an interface to the real-time simulator, which will handle the simulation of the external electrical system. In order to perform HIL testing, a separate platform will be used for MMC controller implementation, also requiring a link to the high-speed FPGA and RTDS.

This separate controller represents a high-level controller, generating the required voltage commands to the individual arms of the converter. Separate arm controllers would then provide the switching signals to the appropriate modules. The controller is also equipped with an internal FPGA so that the fast control loops can be implemented. This experimental setup will thus recreate possible bottlenecks and limitations of communication between the controller and the converter itself.

There will be three main steps to complete this work:

1. Implement the system using RTDS, the high-speed FPGA and the external controller.

2. Verify the correct operation of the system and validate the results by comparing them with off-line simulation results.
3. Study the response of the system under dynamic conditions.

Once completed and verified, this system will enable realistic, real-time simulations of MMCs, helping in the improvement of the understanding of its operation and limitations in a practical system.

1.2 Literature Review

MMC-based systems have been simulated and built. Many papers present results of off-line simulations of the MMC converters using simulation packages such as EMTP-RV, PSCAD-EMTDC and Matlab. Most of these models and simulations use a relatively small number of modules per arm (between 4 and 20) to keep the simulation durations at a reasonable level or due to software limitations on the size of systems, and study relatively simple dynamic cases (if any).

Reference [1] presents a voltage balancing technique with a 4 level model for both simulations (off-line) and experimentation. Dynamic cases study the effects of a change in current command on the converter.

Reference [2] also presents a 4 level converter and simulations.

Reference [3] uses off-line simulations with a 4 level converter and experiments with a 2 level version to test a new control technique. Dynamics cases study the response to a change in DC voltage command and activation/deactivation of capacitor voltage balancing control.

Reference [4] uses off-line simulation to study a back-to-back system with one AC side as a two-phase system and the other one as a three phase system, both with 11 modules per leg. Dynamics simulations cover power flow reversal and changes in commanded DC voltage.

Reference [5] tests the effect of a change in the load phase angle on the harmonics of a system containing 10 levels using off-line simulation.

Reference [6] presents the results of simulations of a 6 level MMC placed in back-to-back configuration, with simulations of changes in real and reactive power on each end, change in DC voltage levels as well as a single phase-fault study.

Reference [7] investigates the MMC in its STATCOM configuration, based on simulations in PSIM and actual experiments. The MMC model used for simulations contains 22 levels; the experiment was limited to a single level.

Reference [8] describes a module voltage balancing technique and uses a 4-level physical converter to test its effectiveness.

Reference [9] presents an actual converter built for experiments consisting of up to 17 modules per level, which represents the largest experimental device reported in the literature.

Reference [10] presents a technique for utilizing redundant and spare modules and performs off-line simulations for a system of 30 modules (28 modules and 2 redundant levels).

Reference [11] presents a review of the current status of the research in voltage equalization between the modules as well as controls, focusing on selective harmonic elimination (SHE), and shows off-line simulations of a 10 module converter.

Reference [12] discusses control of the MMC using space-vector modulation and demonstrates the operation using a 22-level off-line model.

Reference [13] presents and simulates a fundamental frequency switching method using 12 modules per converter arm.
Reference [15] focuses on the circulating currents controls and presents the results of off-line simulation based on 20 module per converter arm.

References [16] and [17] present simulation results of models which have more than 200 levels per arm. These simulations have been performed with simplified models, using off-line simulators.

As can be seen, most papers present off-line simulations with a relatively small number of levels, sometimes coupled with experiments, usually at an even lower number of levels. The experimental results take into account many more potential bottlenecks than off-line simulations, but they quickly become impractical as the number of levels increase, making it difficult to study the effects of adding more and more levels to the converter, which can be more practically done using real-time simulations.

Reference [18] proposes a more efficient algorithm to simulate converters with a large number of levels, relying on the fact that simulation packages represent switches with a small resistance in the ON state, and a large one in the OFF state. The authors shows that the modified model faithfully represents a full converter station (with the exclusion of the switching losses). This method will be the basis of the model implemented in this thesis.

To the best of the author’s knowledge, reference [19] represents the only available publication on real-time simulation of MMCs. The model presented in this paper has 49 levels.

The only other document available covering real-time simulations of MMC comes from RTDS directly and presents their efforts to reproduce the converter using the RTDS platform. This implementation required 5 different processors (2 simulating the modules (1 for the top arms and 1 for the bottom ones) and 3 (one per phase) for the MMC controls (sorting and selection)) per converter, for a total of 10 for a 2 converter HVDC link. By comparison, the system proposed in this thesis will require only 2 processors (1 for each converter (module simulations and voltage selection) and 1 for the controller), or 4 for a 2 converter HVDC link system.

1.3 Thesis Objectives

The main objective of this thesis is to develop a working model of the MMC which can be used for real-time simulation, representing a realistically sized high power MMC system, while minimizing the hardware requirements. The final goal is to simulate in real time a MMC containing a total of 2400 modules, based on the configuration and specifications of the HVDC-link currently under construction between France and Spain [16], which is slated for commissioning in the 1st half of 2014.

To ensure that the developed model is accurate, its performance must be compared to that of another model which is known to be accurate. In this thesis, the comparison will be made with the model developed in the off-line simulation platform PSCAD.

This thesis proposes to reach this goal in the following way:

In the first part of the thesis (chapters 2, 3 and 4), the theory behind the operation of the MMC is presented, by describing the converter’s operation, reviewing control methodologies presented in the literature and creating a test system to be used for simulations.

The following chapters (5 and 6) validate the performance of the real-time system by comparing it to that of the model implemented in PSCAD.

Finally, chapter 7 studies the performance of the real-time model in an HVDC link configuration. This test system includes hardware in the loop testing by introducing a MMC controller implemented on a separate hardware platform.
Chapter 1. Introduction

1.4 Thesis Layout

In the second chapter, the principles of operation and modelling of the MMC will be covered, by first describing the structure and operation of a single module, which will then be included in a single-phase model and finally in a three-phase model.

The third chapter covers the control and switching operations of the converter, reviewing different switching techniques and justifying the selected one. The capacitor voltage sorting strategy and balancing technique is also be presented.

The studied system and its implementation in the developed real-time simulation platform, will be presented in the fourth chapter.

The fifth chapter validates the MMC model used in the real-time simulator by comparing simulation results for a complete converter model consisting of 12 module per arm and including all the necessary switches and controls, to a computationally efficient representation, as implemented in the real-time simulator. Both cases are simulated using the off-line simulation software PSCAD.

Chapter six scales up the efficient MMC model to 400 modules per arm, as in the real-time implementation, and compares the results of simulations performed off-line using PSCAD with those of the real-time simulator, for a single MMC converter station.

The validated MMC implementation is then deployed as part of a HVDC transmission system in chapter seven, and studies are performed in real-time, with a MMC controller implemented on a separate hardware platform and inserted as hardware in the loop, to assess its dynamic performance.
Chapter 2

MMC Principle of Operation and Modeling

The MMC is a type of Voltage Sourced Converter, thus the overall theory and operation principles of the conventional VSCs apply to it. However, there are important differences in the operation of the MMC. Whereas, in traditional IGBT based converters, the switches are connected in series and must be gated simultaneously, the structure of the MMC allows for each module to operate individually. One must first look into the individual module’s structure in order to understand the operation of the converter as a whole.

This chapter presents the principle of operation of the MMC by first describing the operation of a single module, then combining modules to form a single and three-phase converter.

2.1 Module Structure and Operation

The module represents the basic building block of the MMC. Depending on the size of the converter, upwards of 3000 modules may be used. Each individual module is composed of the same basic elements: two IGBTs with anti-parallel diodes and a capacitor. The circuit diagram of a module is shown in Figure 2.1.

Additional protection and bypass circuitry may also be present [16], [22]:

- An anti-parallel thyristor to protect the diodes and switches from the large current experienced during a DC-side fault, until the circuit breaker can be opened.

- A mechanical bypass switch to disconnect the module in case of a failure.

These are not shown here as they are not involved in the normal operation of the module.

The switches are operated to control the output voltage of the module.

Figure 2.2 shows the possible current paths through the module. In sub-figure (a), the upper IGBT (S1) is conducting, with the current flowing out of the positive terminal. If the current is direction reversed, as in sub-figure (b), the upper anti-parallel diode (D1) ensures continuity, allowing current flow while the lower IGBT (S2) is OFF. In both cases, the capacitor is inserted in the circuit, and the output voltage \(v_{\text{out}}\) is equal to the capacitor voltage \(v_c\) (neglecting the path voltage drop).
Sub-figure (c) shows the lower IGBT (S2) conducting with the current flowing out of the negative terminal. As was the case for the upper half of the module, if the current direction is reversed, the lower diode (D2) ensures continuity if the upper IGBT (S1) is not conducting (sub-figure(d)). When the current flows through the lower IGBT (S2) or diode (D2), the capacitor is bypassed and the output voltage of the module is effectively zero (neglecting the path voltage drop).

Both IGBT switches must never be ON at the same time to prevent a short-circuit across the capacitor. If both switches are OFF, the diodes provide continuity; however there is no direct control on the output voltage as it is dictated entirely by the current direction.

Based on Figure 2.2, an individual module can then be in one of 4 states:

(a) Current out of the positive terminal: the capacitor is inserted by closing the upper IGBT.

(b) Current out of the negative terminal: the capacitor is inserted by opening the lower IGBT (the
upper diode ensures continuity).

(c) Current out of the negative terminal: the capacitor is bypassed by closing the lower IGBT.

(d) Current out of the positive terminal: the capacitor is bypassed by opening the upper IGBT (the lower diode ensures continuity).

It is thus possible to connect or bypass the module capacitor irrespective of the current direction. Depending on the direction of the current flow, the capacitor will either be charging or discharging, which means that the capacitor voltage will continually be changing. The capacitor used in the modules has to be sized properly to limit the voltage ripples during normal operation. Controls also have to be designed specifically to limit these fluctuations. More on this in chapter 3.

It is this ability to control the output voltage of the module (either to the capacitor voltage or to 0V) that will be put to use to control the MMC. With multiple modules connected in series, the output voltage of the converter can be adjusted by inserting or bypassing individual modules. This will be covered in more details in the next section.

2.2 Multi-Module Structure and Operation - Single-Phase MMC

In a regular 2-level VSC, assuming the voltage source on the DC side to be fixed, the converter simply connects the positive or negative side of the DC bus alternatively to the AC side. By appropriately switching the connection between the positive and negative voltage, the signal created on the AC side is a series of pulses containing the required frequency and higher harmonic signals, which are removed using the appropriate filters.

If only 2 modules were used in the MMC (one for the positive DC connection and one for the negative one), the operation of the resulting MMC would be equivalent to a conventional VSC. However, in the case of the MMC, \( N \) modules are connected in series on either side of the AC connection point to form a converter leg as shown in Figure 2.3.

The AC system is connected to the mid-point of the leg. Each half of this leg is called an arm of the converter. In this topology, it is possible to control the number of inserted and bypassed modules on each side of the central connection point, allowing for more precise control of \( v_{AC} \).

The following parameters are defined on the figure:

- \( v_S \) defines the voltage at the AC system source.
- \( R \) and \( L \) represent the lumped system resistance and inductance between the source and converter.
- \( v_{AC} \) defines the voltage at the converter connection point with the AC system.
- \( i_{AC} \) defines the current flow in the AC system.
- \( R_S \) and \( L_S \) represent the resistance and inductance of each arm of the converter. A physical inductance, with a typical value of a few tens of mH is located in each arm.
- \( v_L \) and \( v_U \) define the total voltage of the capacitors of the inserted modules of the lower and upper arms respectively.
Chapter 2. MMC Principle of Operation and Modeling

- \( i_L \) and \( i_U \) define the currents flow through the lower and upper arms respectively, with the positive direction defined as flowing from the positive to the negative DC bus terminals.

- The DC bus voltage is defined as \( V_{DC} \) with the positive terminal voltage defined as \( +\frac{V_{DC}}{2} \) and the negative terminal voltage as \( -\frac{V_{DC}}{2} \).

In a MMC, the energy of the DC bus is not stored in a single large capacitor, as it would be in a conventional VSC, but rather divided among the capacitors of the individual modules. The controls have to be designed to keep the voltage distribution as even as possible between the modules of an arm. Techniques to achieve this even distribution will be discussed in the next chapter. For now, the assumption is made that the control system maintains an even voltage distribution among the modules.

In order for the individual module voltages to remain constant over time, the total number of connected modules in a leg must always remain the same. Assuming \( N \) modules per arm, using the case where all the upper arm modules are inserted and none of the lower arm ones are, the average voltage across the module capacitors \( (V_{C_x}) \) will be:

\[
V_{C_x} = \frac{V_{DC}}{N} \quad (2.1)
\]

If a module is inserted in the lower arm, but no module from the upper arm is bypassed, there would then be \( N + 1 \) modules inserted in the system and, in order to satisfy KVL, their average voltage would become \( \frac{V_{DC}}{N+1} \), thus the average module voltage would change. To prevent this from happening, only combinations of \( n \) modules from the upper arm and \( N - n \) from the lower arm are used to obtain the desired output voltage.
Because only half the modules are ever inserted in the system at any instant, the total voltage across all the capacitors (inserted and bypassed) is $2V_{DC}$.

Figure 2.4 shows the output voltage (at the AC connection point) of an ideal MMC (no losses), with 10 modules per arm and the DC bus voltage ($V_{DC}$) is 10V ($\pm$5V). This is a simple case which will serve to illustrate the operation of a MMC under normal condition. The assumption is made here that the voltage is evenly distributed between the capacitors and that they are large enough so that the voltage does not fluctuate (this is not the case in a real converter, but it is used here for the purposes of this explanation).

As can be seen from the figure the output voltage, even for a relatively low number of levels such as is the case here, tracks a sinusoidal wave quite well. On the figure, one can see 4 different sections:

A This section of the figure shows the maximum output voltage of the converter. In order to obtain this maximum voltage, all the modules in the upper arm are bypassed such that $V_{DC}/2$ is connected directly to the output, and all the modules in the lower leg are inserted in the system such that the DC-side voltage is not short circuited. The total voltage across the lower arm modules is thus equal to $V_{DC}$ (10V in this case).

B In this section, the output voltage is progressively lowered to track the sinusoidal waveform. In order to do so, voltage must be inserted between the positive DC voltage and the AC connection point. As such, modules from the upper arm ($SM_x$) are inserted in the system. In order for the number of inserted modules to remain constant; one module must be bypassed every time another one is inserted. Thus, for each module inserted in the upper arm, one is bypassed in the lower arm. After one upper arm module insertion and lower arm module bypass operation, the output voltage thus becomes 4V ($V_{DC}/2 - V_{module}$). As more modules from the upper leg are inserted and modules from the lower leg bypassed, the AC connection point voltage decreases.

C Once all the upper arm modules have been inserted and all the lower arm modules are bypassed, the output voltage of the converter is now $-V_{DC}/2$ (-5V).

D To increase the output voltage once it has reached the minimum, modules from the lower arm must now be inserted and the same amount of modules from the upper arm bypassed.
This example tracks a sinusoidal wave of maximum amplitude. The power flow through the converter is controlled by adjusting the number of inserted modules in each arm of the leg to obtain the desired mid-point voltage. Based on the desired power flow, the commanded output voltage may not require this maximum amplitude command. It is, of course, possible to generate smaller output voltage simply by never reaching the limit cases where all the modules in an arm are inserted (or bypassed), adjusting the value of the output voltage by inserting (or bypassing) modules in the upper or lower arm as necessary.

It is thus possible, by inserting the appropriate number of modules in each arm, to generate \( N + 1 \) voltage levels by inserting anywhere from 0 to \( N \) modules from the upper arm and the complementary number of modules from the lower arm. The number of inserted modules in each arm of the converter can be controlled, generating an adjustable voltage in each arm, represented as voltages \( v_L \) and \( v_U \), which are the voltages required through each arm to generate the desired voltage at the AC connection point.

The output voltage of the MMC can then follow a staircase like pattern with each insertion or bypass of a module only affecting the AC connection point voltage by the value of the voltage across its capacitor, which makes it possible to follow a desired AC signal more closely than would be possible in traditional converters, creating much less harmonic distortion.

The MMC configuration also offers more advantages over the traditional VSC:

1. Not all the switches in a leg are opened or closed at the same time as they would in a two-level VSC, but they are operated at different time instants to follow the sinusoidal reference command more closely, the switching frequency of each switch can thus be low, while still generating a large "apparent" switching frequency.

2. The voltage blocking requirements of an individual switch is limited to the voltage across the module's capacitor.

3. If enough modules are used, the voltage across each switch can be low enough not to require series-connected switches. In a 2-level VSC, each arm (valve) must be able to block several hundreds of kVs while open. An IGBT is usually rated for a few kVs only, so multiple switches must be connected in series to achieve the desired blocking capabilities. During switching, all these devices must operate together. If one IGBT operation is delayed, it is exposed to a high voltage, which could damage it. In the case of the MMC, the high number of modules, each only blocking the voltage across its internal capacitor eliminates this drawback and improves the failure rate.

4. The modular concept allows operation even if some modules have failed. Failed modules can simply be bypassed, and kept bypassed until it is possible to replace them, and operation can continue. The DC bus voltage is then divided among the remaining \( N - 1 \) modules and normal operation can continue.

5. It is possible to design a MMC converter with spare modules which can be used if one module were to fails. If spare modules are available, they can be inserted in the arm as needed.

Multiple techniques can be used to select how many and which modules in each arm are inserted into the circuit and the instants when they are inserted or bypassed. They will be discussed in the next chapter.

As shown in Figure 2.3, series inductors \( (L_S) \) are also present in each arm. In the single phase case, their main use is to limit the fault current. In the event of a fault on the DC-bus, the rapid rise in
current through the converter arms can be limited by the inductors. The presence of these inductors in the MMC is possible because there is always a path between the AC connection point and both the positive and negative terminals of the DC bus and thus current is always flowing in each arm of the converter. This is not the case in conventional VSCs where the AC connection point is alternatively connected to either the positive or negative terminal. If inductors were present in the converter arms (valves), they would prevent such fast changes in current flow in the arm (valve) and generate large voltage peaks every time switching occurs. This represents another difference between the MMC and traditional VSC-based converters.

2.2.1 Converter Model (Single-Phase)

Capacitor Voltages

The modules are connected in series. As such, when they are inserted in the system, their internal capacitors \( C_{\text{module}} \) are connected in series as well. The equivalent inserted capacitance \( C_i \) of a converter arm when \( N \) modules are inserted is thus equal to the equivalent capacitance of \( N \) series connected module capacitors.

\[
C_i = \frac{C_{\text{module}}}{N}. \tag{2.2}
\]

As previously noted, \( N \) will be constant for the converter leg. As such, the equivalent total capacitance of a converter leg will be constant as well. As the capacitors voltage fluctuates with current flow, or if the voltage is not perfectly distributed, the total voltage across the leg will vary, but keeping the number of inserted modules constant and using an effective voltage balancing strategy will ensure that no large fluctuations in total voltage are seen during normal operation.

Letting \( v \) be the total voltage across the inserted capacitors in a converter arm. Given a current \( i \) flowing in that arm at that instant and knowing the value of the equivalent inserted capacitance \( C_i \) from (2.2), it is possible to determine the rate of change in voltage of the capacitors:

\[
\frac{dv}{dt} = \frac{i}{C_i}. \tag{2.3}
\]

With the currents in the lower and upper arms (represented here by \( i_L \) and \( i_U \) respectively) both defined as flowing from the positive to the negative side of the DC link, as in Figure 2.5, and \( n_U \) and \( n_L \) representing the number of modules inserted in each arm; the change in voltage for each arm can be defined from (2.2) and (2.3) as:

\[
\frac{dv_U}{dt} = \frac{n_U i_U}{C_{\text{module}}}, \tag{2.4}
\]

\[
\frac{dv_L}{dt} = \frac{n_L i_L}{C_{\text{module}}}. \tag{2.5}
\]

System Model

Using the assumption that the capacitor voltages are evenly distributed between the modules, one can use KVL on each arm to derive the model equations. Defining the direction of the arm currents as flowing from the positive to the negative side of the DC link and representing the average voltage in a
Figure 2.5: Single phase MMC

capacitor of the upper or lower arm as $v_{CU}$ and $v_{CL}$ respectively, based on the values defined in Figure 2.5:

\[
\begin{align*}
  v_{AC} &= \frac{V_{DC}}{2} - R_S i_U - L_S \frac{d}{dt} i_U - n_U v_{CU}, \\
  v_{AC} &= -\frac{V_{DC}}{2} + R_S i_L + L_S \frac{d}{dt} i_L + n_L v_{CL}.
\end{align*}
\]

Using KCL, the output current can be represented by the sum of the currents of the 2 arms; i.e., $i_{AC} = i_U - i_L$ (the negative sign is due to the reference direction). Adding (2.6) and (2.7), using this representation of the output current, and simplifying the last terms of both equations by representing them as a single term ($n_U v_{CU} = v_U$ and $n_L v_{CL} = v_L$), one gets:

\[
\begin{align*}
  2v_{AC} &= \frac{V_{DC}}{2} - R_S i_U - L_S \frac{d}{dt} i_U - v_U - \frac{V_{DC}}{2} + R_S i_L + L_S \frac{d}{dt} i_L + v_L, \\
  2v_{AC} &= R_S (i_L - i_U) + L_S \frac{d}{dt} (i_L - i_U) - v_U + v_L, \\
  v_{AC} &= -\frac{R_S}{2} (i_U - i_L) - \frac{L_S}{2} \frac{d}{dt} (i_U - i_L) + \frac{v_L - v_U}{2}, \\
  v_{AC} &= -\frac{R_S}{2} (i_{AC}) - \frac{L_S}{2} \frac{d}{dt} (i_{AC}) + \frac{v_L - v_U}{2}.
\end{align*}
\]

Equation (2.8) illustrates the fact that the arm inductor and its internal resistance have a direct
effect on the output voltage through the current flowing in the converter. As seen earlier, this inductor is not present in the conventional VSC system and will have an effect on the controls of the MMC as will be later discussed in Chapter 4.

2.3 Multi-Module Structure and Operation - Three-Phase MMC

The next logical step in the implementation of the MMC is to extend the converter to three phases, simply by adding two more legs to the converter as shown in Figure 2.6. The system is essentially the same as the single phase system presented in the previous section, and has simply been extended to 3 phases. In the figure, $v_S$, $i_{AC}$, $v_{AC}$, $L$ and $R$ are three phase quantities. $R_S$ and $L_S$ are identical for all 6 arms of the converter.

![Figure 2.6: Three phase MMC](image)

The operation of the three phase MMC is essentially the same as the single phase version. The equations developed in the previous section apply to the other two phases of the converter with, of course, the expected phase-shift between them. One notable difference is that there is now a possibility for current to circulate through phases without appearing at either the AC or DC terminal.

These currents are not present in conventional VSCs because the voltage on the DC bus side is imposed by a single capacitor. For the MMC, the voltage is imposed by capacitors distributed in all three legs of the converter. If the total voltage of the inserted modules of the legs differ, an imbalance
is created which causes currents circulation.

During regular operation, the current through each converter arm has an AC component. As such the instantaneous currents of the individual arms differ. If the instantaneous current at the AC connection point of the converter is entering the converter and divides between the upper and lower arms to the DC side, the portion of this current flowing through the upper arm will discharge the capacitors of the inserted modules whereas the lower arms modules will be charged. If the AC current direction is reversed, the current will then be charging the upper arm modules and discharging the lower ones.

Because the three AC currents are phase-shifted, the charging and discharging pattern is also displaced in time between the legs. Modules in one converter leg will have a different instantaneous voltage than in an adjacent leg even if their average voltages over a cycle are the same. Because the total number of inserted modules in each leg is constant, the total inserted voltage in the individual legs fluctuates in magnitude during an AC cycle. Since the fluctuation is not synchronized between the converter legs, the imbalance between the inserted voltages in each leg will generate currents. These currents flow among the legs of the converter, but they are not seen outside of it, they "circulate" through the converter itself. They are called circulating current.

The circulating currents have no effect outside the converter either on the AC or DC side. However, they should be kept as close to possible to 0 to reduce losses in the converter and allow for lower rating of switching elements.

The arm inductors play a role in reducing the magnitude of these currents. The larger the value of the inductance $L_s$, the smaller the circulating currents. A larger inductance however will affect the reaction time of the system as it will not allow rapid changes in currents. As will be seen in chapter 4, systems discussed in the literature usually include an inductor of the order of a few to a few tens of mHs. Specific control strategies can also be used to reduce the circulating currents [14,15]. This will be discussed in more details in the next chapter.

### 2.3.1 Converter Model (Three-Phase)

Contrary to traditional VSCs, in the MMC, there is always a path for current to flow between the terminals of the DC system through all three legs of the converter. As such, both AC and DC currents always flow through all 6 arms of the converter. These can be decomposed into three distinct components:

1. A DC component associated with the DC bus side of the converter. This component naturally flows through each leg as there is a path through the leg between the positive and negative DC buses.

2. An AC component associated with the AC side current. This AC current flows between the three phases of the AC system through the arms of the converter. Instantaneous current entering the converter through phase A for example, exits through phase B and C.

3. A circulating current component, due to imbalances between the module voltages of each arm, which is not seen at the output of the converter.

Based on the following assumptions [5]:

- Under steady-state operation, the DC current ($I_{DC}$) is be divided evenly between all three phases. This is expected as the path impedance between the positive and negative terminals of the DC bus
Chapter 2. MMC Principle of Operation and Modeling

is equivalent for all three legs (same arm inductor values, same number of inserted and bypassed modules).

- The AC currents \(i_{AC_x}\) originate evenly from each arm of the leg (i.e. \(i_{AC} = -i_{LAC}\), based on the defined directions of Figure 2.6). This is a reasonable assumption. Instantaneous AC current entering the converter through phase A exits through phase B or C. There are two paths between any two AC phase connection point through the converter, the upper and the lower arms. As will be seen later, the impedance of the current path through the upper or lower arms is almost the same, regardless of the number of inserted modules in each arm. This is due to the fact that the resistance of a module is similar whether it is inserted or not (more on this in Chapter 4). As the two current paths have similar impedance, the current flowing through them will also be similar.

- The circulating current \((i_{circ_x})\) is the same through the upper and lower arms of a leg, which is expected since the circulating currents do not leave the converter.

The currents through the upper and lower arms can be expressed as:

\[
\begin{align*}
i_{UA} &= \frac{I_{DC}}{3} + \frac{i_{AC_A}}{2} + i_{circ_A}, \\
i_{LA} &= \frac{I_{DC}}{3} - \frac{i_{AC_A}}{2} + i_{circ_A}, \\
i_{UB} &= \frac{I_{DC}}{3} + \frac{i_{AC_B}}{2} + i_{circ_B}, \\
i_{LB} &= \frac{I_{DC}}{3} - \frac{i_{AC_B}}{2} + i_{circ_B}, \\
i_{UC} &= \frac{I_{DC}}{3} + \frac{i_{AC_C}}{2} + i_{circ_C}, \\
i_{LC} &= \frac{I_{DC}}{3} - \frac{i_{AC_C}}{2} + i_{circ_C}.
\end{align*}
\]

Applying KCL, \(I_{DC}\) and \(i_{AC_x}\) can also be expressed in terms of the arm currents:

\[
\begin{align*}
I_{DC} &= i_{UA} + i_{UB} + i_{UC} = i_LA + i_LB + i_LC, \\
i_{AC_A} &= i_{UA} - i_{LA}, \\
i_{AC_B} &= i_{UB} - i_{LB}, \\
i_{AC_C} &= i_{UC} - i_{LC}.
\end{align*}
\]

From (2.15), it can be seen that the arm currents are dependent. Current \(i_{LC}\) for example can be expressed as:

\[
i_{LC} = i_{UA} + i_{UB} + i_{UC} - i_{LA} - i_{LB}.
\]

The circulating currents can be expressed as functions of the arm currents by replacing any \(I_{DC}\) or \(i_{AC}\) term with their equivalent values expressed as arm currents. Using (2.9) as a starting point and replacing \(I_{AC}\) by its equivalent sum of upper arm currents from (2.16):
\[ i_{U_A} = \frac{I_{DC}}{3} + \frac{i_{AC_A}}{2} + i_{circA}, \]
\[ i_{U_A} = \frac{I_{DC}}{3} + \frac{i_{U_A} - i_{LA}}{2} + i_{circA}, \]
\[ i_{circA} = -\frac{I_{DC}}{3} - \frac{i_{U_A} - i_{LA}}{2} + i_{U_A}, \]
\[ i_{circA} = -\frac{I_{DC}}{3} + \frac{i_{U_A} + i_{LA}}{2}. \quad (2.20) \]

Based on the same process, from (2.11) and (2.16), the circulating current of leg B can also be defined as:

\[ i_{circB} = -\frac{I_{DC}}{3} + \frac{i_{U_B} + i_{LB}}{2}. \quad (2.21) \]

Finally, from (2.13), (2.18) the circulating current of leg C is:

\[ i_{circC} = -\frac{I_{DC}}{3} + \frac{i_{U_C} + i_{LC}}{2}. \quad (2.22) \]

It is then possible to show that the circulating currents, as represented here, have no effect outside of the converter by summing the circulating currents in all three branches. Summing (2.20), (2.21) and (2.22) provides:

\[ i_{circA} + i_{circB} + i_{circC} = -I_{DC} + \frac{i_{U_A} + i_{LA} + i_{U_B} + i_{LB} + i_{U_C} + i_{LC}}{2}, \]
\[ i_{circA} + i_{circB} + i_{circC} = -I_{DC} + \frac{I_{DC} + I_{DC}}{2}, \]
\[ i_{circA} + i_{circB} + i_{circC} = 0. \quad (2.23) \]

Circulating currents harmonics

Applying KVL around the DC link through one leg of Figure 2.6, one gets:

\[ \frac{V_{DC}}{2} - v_U - R_s i_U - L_s \frac{di_U}{dt} - R_s i_L - L_s \frac{di_L}{dt} - v_L + \frac{V_{DC}}{2} = 0, \]
\[ V_{DC} - v_U - v_L = R_s (i_U + i_L) + L_s \frac{d(i_U + i_L)}{dt}. \quad (2.24) \]
Chapter 2. MMC Principle of Operation and Modeling

$$V_{DC} - v_U - v_L = 2R_s \left( i_{circ} + \frac{I_{DC}}{3} \right) + 2L_s \frac{d(i_{circ} + \frac{I_{DC}}{3})}{dt},$$

$$\frac{V_{DC}}{2} - \frac{v_U + v_L}{2} = R_s \left( i_{circ} + \frac{I_{DC}}{3} \right) + L_s \frac{di_{circ}}{dt},$$

$$\frac{V_{DC}}{2} - \frac{v_U + v_L}{2} - R_s \frac{I_{DC}}{3} = R_s i_{circ} + L_s \frac{di_{circ}}{dt}. \quad (2.25)$$

The $I_{DC}$ term inside the derivative can be removed since it is assumed to be time invariant (it does vary slightly but the assumption remains acceptable). From (2.25), it can be noted that, changing both reference voltages ($V_U$ and $V_L$) by the same amount will affect the circulating current, but, according to (2.8), will not affect the AC side current, which highlights the independence between the circulating and output currents.

Under steady-state conditions, assuming a low voltage drop through inductor $L_s$, the sum of $V_U$ and $V_L$ will be $V_{DC}$, as the same total number of modules will be inserted in the circuit. The voltages $V_U$ and $V_L$ have sinusoidal amplitudes in order to track the desired output voltage which is sinusoidal in steady-state. One then can represent the reference voltages as time varying signals:

$$v_U(t) = \frac{V_{DC}}{2} \left[ 1 + m\sin(\omega_0 t) \right], \quad (2.26)$$

$$v_L(t) = \frac{V_{DC}}{2} \left[ 1 - m\sin(\omega_0 t) \right], \quad (2.27)$$

where $m$ is the modulation index, varying form 0 to 1. Ignoring circulating currents and assuming that the three phases are balanced, the currents in each arm in the time domain is:

$$i_U(t) = \frac{I_{DC}}{3} + \frac{i_{AC}}{2} = \frac{I_{DC}}{3} + \frac{I_{AC}}{2} \sin(\omega_0 t + \phi),$$

$$i_U(t) = \frac{I_{DC}}{3} \left[ 1 + k\sin(\omega_0 t + \phi) \right], \quad (2.28)$$

$$i_L(t) = \frac{I_{DC}}{3} - \frac{i_{AC}}{2} = \frac{I_{DC}}{3} - \frac{I_{AC}}{2} \sin(\omega_0 t + \phi),$$

$$i_L(t) = \frac{I_{DC}}{3} \left[ 1 - k\sin(\omega_0 t + \phi) \right], \quad (2.29)$$

where:

$$k = \frac{3I_{AC}}{2I_{DC}}. \quad (2.30)$$

The instantaneous power for the upper arm is then [21]:

$$18$$
\[ p_U(t) = v_U(t) \times i_U(t), \]
\[ p_U(t) = \frac{V_{DC}}{2} [1 + m\sin(\omega_0 t)] \frac{I_{DC}}{3} [1 + k\sin(\omega_0 t + \phi)], \]
\[ p_U(t) = \frac{V_{DC}I_{DC}}{6} (1 + m\sin(\omega_0 t) + k\sin(\omega_0 t + \phi) + k\sin(\omega_0 t)\sin(\omega_0 t + \phi)), \]
\[ p_U(t) = \frac{V_{DC}I_{DC}}{6} \left(1 + m\sin(\omega_0 t) + k\sin(\omega_0 t + \phi) + \frac{k}{2} (\cos(-\phi) - \cos(2\omega_0 t + \phi))\right), \]
\[ p_U(t) = \frac{V_{DC}I_{DC}}{6} \left(1 + m\sin(\omega_0 t) + k\sin(\omega_0 t + \phi) + \frac{k}{2} (\cos(\phi) - \cos(2\omega_0 t + \phi))\right). \] (2.31)

The same process can be repeated for the lower arm:

\[ p_L(t) = v_L(t) \times i_L(t), \]
\[ p_L(t) = \frac{V_{DC}}{2} [1 - m\sin(\omega_0 t)] \frac{I_{DC}}{3} [1 - k\sin(\omega_0 t + \phi)], \]
\[ p_L(t) = \frac{V_{DC}I_{DC}}{6} \left(1 - m\sin(\omega_0 t) - k\sin(\omega_0 t + \phi) + \frac{k}{2} (\cos(\phi) - \cos(2\omega_0 t + \phi))\right). \] (2.32)

Summing (2.31) and (2.32):

\[ p_U(t) + p_L(t) = \frac{V_{DC}I_{DC}}{6} \left(1 + \frac{k}{2} (\cos(\phi) - \cos(2\omega_0 t + \phi)) + 1 + \frac{k}{2} (\cos(\phi) - \cos(2\omega_0 t + \phi))\right), \]
\[ p_U(t) + p_L(t) = \frac{V_{DC}I_{DC}}{6} \left(2 + k(\cos(\phi) - \cos(2\omega_0 t + \phi))\right), \] (2.33)

and integrating over time to get the total energy:

\[ \int p_U(t) + p_L(t)dt = \int \frac{V_{DC}I_{DC}}{6} \left(2 + k(\cos(\phi) - \cos(2\omega_0 t + \phi))\right), \]
\[ \int p_U(t) + p_L(t)dt = \frac{V_{DC}I_{DC}}{6} \left(2t + km\cos(\phi)t - \frac{km}{2\omega_0}\sin(2\omega_0 t + \phi)\right). \] (2.34)

In steady-state, the DC part of the energy in the legs does not change, thus the terms 2t and \( km \cos(\phi)t \) must be equivalent. As such:

\[ 2 = km \cos(\phi), \]
\[ km = \frac{2}{\cos(\phi)}. \] (2.35)

Replacing \( km \) from (2.35) in (2.34):
\[
\int p_U(t) + p_L(t) dt = \frac{V_{DC}I_{DC}}{6} \left( 2t - \frac{2}{\cos(\phi)} \cos(\phi)t + \frac{2}{2\omega_0 \cos(\phi)} \sin(2\omega_0 t + \phi) \right),
\]
\[
\int p_U(t) + p_L(t) dt = \frac{V_{DC}I_{DC}}{6} \left( 2t - 2t + \frac{1}{\omega_0 \cos(\phi)} \sin(2\omega_0 t + \phi) \right),
\]
\[
\int p_U(t) + p_L(t) dt = \frac{V_{DC}I_{DC}}{6\omega_0 \cos(\phi)} \sin(2\omega_0 t + \phi).
\]

Equation (2.36) shows that energy stored in the converter fluctuates at a frequency which is twice the fundamental. Thus the voltage in the capacitors will fluctuate with the same frequency.

In steady-state, each phase of the converter will be $2\pi/3$ radians out of phase with other phases in the positive sequence. Since the voltages fluctuate at double the frequency of the fundamental, but the phase offset ($\phi$) remains unchanged, as seen from (2.36), the voltage difference between the phases ($V_{AB}$, $V_{BC}$ and $V_{CA}$) will be in negative sequence, and so will the generated currents.

The circulating currents under normal operating conditions are 2nd harmonic negative sequence currents. As such, it will be possible to isolate them and control them if required. This will be discussed in chapter 4.

### 2.4 Conclusion

In this chapter the principles of operation of the MMC were covered. The first section considers the operation of a single module. Modules were then connected in series to form a single phase converter and the equation defining the relationship between the AC connection point voltage $v_{AC}$, the AC current $i_{AC}$ and the individual arm voltages $v_U$ and $v_L$ was developed. The single phase converter was then expanded to a three phase converter and the three components of the convert arm currents defined. Circulating current harmonics were also derived. With the principles defined, it is then possible to start the design of the controls of the MMC. The next chapter will cover control strategies presented in the literature, and highlight the strategies selected for this work.
Chapter 3

MMC Control

As the MMC is a type of voltage sourced converter, it can be controlled using the same conceptual approaches as other VSCs. However, because of distribution of the voltage among a number of modules and of the presence of inductors in the converter arms, the controls do have to be adapted to the MMC. The controls should also take advantage of the converter topology which enables it to provide greater precision in the control of the voltage presented to the AC side connection. As the energy is stored in multiple capacitors instead of a single large one as is the case in conventional systems, the MMC necessitates specific controls to ensure that it is shared as evenly as possible among all the capacitors in the converter. The controller will also be required to minimize the circulating currents in order to reduce losses.

This chapter describes different strategies presented in the literature and explains the selection of the implementation in this work.

3.1 Capacitor Voltage Balancing

In the MMC, modules are constantly inserted into and bypassed out of the system. In order to keep the capacitor voltages as evenly distributed as possible, not any module should be operated at any given time. The modules inserted or bypassed have to be selected. Failure to adequately balance the voltages not only distorts the output voltage but also can result in equipment damage if individual module voltages fluctuate outside of the rated values of the equipment. This selection is based on the direction of the current in the arm.

The change of a given module’s capacitor voltage is dependent on its inserted/bypassed state, as well as the magnitude and direction of the arm current. When the module is inserted, the capacitor voltage increases (decreases) if the current is flowing into (out of) the module. On the other hand, if the module is in the bypassed state, the capacitor voltage remains unchanged. This fact can be used to balance the capacitor voltages. If a module voltage is lower (higher) than the average voltage per arm, it should be inserted (bypassed) when the arm current is such that it will charge the module capacitor, and bypassed (inserted) otherwise.

Using Figure 3.2 as a reference, if a module is inserted in an arm and current flows through it in the positive direction, this current will cause its capacitor voltage to increase. Oppositely, if the current is flowing from the DC negative to positive, then the capacitor voltage will drop. If the current is positive,
the next inserted module should be the one with the lowest voltage so that it can be charged, whereas, if the direction is opposite, then the capacitor with the highest voltage must be selected.

The current through an arm can be either positive (charging the capacitors) or negative (discharging the capacitors) and modules can be either inserted or bypassed. This creates 4 possible operation cases:

1. The current in the arm is positive and a module must be bypassed. In this case, the inserted module with the highest voltage level should be bypassed.

2. The current in the arm is positive and a module must be inserted. In this case, the bypassed module with the lowest voltage level should be inserted.

3. The current in the arm is negative and a module must be bypassed. In this case, the inserted module with the lowest voltage level should be bypassed.

4. The current in the arm is negative and a module must be inserted. In this case, the bypassed module with the highest voltage level should be inserted.

This information can be obtained by generating a sorted list of the modules by voltage level, also containing the status of the module (inserted or bypassed), to identify the ideal modules to be inserted or bypassed when necessary.

### 3.1.1 Sorting Algorithms

Multiple sorting algorithms have been designed and studied over the years [24], all with different average speeds and complexity. For this thesis, a sorting algorithm based on bubble sort [25], has been selected.
Chapter 3. MMC Control

Table 3.1: Bubble sort example steps

<table>
<thead>
<tr>
<th>Starting Order</th>
<th>Step Description</th>
<th>Resulting Order</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial Order</td>
<td></td>
<td>[2,4,3,1]</td>
</tr>
<tr>
<td></td>
<td>First Pass</td>
<td></td>
</tr>
<tr>
<td>[2,4,3,1]</td>
<td>Compare pos. 1 &amp; 2, no exchange</td>
<td>[2,4,3,1]</td>
</tr>
<tr>
<td>[2,4,3,1]</td>
<td>Compare pos. 2 &amp; 3, exchange</td>
<td>[2,3,4,1]</td>
</tr>
<tr>
<td>[2,3,4,1]</td>
<td>Compare pos. 3 &amp; 4, exchange</td>
<td>[2,3,1,4]</td>
</tr>
<tr>
<td></td>
<td>Second Pass</td>
<td></td>
</tr>
<tr>
<td>[2,3,1,4]</td>
<td>Compare pos. 1 &amp; 2, no exchange</td>
<td>[2,3,1,4]</td>
</tr>
<tr>
<td>[2,3,1,4]</td>
<td>Compare pos. 2 &amp; 3, exchange</td>
<td>[2,1,3,4]</td>
</tr>
<tr>
<td>[2,1,3,4]</td>
<td>Compare pos. 3 &amp; 4, no exchange</td>
<td>[2,1,3,4]</td>
</tr>
<tr>
<td></td>
<td>Third Pass</td>
<td></td>
</tr>
<tr>
<td>[2,1,3,4]</td>
<td>Compare pos. 1 &amp; 2, exchange</td>
<td>[1,2,3,4]</td>
</tr>
<tr>
<td>[1,2,3,4]</td>
<td>Compare pos. 2 &amp; 3, no exchange</td>
<td>[1,2,3,4]</td>
</tr>
<tr>
<td>[1,2,3,4]</td>
<td>Compare pos. 3 &amp; 4, no exchange</td>
<td>[1,2,3,4]</td>
</tr>
<tr>
<td></td>
<td>Sorting Completed</td>
<td></td>
</tr>
</tbody>
</table>

Bubble sort is not the implemented in the simulator, the selected algorithm is odd-even sorting. However, the odd-even sort algorithm selected is based on it, therefore bubble sort is presented here as an introduction, and also provides a useful performance comparison.

**Bubble Sort**

The bubble sort algorithm takes an array of unsorted numbers, then compares the items one by one, exchanging their order if the first item has a higher value. The process is then repeated until the array is completely sorted. Taking as an example a small array of 4 numbers, [2,4,3,1]. Table 3.1 shows the steps required in completing a bubble sort on this set. It can be noticed that the largest item is sorted after a single pass, it ”bubbles” to the top. The algorithm can be improved by taking this into account and reducing the number of steps in each pass, knowing that the last value sorted in the last pass is in its final position. The sorting can be considered as completed if a complete pass does not produce any exchange.

This algorithm is simple to implement and requires little memory compared to other algorithms as items are handled two at a time. As such, it does not increase in complexity with the size of the array to be sorted. It is, however, one of the slowest algorithms for sorting arrays of random numbers. In the worse case, an array of \(N\) numbers will require \(N\) passes to be sorted. In an array of 400 numbers such as is the case here, this represents an impressive 160 000 \((N^2)\) steps, which cannot be completed in appropriate time for real-time control.

**Odd-Even Sorting**

Several sorting techniques optimized for use on FPGAs are discussed in the technical literature, one of which is the odd-even sorting technique [23]. This sorting, which is a parallelized version of the
The odd-even sorting technique takes advantage of the fact that the compare and swap operations are independent. The result of the operation with 2 elements or an array has no effect on any other elements. Thus, multiple compare and swap operations can be executed simultaneously if they are considering different array elements. Because each compare and swap operation requires few resources on the FPGA, it is possible to implement many of them in parallel and vastly increase the speed of the sorting procedure. In the Odd-Even technique, a pair with indexes \( x \) and \( x + 1 \) is considered even if \( x \) is an even number, odd otherwise. The odd-even sorting algorithm is separated into two sequential steps. In the first step, the compare and swap operation is performed on all the even pairs. Since the even pairs are all independent, the operation can be conducted in parallel. The second steps mirrors the first, but this time comparing the odd pairs. Similarly, as the odd pairs are all independent, the compare and swap operation can be conducted in parallel. This sequence is repeated \( N/2 \) times to sort the whole array.

Table 3.2 shows the steps required in completing a odd-even sort on the same set used in the bubble sort example. In this example, there are 2 odd pairs (pairs (1,2) and (3,4)) and one even pair (pair (2,3)).

Even in this small example, one fewer pass and less than half the steps (4 in odd-even compared to 9 in bubble sort) were required to fully sort the array. This improvement becomes more appreciable as the size of the array increases. As such Odd-Even takes full advantage of the scalability and simplicity of the bubble sort algorithm to allow for simple and fast sorting of large arrays. The complexity level of the algorithm remains low, as only simple compare and swap operations are used, and the execution time is reduced drastically by taking advantage of the ability of the FPGA to perform these simple operations in parallel.
3.1.2 Voltage Balancing Without Sorting

Reference [8] proposes a voltage balancing technique requiring no sorting of the modules. This technique, instead of selecting which module is inserted or bypassed from the system whenever required, controls each module individually such that, given a positive arm current, modules with lower voltages are inserted for longer periods while modules with higher voltages are inserted for shorter periods (the control is reversed for negative arm currents).

The concept is simple and relies on the Phase-Shifted Pulse-Width Modulation (PS-SPWM) strategy which will be presented below. Each module’s voltage is individually compared with the average voltage of the arm. The difference is then multiplied by the arm current and sent through a PI controller. The resulting signal is then added to the reference command for this specific module.

The control technique can be explained as follows:

- If a module has lower voltage than the average arm module, the error will be positive. Multiplied by a positive current, this will yield a positive offset which will cause the module to be connected in the system (thus charging) for a longer part or a cycle.

- If the current direction reverses, the correction offset now becomes negative, causing the module to be connected in the system (thus discharging) for a shorter period during a cycle.

- The same control applies in reverse if the module voltage is higher than the average voltage.

- Since the total deviation from the average over all modules must be 0, the overall effect of these changes will not be seen (except for possible harmonics) outside the arm itself.

This technique is appealing as it removes the need for sorting of the capacitor voltages and it actively controls of the voltage of each level. It also helps in the prediction of the losses in each module since the exact switching frequency is always known.

However, the implementation for a large number of levels, such as the 400 modules per arm of the converter of interest here, requires 400 separate reference signals, comparisons and proportional controls for each arm of the converter, greatly increasing the complexity and scale of the control algorithm compared to a simple sort and select technique.

3.1.3 Selection

The odd-even sort technique was selected as the base for the capacitor voltage balancing algorithm. This was an appropriate choice for this application as this algorithm is ideally suited for parallelization and can take advantage of all the resources of the FPGA. Using an clock speed of 100MHz, the sorting algorithm can be completed in as few as 400 passes or 4us, depending on the level of parallelization used, which is more than enough to allow for accurate control of the voltages.

The final implementation thus uses the odd-even algorithm. The voltages are latched at the start of the sorting procedure and are not updated, for sorting purposes, during the process. The amount of resources required to parallelize all 200 compare and swap operations for all 6 MMC arms was too high for the FPGA used. As such, they were divided in 4 steps (the odd and even sorting each being performed in 2 steps), so the sorting algorithm is now completed in $2N$ steps, or $8us$ on the FPGA which still provides enough speed to allow for correct voltage balancing operation.
3.2 Switching Strategy

The primary task required for MMC control is to determine the number of modules to be inserted in each arm at any point in time. Since the MMC allows flexibility in the selection of the inserted modules, new techniques are required.

Ideally, if the current direction is such that it will cause the capacitors voltages to increase, the modules should be inserted starting from one with the lowest voltage and up. If the current direction is reversed, the inserted modules should be immediately replaced by the modules with the highest voltages. This technique would provide low harmonic distortion, and excellent voltage balancing, keeping the voltage evenly distributed between the modules. However, because modules are then constantly switching in and out of the system, this comes at the expense of high switching losses. As such, other techniques requiring lower switching rate while maintaining acceptable capacitors voltage regulation are more desirable.

To minimize losses, modules should only be inserted or bypassed as required to track the commanded voltage, but this may not provide ideal voltage regulation. The selected switching technique must thus find a compromise between voltage regulation and losses. This section presents reputed techniques from the literature and explains the reason behind the final selection.

3.2.1 Nearest Level Voltage Control (NLC)

This method uses the modulation index ($m$) directly to calculate how many modules must be connected in each arm to generate the voltage closest to the required value, as illustrated in Figure 3.3.

![Figure 3.2: Single phase MMC leg](image-url)
This can be implemented as follows:

1. Taking the modulation index (of maximum amplitude 2 (±1)) and multiplying it by half the number of modules in an arm to generate a signal of maximum amplitude equal to the number of modules.

2. Adding to the result half the number of modules in an arm so that the resulting signal now fluctuates between 0 and the total number of modules.

3. The resulting signal is then rounded to the nearest integer which yields the appropriate number of inserted modules in the lower arm.

4. The command for the upper arm is complementary such that the total number of connected modules in a leg is equal to the number of modules in each arm.

This technique has the obvious advantage of being very simple to implement regardless of the number of modules used. It also has the lowest number of switchings since capacitors are only inserted and bypassed once per cycle.

It is not without drawbacks however, as the low number of switchings also generates larger fluctuations in module voltages. Using this technique, the commanded number of inserted modules, following the sinusoidal reference, will increase continuously until it reaches the peak, at which point it will start decreasing continuously. A module inserted just as the commanded number of modules starts to increase cannot be bypassed until the command has reached the peak and has started decreasing again, thus the module will be inserted for at least a half cycle before it can be bypassed, allowing for a long period of voltage fluctuation. This can potentially be prevented by monitoring individual voltages separately and inserting or bypassing modules as required (outside of the basic control) to prevent their voltages from fluctuating too far from the arm average.
3.2.2 Sinusoidal Pulse-Width Modulation (SPWM)

The sinusoidal pulse width modulation is one of the standard techniques used for control of VSCs. It is not optimized for use with the MMCs, but is shown here as a starting point since many of the techniques used for MMC are derived from it.

The idea behind SPWM is simply to compare the target signal to a higher frequency triangular wave (usually at least 10 times faster). If the triangular wave is smaller than the required signal, the resulting command is negative, if the triangular wave is larger than the reference, the command is positive. The command signal thus has the same average value than the reference signal over one triangular wave cycle.

As can be seen from Figure 3.4, the resulting output signal is a series of pulses of varying duration. In the example, the reference signal is a 60Hz sinusoidal waveform and the triangular waveform has a frequency of 1800 HZ. As can be seen from the harmonic content, the first harmonic (60Hz) is represented...
in the signal along with very large harmonics, most notably the at frequency of the triangular waveform, 1800Hz in this case (30th harmonic), whose magnitude is almost as large as the fundamental frequency. After filtering, the resulting signal will track the reference signal.

In the case of the MMC, this technique would group together all the modules composing an arm (either all bypassed or inserted). This, of course, does not take advantage of the modularity of the converter. Thus, this technique is not used for MMCs, but some modifications, presented below, can be made which make it suitable.

### 3.2.3 Phase-Shifted Sinusoidal Pulse-Width Modulation (PS-SPWM)

![Modulating signal and triangular waveforms](image)

![PWM commands to the individual upper arm modules](image)

![Overall number of inserted upper arm modules](image)

![Harmonic Content of signal](image)

Figure 3.5: Representation of the Phase-Shifted Sinusoidal Pulse-Width Modulation (PS-SPWM) method, for a converter with 5 modules per arm and a modulating signal of 0.85 amplitude

A brute force switching strategy is to implement Sinusoidal Pulse Width Modulation for each module individually, while time shifting the different switching times for each modules to take advantage of the modularity of the MMC. As in regular SPWM, the signal to be modulated is compared to a high
frequency triangular waveform.

To take advantage of the higher number of levels, PS-SPWM uses as many different phase-shifted triangular waveforms as there are converter levels [7]. The waveforms are phase-shifted so that the switching instants of the different modules are offset in time, thus reducing the harmonics in the output signal, as illustrated in Figure 3.5.

In the example, the frequency of the triangular waveform is 360Hz, only 6 times that of the modulating signal. It can be seen in the graph showing the harmonic contents of the modulating signal however, that the apparent switching frequency is much higher, in this case, the lower harmonics are centered around 1800Hz, 5 times higher than the individual modules switching frequency as there are 5 modules per arm.

This illustrates a major advantage of the MMC, which is a substantial reduction in losses as each module switches at only a fraction of the overall equivalent switching frequency. This advantage becomes more attractive as the number of modules increases, either producing a higher apparent output frequency, or lowering the switching frequency of individual modules.

From the figure, the underlying sinusoidal waveform can easily be noticed. Compared to the SPWM technique (see Figure 3.4), it is clear that this signal contains much smaller harmonics, as confirmed by the harmonic content. The difference can be clearly seen with only 5 levels. This becomes more visible as the number of modules increases, reducing, and potentially removing altogether, the requirements for filters.

Using as an example a MMC with 400 modules per arm. If each module used a switching frequency of 360Hz, the harmonics generated would be centered around 144kHz. To generate such high frequency harmonics using SPWM in conventional VSCs, this would require every IGBT to switch at this rate, which would create large losses. Such a high frequency is probably not realistic or necessary in any case, but 360Hz switching using SPWM would create large, low frequency harmonics which would require expensive filters to attenuate. However, in the case of the MMC, it is possible to generate a much higher apparent switching frequency while keeping the physical switching frequency at lower levels for each individual module, thus limiting the losses to a level similar to the expected losses using a switching frequency of 360Hz (in this example) on a conventional VSC.

The PS-SPWM method also has the advantage of being similar to regular SPWM as used in conventional converters, and of being relatively simple to implement. However, it does become cumbersome as the number of modules increases. Again using a converter with 400 modules per arm as an example, one can imagine the amount of resources necessary to generate 400 different triangular waveforms, and compare them all to the modulating signal, as well as the control resolution required to generate such a high rate of switching. Lowering the switching frequency for individual modules could help, but switching modules in and out with a certain frequency is required to evenly distribute the voltage across them, so this frequency cannot be reduced to a very small value.

It would be possible to only generate a fraction of the triangular waveforms and group modules such that each waveform comparison controls multiple modules, but this is not taking full advantage of all the modules available and, as such, of the MMC capabilities.

This technique is thus well suited for converters with a smaller number of levels (less than 40 levels or so) and, although it could be implemented on a much higher number of levels, becomes cumbersome and will not be implemented here.
3.2.4 Phase-Disposition Sinusoidal Pulse-Width Modulation (PD-SPWM)

As the name indicates, this technique is also derived from the standard pulse-width modulation technique. In this case however, instead of being phase shifted, the triangular waveforms are displaced symmetrically with respect to the zero-axis [6]. Thus, instead of a single triangular waveform of amplitude 2 \((\pm 1)\). Now \(N\) waveforms are used, each with amplitude \(2/N\), which are offset vertically so that they cover the whole \(\pm 1\) range of the modulating signal. Each waveform represents a module and the comparison that determines whether the module should be connected or not is performed as it would in regular SPWM. The technique is illustrated in Figure 3.6

This technique does, like the previous PS-SPWM technique, take advantage of the high number of modules to create a high overall switching frequency while keeping each individual module’s switching frequency at a lower value.

The frequency of the triangular waveforms in this example is 1800Hz as in the SPWM example. It
can be clearly seen that the apparent switching frequency of the output command is not multiplied by the number of modules as was the case in the PS-SPWM case, this is due to the fact that only one of the triangular waveform at a time can have an effect on the command because each waveform only covers a small portion of the modulating signal range.

Thus, the frequency of the triangular waveforms has to be the same as the expected overall output frequency, but the switchings are divided amongst the different levels so that they each see a fraction of the switching frequency.

Since, for the MMC, the result of PD-SPWM (and most switching techniques) serves to determine how many modules should be inserted in each arm, each triangular waveform need not be linked directly to a particular module. When a module needs to be inserted (or bypassed) in the system, it does not matter which waveform triggered the change, any module can be chosen. Assuming balanced conditions, modules will switch in and out at approximately the same rate to equalize the voltages, so their individual switching frequencies are approximately equal to the triangular waveform frequency divided by the number of modules in an arm. However, this technique does not necessarily guarantee an equal number of switchings for all modules, as modules are inserted or bypassed based on their voltage levels.

It can also be seen from the harmonic content of the switching signal that the harmonics are centered more closely on 1800Hz and not as dispersed as was the case for PS-SPWM. This may be an advantage of PD-SPWM in cases where the switching frequency is low and filtering is required as it would be simpler to filter out harmonics concentrated at one frequency.

As was the case for the PS-SPWM, this technique does become more cumbersome as the number of levels increases. As it does, so do the computational resources required to handle all triangular waveforms. This technique, however can be scaled in such a way that only one triangular waveform is actually required. Because the modulating signal is only ever in the range of one of the triangular waveform, this means that the other waveforms have no effect on the output as the modulating signal is either smaller or larger than any point on the waveform, so they do not intersect. As such it is possible to only consider the waveform that can affect the output command.

This requires a few modifications to the technique, which is in essence the same as the nearest voltage level control, but instead of rounding to the nearest integer, the value is truncated, and the remainder is compared with a triangular waveform of amplitude 1. The result then used as a command for the number of modules inserted in the corresponding arm.

### 3.2.5 Other Techniques

Other methods have been presented using space-vector modulation [12], selective harmonic elimination [11], or pulse time shifting [13]. But they seem to have been dismissed as too complex or inefficient for high number of modules.

### 3.2.6 Selected Method

The method selected for this thesis is the Nearest Level Voltage Control (NLC). With 400 modules per arm, the effective switching frequency for a 60Hz signal will thus be 24 kHz. This technique is also the one selected in the literature for converters with a high number of levels [16], [17].
3.2.7 Implementation

Capacitor voltage balancing will thus be attained by combining two steps. The nearest level voltage control method will be used to determine the number of modules to be inserted in each arm, then the result of the sorting algorithm will be used to select the modules to be inserted or bypassed.

In order to minimize the number of switchings and obtain a more practical control system, modules will only be switched in or out when the commanded number of modules to be inserted is different from the actual number of inserted modules, instead of always selecting the ideal modules at each instant in time.

In this ideal selection; if the current direction changes from negative to positive, all the modules with high voltage are immediately bypassed and replaced by modules with low voltage. Although this method would keep the module voltages almost identical to each other, it would also create a much larger number of switchings and increase the losses in the system.

In NLC, if a module is inserted, it will not be bypassed before the commanded number of inserted modules starts decreasing, which only happens after the modulating signal has reached it’s peak value. As such a module could be inserted continuously for half of a cycle. This will lead to larger fluctuations in the individual module voltages, and discrepancies between the voltages of the different modules, but will also keep the number of switchings and associated losses to a lower level.

Because the NLC technique by itself does not provide enough module switching instants to satisfactorily balance the voltage between all modules (the standard method generates a maximum 60 insertion/bypass per second for each module), a routine where, at a fixed time interval, one module is bypassed and one inserted in the same arm to allow for good voltage regulation was added. This swapping operation does not affect the total number of inserted modules in the arm, but increases the frequency of insertion and bypass of the individual modules, allowing for more precise voltage balancing. Even with this added check, this technique remains simple to implement, and the time interval selected for the swapping operation allows for direct observation of the compromise between switching frequency and voltage balancing.

3.3 Circulating Currents

As discussed in chapter 2, the circulating currents are caused by imbalances in the module voltages between the legs. The imbalances among the modules of a single arm can be minimized simply by appropriately selecting the modules to be inserted or bypassed. However, the imbalances between the legs are part of the normal operation of the converter. Therefore, a dedicated control loop must be designed to minimize them.

Because the phase angle of the currents is different for each phase, the voltage stored in the leg capacitors fluctuates differently between them. Without any control, the voltage imbalance generates circulating currents which flow between the legs. These currents are only limited by leg impedances, mainly the leg inductor. If, for example at a given time, the capacitors of phase A have a higher average voltage than the ones of phase B and C, there will naturally be current circulating out of phase A into the other phases. This difference between the phases, can be mitigated by inserting more than $N$ modules in both legs B and C, where the module voltages are lower, and fewer in leg A, where they are larger. At a specific instant, leg A may have $N - 2$ modules inserted where legs B and C have $N + 1$ modules, thus adjusting the total amplitude of the inserted voltages in each leg individually, simply by
inserting or bypassing additional modules. This technique allows for regulation of the amplitude of the total inserted voltage, mitigating the temporary imbalances between the phases and thus eliminating the circulating currents.

As discussed in the previous chapter, circulating currents have no effect on the outputs of the converter as they are contained in the converter itself, but must be mitigated to reduce losses in the converter itself. As derived in the equations, increasing or decreasing both $v_U$ and $v_L$ by the same amount will have an effect on the circulating currents, but not on the output voltages.

It is also important to notice that circulating currents do help alleviate imbalances between the three phases of the converter. If one phase has consistently lower capacitor voltages, the circulating current will transfer energy from the other two phases to balance the three. So reducing or eliminating circulating currents will have positive effects on losses, size and rating of the switches, but may have negative effects on the ability of the converter to distribute energy between the phases.

3.4 Conclusion

In this chapter, the operation of the MMC was described. Reputed techniques for control of the MMC, a sorting algorithm suitable for FPGA implementation as well as a technique to control circulating currents were described.

The module selection technique selected for the simulator is based on the odd-even sorting algorithm, which is well suited for FPGA implementation. The module switching technique selected is based on the nearest level voltage control (NLC) technique with additional module swaps at fixed interval to maintain good voltage balancing. The circulating current control technique selected inserts or bypasses additional modules in the individual converter legs to balance the overall magnitude of the total inserted voltage in each leg, thus mitigating temporary imbalances between the phases and reducing the circulating currents. The actual implementation of these techniques in the simulator will be discussed in the next chapter.
Chapter 4
Study Systems and Implementation

This chapter provides information about the study system and its implementation in the real-time simulator. First, the specifications of the system implemented in the real-time simulator is presented. The modelling of the MMC as implemented in the FPGA platform is also covered in details, as well as the division of the model between the FPGA platform, the RTDS system and the external cRIO controller. Finally, the implementation of the control techniques selected in the previous chapter in the real-time simulator simulator is discussed in details.

4.1 Converter specifications

The system that will be implemented in the real time simulator has the specifications outlined in [16], which represents the France-Spain HVDC link, to be commissioned in 2014. A one line diagram of the system is shown in Figure 4.1 and the main parameters are outlined in Table 4.1.

![Figure 4.1: One line diagram of the HVDC system used for simulations](image)

The parameters of the cable are available in appendix A.

4.2 Component Selection

Selecting the module capacitors and the arm inductors for the MMC system is an important part of the design process. Their ratings have to be selected to ensure correct operation and control. In this case, they are selected to match the future France-Spain HVDC system.
Table 4.1: Parameters of the converter used for simulations

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC Source Voltage (L-L, rms) ( V_{AC} )</td>
<td>400 kv</td>
</tr>
<tr>
<td>AC Source Frequency</td>
<td>60 Hz</td>
</tr>
<tr>
<td>Transformer Windings</td>
<td>( Y_g / \Delta )</td>
</tr>
<tr>
<td>Transformer Ratio</td>
<td>400 / 333 kV</td>
</tr>
<tr>
<td>Transformer Rating</td>
<td>1059 MVA</td>
</tr>
<tr>
<td>Transformer Impedance</td>
<td>18%</td>
</tr>
<tr>
<td>Number of levels per arm ( N )</td>
<td>400</td>
</tr>
<tr>
<td>Module Capacitor Value ( C_{module} )</td>
<td>12.5 mF</td>
</tr>
<tr>
<td>Expected Capacitor Voltage ( V_{module} )</td>
<td>1.6 kV</td>
</tr>
<tr>
<td>Arm Inductor ( I_{arm} )</td>
<td>50 mH</td>
</tr>
<tr>
<td>DC Voltage ( V_{DC} )</td>
<td>±320 kV</td>
</tr>
<tr>
<td>DC Rated Power ( P_{DC} )</td>
<td>1000 MW</td>
</tr>
</tbody>
</table>

But what could be the expected values for these components in a typical converter? While most published papers on MMCs detail what component values were selected, very few of them explain the reasoning behind the selection. As such, the limited number of sources explaining the reasoning behind the selections of the components that were found were examined and the techniques outlined were applied to determine if the selected component values agree with results obtained using these techniques. The results are shown in appendix B.

4.3 System Description

4.3.1 Hardware In The Loop (HIL)

Real-time simulation provides multiple advantages over conventional off-line simulations. In the MMC case, although conventional simulation tools can accurately simulate the system, off-line simulations often become impractical for large converters containing hundreds of modules in each arm as the computational burden required to handle the large number of switches and the fast rate of switching greatly increases the simulation times of the system. But other than the obvious advantage of being able to simulate the system faster, there are other important advantages to real-time simulations, which allows for hardware in the loop testing and for testing of other performance limitation issues that may be critical to a real-life MMC.

One of the challenges to the control of an MMC lies in the capacitor voltage balancing. If left unchecked, the capacitor voltages will become unbalanced, even during steady-state operation. Imbalances in voltages distort output waveforms, and even can damage the switches. Proper and thorough testing of MMC controllers is of great importance as it ensures satisfactory operation and proper functionality. Thus, MMC controllers functionality has to be verified prior to installation and commissioning. This can be achieved by interfacing the controller platform with a real-time simulator to create a hardware-in-the-loop (HIL) simulation environment.

Sorting and selection algorithms have to be executed in the required time frame to provide constantly
updated information to the model, so that the modules to be inserted into or bypassed out of the system are selected appropriately. This will always be possible in off-line simulations, but real-time will present difficulties as the limited amount of time available to complete the operations may limit the ability to sort the modules or select them appropriately.

This would not represent a major challenge if only a few modules were present in each arm, but with systems containing several hundreds of modules per arm, even these simple operations may become an important limiting factor given the quantity to be performed. A personal computer or real-time simulator, would be hard-pressed to obtain update rates of the order of a few $\mu$s as required. This is why a dedicated FPGA platform is used here, communicating with the real-time simulator.

Communication delays and bottlenecks which are associated with a physical system are also difficult to reproduce using off-line simulations. Using hardware in the loop, the required inter-connections between the different parts of the system inherently introduce delays that can have an important effect on the operation of the converter. In the simulator, communication delays present between the different parts of the system are automatically introduced by hardware. Imperfections in the communication structure such as improper DC-bias of analog signals can also be tested and accounted for.

The control system used in this case is divided into three distinct hardware devices. An FPGA platform is used to solve the converter model, sort the module voltages, and generate the switching commands to the individual modules, an RTDS real-time simulator is used to simulate the electrical system, including the transformers and the DC cable, while the MMC controller is implemented on a cRIO from National instrument.

### 4.3.2 Modelling Technique

The keys for enabling the real-time simulation of a realistic size MMC are to:

1. Adopt a computationally-efficient MMC model.
2. Parallelize the solution of the mathematical model of the MMC.

Due to the presence of hundreds of modules per arm in a realistic MMC (the system of interest in this case has 400), the direct application of the standard modelling approach, where each switch is replaced by a small impedance during the ON state and a large impedance during the OFF state, generates an excessively large admittance matrix which is computationally demanding.

As such, the modelling approach adopted in this work is based on the concept of time-varying Thevenin equivalent [18]. Using this approach, the IGBT and its associated anti-parallel diode are modelled as one bi-directional switch and represented using the two-valued impedance approach, with a small resistance ($R_{ON}$) when conducting and a larger resistance ($R_{OFF}$) when opened. The selected values for $R_{ON}$ and $R_{OFF}$ are shown in Table 4.2

<table>
<thead>
<tr>
<th></th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{ON}$</td>
<td>0.001 $\Omega$</td>
</tr>
<tr>
<td>$R_{OFF}$</td>
<td>1000000 $\Omega$</td>
</tr>
</tbody>
</table>

The capacitor itself is modelled as a controlled voltage source representing the energy stored in the capacitor at the beginning of a simulation time step in series with a resistor ($R_C = \frac{\Delta V}{\Delta t}$) which represents the change in voltage during that time step. The voltage across the individual $R_C$ capacitors is calculated...
at each time step and added to the controlled voltage source output for the next time step. When the
module is bypassed, the controlled value of Thevenin voltage source is 0V, but the voltage stored in the
capacitor is saved and will be used when the module is inserted again. Using a time step of 2.5 µs and
a capacitance of 12.5 mF, the calculated value of $R_C$ in this case is: 0.2 mΩ. The equivalent circuits of
individual are shown in Figure 4.2.

From the simplified module circuit shown in the Figure 4.2, the Thevenin resistance of a module
when inserted or bypassed is:

\[
R_{TH_{\text{inserted}}} = R_{\text{ON}} \left( \frac{R_{\text{OFF}} + R_C}{R_{\text{ON}} + R_{\text{OFF}} + R_C} \right) = 0.001200,
\]

\[
R_{TH_{\text{bypassed}}} = R_{\text{OFF}} \left( \frac{R_{\text{ON}} + R_C}{R_{\text{ON}} + R_{\text{OFF}} + R_C} \right) = 0.000999.
\]

As $R_{\text{ON}}$ and $R_C$ are much smaller than $R_{\text{OFF}}$, both equations represent a small resistance in parallel
with a large one, as such, the equivalent resistance is similar in both cases and it is a fair simplification
to pre-calculate the total resistance of the branch by assuming an average resistance of 0.0011 Ω. This
simplifies the calculations for the real-time system and allows the resistance to be modelled in RTDS
instead of the FPGA, such that the only required output of the FPGA to the RTDS system is the
equivalent voltage of the individual branches. This is also a reasonable simplification as the arm inductor
of 50mH has a much larger impedance at 60Hz than the lumped resistance, so the averaging of the
resistance values will not have a large effect on the overall leg impedance, and on the simulation results.

After calculating the equivalent circuit of all modules, the resulting is 400 series connected resistors
and voltage sources which can be lumped into a single equivalent resistor and source for each arm,
greatly reducing the computational complexity of the system for the simulation. The equivalent model of the converter using this modelling approach is shown in Figure 4.3.

4.4 Implementation

The controls of the system are designed such that RTDS simulator does not require the individual module voltages. The RTDS simulator, representing the electrical network outside the converter, only requires the overall voltage of the inserted modules of each converter arm. As such, the sorting and selection calculations are implemented on the FPGA. The system control layout is similar to the control system successfully used in [9] to control a physical MMC converter. The overall architecture of the system is shown in Figure 4.4.

4.4.1 FPGA Platform

The FPGA platform is responsible for the simulation of the converter itself, while the rest of the electrical system is simulated on RTDS. The FPGA used is an Altera Stratix IV EP4SGX530.

The converter model is at the center of the implementation. At each time step, the change in voltage across the capacitor of the inserted modules is determined by calculating the voltage drop across the equivalent $R_C$ resistor (where $R_C = \frac{\Delta t}{C}$). The result is then added to the capacitor voltage at the end
of the previous step. The voltage across the capacitors of the bypassed modules remains unchanged. The voltages of all the inserted capacitors are then added to generate the overall arm voltage, which is transferred to the RTDS simulator.

For any individual module, the solution for the updated capacitor voltage is dependent solely on the gating signals, the arm currents, and its capacitor voltage from the previous time-step. As such, it is independent from any other module and the calculations can be conducted in parallel, which is ideally suited for FPGA computations. Hence, the implementation on the FPGA, has a number of parallel elements; each one being responsible for solving the equations of a single module. For the overall arm equivalent output voltage, an adder tree is implemented to compute the total of all the inserted module voltages in each arm. Thus the only information required to perform the calculations is the arm currents and the individual switching command for each module.

Module voltage sorting as well as switching and selection is also handled in the FPGA. This represents a likely real-world scenario where measurements and switching would be handled in a dedicated controller. It has the benefit of reducing the amount of data transmission required to the main controller which thus does not need to react on individual capacitor voltages, but rather overall voltage level, leaving the balancing functions in the hands of the dedicated control, also reducing potential delays.

As discussed in chapter 3, balancing of the module voltages is achieved by selecting which modules are inserted and/or bypassed in the converter. The individual voltages are used as inputs to a function which sorts them in ascending order. The sorting algorithm used is the even-odd sort detailed in chapter
3. Even with this highly parallelized implementation, the sorting operation requires 8 µs to complete, which is more than 3 times longer than an RTDS simulation time-step of 2.5 µs, due to the large number of modules to be sorted and the limited amount of resources. Thus, the voltages are latched at the beginning of the sorting operation and kept constant throughout sorting the process (The voltages are updated in the MMC model, but are not updated for the sorting process until the list is completely sorted, at which point they are updated before the next sorting process starts). The assumption is that they will not vary significantly during the sorting operation as the time required to perform the operation is still in the order of a few µs, so the output of the algorithm will be very close to the actual order, with potentially a few modules a few positions off.

The sorted list is then used by a selection algorithm which simply extracts a short list of up to 40 modules.

- The 10 inserted modules with the highest voltages.
- The 10 inserted modules with the lowest voltages.
- The 10 bypassed modules with the highest voltages.
- The 10 bypassed modules with the lowest voltages.

The resulting lists are used to quickly select which modules are to be inserted or bypassed modules when required. This is done by comparing the commanded number of inserted modules with the actual number. If the values are different, modules are inserted or bypassed as required based on their current status (inserted or bypassed), voltage level and the arm current direction. The list could contain fewer modules, but this is done to ensure modules are inserted and bypassed properly even when multiple switchings are required during the time necessary to extract the desired modules from the sorted list.

Modules are inserted or bypassed only when the commanded number of inserted modules differs from the actual one. Because the switching technique used is nearest level control (NLC), this means that under normal conditions, modules will only be inserted and bypassed a maximum of once per cycle (potentially less if the modulation index is small). This small number of switchings is insufficient to correctly balance the module voltages. As such additional swapping operations, where one module is bypassed at the same time another is inserted, were implemented. This operation is executed every 10 µs, which translates to an additional 500 switching cycles per second per module and allows for very good voltage balancing between the modules.

The final list of inserted and bypassed modules is fed back to the MMC model, to update the individual module voltages during the next time-step. This process is synchronized with the RTDS time-step by ensuring that the calculations are performed only when new data is available (except for the sorting function which is continuously processing). A functional block diagram of the FPGA implementation is shown in Figure 4.5.

Because the solution is highly parallelized on the FPGA, it is important to reduce the amount of resources required for individual computations. Given that the change in voltage of a capacitor during time-step is based solely on the arm current at that time (and the fixed resistance $R_C$); the voltage of all the inserted capacitors of a arm fluctuates by the same amount during a time-step. As such, only one multiplication is required to calculate the voltage change ($\Delta V$) of the inserted modules for a given step. This change is then applied to every inserted module using simple adders. To ensure high precision in the calculations, the calculation $\Delta V$ is performed using floating point arithmetic. However, because
Chapter 4. Study Systems and Implementation

Figure 4.5: Block diagram of the MMC implementation in the FPGA

Floating point operations are resource intensive on an FPGA, the update of the individual voltages is done using fixed point addition. The FPGA chip which contains 424,960 logic elements and the MMC model, sorting, switching and selection algorithms utilize around 77% of the total logic, 2% of the DSP blocks, and approximately 1% of the total on chip memory.

Figure 4.6 depicts the adopted method for interfacing the solution of the MMC arms, simulated on the FPGA, with the solution of the rest of the power system on the RTDS. The communication between the two systems inherently introduces a delay. Conveniently, the arm inductors and module capacitors allow for decoupling of the solutions between systems. On the RTDS side, a simplified equivalent representation of the MMC is connected directly to the power system being simulated. This representation has six externally controlled voltage sources and six resistors representing the lumped individual module resistances. On the FPGA side, the model of the individual module capacitor voltages is solved. The FPGA receives the commanded number of inserted modules for each arm from the controller as well as the six arm currents, corresponding to the MMC inductor currents, from RTDS. Based on these currents and the switching commands, the FPGA solves the MMC model and updates the 6 controlled voltage sources for the RTDS.

Interfacing

The communication between RTDS and the FPGA platform is accomplished over a fibre optic interface. Figure 4.7 shows the FPGA with the attached interface.

The interface code was developed by RTDS to offer a connection with Altera FPGA devices. Specific code must be inserted in both the RTDS and FPGA programs and allows the transfer of 32-bit data packets between the 2 devices. 1 variable is transferred on every FPGA scan, which was set at a frequency of 100MHz. The data is first transmitted from RTDS to the FPGA. Once all the information is received, the FPGA makes the appropriate calculations and returns the required data to RTDS. This must be completed before the next RTDS time-step, 2.5 µs later.
Figure 4.6: Partitionning of the MMC solution between the FPGA and RTDS

As such, all the calculations must be completed and the data returned to RTDS within 250 FPGA clock cycles. During that time, the voltage of all the modules must be updated and the new switching command generated. The system is implemented such that module sorting, selection and switching are handled completely on the FPGA. As such, these function do not need to complete in that time frame.

As a minimum for correct operation, the following data must be exchanged between the 2 devices:

From RTDS to the FPGA:
- Arm currents (x6),
- Commanded number of inserted modules for each arm (x6).

From the FPGA to RTDS:
- Equivalent MMC voltages for each of the six arms (sum of all inserted module voltages for each
Additional data, such as individual module voltages, rate of change of voltage or actual number of inserted modules, is also sent from the FPGA to RTDS for debugging and display, but is not required for actual operation.

There is no direct communication between the FPGA and cRIO as no fibre optic interface is available for the cRIO.

### 4.4.2 Controller

The second piece of hardware in the system is a compact RIO (cRIO) 9082 reconfigurable controller from National Instruments. This controller has a built-in FPGA which can be used for fast calculations as well as 8 ports for IO cards. Figure 4.8 show the cRIO used in the system.

![Figure 4.8: cRIO9082 controller used for controller implementation](image)

The controller contains all required controls of an MMC:

- A Phase-Locked Loop (PLL).
- AC current controller (in $dq$ frame).
- DC voltage controller.
- Circulating currents controller (in $dq$ frame).

The controls could be implemented directly in the RTDS system, but is implemented separately to test the hardware in the loop (HIL) capabilities of the system. The cRIO receives voltage and current readings from the RTDS system and returns the required commands to the converter. Communications with the RTDS system are handled using analog signals. The three phase AC side voltage and current as well and the circulating currents are sent to the controller along with the DC voltage.

The phase-locked loop as well as the current and voltage controllers and the circulating current controller are implemented in the cRIO. The resulting commands, sent back to RTDS and ultimately the FPGA responsible for the MMC model simulation, are the commanded voltage at the MMC connection point which is transferred into the commanded number of inserted modules for each arm in RTDS before being sent to the FPGA.

The system implementation is divided between the built-in FPGA and the CPU of the controller. For accurate and fast calculations, the PLL as well as the $dq$ transformations are implemented on the cRIO FPGA, while the PI controllers themselves are implemented in software as they do not require as fast of an update rate. The division of the tasks between the FPGA and software on the cRIO is shown in Figure 4.9.
Control system in \(dq\) frame

With the equations developed in chapter 2, it is possible to design controls for the MMC. This design uses the rotating \(dq\) frame as a basis for the controls, so as to control DC-like values and utilize regular PI controller.

Any three-phase value expressed in the regular \(abc\) frame can be transferred to the rotating \(dq\) reference frame. If the rotational speed of the reference frame is the same as the frequency of the signal, it will then be mapped to a DC signal in that reference frame.

The Park transform is the matrix used to transition any value from the \(abc\)-frame to the \(dq\) frame.

\[
P = \frac{2}{3} \begin{bmatrix}
\sin(\omega t) & \sin(\omega t - \frac{2\pi}{3}) & \sin(\omega t - \frac{4\pi}{3}) \\
\cos(\omega t) & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t - \frac{4\pi}{3}) \\
\frac{1}{2} & \frac{1}{2} & \frac{1}{2}
\end{bmatrix}
\] (4.1)

Using this transform and setting \(\omega\) corresponding to 60Hz (or 377 rad/sec), the fundamental frequency currents and voltages in the \(abc\) frame will become DC values, suitable for control with a standard PI controller.

PLL

The first step in designing the control of the system is to generate the rotating reference frame that will be used in the \(abc\) to \(dq\) transformation. In order to perform this transformation it is necessary to know the frequency and phase of a reference point in the system. The selected reference point in this case is the AC source voltage.

In order to track the phase and frequency correctly, a Phase-Locked Loop (PLL) is required. There are multiple ways to build a PLL and it is not the goal of this thesis so the details will be omitted here. The PLL selected is based on the \(dq\) transformation, it is implemented simply by forcing the \(q\)
component to 0. The block diagram of the PLL as implemented in the cRIO controller is shown in Figure 4.10.

![Block diagram of the PLL as implemented](image)

**Figure 4.10: Block diagram of the PLL as implemented**

With this definition of the reference frame, each part of the \(dq\) frame controls either the real (\(d\)) or the reactive power (\(q\)). It then becomes possible to independently control the two quantities for each converter. For the HVDC link simulated in this thesis, it is then possible to separately control four quantities.

**Overall Control Architecture**

The main controls are divided into two nested control loops.

1. The inner current loop.
2. The outer voltage or power loop.

The inner loop is used to control the currents on the AC system. The measured current values in the \(abc\) reference frame are first transferred to the rotating \(dq\) reference, which generates the 2 DC-like values \(i_d\) and \(i_q\). These values are then compared to their references and the error is used as the input to the current controller, which then generates the voltage commands for the converter. The commands, after being converted back to the \(abc\) frame of reference, are used to adjust the output voltage or each arm of the converter (by controlling the number of inserted modules in each arm), thus controlling the voltage at the AC connection point and forcing a specific current on the AC transmission line.

The reference currents in the \(dq\) frame are generated based on commanded real and reactive power as well as target DC voltage. Depending on the function of the converter in the DC link, the \(d\) component control loop can either be used to regulate the DC voltage, or regulate the real power transfer. In DC links including only two converters, one station is assigned to each function. The \(q\) component is then left to control the reactive power at the AC connection point of the converter at each end of the link.

As was the case for the current control, the control values are measured and compared to their reference; the error is then fed through a PI controller. The output of these control loops is used as a reference point for the current control loops. Both these loops configurations are discussed below in more details. The overall control architecture used in the controller is shown in Figure 4.11.
Outer Voltage and power control loop

Inner current control loop

DC Voltage or Real Power Control

Current Control

Reverse dq transform

Calculation of num. of inserted modules per arm

Converter

Figure 4.11: Overall control architecture implemented in cRIO controller

Circulating Current Control

A separate control loop is used to control the circulating currents. As they do not propagate outside the converter, controls can be designed specifically to limit these currents without interfering with the main controls.

Here again, the control is based on the dq-frame, but instead of rotating in positive sequence at the fundamental frequency, this reference frame will be rotating at twice the frequency and in the negative sequence since, as seen earlier, the circulating currents are twice the frequency and of opposite sequence as the main signals. The control architecture with the added circulating current control loop is shown in Figure 4.12.

Figure 4.12: Overall control architecture implemented in cRIO controller including circulating currents
Because the aim of this controller is to reduce the circulating currents, as much as possible, both reference values are fixed to 0, thus the actual phase of the signal used for the \(dq\) transformation is not important. It is only required that the frequency of the signals be twice the fundamental and in the opposite direction. As such, it is not necessary to implement a separate PLL for this controller, the output of the main PLL can be used, and simply multiplied by -2 to generate the required signal. The output of this controller is added to the output of the current controller to form the final module insertion command to the converter.

The main difference between the circulating current controls and the regular current controls is the way they are applied to the system. In the case of the regular current controls, the output of the controller yields the commanded voltage for one of the arms (in this case \(v_L\)). The commanded voltage for the upper arm is calculated directly from it so that \(N\) modules are inserted in the converter leg. In the case of the circulating currents, the output of the controller is added to both arm voltages in order to affect the magnitude inserted voltage of the leg.

**Interfacing**

The communication between the RTDS system and the cRIO controller is handled with analog inputs and outputs; as there are no fibre optic interfaces available for the cRIO as of yet. The following data is sent from RTDS to the controller.

From RTDS to the cRIO:
- AC voltage (x3)(for PLL reference)
- AC current (x3) (for current control)
- DC voltage (for voltage control)
- Circulating currents (x3) (for circulating current control)

The circulating currents are calculated using all 6 arm currents, the DC current and the AC side currents. All of these signals could be sent to the controller where the calculations could be made, but the calculation is instead performed directly on RTDS to reduce the required number of signals.

The following data is sent from the cRIO to RTDS:
- Commanded voltage a MMC connection point in \(dq\)-frame (x2)

As no fibre optic connection is available for the cRIO at this time, direct connection between the cRIO and FPGA is not possible. Because of this, the commands for the number of modules to be inserted is sent to RTDS and then to the FPGA board. In a physical system, these commands would be sent directly to the converter without this extra transit. This adds an extra layer of delays which would not be present in a real system and will make control more difficult to implement.

Because a real system would not have this extra layer of delay, the response to a command would be received faster. As such, this added layer of complexity does not represent a problem to the extension of the application of the results to a real world system as it actually makes the system more difficult to tightly control. That is, if a control strategy works in this system, it would likely also be effective if the added delay was removed.

The controller determines how many modules are inserted in each arm. The initial intention was to send the commanded number of inserted modules for each phase from the controller through RTDS.
using analog signals, which would be transferred over to the FPGA platform using the fibre optic connection.

This proved to be difficult however, as fluctuating DC offsets and noise in the analog signals generated intermittent harmonics in the signals that would affect the system performance. To counter this issue, the signals sent to RTDS are now the commanded voltages at AC the connection point of the converter in the dq-frame. As they are DC like signals, it is easier to filter out noise and any potential DC offset can also be easily handled by the PI controller, which will automatically adjust the setpoint to cancel any DC offset in the interface. The reverse dq transformation is thus implemented in RTDS, the result is used to generate the number of inserted modules for the individual phases, which is then sent to the FPGA.

4.4.3 RTDS

RTDS is responsible for the simulation of the AC system and the DC link in the case of the HVDC system. The AC systems are represented by an ideal voltage source placed behind a transformer. The RTDS receives the equivalent voltage for each arm from the FPGA, which is set as the reference to the controlled voltage source simulating each arm of the MMC. This information is used to solve the system and the resulting currents are then sent back to the FPGA.

To allow for precise simulation, the electrical circuit is implemented in a small-time step interface, specifically intended to simulate fast switching of converters, which allows for simulation speeds in the few µs range (2.5µs in this case) compared to the 50µs for regular simulations. Each converter is implemented in a different small time-step interface. The connection between the 2 converters is the DC cable, which provides decoupling and allows for the systems to be simulated on two different CPUs.

Using the smaller time step limits the size of the system as well as what circuit elements that can be used, but this is not an issue in this case as the system is simple. If more complex AC systems need to be implemented, they can be implemented in the normal time-step and linked to the small-time step section which would contain only the converter interfaces themselves.

Any control or data display operation required for the system is handled in the slower 50µs time-step. Only the AC system components are simulated in the small time-step section.

4.4.4 Current Control Loop Design

The first layer of control is the inner current control loop. This control loop uses the dq transformation to transfer the three phase sinusoidal currents to DC values, allowing for the use of standard PI control techniques.

Based on the circuit shown in Figure 4.13, it is possible to use the elements of the AC circuit to determine the relationship between the current entering the converter (direction defined as per the figure) and the voltage at the converter connection point:

\[ v_{AC_{abc}} = v_{S_{abc}} - L \frac{di_{AC_{abc}}}{dt} - R i_{AC_{abc}}. \]  

(4.2)

This equation is valid for all three phases and can be transformed into the dq-frame using the Park transform (\(P\)).
Figure 4.13: Single phase MMC leg

\[ P^{-1}v_{AC_{dq}} = P^{-1}v_{S_{dq}} - L \frac{d(P^{-1}i_{AC_{dq}})}{dt} - RP^{-1}i_{AC_{dq}}, \]

\[ v_{AC_{dq}} = v_{S_{dq}} - L P \frac{d(P^{-1}i_{AC_{dq}})}{dt} - Ri_{AC_{dq}}, \]

\[ v_{AC_{dq}} = v_{S_{dq}} - L P \frac{dP^{-1}i_{AC_{dq}}}{dt} - L \frac{di_{AC_{dq}}}{dt} - Ri_{AC_{dq}}, \] (4.3)

Knowing that

\[ P \frac{dP^{-1}}{dt} = \begin{bmatrix} 0 & -\omega & 0 \\ \omega & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}, \]

equation (4.3) becomes:
\begin{align*}
v_{AC_{dq}} &= v_{S_{dq}} - \begin{bmatrix} 0 & -L\omega & 0 \\ L\omega & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} i_{AC_{dq}} - L \frac{di_{AC_{dq}}}{dt} - \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix} i_{AC_{dq}}, \\
v_{AC_{dq}} &= v_{S_{dq}} - \begin{bmatrix} R & -L\omega & 0 \\ L\omega & R & 0 \\ 0 & 0 & R \end{bmatrix} i_{AC_{dq}} - L \frac{di_{AC_{dq}}}{dt}.
\end{align*}

The individual equations for control in the $dq$-frame can thus be extracted:

\begin{align*}
v_{AC_{d}} &= v_{S_{d}} - Ri_{AC_{d}} + L\omega i_{AC_{q}} - L \frac{di_{AC_{d}}}{dt}, \\
v_{AC_{q}} &= v_{S_{q}} - Ri_{AC_{q}} - L\omega i_{AC_{d}} - L \frac{di_{AC_{q}}}{dt}.
\end{align*}

These can in turn be represented as transfer functions:

\begin{align*}
v_{AC_{d}} &= v_{S_{d}} - Ri_{AC_{d}} + L\omega i_{AC_{q}} - s L i_{AC_{d}}, \\
(R + sL)i_{AC_{d}} &= -v_{AC_{d}} + v_{S_{d}} + L\omega i_{AC_{q}}, \\
i_{AC_{d}} &= \frac{1}{R + sL} \left( -v_{AC_{d}} + v_{S_{d}} + L\omega i_{AC_{q}} \right), \\
v_{AC_{q}} &= v_{S_{q}} - Ri_{AC_{q}} - L\omega i_{AC_{d}} - s L i_{AC_{q}}, \\
(R + sL)i_{AC_{q}} &= -v_{AC_{q}} + v_{S_{q}} - L\omega i_{AC_{d}}, \\
i_{AC_{q}} &= \frac{1}{R + sL} \left( -v_{AC_{q}} + v_{S_{q}} - L\omega i_{AC_{d}} \right).
\end{align*}

These equations yield the relation between the AC currents and the voltage at the output of the converter. In regular VSC converters, this would be the control signal. In the MMC, however, the arm inductors create a separate voltage drop in the converter arm. This difference must be taken into consideration when generating the required control signals. Based on the single-phase model of the MMC, the inner loop equation has been derived in section 2.2.1:

\begin{align*}
v_{AC} &= \frac{R}{2} (i_{AC}) - \frac{L}{2} \frac{di_{AC}}{dt} + \frac{v_{L} - v_{U}}{2}.
\end{align*}

Ignoring the circulating current controls, the total of $v_{L}$ and $v_{U}$ must always be equal to $V_{DC}$ in steady-state to keep the capacitor voltages constant, thus:

\begin{align*}
V_{DC} &= v_{L} + v_{U}.
\end{align*}
- The DC current will not cause a voltage drop through the inductors as it is constant.

- The AC current is defined as evenly distributed (and of opposite direction) between the lower and upper arms. Thus, the voltage drop created through the upper arm inductor by the AC current will be equal and opposite to the drop through the lower arm inductor. As such, the total voltage across the two arm inductors of a converter leg caused by AC currents is 0.

- The circulating currents are controlled via a separate controller and are considered to be zero for this control.

Voltage $v_L$ was selected to be the output of the controller. Given that they are exact opposite of each other, $v_U$ could have been selected as well. Using the previous result to remove $v_U$ from (4.9):

$$v_{AC} = -\frac{R_s}{2}(i_{AC}) - \frac{L_s}{2} \frac{d(i_{AC})}{dt} + \frac{-V_{DC} + v_L + v_L}{2},$$

$$2v_{AC} = -R_s i_{AC} - L_s \frac{d(i_{AC})}{dt} - V_{DC} + 2v_L.$$ \hspace{1cm} (4.11)

This equation can be transferred to the $dq$-frame of reference:

$$2P^{-1}v_{AC_dq} = -R_s P^{-1}i_{AC_dq} - L_s \frac{d(P^{-1}i_{AC_dq})}{dt} - V_{DC} + 2P^{-1}v_{L_dq},$$

$$2v_{AC_dq} = -R_s i_{AC_dq} - L_s P \frac{d(P^{-1}i_{AC_dq})}{dt} - P V_{DC} + 2P \cdot v_{L_dq},$$

$$2v_{AC_dq} = -R_s i_{AC_dq} - L_s P \frac{dP^{-1}}{dt} i_{AC_dq} - L_s \frac{di_{AC_dq}}{dt} - P V_{DC} + 2P \cdot v_{L_dq}.$$ \hspace{1cm} (4.12)

With $P \frac{dP^{-1}}{dt}$ as derived earlier, the equation becomes:

$$2v_{AC_dq} = -\begin{bmatrix} R_s & 0 & 0 \\ 0 & R_s & 0 \\ 0 & 0 & R_s \end{bmatrix} i_{AC_dq} - \begin{bmatrix} 0 \\ L_s \omega \\ 0 \end{bmatrix} i_{AC_dq} - \begin{bmatrix} 0 \\ -L_s \omega \\ 0 \end{bmatrix} i_{AC_dq} - L_s \frac{di_{AC_dq}}{dt} - \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} + 2v_{L_dq},$$

$$2v_{AC_dq} = -\begin{bmatrix} \cos(\omega t) & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t - \frac{4\pi}{3}) \\ \sin(\omega t) & \sin(\omega t - \frac{2\pi}{3}) & \sin(\omega t - \frac{4\pi}{3}) \end{bmatrix} \begin{bmatrix} V_{DC} \\ V_{DC} \end{bmatrix} + 2v_{L_dq}.$$ \hspace{1cm} (4.13)

Ignoring the DC voltage, which is not seen on the AC-side, the equations in the $dq$ reference frame are:
\[
2v_{AC_d} = -R_s i_{AC_d} + L_s \omega i_{AC_q} - L_s \frac{di_{AC_d}}{dt} + 2v_{L_d},
\]
\[
v_{AC_d} = -\frac{R_s i_{AC_d}}{2} + \frac{L_s \omega i_{AC_q}}{2} - \frac{L_s}{2} \frac{di_{AC_d}}{dt} + v_{L_d},
\]
\[
2v_{AC_q} = -R_s i_{AC_q} - L_s \omega i_{AC_d} - L_s \frac{di_{AC_q}}{dt} + 2v_{L_q},
\]
\[
v_{AC_q} = -\frac{R_s i_{AC_q}}{2} - \frac{L_s \omega i_{AC_d}}{2} - \frac{L_s}{2} \frac{di_{AC_q}}{dt} + v_{L_q}.
\]

These can in turn be represented as transfer functions:

\[
v_{AC_d} = -\frac{R_s i_{AC_d}}{2} + \frac{L_s \omega i_{AC_q}}{2} - \frac{s L_s i_{AC_d}}{2} + v_{L_d},
\]
\[
(R + sL)i_{AC_d} = \left(-\frac{s L_s - R_s}{2}\right)i_{AC_d} - \frac{L_s \omega i_{AC_q}}{2} - v_{L_d} + v_{S_d} + L \omega i_{AC_q},
\]
\[
\left(R - \frac{R_s}{2} + s \left(L - \frac{L_s}{2}\right)\right)i_{AC_d} = \left(-\frac{L_s}{2} + L\right) \omega i_{AC_q} - v_{L_d} + v_{S_d},
\]
\[
i_{AC_d} = \frac{1}{R + sL} \left(-\frac{s L_s - R_s}{2}\right)i_{AC_d} - \frac{L_s \omega i_{AC_q}}{2} - v_{L_d} + v_{S_d} + L \omega i_{AC_q},
\]
\[
(R + sL)i_{AC_q} = \left(s L_s + R_s\right)i_{AC_q} - \left(-\frac{L_s}{2} + L\right) \omega i_{AC_d} + \left(-\frac{L_s}{2} + L\right) \omega i_{AC_d} - v_{L_q} + v_{S_q},
\]
\[
\left(R - \frac{R_s}{2} + s \left(L - \frac{L_s}{2}\right)\right)i_{AC_q} = \left(-\frac{L_s}{2} + L\right) \omega i_{AC_d} - v_{L_q} + v_{S_q},
\]
\[
i_{AC_q} = \frac{1}{R + sL} \left(s L_s + R_s\right)i_{AC_q} + \left(-\frac{L_s}{2} + L\right) \omega i_{AC_d} - v_{L_q} + v_{S_q}.
\]

Substituting the resulting values of \(v_{AC_d}\) and \(v_{AC_q}\) from (4.16) and (4.17) in (4.7) and (4.8):

Equations (4.18) and (4.19) can be used to control the currents through the converter. A block diagram representation of the system and the controller in the \(dq\)-frame is shown in Figure 4.14.

The measured current in the \(dq\)-frame is compared to the commanded value to create the error signal, which is sent through the PI controller to generate the desired control signal. As can be seen from the diagram of the system. The voltage of the AC system influences the current output, as does the current on the other part of the \(dq\)-frame. These values can be measured and accounted for by offsetting the
The actual control signal before it enters the system, thus cancelling their effect.

The $K$ and $a$ parameters of the controller can be designed using well known closed loop system transfer function techniques, adjusting the phase and gain margins. The closed loop transfer function of the system consists of the overall combined transfer functions of the plant, filter and controller. Software packages such as Matlab can be used to determine the gain and phase margins of the system.

### 4.4.5 Voltage Control Loop Design

Once the current controller has been designed and implemented, the outer controls can be implemented. Generally, for a configuration consisting of 2 converters, one of the converters is used to control the power flow through the DC link, understanding that the power entering the line must exit at the other end (minus the losses). This is done simply by measuring the power and adjusting the commanded current reference until the target power value is met. Assuming that the AC voltage is well regulated, the relation between power and current is linear. The current thus can be adjusted directly based on the error between the commanded and measured power values (taking into account the delays created by the power measurements).

The other converter is responsible for controlling the DC link voltage level which is indirectly related to input current. This control is more complex, as the reaction of the voltage to a change in current is not as direct as is the case for power. Thus the control of the system voltage must be designed to ensure that it can operate quickly and generate a stable response. The equation linking the change in voltage across a capacitor with the current passing through it is:

$$i(t) = C \frac{dv(t)}{dt}.$$  \hspace{1cm} (4.20)
The energy stored in a capacitor is:

\[ E = \frac{1}{2} CV^2. \]  

(4.21)

The total power to the capacitors can be expressed as:

\[ \frac{1}{2} C \frac{dV^2}{dt} = -P_{DC} + P_{AC}, \]

\[ \frac{1}{2} C \frac{dV_{DC}^2}{dt} = -\frac{V_{DC}^2}{R_{DC}} + \frac{3}{2} v_d i_d, \]  

(4.22)

where \( R_{DC} \) is the resistance on the DC bus which, in a single converter system, represents the power absorbed on the DC side. In a two-converter system, the power leaving the link at the inverter side (minus the loses on the DC link, which is represented by the resistor) would play the equivalent role. Because the rotational frame is defined by the PLL such that \( v_q \) reference is always 0, it can be removed from the equation.

The capacitor value defined here is not the capacitor of one module. Rather, it is the equivalent capacitor of the converter, with is equal to the equivalent capacitor of all the inserted module capacitors. Under steady-state conditions, each leg will have \( N \) capacitors inserted (either in the lower or upper arm). These capacitors are connected in series, so the overall capacitance is equal to that of \( N \) capacitors connected in series, placed in parallel with the equivalent capacitors of the other two legs:

\[ C_{eq} = 3 \frac{C_{module}}{N}. \]

Although there are \( N \) modules inserted in each leg at any time, there are actually \( 2N \) module in that leg, so assuming the voltage is distributed evenly amongst all the capacitors, the average voltage change is actually half the value calculated above, so (4.22) has to be updated to:

\[ \frac{1}{4} C_{eq} \frac{dV_{DC}^2}{dt} = -\frac{V_{DC}^2}{R_{DC}} + \frac{3}{2} v_d i_d. \]  

(4.23)

Using \( V_{DC}^2 \) as the state variable, the function relating it to the control current \( i_d \) can be extracted from (4.23):

\[ V_{DC}^2 = \left( \frac{3}{4} v_d \right) \left( \frac{1}{C_{eq}} + \frac{1}{R_{DC}} \right) i_d. \]  

(4.24)

This provides a relationship between the DC voltage and the required \( i_d \) current command. Figure 4.15 shows the overall control system including the voltage control.

Because the number of inserted modules in a converter leg is constant, the inserted equivalent capacitor value is as well, making it possible to use the standard phase and gain margin methods to determine the values of the integral and proportional parameters of the controller to obtain good and rapid control of the DC bus voltage.
4.4.6 Circulating Current Control Design

The control technique used to control the circulating currents is similar to the current control loop. Simply transfer measured values to the \(dq\)-frame and use a standard PI controller to reduce them to 0 if possible [15]. Knowing from the previous chapter that the circulating currents are negative sequence and double the frequency, the \(dq\) transform is adjusted using twice the base frequency to convert the circulating currents into DC values. The resulting commands are then transferred back to the \(abc\) frame and added directly to the command resulting from the main current control loop before the number of inserted modules is calculated. Based on Figure 4.13, the inner converter voltage equation is:

\[
V_{DC} = v_U + R_S i_U + L_S \frac{d i_U}{dt} + R_S i_L + L_S \frac{d i_L}{dt} + v_L,
\]

\[
V_{DC} = v_U + v_L + R_S (i_U + i_L) + L_S \frac{d (i_U + i_L)}{dt}.
\] (4.25)

The currents can be split into their three constituting components (DC, AC and circulating). From (2.9) and (2.10):

\[
V_{DC} = v_U + v_L + R_S \left( \frac{I_{DC}}{3} + \frac{i_{AC}}{2} + i_{circ} + \frac{I_{DC}}{3} - \frac{i_{AC}}{2} + i_{circ} \right)
+ L_S \frac{d \left( \frac{I_{DC}}{3} + \frac{i_{AC}}{2} + i_{circ} + \frac{I_{DC}}{3} - \frac{i_{AC}}{2} + i_{circ} \right)}{dt},
\]

\[
V_{DC} = v_U + v_L + R_S \left( \frac{2I_{DC}}{3} + 2i_{circ} \right) + L_S \frac{d \left( \frac{2I_{DC}}{3} + 2i_{circ} \right)}{dt},
\]

\[
V_{DC} = v_U + v_L + R_S \left( \frac{2I_{DC}}{3} + 2i_{circ} \right) + L_S \frac{d (2i_{circ})}{dt},
\]

\[
V_{DC} - v_U - v_L - R_S \frac{2I_{DC}}{3} = 2R_S i_{circ} + 2L_S \frac{d (i_{circ})}{dt}.
\] (4.26)
The term \( I_{DC} \) was removed from the derivative as it is constant. This equation is transferred into the \( dq \)-frame:

\[
P^{-1}V_{DC} - P^{-1}v_{Udq} - P^{-1}v_{Ldq} - R_S \frac{2P^{-1}I_{DC}}{3} = 2R_S P^{-1}i_{circdq} + 2L_S \frac{d(P^{-1}i_{circdq})}{dt},
\]

\[
-(v_{Udq} + v_{Ldq}) = 2R_S i_{circdq} + 2L_S P \frac{d(P^{-1}i_{circdq})}{dt},
\]

\[
-\frac{v_{Udq} + v_{Ldq}}{2} = R_S i_{circdq} + L_S P \frac{dP^{-1}}{dt} i_{circdq} + L_S \frac{di_{circdq}}{dt}.
\]  

(4.27)

The \( V_{DC} \) and \( I_{dc} \) terms have been removed from the left side of the equation as they contain no \( d \) or \( q \) components, only zero sequence terms. Knowing that:

\[
P \frac{dP^{-1}}{dt} = \begin{bmatrix} 0 & -\omega \\ \omega & 0 \\ 0 & 0 \end{bmatrix},
\]

the equation becomes:

\[
\frac{v_{Udq} + v_{Ldq}}{2} = \begin{bmatrix} R_S & 0 & 0 \\ 0 & R_S & 0 \\ 0 & 0 & R_S \end{bmatrix} i_{circdq} + \begin{bmatrix} 0 & -\omega L_S & 0 \\ \omega L_S & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} i_{circdq} + L_S \frac{di_{circdq}}{dt},
\]

\[
\frac{v_{Udq} + v_{Ldq}}{2} = \begin{bmatrix} R_S & -\omega L_S & 0 \\ \omega L_S & R_S & 0 \\ 0 & 0 & R_S \end{bmatrix} i_{circdq} + L_S \frac{di_{circdq}}{dt}.
\]  

(4.28)

The term \( \frac{v_{Udq} + v_{Ldq}}{2} \) constitutes the command for the circulating current controller. As seen before, in order to control the circulating currents, the arm voltages \( v_L \) and \( v_U \) must be controlled together and fluctuate by the same amount. To simplify the equations, \( \frac{v_{Udq} + v_{Ldq}}{2} \) is replaced by \( V_{cmddq} \) below. From 4.28, the individual equations in the \( d \) and \( q \) reference can be extracted and represented as transfer functions:

\[
-V_{cmddq} = (R_S + s L_S) i_{circdq} - \omega L_S i_{circq},
\]  

(4.29)

\[
-V_{cmdq} = (R_S + s L_S) i_{circq} + \omega L_S i_{circdq}.
\]  

(4.30)

Isolating the circulating current terms from (4.29) and (4.30):
\[
(R_S + sL_S) i_{circ_d} = -V_{cmd_d} + \omega L_S i_{circ_q},
\]
\[
i_{circ_d} = \frac{1}{R_S + sL_S} \left( -V_{cmd_d} + \omega L_S i_{circ_q} \right),
\]
\[
(R_S + sL_S) i_{circ_q} = -V_{cmd_q} - \omega L_S i_{circ_d},
\]
\[
i_{circ_q} = \frac{1}{R_S + sL_S} \left( -V_{cmd_q} - \omega L_S i_{circ_d} \right).
\]

This controller is thus similar to the current controller, without the presence of \( v_S \) as an offset and the cross-terms are only regulated by the arm inductances. The diagram of the controller and system is shown in Figure 4.16.

The resulting \( V_{cmd} \) is added to both the upper and lower arm controls, applying the same control to both \( v_L \) and \( v_U \) such that, as covered previously, it has no effect outside the converter but only affects the circulating currents.

When the circulating current controls are enabled, more or fewer than \( N \) modules can be connected in a leg at any point in time. As the circulating currents are due to an imbalance in the capacitor voltage levels caused by the different phase offsets between the currents in each phase, one way to fix this imbalance is to insert more (or fewer) modules in a leg, thus creating a overall voltage magnitude that is uniform across all three phases. This technique can help greatly reduce the losses due to circulating currents.
currents and increase the efficiency of the converter.

The circulating currents also inherently help balance the voltages between the legs. If a situation arises that causes a large imbalance between the phases, this mechanism will not be available to correct it if the circulating currents are controlled to 0. It may thus be useful to explore the controlled use of circulating currents to correct imbalances between the phases.

### 4.5 Conclusion

This chapter covered the implementation of the MMC controls in the real-time simulator. The division of the simulation system between the FPGA, RTDS and cRIO hardware platforms was discussed as well as the interfaces between them. The modelling technique for the MMC as implemented in the FPGA platform was presented as well. Equations necessary for the implementation of the controls were derived and the control loops design presented.

With the implementation now well defined, the next chapter will focus on the modelling aspect and compare a model of the MMC containing all switches to the system created using the modelling technique presented in this chapter, using a lumped representation of the individual modules, to ensure that they provide equivalent results.
Chapter 5

Model Validation (Off-line Simulation)

Before implementing the MMC model in the FPGA platform of the real-time simulator, it is important to determine if the modelling technique presented in section 4.3.2 is correct. The model implemented on the FPGA uses equivalent resistances for the IGBTs ON and OFF states, and lumps them into one single variable resistor. The capacitor voltages are individually updated, and the total inserted module voltages is also lumped and represented as a single controlled voltage source. It is important to ensure that the model used and implementation accurately represent the behaviour of the MMC. To verify that this is the case, the MMC model as it will be implemented in the FPGA must be compared with a model known to be accurate. The goal of these simulations is simply to confirm the correct operation of the models, as such, they do not need to be performed in real-time, as such, they were implemented completely off-line, using PSCAD. Two distinct MMC models were implemented and simulated:

1. A MMC model including all individual IGBTs, diodes and capacitors for every module of the converter (referred to as the full model below).

2. A MMC model implemented using the modelling technique presented in section 4.3.2, which lumps the individual module voltages and resistances into one equivalent resistance and controlled voltage source for each arm (referred to as the lumped model below).

As is would not be practical to implement a MMC containing 400 modules per arm in PSCAD, considering all 4800 IGBTs and diodes, the system simulated in this chapter is a smaller MMC, containing 12 modules per arm. This system size is sufficient to provide a good comparison of the simulation results of the two models and ensure that the lumped modelling technique used in the FPGA implementation is an accurate representation of the MMC.

This chapter shows the results of several simulation scenarios comparing the response of both models to changes in control reference point as well as disturbances caused by faults.

5.1 Study System

The system implemented for the off-line PSCAD simulations consists of an ideal voltage source as well as a transformer on the AC side and a fixed load on the DC side. As such, it is possible to evaluate
solely the performance for the MMC itself and its reaction to changes in command references or faults. The system used for the simulations is shown in Figure 5.1 and the system parameters are given in Table 5.1.

![Figure 5.1: One line diagram of the system used used in simulations for comparison of full and lumped MMC models](image)

The converter parameters were selected to resemble the converters of the HVDC link currently under construction between France and Spain described in [16], with the power and voltages reduced to fit the lower number of levels. The DC side load is represented with fixed resistances to allow for DC voltage control. The control technique used in this converter is similar to one that would be used to control a MMC with a higher number of levels, the only major difference being the lower number of levels leading to faster sorting and selection, which is not an issue here given the fact that this simulation is performed off-line. Gain parameters were also selected specifically to stabilize the system.

The ON resistance of all diodes and thyristors is set to 0.01 Ω, and the OFF resistance to 1 MΩ for both models. The system includes only the components required for accurate simulation, omitting bypass switches and thyristors, as they are not relevant in this case.

### 5.1.1 Implementation

Function blocks were created in PSCAD to sort the voltages, one for each arm, based on the bubble sort algorithm presented earlier. The standard algorithm was implemented here instead of the parallelized odd-even sort implemented in the FPGA. The resulting order of capacitor voltages is then used to select which modules in each arm is connected to the system and the modules are switches using the NLC method.

Modules are inserted or bypassed only when the commanded number of inserted module changes. Because the NLC control technique does not provide for enough switching opportunities to keep the capacitor voltage balanced, modules are additionally swapped every 250 μs. At each swapping instant, one module is inserted in the arm as another is bypassed, allowing for a more precise distribution of the voltages across the capacitors, as the increased number of switchings allows for a better selection of the inserted and bypass modules.
Table 5.1: Specification of the converter and controls used in simulations for comparison of complete and implemented MMC models

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC Source Voltage (L-L, rms) ( (V_{AC}) )</td>
<td>10 kV</td>
</tr>
<tr>
<td>AC Source Frequency</td>
<td>60 Hz</td>
</tr>
<tr>
<td>AC System Resistance</td>
<td>0.1 Ω</td>
</tr>
<tr>
<td>AC System Inductance</td>
<td>0.1 mH</td>
</tr>
<tr>
<td>Transformer Windings ( Y_g / \Delta )</td>
<td></td>
</tr>
<tr>
<td>Transformer Ratio (L-L, RMS) ( 12 / 10 \text{kV} )</td>
<td>18.4 MVA</td>
</tr>
<tr>
<td>Transformer Impedance</td>
<td>18%</td>
</tr>
<tr>
<td>Number of Modules per Arm ( (N) )</td>
<td>12</td>
</tr>
<tr>
<td>Module Capacitor Value ( (C_{module}) )</td>
<td>12.5 mF</td>
</tr>
<tr>
<td>Expected Capacitor Voltage ( (V_{module}) )</td>
<td>1.6 kV</td>
</tr>
<tr>
<td>Arm Inductor ( (I_{arm}) )</td>
<td>2.5 mH</td>
</tr>
<tr>
<td>DC Voltage ( (V_{DC}) )</td>
<td>± 9.6 kV</td>
</tr>
<tr>
<td>DC Rated Power ( (P_{DC}) )</td>
<td>18.4 MW</td>
</tr>
<tr>
<td>Total DC Side Resistance ( (R_{DC}) )</td>
<td>20 Ω</td>
</tr>
<tr>
<td>Switches ON Resistance ( (R_{ON}) )</td>
<td>0.01 Ω</td>
</tr>
<tr>
<td>Switches OFF Resistance ( (R_{OFF}) )</td>
<td>1 MΩ</td>
</tr>
</tbody>
</table>

**Controller Gains**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current Proportional Gain</td>
<td>2</td>
</tr>
<tr>
<td>Current Integral Time Constant</td>
<td>0.003s</td>
</tr>
<tr>
<td>Current Cross Terms Gain</td>
<td>0.2</td>
</tr>
<tr>
<td>Voltage Proportional Gain</td>
<td>2</td>
</tr>
<tr>
<td>Voltage Integral Time Constant</td>
<td>0.01s</td>
</tr>
<tr>
<td>Circulating Current Proportional Gain</td>
<td>0.2</td>
</tr>
<tr>
<td>Circulating Current Integral Time Constant</td>
<td>0.03s</td>
</tr>
<tr>
<td>Circulating Current Cross Terms Gain</td>
<td>0.2</td>
</tr>
</tbody>
</table>

Assuming a full amplitude output waveform, using the NLC control technique only, each module is inserted and bypassed once per cycle (inserted once and bypassed once), for an overall switching frequency of 120Hz. With the additional swapping of modules introduced here, the average switching frequency of each module is 450Hz.

Currents through the arms and on the AC side are monitored for control as well as voltages on the AC and DC side. The current, voltage and circulating current controls are implemented in the \( dq \)-frame, using PI controllers as presented in section 4.4.2 of the previous chapter.

The second simulation system was implemented using the lumped modelling technique, as presented in section 4.3.2. As the modules are represented by a single resistor and controlled voltage source per arm instead of modelling all the switches and modules separately, the simulation times are greatly reduced, even for relatively small systems such as this one. The controls are implemented exactly as for the full
model simulation.

For this simple system, the time required to perform a 1.5 seconds simulation was reduced from approximately 5:30 minutes for the full model including all the switches to 30 seconds for the lumped model, for a 1100% improvement in simulation time. As the size of the converter increases, and with it, the size of the admittance matrix to invert and the frequency at which it has to be inverted, it is expected that the gain in simulation time would keep improving.

5.2 Test Scenarios

Five test scenarios were selected:

1. Activation of the circulating current controller.
2. Reactive current command change from 0.5 pu to -0.5 pu.
3. DC voltage reference command change from 0.9 pu to 1.1 pu.
4. Single phase line to ground fault at the point of AC connection, on the secondary side of the transformer.
5. DC side fault to ground.

These scenarios were chosen to represent a range of operation of the converter, change in the current reference directly, in the voltage reference and more unusual and unbalanced scenarios represented by the fault cases.

The first test scenario represents a fairly minor change, and was selected as a starting point to ensure that the control are implemented correctly and that the commanded voltage and reactive current remain stable through the activation of the circulating current controller. This test also shows the effects of the currents on this specific system including their effect on the capacitor voltages in both models.

The second scenario allows for testing of the inner-loop current controller, as well as for the decoupling of the real and reactive controls through \(d\) and \(q\). As such, this rapid change in the reactive current \(i_q\) reference should have little effect on the real power transfer, controlled by \(i_d\). A change in reactive current reference should have a relatively minor effect inside the converter.

Scenario number three evaluates the correct operation of the outer-loop voltage control, generating the reference \(i_d\) command to the inner-loop current controller. This controller was indirectly tested in the previous scenario when the DC voltage had to be maintained through a change in reactive current reference, but here the stability and dynamic operation of the controller will be tested. As the \(i_d\) and \(i_q\) controls have been designed to decouple both values, the reference change in \(V_{DC}\), affecting directly \(i_d\) should have little effect on \(i_q\).

The fourth scenario tests the performance of the controls to an asymmetric fault located directly at point of connection of the converter, which will force a much stronger reaction from the controls and impose a more unusual strain on the model. This case should generate large circulating currents and provide a good test of the accuracy of the lumped model when compared to the full model.

The final simulated case tests the performance of the control to a fault to ground located directly at the positive DC bus terminal of the converter and provides a difficult test for the controls and models, completing the comparison between the response of both MMC model implementations. This fault
should generate even larger perturbations in arm currents and module voltages, although symmetrically
to all three phase contrary to the previous AC fault case.

The parameters compared during the simulations are:

1. Capacitor voltages.
2. Arm currents.
3. Circulating currents.
4. AC currents in $dq$-frame.
5. DC Voltage.
6. Positive and Negative MMC DC terminal voltage with respect to ground (only for scenarios 4 and 5)

If the internal measures of the converter, represented by the capacitor voltages, arm and circulating
currents are the same, the conclusion can be made that the models are equivalent. The AC currents
and DC voltages are also compared to verify that the controls perform in a similar way for both models.
The positive and negative terminal voltages have been included only for the fault scenarios as they do
not exhibit any interesting behaviour during the others.

5.2.1 Circulating current controls activation

Table 5.2: Information for the PSCAD simulations of the circulating current controller activation,
comparing the 12 levels full MMC model with the lumped model

<table>
<thead>
<tr>
<th>Disturbance</th>
<th>Activation of the Circulating Current Controller</th>
</tr>
</thead>
<tbody>
<tr>
<td>Disturbance Instant</td>
<td>1 sec</td>
</tr>
<tr>
<td>Reference Commands</td>
<td>Before Disturbance After Disturbance</td>
</tr>
<tr>
<td>Reactive Current Reference</td>
<td>0 pu 0 pu</td>
</tr>
<tr>
<td>DC Voltage Reference</td>
<td>1 pu 1 pu</td>
</tr>
<tr>
<td>Circulating Current Control</td>
<td>OFF ON</td>
</tr>
</tbody>
</table>

For the first simulated case, the reference current and voltage commands remain constant, but the
circulating current control, which is originally disabled, is activated at $t = 1$sec. The activation of
the controller minimizes the contribution of the circulating currents on the overall arm currents, which
affects the capacitor voltage fluctuations. Important simulation parameters are shown in Table 5.2.

As the circulating currents are contained inside the converter; it is expected that the activation of the
controller will have no effect on the outside signals (AC currents and DC voltage). The lower currents
after the activation of the controller should be reflected in smaller arm currents and oscillations of the
module capacitors.

The results are presented in figures formatted as follows: the left side sub-plots on the figure shows
the results of both simulations, overlapped in a single plot. The sub-plots located on the right side show
the difference between the simulations results at each simulation instant. The simulation results are
shown in Figure 5.2.
Figure 5.2: Comparison between the simulation results of the full and lumped models of a 12 levels
MMC converter during the activation of the circulating current controller

Simulation Results

As the figure shows, the result of the simulations performed using the full and lumped models match
very well in this case. With all the signals tracking very well between the two models.

The first row of sub-plots (a & b) in the figure presents the voltage of one module capacitor, located
in the upper arm of phase A. It may appear as if the voltages have not yet reached steady-state at the
time the controller is activated, but this is not the case. The system has reached steady-state, however
oscillations of the the voltage measurement are noticeable in the plot in due to the large circulating
currents. As soon as the circulating current controller is activated, the oscillations disappear. It can
also be noted that the amplitude of the fluctuations is smaller after the activation of the controls, which
is as expected, as the arm currents are reduced as the circulating currents amplitude is reduced. Sub-
plot b, showing the difference between the simulation results of both models shows that they yield very
similar results, both in steady-state and during the transition, with the differences being attributable
to differences in the timing and order of the selection of the individual modules and being very small
compared to the amplitude of the signals tracked.

The second row of sub-plots (c & d) shows the upper arm current of phase A. The current does not
appear to be oscillating like was the case for the capacitor voltages, but the attentive eye will notice
that the waveform before the activation of the controller is not sinusoidal. The 2nd harmonic circulating
currents are in phase with the arm currents, making the oscillations more difficult to notice. The effects
of the circulating current is more easily noticed when comparing the arm currents before and after the
activation of the controller; as the waveform is a cleaner sinusoidal and the apparent offset created by
the circulating current is eliminated. The difference between the result of the simulation of the two
models are negligible, as highlighted in sub-plot d.

The third row (sub-plots e & f) shows the circulating current measured in phase A. As can be
noted, the current magnitude before the activation of the controller is almost 0.15 pu. The current
is not completely eliminated after the activation of the controller: it is clearly much smaller and of a
much higher frequency, but the amplitude is still relatively large. This is due to the limited number of
modules in the converter. The technique used to control the circulating currents is to insert of bypass
additional modules in the individual legs. For each additional inserted module, the total inserted voltage
of the leg changes by \(\frac{1}{12}\) of the total DC voltage. This creates a noticeable change in the output
voltage whenever an additional module is inserted or bypassed. These fluctuations are visible here, as the
circulating currents are minimized after the controller is activated, but large high frequency noise is still
present in the currents, and noticeable on the DC voltage, due to the constant inserting and bypassing
of modules. For converters with a larger number of levels, inserting of bypassing an additional module
in individual legs has a smaller relative effect on the total inserted voltage, thus the circulating currents
and DC Voltage are better behaved after the activation of the controller, which will be the case in the
model implemented in the real-time simulator which has 400. It can nevertheless be seen that controller
effectively reduces the circulating currents in the converter, as they are at approximately 1/3rd of their
original levels after the control activation. This causes a reduction in the amplitude of the fluctuations
of the converter module voltages and arm currents. Sub-plot f shows here again that both models yield
equivalent results.

The fourth row of sub-plots (g & h) shows the AC side currents in the \(dq\) reference. As sub-plot g
shows, the activation of the circulating current controller has almost no effect on the AC side currents
as both are unaffected by the activation, which is as expected, as the circulating currents do not leave
the converter. Sub-plot h shows that the results track almost perfectly for both simulations.

The last row of sub-plots (i & j) shows the measured voltage across the DC side resistors. The
activation of the circulating current controller does create disturbances on the DC voltage. This is to be
expected given the noise generated by the circulating current controller. The amplitude of the inserted
voltage in each leg constantly changes when additional modules are inserted or bypassed to control the
circulating currents. These fast oscillations transfer over to the DC bus directly, as there are no filters
or dampers in the system as simulated. It can be seen, however, that the average voltage of the DC bus
remains consistent with the commanded reference. Sub-plot j shows that the simulation results agree
for both models.
Simulation Conclusion

This first test scenario thus shows that, for both models, the circulating currents have the expected effects on the controller. The activation of the controller limits the amplitude of the circulating currents effectively, although it does produce some high frequency noise on the signals. After activation, oscillations in the module capacitor voltages and arm currents are reduced noticeably, whereas external signals are mostly unaffected (other than the high frequency noise on the DC bus voltage), as expected. The simulation results for both models are very similar, confirming the accuracy of the lumped model model in this case.

5.2.2 Change in reactive current command

Table 5.3: Information for the PSCAD simulations of a reactive current control reference step change, comparing the 12 levels full MMC model with the lumped model

<table>
<thead>
<tr>
<th>Disturbance</th>
<th>Step change in reactive current ($i_q$) reference from 0.5 pu to -0.5 pu</th>
</tr>
</thead>
<tbody>
<tr>
<td>Disturbance Instant</td>
<td>1 sec</td>
</tr>
<tr>
<td>Reference Commands</td>
<td>Before Disturbance</td>
</tr>
<tr>
<td>Reactive Current Reference</td>
<td>0.5 pu</td>
</tr>
<tr>
<td>DC Voltage Reference</td>
<td>1 pu</td>
</tr>
<tr>
<td>Circulating Current Control</td>
<td>ON</td>
</tr>
</tbody>
</table>

The second test case introduces a first change in command reference. In this scenario, the reactive current command is changed instantly from 0.5 pu to -0.5 pu at $t = 1$ sec, while the DC voltage reference remains unchanged at 1 pu. For this test, the circulating current controller is activated throughout. Important simulation parameters are shown in Table 5.3, and the result of the simulation is shown in Figure 5.3.

In this case, it is expected that the reference change in reactive current ($i_q$) will propagate through the converter as AC currents circulate through the MMC. As such, arm currents as well as capacitor voltage fluctuations will be affected by the change. As the controller is designed to decouple the real and reactive components, it is expected that the $i_d$ current component will remain mostly unaffected by the change, as will the DC side voltage. The circulating current controller is activated throughout the simulation, thus it is expected that the circulating currents will display short and limited transient during the reference change, and quickly return to their pre-event level as the system settles.

Simulation Results

As can be seen from the figure, the simulation results match very well between the 2 models. The system reacts very well to the command and settles back quickly to the new steady-state point.

As can be seen from sub-plot a, the change in reactive current reference does have an effect on the internal MMC operation. As AC currents flow through the converter, a change in the external AC current is also detected internally. This reference change thus affects the capacitor voltages fluctuations. The capacitor voltages are slightly different between the simulations on certain occasions which is explained by the selection and switching algorithms, which many not always insert or bypass the same modules.
Figure 5.3: Comparison between the simulation results of the full and lumped models of a 12 levels MMC converter for a step change in reactive current reference.

at the exact same instants. However, sub-plot b shows that the overall voltage of the modules are very similar with no notable difference between the two simulations even during the transient.

The upper arm current of phase A, shown in sub-plot c is also affected by the reference change, as expected, with very small, but noticeable differences in the envelope and amplitude of the sinusoidal signal after the reference change.

In this scenario, the circulating current controller is active. As such, the oscillations in the currents are small, only the noise caused by the insertion and bypass of modules is visible. There is a limited, but noticeable transient in sub-plot e at the time of the reference change. The control quickly reacts and limits the amplitude circulating currents. As can be seen in sub-plot f, the disturbance is controlled in the same manner in both cases, creating no noticeable difference spike, even during the transient.

Sub-plot g, showing the AC side currents, confirms that the reactive current reference change was
Chapter 5. Model Validation (Off-line Simulation)

applied as expected. The reactive current $i_q$ quickly settles at the new reference with very limited oscillations. This change also has an effect on the real current $i_d$ which shows that the 2 components are not perfectly decoupled, however, given the amplitude of the change in $i_q$, the effect on $i_d$ is very limited. The $i_d$ signal does take a little longer to settle, which is to be expected as its reference is generated by the outer-loop voltage controller. Sub-plot h shows no noticeable discrepancies during the transient.

As can be expected after noticing disturbances in $i_d$ during the transient, the DC voltage, shown in sub-plot i, is also affected. The disturbances in the voltage level closely follow the ones in the real current $i_d$, confirming the correct definition of $i_d$ as the component of the $dq$ representation of the current responsible for real power transfer control. The high frequency oscillations on the voltage caused by the circulating current controller are visible in this case as well, but both models yield equivalent results.

**Simulation Conclusion**

This second scenario shows that the response of the system to a change in reactive current reference is almost identical between the two modelled systems. The change in reactive current command does, as expected, affect the arm currents and capacitor voltages, but the system settles quickly after the command change. A short transient in $i_d$ and $V_{DC}$ after the reactive current reference change shows that the real and reactive components of the system are not perfectly decoupled in the controller, however, given the magnitude of the reactive current change, the response is considered acceptable for the purpose of the comparison.

**5.2.3 Change in DC voltage reference**

Table 5.4: Information for the PSCAD simulations of a DC voltage reference step change, comparing the 12 levels full MMC model with the lumped model

<table>
<thead>
<tr>
<th>Disturbance</th>
<th>Step change in DC voltage reference from 0.9 pu to 1.1 pu</th>
</tr>
</thead>
<tbody>
<tr>
<td>Disturbance Instant</td>
<td>1 sec</td>
</tr>
<tr>
<td>Reference Commands</td>
<td>Before Disturbance</td>
</tr>
<tr>
<td>Reactive Current Reference</td>
<td>0 pu</td>
</tr>
<tr>
<td>DC Voltage Reference</td>
<td>0.9 pu</td>
</tr>
<tr>
<td>Circulating Current Control</td>
<td>ON</td>
</tr>
</tbody>
</table>

This third test scenario simulates a change in the DC voltage reference command. In this scenario, the reactive current command is set at 0 pu, while the DC voltage reference steps from 0.9 to 1.1 pu at $t = 1$ sec. For this test, the circulating current controller is activated throughout. Important simulation parameters are shown in Table 5.4, and results of the simulation in Figure 5.4.

This reference change will directly affect the individual capacitor module voltages, which will now support a higher voltage level. As the DC side is represented by a fixed load, the system will transfer more power after the change to support the desired voltage. As such, the AC and arm currents are expected to increase. The reactive command remains unchanged, thus the $i_q$ component of the AC current should be unaffected. However, the previous scenario has shown that the $i_d$ and $i_q$ components are not perfectly decoupled, so a short transient is expected. As the circulating current controller is active
in this simulation, current should remain unaffected, with the possible exception of a short transient.

![Graphs showing simulation results and differences between full and lumped models.](image)

Figure 5.4: Comparison between the simulation results of the full and lumped models of a 12 levels MMC converter for a DC voltage reference step change

**Simulation Results**

The figure shows that the models produce equivalent results in this scenario as well. Some discrepancies are noticeable during the transient, most noticeably on the arm and circulating currents, but their amplitude is limited and they settle quickly with the DC voltage.

Sub-plot a shows that the control operates smoothly and the capacitor voltages settle at the new reference value within approximately 100ms. The higher voltage reference, sustained by larger arm currents does increase the amplitude of voltage fluctuations.

The upper arm current of phase A, shown in sub-plot c is also affected by the reference change, as expected since more power is transferred through the converter to the DC side. Sub-plot d shows short
lived differences between the individual simulation results as the control settles to the final value, but their overall amplitude is much less than 10% of the total current or voltage, and their duration is very short. Looking at sub-plot f, the fluctuations track the circulating currents. As such, slight offsets in the timing of the reaction of the controllers between the two simulations seem to be the most likely culprit for the discrepancies in arm currents. The discrepancies are not noticeable in sub-plot c; the models match even during these fast transients.

Here again, most oscillations in the circulating currents are very small, mostly hidden in the noise caused by controller. There are noticeable oscillations in sub-plot e for 200ms after the reference change, as the control adjusts to changing module voltages and arm currents. The controls perform well and limit the circulating current magnitude. Sub-plot f shows some discrepancies between both simulations. They are, however, very short lived and most likely caused by small timing differences in the operation of the controllers between the simulations. As the envelope of the signals, as shown in sub-plot e, are very similar between the simulations, the models can be considered to match well regardless.

Sub-plot g, shows that the decoupling of the two signals ($i_d$ and $i_q$) is not perfect, but here again, the effect on $i_q$ is limited given the large change in $i_d$. There is a small discrepancy, shown in sub-plot h, between the simulations as the voltage settles to the new steady-state position, especially in $i_d$. But these differences are small (much less than 5% of the total current) and short lived, here again most likely caused by slight timing differences in the control reactions between the models.

Sub-plot i shows that the DC voltage control performs nicely and the system settles at the new operating point in 150ms with limited overshoot. Sub-plot j shows almost no discrepancy between both simulations.

**Simulation Conclusion**

This scenario shows that the response of the system to a change in DC voltage reference is very similar between the two models. The change in DC voltage causes the expected changes in module voltages and fluctuations as well as arm current, confirming the correct implementation of the models. Some differences are noticeable between the results, but they are short lived and limited in amplitude, likely caused by controller timing differences between the 2 simulations. The envelopes of the signals track very well however and both models are still considered to be equivalent in this case.

### 5.2.4 Single Phase Fault at the point of AC connection

Table 5.5: Information for the PSCAD simulations of a 100ms single phase-to-ground AC fault at the converter, comparing the 12 levels full MMC model with the lumped model

<table>
<thead>
<tr>
<th>Disturbance</th>
<th>100m single phase-to-ground on phase A at the point of AC connection of the converter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Disturbance Instant</td>
<td>1 sec</td>
</tr>
<tr>
<td>Reference Commands</td>
<td>Before Disturbance</td>
</tr>
<tr>
<td>Reactive Current Reference</td>
<td>0 pu</td>
</tr>
<tr>
<td>DC Voltage Reference</td>
<td>1 pu</td>
</tr>
<tr>
<td>Circulating Current Control</td>
<td>ON</td>
</tr>
</tbody>
</table>
The fourth test scenario considers a 100ms line-to-ground fault, applied on phase A directly at the point of connection of the AC system with the converter. This will generate asymmetric arm currents and circulating currents as well as important fluctuations in the module capacitor voltages of phase A. The reactive current and DC voltage command references are fixed throughout at 0 pu and 1 pu respectively and the circulating current controls are active. Important simulation parameters are shown in Table 5.5, and results of the simulation in Figure 5.5.

Figure 5.5: Comparison between the simulation results of the full and lumped models of a 12 levels MMC converter during a 100ms single phase-to-ground AC fault at the converter

Simulation Results

When the fault is triggered, the point of common connection of the converter at phase A is stuck to ground. However, as the secondary side of the transformer is an ungrounded delta, the AC side voltages of phases B and C are allowed to float and the phase-to-phase voltage on the secondary side \((V_{ab}, V_{bc}, V_{ca})\)
remain as before the fault. The converter is thus still able to maintain the DC voltage by drawing more power from phases B and C. Large imbalances are created however as the current flow through leg A is affected by the fault. These imbalances generate circulating currents through the converter legs.

The figure shows that both models yield almost identical simulation results, with very limited discrepancies.

Sub-plot a shows that, upon triggering of the fault, the capacitor voltages suddenly drop, but settle as the system reaches a stable operating point, maintaining operation through the fault. The voltages quickly return to their original value after the fault clears.

The upper arm current of phase A, shown in sub-plot c, is also reduced during the fault, as there is no more current input from the AC system, but circulating currents appear and provide voltage support for the modules in the leg. It can be noticed that the average value of the current signal is different, as a DC offset is introduced through the circulating currents and represents the power being transferred from legs B and C which help support capacitor voltages in leg A. It can be noticed that the arm currents follow the circulating current closely, showing that a large part of the current flowing through the arm (and leg) is generated by the imbalance inside the converter.

The circulating current controller is active throughout this simulation, but the imbalances between the different converter legs are too severe and circulating current is still present. One interesting note, the circulating currents in this case are first harmonic (and DC), instead of the usual second, which makes sense in this case as only one of the phases (A) has lost current influx from the AC system. Currents thus circulate internally to correct the imbalance, which in this case has 60Hz frequency. As the circulating current controller is designed to minimize second harmonic currents, these first harmonic currents are not neutralized and are allowed to flow. Both simulated models produce almost identical results here as well despite the imbalance.

Sub-plot g shows that the flow of real current $i_d$ increases during the fault, as expected as the current flowing through phase A now drains through the fault and is not transferred to the DC side. Thus additional power must be transferred to maintain the desired voltage level. The sub-plot also shows that the reactive current controller performs well and maintains the current $i_q$ at the desired 0 pu throughout.

Sub-plot i shows that the DC voltage is well supported even during the fault, as current still flows through the converter. The voltage barely deviates from the target of 1 pu and has almost returned to the reference value by the time the fault clears. The clearing of fault causes a small rise in voltage, as power is now flowing again through phase A, which settles back nicely.

As can be seen from sub-plot k, with the voltage at the point of connection at phase A stuck to ground during the fault, as the number of modules inserted in each arm is changing, so are the DC terminals voltages. However, the voltage between the positive and negative terminals remains constant during the fault. The difference between the simulation results, shown in sub-plot l is of the order of 1% of the signal amplitudes, and as such, the simulations are considered to match.

**Simulation Conclusion**

The delta-connected secondary side enables the system to maintain phase-to-phase voltage on the AC side during the fault, which allows for power transfer through the converter. The AC current from phase A, which does not reach the converter any more, is partially replaced internally by large circulating currents, supporting the voltage of the capacitors of leg A and allowing for continued operation. The system performs well and remains stable throughout. This scenario shows that the response of the system
to an asymmetrical phase-to-ground fault on phase A at the point of connection of the converter to the AC system is very similar between both systems, confirming the accuracy of the lumped model, even when large imbalances are present in the AC system.

### 5.2.5 DC fault

Table 5.6: Information for the PSCAD simulations of a 100ms phase-to-ground fault at the positive DC terminal, comparing the 12 levels full MMC model with the lumped model

<table>
<thead>
<tr>
<th>Disturbance</th>
<th>100m phase-to-ground fault at the positive terminal of the DC bus</th>
</tr>
</thead>
<tbody>
<tr>
<td>Disturbance Instant</td>
<td>1 sec</td>
</tr>
<tr>
<td>Reference Commands</td>
<td>Before Disturbance</td>
</tr>
<tr>
<td>Reactive Current Reference</td>
<td>0 pu</td>
</tr>
<tr>
<td>DC Voltage Reference</td>
<td>1 pu</td>
</tr>
<tr>
<td>Circulating Current Control</td>
<td>ON</td>
</tr>
</tbody>
</table>

This last simulation considers a 100ms fault to ground directly at the positive DC bus. The reactive current and DC voltage command references are fixed throughout at 0 pu and 1 pu respectively and the circulating current controls are active. Important simulation parameters are shown in Table 5.6, and results of the simulation in Figure 5.6.

It is expected that the fault will create large disturbances in the system. As the positive DC terminal will be forced to ground, and the secondary side of the transformer is ungrounded, the secondary side voltages will float and that the negative DC voltage terminal will support the full voltage of the DC link. As the DC side resistance will effectively be reduced by half, the power transfer will double to maintain voltage support during the fault, with the associated effects on the arm currents and capacitor voltage fluctuations.

### Simulation Results

When the fault is triggered, the positive side of the DC bus is immediately fixed to 0V. As can be seen from the plots however, the system still manages to support the DC voltage by increasing the real power transfer (through $I_d$). As the transformer’s secondary side is delta-connected and not grounded, the voltages are allowed to float and what was previously the positive terminal of the DC bus now becomes the ground reference. Phase-to-phase voltage is maintained on the secondary side and the negative DC terminal which previously supported a voltage of -9.6 kV now supports twice that amount. The results would have been much different had the secondary side been a grounded Wye connection as this DC offset would not have been possible. But here, the arm currents increase during the fault as some current sinks through the fault, but the converter manages to maintain a stable equilibrium during the event.

The figure shows that, as in the previous scenarios, the models produce almost identical results. Even the large changes in AC and arm currents as well as the capacitor DC voltages produce no notable difference between the models.

Sub-plot a shows that; upon triggering of the fault, the voltages suddenly drop, but the system quickly reacts by increasing power transfer to the converter and they are inching back towards their
Figure 5.6: Comparison between the simulation results of the full and lumped models of a 12 levels MMC converter during a 100ms phase-to-ground fault at the positive DC terminal

pre-fault levels by the time it clears. The higher currents do cause larger fluctuations during the fault, but the system remains stable. The voltages quickly return to their original value after the fault clears.

Sub-plot c shows that the arm currents increase during the fault, which is expected as a the DC side resistance (representing the load) is halved by the fault (as one of the 2 resistors is now grounded on both sides). Additional current is thus required to maintain the commanded voltage on the DC bus.

The circulating current controller is active throughout this simulation and, as the fault is symmetrical on all three phases, performs well during the transient. Disturbances are noticeable in sub-plot e, particularly at the triggering of the fault, but the controller maintains the circulating currents to an acceptable level throughout.

From sub-plot g, the flow of real current \(i_d\) increases during the fault, as expected. The sub-plot also shows that the reactive current control performs well and maintains the current \(i_q\) at the desired 0 pu
throughout.

Sub-plot i shows that the DC voltage is well supported even during the fault. After an initial drop as the fault is triggered, the voltage inches back towards 1 pu as the voltage controller increases the setpoint for $i_d$ to bring back the DC voltage to the commanded level. Once the fault clears, the voltage peaks as the power transferred is now higher than in the original steady-state, but quickly settles back to 1 pu as the controller adjusts to the fault clearing.

Sub-plot k shows that the DC terminal voltages do float with respect to ground, and as the positive terminal is now stuck to ground because of the fault, the negative terminal floats down to compensate. The differences between the results of both simulations are negligible in this case as they are less than 1% of the signal amplitudes.

**Simulation Conclusion**

The delta-connected secondary side enables the system voltage to float during the fault, which allows for continued operation of the converter. The DC side resistance is effectively halved during the fault, as such, the current command $i_d$ must be increased to maintain the commanded DC voltage, but the system performs well and remains stable throughout. This scenario shows that the response of the system to a ground fault at the positive DC terminal of the converter is very similar between both models, confirming the accuracy of the implemented model, even under large disturbances.

### 5.3 Conclusion

As the five test scenarios show, the lumped modelling technique used in the real-time simulator accurately represents the behaviour of the MMC. The comparison of the simulation results performed using the full model including all the necessary switches and capacitors, to the lumped modelling approach, where the resistance and capacitor voltage values of the individual modules are grouped into a single resistor and controlled voltage source per arm shows that both systems react almost identically to changes in command references as well as during fault scenarios.

When discrepancies are noticed, it is usually only for the circulating currents and can be attributed to discrepancies in reaction time between the models. In all cases, the discrepancies are of very high frequency, have a short duration and have little to no effect on the currents and voltages in the system.

This chapter has confirmed that the selected modelling technique for the MMC yields appropriate results. Because simulating a converter including 400 modules per arm using PSCAD, while considering all the switches and capacitors would be impractical, the converter considered for this comparison had 12 modules per arm. The next chapter will update the lumped model used to include 400 modules per arm, and compare the results of off-line simulations performed using PSCAD to simulations performed using the real-time simulator and the MMC model implemented on the FPGA.
Chapter 6

Validation of the Real-Time Simulation Model based on comparisons with Off-line Simulation Model

The lumped modelling technique used in the real-time FPGA implementation was tested in chapter 5 and shown to yield equivalent results in PSCAD simulations to a model considering all switches and capacitors of the MMC. Due to the impracticality of simulating a converter containing hundreds of modules per arm, the converter used for the comparison only contained 12. As presented in chapter 4 however, the system implemented on the real-time simulator will be based on the future France-Spain HVDC link system, which contains 400 modules. These 400 modules will allow for 401 different output levels (0 to $N$ modules inserted in each arm).

In this chapter, the lumped model implemented in PSCAD for the comparisons performed in chapter 5 is modified to contain 400 modules per arm. Simulations are performed to compare the response of this larger system, as implemented in PSCAD, to the real-time implementation on the FPGA, and thus confirm the correct operation of the converter in the real-time MMC simulation system.

6.1 Study System

As in the previous chapter, the study system is a simple system with an ideal AC voltage source as well as a transformer on the AC side and a fixed impedance on the DC side. As such, it is possible to evaluate solely the performance for the MMC itself and the control system’s reaction to changes in command references or faults. In this chapter, the converter contains 400 modules instead of the 12 modules simulated previously. The system used for simulation is shown in Figure 6.1 and the major details are outlined in Table 6.1.

This system follows the specifications of the HVDC link which will later be used as a case-study for a complete HVDC link. The DC side resistances have been selected to match the rated power of 1000MW at the rated voltage of ±320kV.
Chapter 6. Validation of the Real-Time Simulation Model based on comparisons with Off-line Simulation Model

Figure 6.1: One line diagram of the 401 levels converter used for comparison between Real-Time and PSCAD model simulations

6.1.1 Implementation

The PSCAD implementation was created simply by expanding the 12 modules model used previously to 400 modules. The control implementation remains unchanged, with the voltage sorting and module selection simply extended to accommodate the larger number of modules. Because the dynamics of the system are different, control gains have been modified as well.

The real-time simulator includes one FPGA where the converter model is implemented and RTDS, simulating the AC and DC systems as well as the controls, which are implemented locally for this test. This is done to prevent additional delays and noise issues arising from adding an additional piece of hardware in the system. As the goal of these simulations is to validate the real-time model implementation with the PSCAD off-line model, this added source of delays and errors would only make comparisons more difficult. The electrical system is implemented in the small-time step module of RTDS and the controls in the regular 50 µs time step. This may cause some discrepancies as the controls are not updated as often compared to PSCAD where they are updated at every time step, but should nevertheless be sufficient to compare both models.

The converter models used for the simulation are the same in both systems, but because of differences between the implementation, it is expected that the results may not match as closely as they did in the previous chapter. The implementation in the real-time simulation brings potential issues with voltage balancing, especially module voltage sorting and selection, which will not be completed at every time-step as is the case in PSCAD. Additionally, delays and other latency limitations may affect the real-time system and are not present in the PSCAD model.

It is also worth noting that is it very difficult to perfectly synchronize the timing of the changes in real-time. Whereas in PSCAD, fault and reference change instants can be perfectly timed, this is a much more complex task in a real-time platform. As such, the events were first simulated in real-time, then reproduced as closely as possible by adjusting the phase of the voltage source in the PSCAD scenario. It is nevertheless possible that timing of the events be slightly offset, which could create discrepancies between the results of the simulations.
Chapter 6. Validation of the Real-Time Simulation Model based on comparisons with Off-line Simulation Model

Table 6.1: Specification of the converter used for comparison between Real-Time and PSCAD model simulations

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC Source Voltage (L-L, rms) (V&lt;sub&gt;AC&lt;/sub&gt;)</td>
<td>400 kv</td>
</tr>
<tr>
<td>AC Source Frequency</td>
<td>60 Hz</td>
</tr>
<tr>
<td>AC System Resistance</td>
<td>0.1 Ω</td>
</tr>
<tr>
<td>AC System Inductance</td>
<td>0.1 mH</td>
</tr>
<tr>
<td>Transformer Windings</td>
<td>Y&lt;sub&gt;g&lt;/sub&gt; / ∆</td>
</tr>
<tr>
<td>Transformer Ratio(L-L, RMS)</td>
<td>400 / 333 kV</td>
</tr>
<tr>
<td>Transformer Rating</td>
<td>1059 MVA</td>
</tr>
<tr>
<td>Transformer Impedance</td>
<td>18%</td>
</tr>
<tr>
<td>Number of Modules per Arm (N)</td>
<td>400</td>
</tr>
<tr>
<td>Module Capacitor Value (C&lt;sub&gt;module&lt;/sub&gt;)</td>
<td>12.5 mF</td>
</tr>
<tr>
<td>Expected Capacitor Voltage (V&lt;sub&gt;module&lt;/sub&gt;)</td>
<td>1.6 kV</td>
</tr>
<tr>
<td>Arm Inductor (I&lt;sub&gt;arm&lt;/sub&gt;)</td>
<td>50 mH</td>
</tr>
<tr>
<td>DC Voltage (V&lt;sub&gt;DC&lt;/sub&gt;)</td>
<td>± 320 kV</td>
</tr>
<tr>
<td>DC Rated Power (P&lt;sub&gt;DC&lt;/sub&gt;)</td>
<td>1000 MW</td>
</tr>
<tr>
<td>Total DC Side Resistance (R&lt;sub&gt;DC&lt;/sub&gt;)</td>
<td>400 Ω</td>
</tr>
<tr>
<td>Switches ON Resistance (R&lt;sub&gt;ON&lt;/sub&gt;)</td>
<td>0.001 Ω</td>
</tr>
<tr>
<td>Switches OFF Resistance (R&lt;sub&gt;OFF&lt;/sub&gt;)</td>
<td>1 MΩ</td>
</tr>
</tbody>
</table>

**Controller Gain**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current Proportional Gain</td>
<td>0.5</td>
</tr>
<tr>
<td>Current Integral Time Constant</td>
<td>0.05s</td>
</tr>
<tr>
<td>Current Cross Terms Gain</td>
<td>0.2</td>
</tr>
<tr>
<td>Voltage Proportional Gain</td>
<td>4</td>
</tr>
<tr>
<td>Voltage Integral Time Constant</td>
<td>0.005s</td>
</tr>
<tr>
<td>Circulating Current Proportional Gain</td>
<td>0.65</td>
</tr>
<tr>
<td>Circulating Current Integral Time Constant</td>
<td>0.025s</td>
</tr>
<tr>
<td>Circulating Current Cross Terms Gain</td>
<td>0.2</td>
</tr>
</tbody>
</table>

6.2 Test Scenarios

The test scenarios selected are the same as in the previous chapter; chosen here again to represent a range of operation of the converter.

1. Activation of the circulating current controller
2. Reactive current command change from 0.5 pu to -0.5 pu
3. DC voltage reference command change from 0.9 pu to 1.1 pu
4. Single phase line to ground fault at the point of AC connection, on the secondary side of the transformer
5. DC side fault to ground

The parameters compared during the simulations are also the same:

1. Capacitor voltages
2. Arm currents
3. Circulating currents
4. AC currents in \( dq \)-frame
5. Positive and Negative MMC DC terminal voltage with respect to ground (only for scenarios 4 and 5)

Here again, the positive and negative DC terminal voltages (measured with respect to ground) are shown during the fault scenarios only as they do provide additional information in these specific cases.

### 6.2.1 Circulating current controls activation

Table 6.2: Information for the simulation of circulating current control activation, comparing the 401 levels implementations between PSCAD and FPGA

<table>
<thead>
<tr>
<th>Disturbance Instant</th>
<th>Reference Commands</th>
<th>Activation of the Circulating Current Controller</th>
</tr>
</thead>
<tbody>
<tr>
<td>Before Disturbance</td>
<td>0 pu</td>
<td>OFF</td>
</tr>
<tr>
<td>After Disturbance</td>
<td>1 pu</td>
<td>ON</td>
</tr>
</tbody>
</table>

The first simulation considers the activation of the circulating current controller, which is originally disabled, and is activated at \( t = 1 \) sec. The activation of the controller minimizes the contribution of the circulating currents on the overall arm currents, which will affect capacitor voltage fluctuations. The reference current and DC voltage remain fixed during the test. Important simulation parameters are shown in Table 6.2. The simulation results are shown in Figure 6.2.

**Simulation Results**

Both platforms produce very similar results in this scenario. Both models match very well in steady-state and during the transient, with the arm and circulating currents showing limited differences during the transient.

From sub-plots a and b, the individual capacitor voltages track well. The difference is limited to noise level, well below 0.05 pu, and may easily be attributed to the selection algorithm which may not insert and bypass modules at the exact same instants in both models, or to imperfect sorting in real-time. The results do show that the voltage balancing technique implementation in the FPGA model works well. As expected the reduction in arm currents after the circulating current controller is activated decreases the fluctuations on the capacitor voltages.
There is some discrepancy in the arm currents between the models. Although it is hard to notice from sub-plot c which superposes both traces, sub-plot d clearly shows a difference exists. Sub-plot d’s scaling does exacerbate the differences, but they are there nonetheless. This is most likely due to the delays in the real-time system which uses the arm inductors to decouple the solution between the FPGA and the RTDS. This introduces a short but non-zero delay. As the arm currents change quickly, this is enough to create differences between the simulation results. The differences are very consistent both before and after the change however, as such, they do not constitute an issue when comparing the models. Also noticeable on in sub-plot c are the effects of the circulating currents on the arm currents, where additional ripples are clearly noticeable before the controller is activated.

The circulating currents match both before and after the activation of the controls, as highlighted in sub-plots e and f. Little to no discrepancy is visible throughout. Some short disturbances are visible
during the transient, but are limited in amplitude and time. Also of note, the circulating current controller performs much better when using this high number of levels compared to the 12 module converter of chapter 5. As mentioned previously, the circulating current controller regulates the amplitude of the total inserted voltage in a leg by inserting or bypassing additional module as required. In this case, each capacitor has a voltage of $\frac{1}{400}$ of $V_{DC}$. As such inserting additional modules in this converter has a much smaller effect on the total inserted voltage in the leg, and the controller can much more precisely adjust the voltage output, allowing for better control of the circulating currents, which are reduced to almost 0, without generating noticeable high frequency noise.

As sub-plot g shows, the activation of the circulating current controller has almost no effect on the AC side currents, which is as expected. The same can be said of the DC voltage, which is left almost undisturbed by the activation of the controller, except for a very minor fluctuation at the time of activation which is quickly settled, as highlighted in sub-plot i.

Simulation Conclusion

This first test scenario shows that, for both models, the circulating currents control has the expected effects. The activation of the controller limits the amplitude of the circulating currents effectively, and provides very good results, with the circulating currents attenuated to almost 0. The simulation results for both implementations are very similar, with discrepancies mostly notable in the arm currents and likely due to simulation delays in the real-time system as they are very consistent both before and after the transient.

6.2.2 Change in reactive current command

Table 6.3: Information for the simulation of a step change in reactive current command, comparing the 401 levels implementations between PSCAD and the FPGA

<table>
<thead>
<tr>
<th>Disturbance</th>
<th>Step change in reactive current ($i_q$) reference from 0.5 pu to -0.5 pu</th>
</tr>
</thead>
<tbody>
<tr>
<td>Disturbance Instant</td>
<td>1 sec</td>
</tr>
<tr>
<td>Reference Commands</td>
<td>Before Disturbance</td>
</tr>
<tr>
<td>Reactive Current Reference</td>
<td>0.5 pu</td>
</tr>
<tr>
<td>DC Voltage Reference</td>
<td>1 pu</td>
</tr>
<tr>
<td>Circulating Current Control</td>
<td>ON</td>
</tr>
</tbody>
</table>

In this second test scenario, the reactive current changes instantly from 0.5 pu to -0.5 pu at $t = 1$ sec, while the DC voltage reference remains unchanged at 1 pu and the circulating current controller is activated throughout. Important simulation parameters are shown in Table 6.3, and the result of the simulation is shown in Figure 6.3.

Simulation Results

In this scenario, both models produce equivalent results both in steady-state and during the transient. The only noticeable difference is in the AC current $i_d$, which, as will be seen below, can most likely be attributed to an angle difference of the PLL between both platforms.
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As can be seen from sub-plot a, the change in reactive current reference affects capacitor voltages, as different AC currents flow through the converter before and after the change. There is a short transient after the reference change, but the system settles quickly afterwards.

In this case again, with the adjusted scales, sub-plot d shows that the arm currents differ between both systems although again, it is very hard to distinguish by looking only at sub-plot c. Again, these discrepancies can be explained by delays in the real-time system.

The circulating currents also match very well between the models, with only minor differences detected during the transient, as shown in sub-plots e and f. The controls react well, with only fluctuations of small magnitude which settle within 50ms.

Sub-plot g confirms that the reactive current reference change was performed as expected. The reactive current $i_q$ quickly settles at the new reference with very limited oscillations. This change also
has an effect on the real current $i_d$, which shows a noticeable reaction during the transient. This shows that the $d$ and $q$ components are not perfectly decoupled. However, the response is the same in both system, and as such, does not present a problem in the comparison of the responses.

Here, the current $i_d$ has a small offset both before and after the change, as shown in sub-plot h. However, both system match very well during the transient and their response is very similar. This difference is not noticeable in the internal converter signals (module voltages, arm and circulating currents), as such it seems that this is not due to a modelling difference, and can most likely attributed to an offset in the PLL angle between the 2 systems, as the PLL is updated every 50µs in the RTDS platform, compared to 2.5µs in PSCAD. This represents a potential difference of almost 0.02 radians in the angle, which can explain the differences noted here. The $i_q$ signal is controlled directly to the reference value, so it is forced back to the commanded value, whereas the $i_d$ signal indirectly controls the DC voltage, as such, if the angle is different, the system corrects for $i_q$, but not $i_d$, as the DC voltage is still at the reference value. Offsets such as this are not noticeable in the other scenarios as $i_q$ is controlled to 0, as a small offset in angle would not greatly affect $i_d$.

The transient noticed on $i_d$ is reflected on the DC voltage, as shown in sub-plot i. The disturbances in the voltage closely follow the ones in the real current $i_d$ as expected.

**Simulation Conclusion**

This second scenario shows that the response of the system to a change in reactive current reference is almost identical between the two systems. The change in the reactive current command affects the arm currents and capacitor voltages as expected, and the system settles quickly after the command change. A short transient in $i_d$ and $V_{DC}$ after the reactive current reference change shows that the real and reactive components of the system are not perfectly decoupled by the controller, however this does not represent a problem for the comparison of the system responses which are very similar.

Additional delays present in the FPGA real-time system creates discrepancies in the arm and circulating currents, but all are of small magnitude and consistent before and after the change. The results also shows a small offset in current $i_d$ both before and after the reference change, but as the converter internal currents and voltages track well, this is most likely due to a discrepancy located outside of the converter model, likely the transformer or PLL. Despite this offset, the models can still be considered to be equivalent representations of the MMC.

### 6.2.3 Change in DC voltage reference

Table 6.4: Information for the simulation of a step change in DC Voltage command, comparing the 401 levels implementations between PSCAD and FPGA

<table>
<thead>
<tr>
<th>Disturbance</th>
<th>Step change in DC voltage reference from 0.9 pu to 1.1 pu</th>
</tr>
</thead>
<tbody>
<tr>
<td>Disturbance Instant</td>
<td>1 sec</td>
</tr>
<tr>
<td>Reference Commands</td>
<td></td>
</tr>
<tr>
<td>Reactive Current Reference</td>
<td>Before Disturbance</td>
</tr>
<tr>
<td>DC Voltage Reference</td>
<td>0 pu</td>
</tr>
<tr>
<td>Circulating Current Control</td>
<td>0.9 pu</td>
</tr>
<tr>
<td></td>
<td>ON</td>
</tr>
</tbody>
</table>
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The third test scenario involves a change in the DC voltage reference command. In this scenario, the reactive current command is set at 0 pu, while the DC voltage reference steps from 0.9 to 1.1 pu at $t = 1$ sec. For this test, the circulating current controller is activated throughout. Important simulation parameters are shown in Table 6.4, and results of the simulation in Figure 6.4.

![Simulation and difference results for different variables](image)

**Figure 6.4:** Comparison between simulation results for PSCAD and FPGA implementations of a 401 levels MMC converter for a step change in DC Voltage command

**Simulation Results**

Here again, the models produce very similar results, with only very short lived discrepancies noticeable in the AC currents at beginning of the transient.

Sub-plots a and b show that the capacitor voltages are almost identical between the systems both in steady-state and during the transient. One can notice that the envelope of the difference is slightly larger after the change, but this is simply related to the larger fluctuations, which is expected as the
increased power transfer also creates larger arm currents.

As in the previous scenarios, the arm currents are not perfectly matched (sub-plot d) although they do match well when superimposed on the same plot (sub-plot c), this again can be attributed to internal delays or offsets on the real-time system, and are not a cause for concern. In this case as well, as the reaction during the change is almost identical.

The circulating currents match well between the 2 cases, as shown in sub-plots e and f. The reference change creates fluctuations of limited amplitude which settle within 75ms.

The AC currents sub-plot (g) shows that the decoupling of the two signals ($i_d$ and $i_q$) is not perfect here again, but this fact does not represent a problem as both system behave similarly. Short spikes in the difference between the signals can be noticed in sub-plot h, likely due to a slight time shift in the activation of the controls. However, the results do match very well in this test.

Sub-plot i shows that the DC voltage control performs nicely and the system settles at the new operating point in 100ms with limited overshoot.

Simulation Conclusion

This scenario shows that the response of the system to a change in DC voltage reference is very similar between the two models of the systems. Any discrepancy can be attributed to additional delays and imperfect timing in the triggering of the change between both models, but the left side plots showing the results of both simulations superimposed highlight the fact that the two systems match almost perfectly. The DC control performs well, settling at the new commanded voltage quickly, and with very limited overshoot.

6.2.4 Single Phase Fault at the point of AC connection

Table 6.5: Information for the simulation of a 100ms single phase-to-ground AC fault at the converter, comparing the 401 levels implementations between PSCAD and FPGA

<table>
<thead>
<tr>
<th>Disturbance Instant</th>
<th>100m single phase-to-ground on phase A at the point of AC connection of the converter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Disturbance</td>
<td>1 sec</td>
</tr>
<tr>
<td>Reference Commands</td>
<td>Before Disturbance After Disturbance</td>
</tr>
<tr>
<td>Reactive Current Reference</td>
<td>0 pu</td>
</tr>
<tr>
<td>DC Voltage Reference</td>
<td>1 pu</td>
</tr>
<tr>
<td>Circulating Current Control</td>
<td>ON</td>
</tr>
</tbody>
</table>

The next test scenario considers a 100ms line-to-ground fault, applied on phase A directly at the point of connection of the AC system with the converter. The reactive current and DC voltage command references are fixed throughout at 0 pu and 1 pu respectively and the circulating current controls are active. Important simulation parameters are shown in Table 6.5, and results of the simulation in Figure 6.5.
Simulation Results

As noted in the previous chapter, when the fault is triggered, the point of common connection of the converter at phase A is stuck to ground. However, as the secondary side of the transformer is an ungrounded delta, the converter is still able to maintain the DC voltage at the expected value by drawing more power from the other 2 phases. Large imbalances are created however as the current flow through leg A in particular is affected by the fault, as such, circulating currents appear to counteract the imbalances between the different leg capacitor voltages.

The results as a general match very well between the cases, with the AC side currents the only major source of discrepancy between the result of the simulations.

Sub-plot a shows, upon triggering of the fault, the voltages suddenly drop, but settle at a lower operating point where the system reaches a new steady-state, maintaining operation through the fault,
and return to their original values after the fault clears. Voltage fluctuations are reduced during the fault as the arm current is also lower.

The upper arm current of phase A, shown in sub-plot c is also reduced during the fault, as there is no more current input from the AC system, but circulating currents provide voltage support for the leg modules. Here again, both simulated models yield similar results as shown in sub-plot d, with the discrepancies being attributable to additional delays in the real-time system. A DC offset in the arm current is noticeable during the fault, compared to the pre-fault current, which agrees with the fact that power is transferred from the other converter legs to support voltage in leg A.

As shown in sub-plot e, and as was the case in the similar test performed in the previous chapter, the circulating currents in this case are first harmonic, instead of the expected second, as the fault only directly affects phase A. The DC offset in the circulating current represents the re-distribution of the power between the legs. As the circulating current controller is designed to minimize second harmonic currents, these first harmonic currents are not neutralized and are allowed to flow. Both simulated models produce almost identical results here as well despite the imbalance.

Sub-plot g shows that both AC current components ($i_d$ and $i_q$) match very well throughout. There is a short spike at the instant the fault clears, most likely caused by a slight offset in the timing of the fault clearing between the two models.

Sub-plot i shows that the DC voltage is well supported even during the fault, as current still flow through the converter. The voltage barely deviates from the target of 1 pu and has almost returned to the reference value by the time the fault clears, which causes a small rise in voltage, as power is now flowing again through phase A, which settles back nicely.

Sub-plot k shows the effect of the fault on the DC terminal voltages. The relative difference between the terminals remains consistent during the fault, as shown in sub-plot g, but the voltages when measured with respect to the ground reference do show large fluctuations. This is due to the fact that the mid-point voltage of phase A is fixed by the fault to ground. As modules are inserted and bypassed in each arm, the voltage at the DC terminals is directly affected. Both models do track well during the fault.

**Simulation Conclusion**

The delta-connected secondary side allows the system to maintain voltage support on the AC side during the fault, allowing for continued power transfer through the converter. The AC current from phase A, which sinks to ground at the fault point, is replaced partially internally by sizeable circulating currents, supporting the voltage of the capacitors of leg A and allowing for continued operation through the fault.

The system performs well and remains stable throughout. This scenario shows that the response of the system to a an asymmetrical phase-to-ground fault on phase A at the point of connection of the converter to the AC system is very similar between both simulation platforms, confirming the accuracy of the real-time simulation model, even when large imbalances are present in the AC system.

### 6.2.5 DC fault

This last simulation considers a 100ms fault to ground directly at the positive terminal of the DC bus which will generate even larger perturbations in arm currents and module voltages then the previous test, although symmetrically to all three phases. The reactive current and DC voltage command references are fixed throughout at 0 pu and 1 pu respectively and the circulating current controls are active.
Table 6.6: Information for the simulation of a 100ms phase-to-ground fault at the positive DC terminal, comparing the 401 levels implementations between PSCAD and FPGA

<table>
<thead>
<tr>
<th>Disturbance</th>
<th>100m phase-to-ground fault at the positive terminal of the DC bus</th>
</tr>
</thead>
<tbody>
<tr>
<td>Disturbance Instant</td>
<td>1 sec</td>
</tr>
<tr>
<td>Reference Commands</td>
<td>Before Disturbance</td>
</tr>
<tr>
<td>Reactive Current Reference</td>
<td>0 pu</td>
</tr>
<tr>
<td>DC Voltage Reference</td>
<td>1 pu</td>
</tr>
<tr>
<td>Circulating Current Control</td>
<td>ON</td>
</tr>
</tbody>
</table>

Simulation parameters are shown in Table 6.6, and results of the simulation in Figure 6.6.

Figure 6.6: Comparison between simulation results for PSCAD and FPGA implementations of a 100ms phase-to-ground fault at the positive DC terminal
Chapter 6. Validation of the Real-Time Simulation Model based on comparisons with Off-line Simulation Model

Simulation Results

As in the previous chapter, when the fault is triggered, the positive side of the DC bus is immediately fixed to 0V. As the transformer secondary is delta-connected and not grounded, phase-to-phase voltage is maintained on the secondary side and the negative DC terminal which previously supported a voltage of -320 kV now supports twice that amount. The arm currents increase during the fault as the DC side resistance is effectively halved as the positive side resistance grounded at both ends.

The figure shows that the models match very well in this scenario. With short transients at the fault triggering and clearing instants, due to imperfect synchronization of the triggering instant between the platforms. Other than the fluctuations of the arm currents, attributed to delays in the real-time system, the models match very well even in this extreme case.

Sub-plot a shows that, upon triggering of the fault, the voltages suddenly drop, but the system quickly reacts by increasing power transfer to the converter and the voltages are inching back towards the pre-fault value by the time the fault clears. The higher currents cause larger voltage fluctuations during the fault, but the system remains stable. The voltages quickly return to their original value after the fault clears.

Sub-plot c shows an arm current increase during the fault, which is explained by the reduced DC side resistance. The discrepancies observed in sub-plot d can be attributed to delays in the real-time system and imperfect timing in the triggering of the fault event.

The circulating current controller is active throughout this simulation and, as the fault is symmetrical on all three phases, manages to ride through the fault without problems. Short lived disturbances are noticeable at the triggering and clearing instants, but both simulations produced equivalent results.

From sub-plot g, the flow of real current $i_d$ increases during the fault, as expected as total DC side resistance is halved thus additional power must be transferred to maintain the desired voltage level. The plot also shows that the reactive current control performs well and maintains the current $i_q$ at the desired 0 pu throughout, with small fluctuations at the fault triggering and clearing instants.

Sub-plot i shows that the DC voltage is well supported even during the fault. After an initial drop as the fault is triggered, the voltage inches back towards 1 pu as the current control increases the $i_d$ command. Once the fault clears, the voltage peaks as the power transfer is now much higher, but quickly settles back to 1 pu as the controller adjusts the command. Sharp spikes in voltage are seen in both simulations, and the discrepancy between the 2 results as noticed in sub-plot j is due to imperfect timing of the fault in the 2 simulations. The overall results nevertheless track very well.

Sub-plot k shows the DC terminal voltages measured with respect to the ground reference. As expected, the positive terminal voltage is stuck to ground during the fault, which causes the voltage at the negative terminal to double to -640 kV. Both simulations perform almost identically during the fault.

Simulation Conclusion

The delta-connected secondary side enables the system to maintain voltage support on the DC bus throughout the fault. Current does sink at the fault location, as such, the current command $i_d$ is increased to maintain the commanded DC voltage, but the system performs well and remains stable throughout. This would most likely cause issues with voltage insulation in a physical system, and would require additional measures to limit this effect, but are not a problem in this case as the goal is simply
to compare the simulation results. This scenario shows that the response to a ground fault at the positive DC terminal of the converter is very similar between both systems, confirming the accuracy of the real-time system implementation, even under large disturbances.

6.3 Conclusion

This chapter confirmed that the results of simulations performed using PSCAD match extremely well with those of simulations performed using the real-time simulator implementation. For all five cases recorded, all noticeable discrepancies were largely attributable to delays in the real-time system that are not present in the PSCAD simulations or imperfect timing of the triggering instants. The only noteworthy differences between the results are for the AC currents component, which have shown a small offset in the reactive current control case, which is different but stable both before and after the change. As the AC currents are measured outside the converter, and all the internal converter measurements match, the source is likely outside the converter model itself, with the most probable source being a phase shift on the angle output of the PLL due to limitations of the execution speed of the PLL controls in the real-time system. In all other cases, the results of simulations match very well between the off-line and real-time models.

Despite the potential issues with modelling discrepancies, delays and noise, the results of the simulations performed in this chapter match extremely well between off-line and real-time. The system implemented in the real-time platform was kept simple, with no HIL included to prevent the introduction of additional sources of error, and the results show that the implementation of the MMC model in the FPGA performs very well.

Now that the correct operation of the implemented model has been verified, it can be placed in a larger HVDC link system and it is now possible to perform HIL simulations, which will be the focus of the next chapter.
Chapter 7

Performance Evaluation of
MMC-based Two-Terminal HVDC
using HIL

The model as implemented in the FPGA platform as part of the real-time simulator has been shown in the previous chapter to yield equivalent simulation results to off-line simulations performed in PSCAD. The simulations performed were of a simple system and did not include any hardware in the loop testing. This was done to allow for as direct a comparison as possible between both systems.

Once it has been shown that the models are equivalent it is now possible to perform HIL testing using the real-time simulator. It is also possible to use multiple FPGA boards to simulate a more complex HVDC system.

This chapter shows simulation results of an HVDC link implemented in the real-time simulation platform. The system also includes hardware in the loop testing, as one of the MMC controllers is implemented on a cRIO platform form national instruments.

7.1 System Description

The study system in this case is modelled on the France-Spain HVDC link presented in [16] and introduced in chapter 4. A one line diagram of the system is shown in figure 7.1 and the main parameters are outlined in Table 7.1.

The system is a HVDC link where both converters are connected to ideal AC systems, consisting of an ideal source and a transformer. The link between both converters is a 70km cable. The cable construction was not described in the reference, as such a standard xPLE configuration from ABB was used. The cable is also as described in CIGRE DC Grid Test system. The parameters of the cable are available in appendix A.

As can be noticed form the table, the internal current controller had to be tuned down slightly for the HIL controller, as the additional delay and noise generated oscillation in the system under certain conditions. The oscillations were limited in size and the system remained stable, nevertheless, the controls we relaxed to prevent their apparition.
Figure 7.1: One line diagram of the HVDC system used for simulations

Table 7.1: Specification of the converter used for simulations

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC Source Voltage (L-L, rms) ($V_{AC}$)</td>
<td>400 kv</td>
</tr>
<tr>
<td>AC Source Frequency</td>
<td>60 Hz</td>
</tr>
<tr>
<td>AC System Resistance</td>
<td>0.1 Ω</td>
</tr>
<tr>
<td>AC System Inductance</td>
<td>0.1 mH</td>
</tr>
<tr>
<td>Transformer Windings</td>
<td>$Y_g / \Delta$</td>
</tr>
<tr>
<td>Transformer Ratio (L-L, RMS)</td>
<td>400 / 333 kV</td>
</tr>
<tr>
<td>Transformer Rating</td>
<td>1059 MVA</td>
</tr>
<tr>
<td>Transformer Impedance</td>
<td>18%</td>
</tr>
<tr>
<td>Number of Modules per Arm ($N$)</td>
<td>400</td>
</tr>
<tr>
<td>Module Capacitor Value ($C_{module}$)</td>
<td>12.5 mF</td>
</tr>
<tr>
<td>Expected Capacitor Voltage ($V_{module}$)</td>
<td>1.6 kV</td>
</tr>
<tr>
<td>Arm Inductor ($I_{arm}$)</td>
<td>50 mH</td>
</tr>
<tr>
<td>DC Voltage ($V_{DC}$)</td>
<td>$\pm$ 320 kV</td>
</tr>
<tr>
<td>DC Rated Power ($P_{DC}$)</td>
<td>1000 MW</td>
</tr>
<tr>
<td>Switches ON Resistance ($R_{ON}$)</td>
<td>0.001 Ω</td>
</tr>
<tr>
<td>Switches OFF Resistance ($R_{OFF}$)</td>
<td>1 MΩ</td>
</tr>
<tr>
<td><strong>Controller Gain</strong></td>
<td></td>
</tr>
<tr>
<td>Current Proportional Gain</td>
<td>0.5, (0.3 HIL)</td>
</tr>
<tr>
<td>Current Integral Time Constant</td>
<td>0.05s</td>
</tr>
<tr>
<td>Current Cross Terms Gain</td>
<td>0.09</td>
</tr>
<tr>
<td>Voltage Proportional Gain</td>
<td>4</td>
</tr>
<tr>
<td>Voltage Integral Time Constant</td>
<td>0.005s</td>
</tr>
<tr>
<td>Circulating Current Proportional Gain</td>
<td>0.65</td>
</tr>
<tr>
<td>Circulating Current Integral Time Constant</td>
<td>0.025s</td>
</tr>
<tr>
<td>Circulating Current Cross Terms Gain</td>
<td>0.18</td>
</tr>
</tbody>
</table>

7.1.1 Implementation

The system implementation takes advantage of the hardware-in-the-loop capability of the real-time simulation platform, as one of the MMC controllers is implemented on a separate National Instrument
cRIO controller. The second MMC controller implementation remains on the RTDS system. Both controllers could be implemented on separate cRIOS, the limitation at this point being the number of available analog outputs of the RTDS simulator.

Nevertheless one external controller is enough to show the capability of the system to perform hardware-in-the-loop testing. The two converters are implemented on separate FPGA boards. The interface between the different devices is as described in chapter 4.

The controller implemented on the cRIO (MMC-1) controls reactive power and regulates the DC voltage of the system. The controller implemented on the RTDS simulator (MMC-2) controls reactive power as well as real power transfer through the link. A diagram of the implementation is shown in figure 7.2. Pictures of the system setup are available in appendix E.

![Figure 7.2: Block diagram of the system implementation including hardware in the loop](image)

### 7.2 Test Scenarios

The test scenarios were selected to highlight the stability and performance of the model under various conditions.

1. Activation of the circulating current on the HIL converter (MMC-1)
2. Reactive current command step change from -0.5 pu to 0.5 pu at MMC-2
3. Reactive current command step change from -0.5 pu to 0.5 pu at MMC-1
4. Real power transfer reversal, change from -0.8 pu to 0.8 pu at MMC-2
5. DC voltage reference command step change from 0.9 pu to 1.1 pu at MMC-1
6. Single phase line to ground fault at the point of AC connection, on the secondary side of the transformer at MMC-1
7. Single phase line to ground fault at the point of AC connection, on the secondary side of the transformer at MMC-2

8. DC side fault to ground at the positive DC terminal of MMC-1

The scenarios were selected, as in the previous two chapters, to represent a large array of operating conditions of the converter, and more unusual fault scenarios.

The first scenario here again represents a simple starting test to ensure that the circulating current controller of the HIL platform is implemented and performs correctly and that the overall system is stable during the activation.

The second and third scenarios represent changes in reactive power commands at either end of the HVDC link. These change should be affect only one side of the converter, as the reactive power is not transferred through the DC link. Nevertheless, potentially imperfect decoupling of the \(d\) and \(q\) components could create transient changes in the real power transfer or DC voltage that would propagate to the other end of the DC link. These test thus represent a good starting point to test the stability of the system and the performance of the HIL controller.

The next two cases (four and five) represent tests for the voltage controller of the system. In the first, the power transfer direction is reversed and the voltage controller must adjust to maintain the DC voltage. In the second the DC voltage reference in changed directly. The DC voltage control is implemented on the HIL cRIO platform. As such, additional delays are present in the system which make control more difficult. These two scenarios thus represent good tests of the effectiveness of the controls, and of the stability of the system as a whole.

Next comes the more unusual fault scenarios (6 and 7) where a single phase AC phase-to-ground fault is applied at each end of the converter. This tests the ability of the system to sustain operation through more extreme events, also testing the response to the same scenario at either end of the link, where one end controls power transfer and the other DC voltage and allowing for a comparisons of the system reaction in both cases.

Finally, the last test simulated a DC fault to ground at the positive terminal of MMC-1. As this controller is implemented on the cRIO platform, this scenarios tests the effectiveness of the controller despite the additional delays introduced by the communication between the 2 hardware devices.

These 8 scenarios will provide a good overview of the stability of the system and the quality of the controls.

The parameters tracked during the simulations are:

1. Capacitor voltages
2. DC Voltage
3. Circulating Currents
4. Arm currents
5. AC currents in \(dq\)-frame

These parameters should provide a good representation of the operation of the system in the different scenarios, with internal parameters (capacitor voltages, circulating currents and arm currents) providing an overview of the operation of the converters themselves and the external parameters (AC currents...
Chapter 7. Performance Evaluation of MMC-based Two-Terminal HVDC using HIL

and DC voltage) providing details on the operation of the controls. All parameters are tracked at both converters.

7.2.1 Circulating currents controls activation

Table 7.2: Information for the simulation of the activation of the circulating current controller in MMC-1 of the 401 levels HVDC link implementation in the real-time simulation platform

<table>
<thead>
<tr>
<th>Disturbance</th>
<th>Activation of the circulating current controller in both converters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Disturbance Instant</td>
<td>0.61 sec</td>
</tr>
<tr>
<td>MMC-1</td>
<td>Before Disturbance</td>
</tr>
<tr>
<td>Reactive Current Reference</td>
<td>0 pu</td>
</tr>
<tr>
<td>DC Voltage Reference</td>
<td>1 pu</td>
</tr>
<tr>
<td>Circulating Current Control</td>
<td>OFF</td>
</tr>
<tr>
<td>MMC-2</td>
<td>Before Disturbance</td>
</tr>
<tr>
<td>Reactive Current Reference</td>
<td>0 pu</td>
</tr>
<tr>
<td>Power Transfer Reference</td>
<td>0.8 pu</td>
</tr>
<tr>
<td>Circulating Current Control</td>
<td>ON</td>
</tr>
</tbody>
</table>

The first simulation case simply tests the activation of the circulating current controls at MMC-1. This determines if the added delay and potential noise issues associated with the handling the controls on the external cRIO have a significant effect on the quality of the controls. The reactive power reference is set to 0 pu at both terminals, the DC voltage reference to 1 pu at MMC-1 and the real power transfer to 0.8 pu at MMC-2 (power flowing from MMC-2 to MMC-1). Simulation parameters are shown in Table 7.2 and the results are shown in figure 7.3.

This test should create limited disturbances on the system as a whole, with the arm and circulating currents, as well as module voltage fluctuations at MMC-1 the only values expected to experience a noticeable change. As the circulating currents have no effect outside the converter, it is not expected that any other signal should be perturbed by the event.

As shown in the figure, the system remains stable after the activation of the circulating current controllers. As expected, the activation of the controllers had no notable effect on the external currents and voltages.

The controller performed as expected, removing the circulating currents almost instantly, with no noticeable difference in performance between the HIL controller of MMC-1 and tests performed in the previous chapter where the controller was implemented on RTDS. As expected the reduction in the circulating currents causes a reduction in arm currents, which also became cleaner sinusoidal signals after the activation of the controls, which in turn reduced the amplitude of the oscillations of the module voltages. One can also notice the offset in DC voltages at either end of the DC link, in matching the defined direction of the power flow from MMC-2 to MMC-1.
7.2.2 Reactive current command change at MMC-2

The second scenario studied involves a step change in the reactive power command at MMC-2. The reactive power control affects only one AC system, and as such, the opposite side of the link should be unaffected by the change in reference. The test is performed first at MMC-2 as its controller is implemented locally on RTDS and does not suffer from potential issues such as communication delays and noise as the MMC-1 controller does.

The test is a change in reference from -0.5 to 0.5 pu at MMC-2 with the DC voltage reference set to 1.0 pu at MMC-1 and the real power transfer set to 0.8 pu at MMC-2 (power flowing from MMC-2 to MMC-1). The results are shown in figure 7.4 and important simulation parameters in Table 7.3.

As the results show, the system can quite easily handle such a change in the reactive power reference.
Table 7.3: Information for the simulation of a change in the reactive power reference from -0.5 to 0.5 pu at MMC-2 of the 401 levels HVDC link implementation in the real-time simulation platform

<table>
<thead>
<tr>
<th>Disturbance</th>
<th>Change in reference reactive power at MMC-2 from -0.5 to 0.5 pu.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Disturbance Instant</td>
<td>0.2 sec</td>
</tr>
<tr>
<td>MMC-1</td>
<td>Before Disturbance</td>
</tr>
<tr>
<td></td>
<td>After Disturbance</td>
</tr>
<tr>
<td>Reactive Current Reference</td>
<td>0 pu</td>
</tr>
<tr>
<td>DC Voltage Reference</td>
<td>1 pu</td>
</tr>
<tr>
<td>Circulating Current Control</td>
<td>ON</td>
</tr>
<tr>
<td>MMC-2</td>
<td>Before Disturbance</td>
</tr>
<tr>
<td></td>
<td>After Disturbance</td>
</tr>
<tr>
<td>Reactive Current Reference</td>
<td>-0.5 pu</td>
</tr>
<tr>
<td>Power Transfer Reference</td>
<td>0.8 pu</td>
</tr>
<tr>
<td>Circulating Current Control</td>
<td>ON</td>
</tr>
</tbody>
</table>

at MMC-2. The reactive power level is adjusted almost instantly and the system settles very nicely at the new operating point. As can be seen, the change in the reactive command also causes a short perturbation on the real component of the current, showing good, but imperfect decoupling of the two components. This increase has a minor effect on the DC voltage which exhibits small oscillations for approximately 50ms after the reference change. These oscillations propagate to the opposite end of the DC cable, although they are much smaller in magnitude. Other than these fluctuations, the currents and voltages of MMC-1 remain unaffected by the change as expected.

As can be seen, after the short transient caused by the reference change, the tracked values at MMC-1 are restored to their pre-event levels and operation continues almost unaffected. The measured signals at MMC-2 also quickly return to steady-state, although it can be noticed that, as expected, the phase of the arm currents is different. This is most easily noticeable by looking at the capacitor voltage fluctuations which are different in the new steady-state.

### 7.2.3 Reactive current command change at MMC-1

This scenario also involves the same change in reactive power setpoint as the previous one, but this time at MMC-1. The reaction of the system could differ here from the previous scenario as the controller for MMC-1 is implemented in the cRIO instead of locally on RTDS itself. The added delays and noise could influence the response of the system. Also, MMC-1 is tasked with controlling the DC voltage of the system whereas MMC-2 controls the real power transfer, which could affect the response.

As in the previous scenario, the reactive command change is not expected to create large disturbances at MMC-2. The imperfect decoupling of the real and reactive component should, however, cause some disturbances on the DC voltage, which may perturb the controls at that end of the HVDC link. The results are shown in figure 7.5 and simulation parameters in Table 7.4.

As the results show, and as expected, the change in reactive power command at MMC-1 did not create large disturbances on the system. The circulating currents at MMC-1 are the only one of the measured signals showing a clear reaction to the reference change, but they do settle back quickly and are only of small amplitude even at their maximum. The reference change is executed quickly, and with
Figure 7.4: Simulation results of the 401 levels HVDC link implementation in the real-time simulation platform for a change in the reactive power reference from -0.5 to 0.5 pu at MMC-2 (left side plots show MMC-1, right side MMC-2)

little overshoot.

Comparing the results with the previous case, where the change was implemented at MMC-2, one can notice that the overshoot in the response is slightly larger here, which may be due to the more relaxed controller gains, and possibly to delays in the controls. Nevertheless, the system settles back nicely and quickly. The phase shift in the arm currents of MMC-1 is noticeable in this case as well, especially when considering the module individual voltage fluctuations.

The perturbations introduced at MMC-1 are also noticed at MMC-2, however they are very small at that point and barely require a reaction by the controller of MMC-2. A small fluctuation is noticeable on the DC voltage as well as the $d$ component of the AC current, but these are noticeably smaller than oscillations at MMC-1 in the previous case. This is most likely due to the fact that the reference change is performed at the converter responsible for DC voltage control. The control can thus react quickly to
Table 7.4: Information for the simulation of a change in the reactive power reference from -0.5 to 0.5 pu at MMC-1 of the 401 levels HVDC link implementation in the real-time simulation platform

<table>
<thead>
<tr>
<th>Disturbance</th>
<th>Change in reference reactive power at MMC-1 from -0.5 to 0.5 pu.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Disturbance Instant</td>
<td>0.2 sec</td>
</tr>
<tr>
<td><strong>MMC-1</strong></td>
<td>Before Disturbance</td>
</tr>
<tr>
<td>Reactive Current Reference</td>
<td>-0.5 pu</td>
</tr>
<tr>
<td>DC Voltage Reference</td>
<td>1 pu</td>
</tr>
<tr>
<td>Circulating Current Control</td>
<td>ON</td>
</tr>
<tr>
<td><strong>MMC-2</strong></td>
<td>Before Disturbance</td>
</tr>
<tr>
<td>Reactive Current Reference</td>
<td>0 pu</td>
</tr>
<tr>
<td>Power Transfer Reference</td>
<td>0.8 pu</td>
</tr>
<tr>
<td>Circulating Current Control</td>
<td>ON</td>
</tr>
</tbody>
</table>

The change triggered by the transient and keep the DC voltage closer to the desired value, instead of reacting to the change only after it propagates from MMC-2 as was the case in the previous scenario. This immediacy of the reaction limits the fluctuations on the DC cable and minimizes the required response at the opposite end of the link.

### 7.2.4 Power transfer reversal

Table 7.5: Information for the simulation of a reversal in the power transfer of the 401 levels HVDC link implementation in the real-time simulation platform

<table>
<thead>
<tr>
<th>Disturbance</th>
<th>Reversal of the power transfer for -0.8 pu (flowing from MMC-1 to MMC-2) to 0.8 pu (flowing from MMC-2 to MMC-1), ramped over 25ms</th>
</tr>
</thead>
<tbody>
<tr>
<td>Disturbance Instant</td>
<td>0.2 sec</td>
</tr>
<tr>
<td><strong>MMC-1</strong></td>
<td>Before Disturbance</td>
</tr>
<tr>
<td>Reactive Current Reference</td>
<td>0 pu</td>
</tr>
<tr>
<td>DC Voltage Reference</td>
<td>1 pu</td>
</tr>
<tr>
<td>Circulating Current Control</td>
<td>ON</td>
</tr>
<tr>
<td><strong>MMC-2</strong></td>
<td>Before Disturbance</td>
</tr>
<tr>
<td>Reactive Current Reference</td>
<td>0 pu</td>
</tr>
<tr>
<td>Power Transfer Reference</td>
<td>-0.8 pu</td>
</tr>
<tr>
<td>Circulating Current Control</td>
<td>ON</td>
</tr>
</tbody>
</table>

Once it is shown that the system can handle simple reactive power reference changes well, the next step involves a more difficult case where power transfer direction is changed. The power transfer reference is controlled at MMC-2 and is changed from -0.8 pu (flowing from MMC-1 to MMC-2) to 0.8 pu (flowing from MMC-2 to MMC-1). This change is applied as a ramp over 25ms. The reactive power references
are set to 0 pu at both terminals and the DC voltage reference to 1 pu at MMC-1.

This case will test both the real power and DC voltage controllers. The real power transfer reversal will affect the DC voltage levels, and the voltage controller implemented at MMC-1 will have to react to maintain it at the desired value. Given the magnitude and speed of the change, it is expected that the DC voltage will experience sizeable fluctuations as a result of the reference change. All of the measured signals should be affected during by the change. Important simulation parameters are shown in Table 7.5 and simulation results in figure 7.6.

As the figure shows, MMC-2 tracks the commanded reference well, with only some oscillations noticeable as the system settles at the new operating point. The controller fully settles within 100ms of the end of the reference change (125ms after the start of the change). The $i_{q}$ component of the AC current is not strongly affected by the change, showing good decoupling of the signals, and settles nicely.
could be expected, circulating currents of limited amplitude are noticeable during the reference change, but are again nicely controlled. As the voltage level at MMC-1 is fixed by the controller, it increases at MMC-2 in order to reverse power transfer direction. This is reflected in the capacitor voltage of the modules which stabilize at a higher level than before the change. It can also be noticed that the DC component of the arm currents has changed from positive to negative, also reflecting the change in direction of the power flow.

At the other end of the link, the change in the power reference causes an initial increase in the DC voltage. The voltage controller thus adjust the real power contribution to maintain the voltage as desired. This is a slower, reactionary process in this case, and as such, the signals take slightly longer to settle on this side. However, the transition remains smooth and clean. Here again, small circulating currents are noticeable during the transition, but settle quickly afterwards. As the DC voltage value

Figure 7.6: Simulation results of the 401 levels HVDC link implementation in the real-time simulation platform for a reversal in power transfer (left side plots show MMC-1, right side MMC-2)
is fixed by the controller at this end of the link, the capacitor voltages are less affected by the change, although it is clear that the signal is different after the change, because of the change in the arm currents, which now have a different DC offset, due to the change in power flow direction. Overall, the system reacts as expected and settles nicely in response to this commanded reversal in real power transfer.

### 7.2.5 DC voltage reference change

Table 7.6: Information for the simulation of a change in DC voltage reference form 0.9 to 1.1 pu of the 401 levels HVDC link implementation in the real-time simulation platform

<table>
<thead>
<tr>
<th>Disturbance</th>
<th>Change of the DC voltage command form 0.9 to 1.1 pu</th>
</tr>
</thead>
<tbody>
<tr>
<td>Disturbance Instant</td>
<td>0.2 sec</td>
</tr>
<tr>
<td>MMC-1</td>
<td></td>
</tr>
<tr>
<td>Reactive Current Reference</td>
<td>0 pu</td>
</tr>
<tr>
<td>DC Voltage Reference</td>
<td>0.9 pu 1.1 pu</td>
</tr>
<tr>
<td>Circulating Current Control</td>
<td>ON</td>
</tr>
<tr>
<td>MMC-2</td>
<td></td>
</tr>
<tr>
<td>Reactive Current Reference</td>
<td>0 pu</td>
</tr>
<tr>
<td>Power Transfer Reference</td>
<td>0.8 pu 0.8 pu</td>
</tr>
<tr>
<td>Circulating Current Control</td>
<td>ON</td>
</tr>
</tbody>
</table>

While MMC-2 controls the real power transfer, MMC-1 controls the DC voltage level. This fifth scenario tests the response of this control to a step change in DC voltage reference from 0.9 to 1.1 pu. The real power transfer reference is set to 0.8 pu (power flowing from MMC-2 to MMC-1) and reactive power reference set to 0 pu at both terminals.

This scenario test the DC voltage controls by directly applying a command change, contrary to a change in power transfer forcing the control to stabilize the voltage as was the case in the previous scenario. In this case, the real power transfer controls of MMC-2 will react to the change. The results are shown in figure 7.7 and simulations parameters in Table 7.6.

As can be seen from the figure the system reacts well to the change in voltage reference. Upon triggering of the change, the power flow at MMC-1 reverses almost immediately, allowing for a fast rise in the capacitor voltages. The DC voltage overshoots by approximately 30% and settles back in 150ms, which is in line with the time that was required to settle in the power transfer reversal case.

The capacitor voltages settle to a higher average voltage as expected, and the amplitude of the fluctuations are not greatly affected as one would expect as the amount of power transferred has not changed. It may have been reasonable to expect smaller fluctuations as the voltage increase at a fixed power also signifies a lower current, but the fluctuations in the capacitor voltages are caused by the AC portion of the current as well as the circulating currents. The circulating currents are controlled to be almost 0 and the AC currents have not changed as the commanded current setpoints are fixed in this scenario.

As expected, the DC voltage change was reflected almost identically in MMC-2, but this change had a limited effect on the AC side currents and power, with a drop to approximately 0.5 pu returning to
Figure 7.7: Simulation results of the 401 levels HVDC link implementation in the real-time simulation platform for change in DC voltage reference from 0.9 to 1.1 pu (left side plots show MMC-1, right side MMC-2)

the target of 0.8 pu in less than 100ms, highlighting the suitability of the controls in this situation. In this case again, for both converters, the imperfect decoupling of $i_d$ and $i_q$ along with the rapid change in the DC voltage also create transient fluctuations on the $i_q$ component of the AC currents which quickly disappear once the system settles.

7.2.6 AC Fault at MMC-1

The next scenario considers a more unusual scenario, where a single phase-to-ground fault is applied at the point of connection of MMC-1 with the AC system. As in the previous chapters, the secondary side of the transformer is not grounded. As such, the line-to-line voltage levels will not be affected by the fault, although the line-to-neutral voltages will fluctuate. The current flow will be affected, as current
Table 7.7: Information for the simulation of a single phase-to-ground fault at the point of connection of MMC-1 of the 401 levels HVDC link implementation in the real-time simulation platform

<table>
<thead>
<tr>
<th>Disturbance</th>
<th>Single 200ms phase-to-ground fault on phase A at the point of connection of MMC-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Disturbance Instant</td>
<td>0.2 sec</td>
</tr>
<tr>
<td>MMC-1</td>
<td>Before Disturbance</td>
</tr>
<tr>
<td>Reactive Current Reference</td>
<td>0 pu</td>
</tr>
<tr>
<td>DC Voltage Reference</td>
<td>1 pu</td>
</tr>
<tr>
<td>Circulating Current Control</td>
<td>ON</td>
</tr>
<tr>
<td>MMC-2</td>
<td>Before Disturbance</td>
</tr>
<tr>
<td>Reactive Current Reference</td>
<td>0 pu</td>
</tr>
<tr>
<td>Power Transfer Reference</td>
<td>0.8 pu</td>
</tr>
<tr>
<td>Circulating Current Control</td>
<td>ON</td>
</tr>
</tbody>
</table>

will no longer flow to the converter through phase A. It is expected that circulating currents will allow for transfer of power between legs B and C back to leg A in order to correct the voltage imbalance created by the fault, as was the case in the previous tests. What is less clear however, is how well the voltage control will perform during the fault. In this case, it is implemented on the cRIO controller, which introduces delays and noise, potentially limiting its effectiveness. The presence transmission cable and the second converter also may affect the results.

For this scenario, the reactive power commands have been fixed to 0 pu at both ends of the HVDC link. The voltage reference at MMC-1 is set to 1 pu and the power transfer command to 0.8 pu (flow from MMC-2 to MMC-1). The circulating current controller is active throughout the simulation. Information about the test scenario is available in Table 7.7 and simulation results are shown in figure 7.8.

As the figure shows, the system continues operation through the fault and returns to pre-fault currents and voltages very quickly once the fault clears. During the fault, the oscillations are much larger than what was seen in a similar case in chapter 6. This can be explained by the fact that the DC side is not simply a resistive load as was the case previously, but the DC voltage is also affected by MMC-2 and the current flow into MMC-1 from the DC side.

This contribution affects the system during the fault as current will naturally flow to the fault point. As in the previous chapters, circulating currents at 60Hz appear during the fault to compensate for the imbalance and are not limited by the controller which focuses on the usual 120Hz frequency. Sub-plot k also shows that large oscillations are present on the DC line, varying with the number of inserted modules on each side of the fault point, whose voltage level is no longer allowed to fluctuate. This contributes to large currents through the upper arm of leg A and in turn, to large oscillations of the module voltages, which are also noticeable on the DC voltage and AC currents.

The large currents on the DC cable also cause voltage fluctuations at the opposite end of the link, although attenuated in magnitude. These are small and of higher frequency, and as such, do not have a large impact on the signals measured at that end. The oscillations do transfer back to the AC side, as changes in DC voltage affect the voltage at the AC connection point, and with it, the power transferred, but the magnitude of the oscillations is limited and contained. The reactive current ($i_q$) remain almost unaffected. These oscillations also affect the arm currents, which exhibit different frequency contents.
during the fault, with limited impact on the amplitude as the average DC voltage remains unchanged. These changes in arm currents have little noticeable effect on the module voltages.

The controller as implemented is sufficient to ride through the fault and recover correctly. However, the large currents and harmonics displayed during the event may cause many problems in a real-world system. More investigations on additional controls and protection schemes may be required to improve the response of the system in this scenario.

### 7.2.7 AC Fault at MMC-2

A similar fault was simulated at the at the other terminal, to determine if the location of the fault would have an effect on the system reaction. Here, the affected controller controls the power transfer instead
Table 7.8: Information for the simulation of a single phase-to-ground fault at the point of connection of MMC-2 of the 401 levels HVDC link implementation in the real-time simulation platform

<table>
<thead>
<tr>
<th>Disturbance</th>
<th>Single 200ms phase-to-ground fault on phase A at the point of connection of MMC-2</th>
<th>Disturbance Instant</th>
<th>0.2 sec</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>MMC-1</td>
<td></td>
</tr>
<tr>
<td>Reactive Current Reference</td>
<td></td>
<td>Before Disturbance</td>
<td>0 pu</td>
</tr>
<tr>
<td>DC Voltage Reference</td>
<td></td>
<td>After Disturbance</td>
<td>0 pu</td>
</tr>
<tr>
<td>Circulating Current Control</td>
<td></td>
<td></td>
<td>ON</td>
</tr>
<tr>
<td>MMC-2</td>
<td></td>
<td>Before Disturbance</td>
<td>0 pu</td>
</tr>
<tr>
<td>Reactive Current Reference</td>
<td></td>
<td>After Disturbance</td>
<td>0 pu</td>
</tr>
<tr>
<td>Power Transfer Reference</td>
<td></td>
<td></td>
<td>0.8 pu</td>
</tr>
<tr>
<td>Circulating Current Control</td>
<td></td>
<td></td>
<td>ON</td>
</tr>
</tbody>
</table>

of the DC voltage, which may also affect the system’s reaction. The control parameters have been left as in the previous test scenario, and are shown in Table 7.8. The simulation results are shown in figure 7.9.

As can be seen from the figure, the system reaction to the fault at MMC-2 is similar to the previous case where the fault was located at MMC-1. Where the converter near the fault point displays large, but stable fluctuations during the fault, which settle quickly once the fault clears. Here again, full line-to-line voltage is available on the secondary side of the transformer during the fault as the connection is ungrounded. Large 60Hz circulating currents and current fluctuations on the DC line are generated during the fault, and help maintain the voltage level through leg A of the converter. As in the previous case, the arm currents and module voltages of phase A display major fluctuations caused by the fact that the voltage at the point of AC connection is now fixed by the fault and thus cannot fluctuate.

Here again, the large currents on the DC cable cause higher frequency fluctuations of limited amplitude on the DC voltage at MMC-1, which have noticeable effects on the AC side currents as they are too fast for the controllers to properly attenuate. Some perturbation are also noticeable on the arm currents and capacitor voltages, although both remain stable during the event. The circulating currents at the converter do remain well controlled throughout.

In this case again, the controller keeps the system stable during the fault and recovers quickly, but the large currents and harmonics may not be sustainable for a physical system and more work on the controller or protection system to handle situations like this is likely necessary.

7.2.8 DC fault

The last simulation performed tests the system’s response to a fault on the DC bus, located at the positive terminal of MMC-1. This fault will affect the DC voltage and all 3 legs simultaneously. As was the case in the previous chapters, because of the absence of a ground connection on the secondary side of the transformer, it is expected that the voltage will be allowed to float and that the negative DC bus will support the full -640 kV during the fault. As such, other than the transient at the instant of the fault itself, it is expected that the system will ride through the fault well, without major disturbance.
As can be seen from the figure, and as expected, the system reacts well to the fault, and the DC terminals voltage levels are allowed to float such that, other than a short transient at the moment of the fault, the system remains largely unaffected by the fault. The DC terminal voltage at the positive terminal of MMC-1 is stuck at ground during the fault and the negative terminal voltage with respect to the ground reference drops to -640 kV as a result. Large current oscillation are noticeable during the change, due to the temporary imbalance between the terminal voltages at either end of the line.

A very interesting note is that there is no noticeable transient at the moment of the fault clearing at 0.4 sec. This is due to the fact that the system does not force back the DC voltages back to the pre-fault levels or ±320 kV. Rather, they remain at 0 and -640 kV as during the fault, as shown in sub-plot l. This is again due to the lack of a ground reference. The system was implemented as in reference [16].
Table 7.9: Information for the simulation of a single ground fault at the positive DC terminal of MMC-1 of the 401 levels HVDC link implementation in the real-time simulation platform

<table>
<thead>
<tr>
<th>Disturbance Instant</th>
<th>Single ground fault at the positive DC terminal of MMC-1</th>
</tr>
</thead>
<tbody>
<tr>
<td>MMC-1</td>
<td>Before Disturbance</td>
</tr>
<tr>
<td>Reactive Current Reference</td>
<td>0 pu</td>
</tr>
<tr>
<td>DC Voltage Reference</td>
<td>1 pu</td>
</tr>
<tr>
<td>Circulating Current Control</td>
<td>ON</td>
</tr>
<tr>
<td>MMC-2</td>
<td>Before Disturbance</td>
</tr>
<tr>
<td>Reactive Current Reference</td>
<td>0 pu</td>
</tr>
<tr>
<td>Power Transfer Reference</td>
<td>0.8 pu</td>
</tr>
<tr>
<td>Circulating Current Control</td>
<td>ON</td>
</tr>
</tbody>
</table>

However, there is likely a capacitance or resistance to ground in the system which is not simulated, and would force the voltages back to their pre-fault levels in the real-world system.

This simulation shows that the system can ride through a DC fault as implemented, but obviously, the system implementation will require improvements to more closely represent a real-world scenario. The controller, as implemented does perform correctly however, as the DC voltage is maintained during and after the fault.

7.3 Conclusions

The results above show that the system controls are stable and can correctly apply reference changes of real and reactive power as well as DC voltage reference. The simulated cases also show that the system can ride through different fault scenarios, reacting as expected and quickly restoring the system to the target values once the fault clears. However, large and potentially damaging currents and voltages are generated during the fault event and control or protection improvements may be necessary in physical systems.

No major discrepancies can be noted between the reaction of the MMCs whether the controller is implemented in a separate cRIO platform or directly in the RTDS system, confirming the correct design of the system for HIL testing.

The real-time simulation platform has thus shown its ability to simulate a HVDC link including two separate 401-level converters, in real-time and using HIL. Should more FPGA boards, cRIO controllers and analog outputs for the RTDS made available, the system can thus be expanded to simulate a more complex DC grid as required and thus enable testing or more and more complex systems and controllers.
Figure 7.10: Simulation results of the 401 levels HVDC link implementation in the real-time simulation platform for a single ground fault at the positive DC terminal of MMC-1 (left side plots show MMC-1, right side MMC-2 (unless otherwise specified))
Chapter 8

Conclusions

8.1 Summary

In this thesis, a modelling approach developed in [18] was used to successfully develop a modular multi-level converter (MMC) model suitable for real-time simulation.

The thesis covered the principles of operation and modelling of the MMC, by describing the structure of a single module and interconnecting several modules to form the three-phase converter system of interest. MMC specific control requirements were also covered: modules need to be appropriately inserted and bypassed to balance capacitor voltages and circulating currents should be controlled to a minimum. The sorting and selection approach was covered. Standard control techniques were presented and discussed, which led to the selection of Nearest Level Control (NLC) as the most suitable for this implementation. The implementation of the system on the real-time platform as well as the modelling technique used were described. The division of the simulated system components between the three hardware devices (FPGA, RTDS and cRIO) as well as the interconnection between them were presented. The implementation of the control loops based on the system equations was also covered.

The implemented model was then tested in PSCAD simulations showing that the modelling approach used in the real-time platform implementation yields similar results to a model considering all individual switches and modules. The results of PSCAD simulations where then compared to the results of simulations performed using the developed real-time simulator and shown to match, confirming the correct implementation of the model in the real-time simulator.

Finally, a HVDC link system, based on the configuration and specifications of the France-Spain HVDC interconnection currently under construction, was implemented using 2 FPGA boards and including hardware in the loop control. Different simulation scenarios have shown that the system reacts as expected to changes in command reference and disturbances. The results also highlight the HIL simulation capability of the real-time simulator and show that the system reacts well and remains stable under various situations.

8.2 Conclusions

This thesis has demonstrated the implementation of a model of the MMC on an FPGA device, allowing for connection with a real-time simulator as well as external controllers (in this case a NI cRIO controller).
for hardware in the loop simulation. An algorithm has been implemented to control not only real and reactive power through the converter, but also limit circulating currents through the converter itself.

The lumped model implemented, based on the time-varying Thevenin equivalent, produces simulation results almost identical to simulations performed using a model considering all individual switches and capacitors of a complete MMC model in PSCAD simulations. The PSCAD simulation results were compared to the results of simulations performed using the real-time simulation platform developed and shown to match within a few percent in all the studied cases, with any discrepancy easily attributable to additional delays or imperfect sorting in the real-time system.

It was also demonstrated that it is possible to use multiple FPGA boards to simulate multiple MMC converters, which can be connected to the RTDS system to create a HVDC link, and could eventually be expanded to create a DC grid, with the main limitation being the hardware availability. The developed FPGA platform thus represents a viable option to perform more complex DC grid simulations and hardware in the loop testing for systems including one or multiple MMC converters.

The simulations performed in chapter seven for the HVDC link have shown that the system is implemented properly and accurately responds to change in controls reference points, settling fast to new target references, with limited overshoot. It did show that the implemented system and controls allow for the apparition of very large currents, as well as for large voltage when measured with respect to ground during fault scenarios. These could cause problems in physical systems. As such, improvements to the control method or protection scheme would likely be necessary. The simulations performed nevertheless show that the controls as implemented perform well for more standard command reference changes scenarios and maintain stability during the fault events.

The configuration of the MMC, highlighted by the distribution of the energy storage capacitors in the converter arms provides multiple advantages over traditional VSC systems. However, this same configuration causes additional control and simulation difficulties. The real-time simulator system implemented in this thesis allows for hardware in the loop testing which can ensure correct implementation of controls before they are applied to a real-world system and help improve understanding of the behaviour of the system. As such, the simulation platform represents a very useful tool for MMC testing, especially under transient conditions, and can help in the design of better controls for this promising new converter configuration.

8.3 Contributions

This thesis has shown the implementation of a MMC model in an FPGA platform which allow for real-time and HIL simulation of single, or multi-converter systems.

The contributions of this work can be summarized as follows.

1. The implementation of the MMC model in an FPGA platform, which can be connected to a RTDS system and implemented as part of a larger electrical system for real-time simulation. This model is contained in a single FPGA board, and multiple boards can be connected to the RTDS system to perform simulations of an HVDC link, or eventually a more complex DC grid.

2. The implementation of the selection and sorting algorithms on the FPGA so that the converter model can be completely self-contained and only require arm currents a required number of inserted modules from the controller to produce the inserted voltages in each arm.
3. Implementation of MMC controls, including circulating currents, in a third party controller (cRIO) and connection to the real-time simulation system to perform hardware in the loop testing.

### 8.4 Future Work

The system as implemented represents a strong starting point for investigation of the transient response of the MMC in real-time and HIL testing. The following is suggested in continuation of the work performed in this thesis.

- Investigation of potential uses of the circulating currents to help re-balance the leg voltages during asymmetric faults.
- Implementation of a module swapping technique based on distance from arm average voltage.
- Study of the response of the system under different conditions based on different sorting, insertion and bypass speeds.
- Implementation of the communications between RTDS and the cRIO using digital communications to reduce noise and improve performance.
- Implementation of the converter model in the NI PXI platform, which offers more flexibility and size for FPGA controls, potentially improving communication between the MMC model and the HIL controller.
- Implementation of bypass switches for modules and development of control strategies to mitigate the effects of faults.
- Implementation and testing of a standby/spare module control strategy.
- Deployment of multiple converters as part of a more complex DC grid to be used for supervisory controls testing and advanced fault analysis.

#### 8.4.1 Investigation of potential uses of circulating currents control

The circulating current controls as implemented aim to keep the circulating currents as close to 0 as possible, which is ideal in steady-state. In the case or an asymmetric fault however, should the fault cause one of the legs module voltages to drop with respect to the others, circulating currents would inherently help re-balance them. If the circulating currents are forced to 0 with controls, they are not available as a mean to re-balance the capacitor voltages. In theory, it would be possible to control the circulating currents in order to help re-balance the voltages faster as the fault clears.

As was also seen in some simulated cases, in the case of some asymmetrical faults, the circulating currents are not of the expected 2nd harmonic and, as such, are not limited by the controller. The usefulness and complexity of implementing improved controls also limiting these first harmonic components could be investigated.
8.4.2 Implementation of a module swapping technique based on distance from arm average voltage

As implemented, in addition to the insertion and bypass of modules required to produce the expected output voltage, modules are swapped in and out of the arm on regular time intervals to help improve the voltage distribution between the different modules of a arm. This provides an even distribution of the voltages between the different modules, but it is probable that this technique requires more switchings than is strictly required. A more efficient technique may compare individual voltages of the modules with the arm average and insert and bypassed modules based on a predefined distance from the average, thus only swapping modules as necessary instead of based on a simple time interval.

8.4.3 Study of the system response for different sorting, insertion and bypass speeds

The system as implemented effectively distributes the voltages between the different modules of each arm. But would the system perform as well if the sorting of the module voltages was performed half as fast? Slowing down the module sorting and selection would free up resources on the FPGA to implement more complex selection methods, or simply larger MMCs, but it is important to ensure that they do not degrade the performance of the system.

The same can be said of the inserting and bypassing of modules. The system as implemented performs well, but would it perform evenly well if modules were inserted or bypassed less often? This is an interesting question as fewer switching instants limits the switching losses, and thus help improve the efficiency of the converter, but may deteriorate the quality of the voltage distribution. The trade-off between different speeds and implementations could be studied using this system.

8.4.4 Implementation of digital communications between cRIO and RTDS

The communications between RTDS and the external cRIO are handled over analog interfaces. The obvious problems with analog signals are present however, as noise and offsets limit the effectiveness of the controls. This problem forced a modification in the communications between the devices, requiring the commands from the cRIO to RTDS to be send in the dq frame instead of the regular abc frame and moving the implementation of the reverse dq transformation back to the RTDS instead of the cRIO, in order to alleviate problems related to noise and analog offsets. It may be possible to develop a digital interface that would eliminate these problems and allow for the complete controller to be implemented as intended: on the external hardware.

8.4.5 Implementation of the converter model in the NI PXI platform

The cRIO series of controller, used as an external controller in this simulator, has an internal FPGA which could potentially be used to implement the FPGA converter model. Unfortunately, the FPGA boards integrated in the controls are not large enough to contain the 400 modules per arm converter model and required selection algorithm. The National Instrument PXI controller platform allows for more flexibility for FPGA implementation by integrating larger FPGA boards and has the capability of inserting multiple board in a single chassis.
As such, the PXI platform offers the possibility of integrating the MMC model directly on these FPGA boards and simplify the communication between the model and the external controller, which could be implemented directly on the PXI platform. However, this would require however an efficient method of communication between the PXI controller and the RTDS system due to the much larger number of signals to be transferred (not only do the controller signals need to be transferred, but also the signals coming from the converter model). As such, the number of available analog signals could quickly become insufficient and communications over a fibre optic interface would represent a much more desirable method.

As of now, there are no defined way of communicating between the RTDS and PXI controller, but discussions have been started with NI to define what would be required to make this possible. It is conceivable that a solution would be available in the near future, at which point, implementing the converter model on the PXI controller would greatly simplify the implementation of the real-time simulator.

8.4.6 Implementation of bypass switches for modules and development of control strategies

As the simulations have shown very large currents and voltages are present in the converter, during fault events. These voltages and currents could potentially cause problems in physical systems. In the literature, there is often a mention of bypass switches used to protect the IGBTs and capacitors from large currents during fault incidents. These have not been implemented in this system, but adding these to the model would allow for the study of potential bypassing strategies to mitigate the effects of these currents during a fault. Additional control strategies could also be developed to mitigate the effects of the faults on the system.

8.4.7 Implementation and testing of a standby/spare module control strategy

One of the interesting features of the MMC resides in its ability to operate even when some modules are experiencing problems. If a module is malfunctioning, it can simply be bypassed and the converter operation can continue with one less level. This also leads to the possibility of including a few spare modules in a converter arm, which can be used in the case of such a failure. Specific controls would be required to allow for the seamless activation of these modules in the converter arm.

8.4.8 Deployment of multiple converters as part of a more complex DC grid

The system implemented thus far included only two converters, which is sufficient to test controls for simple systems. There is a clear trend however, towards developing controls for more complex DC grids which, on top of individual converter controls, require overarching system controllers, especially in the case of faults or other unusual events. The simulator as developed here is not limited to a simple 2 converter HVDC link and more converters could be added simply by adding more FPGA boards in order to implement more converters.

It would also be possible to implement a combination of MMC converters and conventional VSC converters in a DC grid and study it as a system in order to understand the interactions and limitations.
of the different types of converters. These regular VSCs, as they are much simpler to simulate due to their limited number of elements, could be implemented directly on RTDS and would not require any additional hardware assuming the RTDS system used is powerful enough to handle the required number of converters.
References


References

Appendices
Appendix A

Transmission Cable Parameters

Table A.1: Specification of the cable used for HVDC system simulations

<table>
<thead>
<tr>
<th>Data Source</th>
<th>ABB XLPE Submarine</th>
</tr>
</thead>
<tbody>
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<td>$D_{core}(mm)$</td>
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</tr>
<tr>
<td>$\rho_{core}(\Omega m)$</td>
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<tr>
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</tr>
<tr>
<td>$tan\psi_1$</td>
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</tr>
<tr>
<td>$R_{in}(mm)$</td>
<td>47.95</td>
</tr>
<tr>
<td>$R_{ext}(mm)$</td>
<td>51.05</td>
</tr>
<tr>
<td>$\rho_{sh}(\Omega m)$</td>
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</tr>
<tr>
<td>$\epsilon_r$</td>
<td>2.3</td>
</tr>
<tr>
<td>$tan\psi_2$</td>
<td>0.001</td>
</tr>
<tr>
<td>$R'_{in}(mm)$</td>
<td>55.05</td>
</tr>
<tr>
<td>$R'_{ext}(mm)$</td>
<td>60.55</td>
</tr>
<tr>
<td>$\rho'_{arm}(\Omega m)$</td>
<td>$13.8 \times 10^{-8}$</td>
</tr>
<tr>
<td>$\epsilon_r$</td>
<td>2.3</td>
</tr>
<tr>
<td>$tan\psi_3$</td>
<td>0.001</td>
</tr>
<tr>
<td>$S_{cable}(mm)$</td>
<td>135.1</td>
</tr>
<tr>
<td>Depth (m)</td>
<td>1.5</td>
</tr>
<tr>
<td>Distance between cables (m)</td>
<td>0.5</td>
</tr>
<tr>
<td>DC Resistance ($\Omega/km$)</td>
<td>$1.853 \times 10^{-2}$</td>
</tr>
<tr>
<td>Capacitance ($\mu F/km$)</td>
<td>0.16</td>
</tr>
<tr>
<td>Inductance ($\mu H/km$)</td>
<td>1.35</td>
</tr>
<tr>
<td>Rated Current (A)</td>
<td>$\pm 1290$</td>
</tr>
</tbody>
</table>
Figure A.1: Cross section of the DC cable showing the parameters position
Appendix B

Capacitor and Inductor Selection

B.1 Capacitor Value Selection

Selection of the capacitors is a trade-off between capacitor size (and price) and acceptable voltage ripple. As the equations developed earlier in chapters 2 & 3 show, the currents in the upper and lower arms have a DC component, a 1\textsuperscript{st} harmonic component corresponding to the output current to the AC system and a 2\textsuperscript{nd} harmonic component corresponding to the circulating currents. These currents, based on their direction and size, will generate voltage ripples on the module capacitors. These will occur during normal operation and cannot be completely eliminated.

In this thesis, the capacitor value has been selected to match the system of [16], where the selected value is based on the total energy stored in the converter, which affects the voltage ripple on the capacitors. The target stored energy storage level is selected to be 30-40 kJ/MVA which was taken from a document presented by ABB [20]. This value range should translate in to a voltage ripple of approximately 10%. Obviously, the energy here is not stored in a single capacitor as it would in conventional VSCs, so the selection method must be adapted to compensate for this fact.

Higher capacitance values will reduce the ripples, but will increase the physical size of the capacitors, modules and total installation as well as the overall cost of the converter. Larger capacitors will also slow down the response of the system for voltage regulation of the DC bus. As such, capacitors are ideally chosen to be as small as possible while keeping the ripples in an acceptable range.

B.1.1 Capacitor selection based on energy storage

The energy stored in a capacitor is:

\[ E = \frac{1}{2} CV^2 \]  \hspace{1cm} (B.1)

It is possible to determine the required individual capacitor value by replacing the total energy level desired, based on the selected value of 30 to 40 kJ/MVA, in the equation. The individual capacitor values can be selected simply by adding the energy stored in all the capacitors and dividing by the nominal capacity of the converter. After isolating the capacitor value from the equation above, one obtains:

\[ C = \frac{2 \times \frac{S \times E_{MMC}}{6 \times N_{arm} \times V_C^2}}{\text{ }} \]  \hspace{1cm} (B.2)
Appendix B. Capacitor and Inductor Selection

Where:
- $S$ is the nominal capacity of the converter (MVA)
- $E_{MMC}$ is the selected value of energy stored per MVA (30 to 40 kJ/MVA)
- $N_{arm}$ is the number of capacitors per arm
- $V_C$ is the voltage stored in each module

B.1.2 Technique verification

Since no other capacitor selection technique has been found to be described in the literature, some double checking is necessary to ensure the method yields acceptable results. The method is being described in documents published by ABB which gives it credibility, but a good way to test the method is to compare its results with values used in simulations and experiments published. The results are shown in Table B.1 below, assuming stored energy of 40 kJ/MVA.

Table B.1: Comparisons of capacitor value selection found in literature with capacitor selection method result (assuming stored energy of 40 kJ/MVA)

<table>
<thead>
<tr>
<th>Ref.</th>
<th>MMC Rating (MVA)</th>
<th>DC Voltage (kV)</th>
<th># Modules (per arm)</th>
<th>Cap. Used (mF)</th>
<th>Cap. Calc. (mF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[1] (Matlab)</td>
<td>0.03</td>
<td>2</td>
<td>4</td>
<td>1</td>
<td>0.4</td>
</tr>
<tr>
<td>[1] (Experiment)</td>
<td>0.0002</td>
<td>0.2</td>
<td>4</td>
<td>1</td>
<td>0.267</td>
</tr>
<tr>
<td>[2] (PSIM)</td>
<td>0.0176</td>
<td>0.8</td>
<td>4</td>
<td>5</td>
<td>1.467</td>
</tr>
<tr>
<td>[3] (PSCAD)</td>
<td>1</td>
<td>9</td>
<td>4</td>
<td>1.9</td>
<td>0.658</td>
</tr>
<tr>
<td>[4] (Simulation)</td>
<td>15</td>
<td>28.5</td>
<td>11</td>
<td>1.3</td>
<td>2.709</td>
</tr>
<tr>
<td>[5] (Simulation)</td>
<td>6.24</td>
<td>8.825</td>
<td>10</td>
<td>3</td>
<td>10.683</td>
</tr>
<tr>
<td>[6] (PSCAD)</td>
<td>50</td>
<td>60</td>
<td>6</td>
<td>2.5</td>
<td>1.111</td>
</tr>
<tr>
<td>[7] (PSIM)</td>
<td>5</td>
<td>72.6</td>
<td>22</td>
<td>2.35</td>
<td>0.209</td>
</tr>
</tbody>
</table>

As can be seen from the table, the technique described here, yields, results that are similar to the values used in the literature. In most cases, slightly smaller values, and in 2 cases here, larger values than the ones used. Thus, the method can be used confidently to determine an acceptable capacitor value for the converter.

B.2 Leg Inductor Value Selection

Capacitors are not the only element to be selected when designing a MMC. As discussed earlier, contrary to traditional VSC based converters, the MMC also includes inductors in each arm. These inductors have two main functions:

1. They help suppress the circulating currents in multiple phase systems, created by the inequality of the generated phase voltages.
2. Because the arm inductors are in series with the distributed energy storage capacitors, they can help limit the rise of fault currents through the converter.
Appendix B. Capacitor and Inductor Selection

These inductors, however, have a negative effect on controls, slowing down the reaction of the system as they limit the rate of change of current through the converter. Thus, in an ideal scenario, their inductance value would be zero. But this would also lead to large losses due to circulating currents and large fault currents, negating an important advantage of the MMC. In this case again, the value has been selected to match the model of [16].

[21] proposes two criteria based on these two main functions, to be used for the selection of the values of these arm inductors. To limit the circulating and fault currents, the highest acceptable levels for each case can be determined and the corresponding inductor value determined. The largest value obtained would represent the value used in the system, this technique can be used to verify that the selected value is reasonable.

B.2.1 Limiting circulating currents [21]

It was shown earlier that the circulating currents are 2nd harmonic and negative sequence. When considering the circulating currents, there will be a second harmonic negative sequence voltage added to the voltage in each arm. The voltages thus become:

\[
v_U(t) = \frac{V_{DC}}{2} [1 - m \sin(\omega_0 t)] + \frac{V_{2f}}{2} \sin(2\omega_0 t + \phi) \tag{B.3}
\]

\[
v_L(t) = \frac{V_{DC}}{2} [1 + m \sin(\omega_0 t)] + \frac{V_{2f}}{2} \sin(2\omega_0 t + \phi) \tag{B.4}
\]

Where \(V_{2f}\) is the magnitude of the voltage ripple and \(\phi\) its phase angle, which are unknown.

The double frequency voltage will create a double frequency current through the arm inductors, which, neglecting the arm resistance, can be defined as:

\[
i_{2f}(t) = \int \frac{v_{2f}(t)}{L_s} dt \\
= -\frac{V_{2f}}{4\omega_0 L_s} \cos(2\omega_0 t + \phi) \\
= I_{2f} \cos(2\omega_0 t + \phi) \tag{B.5}
\]

Where \(I_{2f}\) is the peak value of the current which is also unknown. From the previous equations, the total current in the upper and lower arms, including circulating currents, can be re-written to be:

\[
i_U(t) = \frac{I_{DC}}{3} [1 + k \sin(\omega_0 t + \phi)] + I_{2f} \cos(2\omega_0 t + \phi) \tag{B.6}
\]

\[
i_L(t) = \frac{I_{DC}}{3} [1 - k \sin(\omega_0 t + \phi)] + I_{2f} \cos(2\omega_0 t + \phi) \tag{B.7}
\]

Using the updated values of the current and voltage, it is now possible to calculate the energy absorbed in both halves of the leg.
Appendix B. Capacitor and Inductor Selection

\[ W_P(t) = \int (v_U(t)i_U(t) + v_L(t)i_L(t)) \, dt \]

\[ = \int \left[ \frac{V_{DC}}{2} \left[ 1 - m \sin(\omega_0 t) \right] + \frac{V_{2f}}{2} \sin(2\omega_0 t + \phi) \right] \left[ \frac{I_{DC}}{3} \left[ 1 + k \sin(\omega_0 t + \phi) \right] + I_{2f} \cos(2\omega_0 t + \phi) \right] \, dt \]

\[ = \frac{V_{DC}I_{DC}}{6} \left[ 2 - mk \cos(\phi) \right] t + \left( \frac{V_{DC}I_{DC}mk}{12\omega_0} + \frac{V_{DC}I_{2f}}{2\omega_0} \right) \sin(2\omega_0 t + \phi) \]

\[ - \frac{V_{2f}I_{DC}}{6\omega_0} \cos(2\omega_0 t + \phi) - \frac{V_{2f}I_{2f}}{8\omega_0} \cos(4\omega_0 t + 2\phi) \]  

(B.8)

In steady-state, the total energy change should be zero, so the DC terms must add up to 0. As such:

\[ 2 - mk \cos(\phi) = 0 \]

\[ mk \cos(\phi) = 2 \]

\[ mk = \frac{2}{\cos(\phi)} \]  

(B.9)

Replacing in equation B.8:

\[ W_P(t) = \left( \frac{V_{DC}I_{DC}}{6\cos(\phi)\omega_0} + \frac{V_{DC}V_{2f}}{2\omega_0} \right) \sin(2\omega_0 t + \phi) - \frac{V_{2f}I_{DC}}{6\omega_0} \cos(2\omega_0 t + \phi) \]

\[ - \frac{V_{2f}I_{2f}}{8\omega_0} \cos(4\omega_0 t + 2\phi) \]  

(B.10)

From equation B.5, replace \( I_{2f} \) by its equivalent \( \frac{V_{2f}}{4\omega_0 L_s} \):

\[ W_P(t) = \left( \frac{V_{DC}I_{DC}}{6\cos(\phi)\omega_0} + \frac{V_{DC}V_{2f}}{8\omega_0^2 L_s} \right) \sin(2\omega_0 t + \phi) - \frac{V_{2f}I_{DC}}{6\omega_0} \cos(2\omega_0 t + \phi) \]

\[ - \frac{V_{2f}^2}{32\omega_0^2 L_s} \cos(4\omega_0 t + 2\phi) \]  

(B.11)

Knowing that \( V_{DC} \) is much larger than the second harmonic term \( V_{2f} \). The last term in the equation can be neglected as it will not have a significant effect on the result. Also, given a value of \( L_s \) in the few mH range, a target frequency of 60Hz and knowing the \( V_{DC} \) is much larger than \( I_{DC} \), one can see that:

\[ \frac{V_{DC}V_{2f}}{8\omega_0^2 L_s} >> \frac{V_{2f}I_{DC}}{6\omega_0} \]

So the \( \cos \) term in the equation can be removed as well. The simplified equation now becomes:

\[ W_P(t) = \left( \frac{V_{DC}I_{DC}}{6\cos(\phi)\omega_0} + \frac{V_{DC}V_{2f}}{8\omega_0^2 L_s} \right) \sin(2\omega_0 t + \phi) \]  

(B.12)

If the control method used allows for an even distribution of the DC voltage across all modules, the second harmonic voltage ripple will also be distributed evenly through the leg. The voltage of the modules can thus be expressed as:
The total energy stored in the capacitors is then:

\[
W_C(t) = 2N \frac{1}{2} C v_c(t)^2
\]

\[
= NC \left( \frac{V_{DC}^2}{N^2} + \frac{V_{DC} V_{2f}}{N^2} \sin(2\omega_0 t + \phi) + \frac{V_{2f}^2}{N^2} \sin^2(2\omega_0 t + \phi) \right)
\]

\[
= \frac{V_{DC}^2 C}{N} + \frac{V_{DC} V_{2f} C}{N} \sin(2\omega_0 t + \phi) + \frac{V_{2f}^2 C}{N} \sin^2(2\omega_0 t + \phi)
\] (B.14)

The second harmonic terms equations B.12 and B.14 must match in steady-state. It is thus possible to express \( V_{2f} \) in terms of known values:

\[
\frac{V_{DC} I_{DC}}{6 \cos(\phi) \omega_0} + \frac{V_{DC} V_{2f}}{8 \omega_0^2 L_s} = \frac{V_{DC} V_{2f} C}{N}
\]

\[
\frac{V_{DC} I_{DC}}{6 \cos(\phi) \omega_0} = V_{2f} \left( \frac{V_{DC} C}{N} - \frac{V_{DC}}{8 \omega_0^2 L_s} \right)
\]

\[
V_{2f} = \frac{V_{DC} I_{DC}}{6 \cos(\phi) \omega_0} \frac{1}{\frac{V_{DC} C}{N} - \frac{V_{DC}}{8 \omega_0^2 L_s}}
\]

\[
V_{2f} = \frac{I_{DC}}{6 \cos(\phi) \omega_0} \frac{1}{\frac{4 N \omega_0 L_s}{8 \omega_0^2 L_s C - N}}
\]

\[
V_{2f} = \frac{I_{DC}}{3 \cos(\phi)} \frac{4 N \omega_0 L_s}{8 \omega_0^2 L_s C - N}
\] (B.15)

The peak value of the second harmonic current can thus be calculated. From equation B.5, replace \( V_{2f} \) by \( 4I_{2f} \omega_0 L_s \):

\[
I_{2f} = \frac{1}{4 \omega_0 L_s} \frac{I_{DC}}{3 \cos(\phi)} \frac{4 N \omega_0 L_s}{8 \omega_0^2 L_s C - N}
\]

\[
I_{2f} = \frac{I_{DC}}{3 \cos(\phi)} \frac{N}{8 \omega_0^2 L_s C - N}
\] (B.16)

From this equation, it is possible to limit the peak value of the circulating currents by selecting the desired inductor.
\[ I_{2f} = \frac{I_{DC} \cos(\phi)}{8\omega_0^2 L_s C - N} \]
\[ I_{2f}(8\omega_0^2 L_s C - N) = \frac{I_{DC} N}{3\cos(\phi)} \]
\[ L_s = \frac{1}{8\omega_0^2 I_{2f} C} \left( \frac{I_{DC} N}{3\cos(\phi)} + N I_{2f} \right) \]
\[ L_s = \frac{N}{8\omega_0^2 C} \left( \frac{I_{DC}}{3I_{2f} \cos(\phi)} + 1 \right) \]
\[ L_s = \frac{N}{8V_{DC}\omega_0^2 C} \left( \frac{V_{DC}I_{DC}}{3I_{2f} \cos(\phi)} + V_{DC} \right) \]
\[ L_s = \frac{N}{8V_{DC}\omega_0^2 C} \left( \frac{P_A}{3I_{2f}} + V_{DC} \right) \]  

(B.17)

Where \( P_A \) is the apparent power through the converter, defined as \( \frac{V_{DC}I_{DC}}{\cos(\phi)} \). If the inductor value is relatively small, which it will be, \( \phi \) will be very close to 0, so that \( P_A \) can be approximated by \( V_{DC}I_{DC} \).

Given this equation and the target maximum circulating current ripple, it is now possible to select an appropriate value for the inductor.

### B.2.2 Verification

These calculations can be verified simply by conducting a PSCAD simulation and verifying the magnitude of the circulating currents obtained. The system used in the simulations is smaller than the final system in order to reduce the required simulation times.

The parameters of the simulation are shown in Table B.2:

| Number of Modules \( N \) | 15 |
| DC Link Voltage \( V_{DC} \) | 15 kV |
| Frequency \( \omega_0 \) | 377 rad/s |
| Module Capacitor \( C \) | 10 mF |
| Apparent Power \( P_A \) | 15 MVA |
| Desired Ripple \( I_{2f} \) | 5% 10% 20% |
| Required Inductor \( L_s \) | 10.11mH 5.71mH 3.52mH |
| Actual Ripple | 6.47% 12.58% 24.32% |

Figure B.1 shows the currents in the upper and lower arms of the converter, as well as the circulating currents through the converter with the inductors set to 10.11 mH, which should create ripples of approximately 5%.

As can be seen, the arm currents fluctuate between -1100 and 600 amps, and the circulating currents fluctuate between -55 and 55 amps. The ratio of amplitudes is thus approximately 6.47 %, which is slightly above the expected value, but still within a reasonable range. The simulations run with the inductors calculated for 10% and 20% current ripple sizes also yield results slightly above the expected result. The results are shown in Table B.2. Even though the measured values are different from the
Appendix B. Capacitor and Inductor Selection

Figure B.1: Upper arm, lower arm and circulating currents of phase A, with leg inductor of 10.11 mH calculated ones, the results are similar enough to show that the technique provides a reasonable approximation of the size of the circulating currents as limited by the arm inductors. It is thus possible to chose a value of inductance in order to limit these currents, based on this method.

B.2.3 Limiting Fault currents [21]

The second factor to consider in selecting the size of the arm inductor is the maximum rate of change of the fault currents. In the case of a fault, the arm current rise will be limited by the inductor values. Taking into consideration the worse case incident represented by a fault on the DC side, the rise in the current can be studied for a short period of time. The assumption here is that the transients are short enough that the capacitor voltages remain constant over the transient interval. In this case, the current through one phase of the converter can be calculated to be (ignoring arm resistances).

\[ L_s \frac{di_U}{dt} - V_{DC} = 0 \]  

(B.18)

Because the transient currents will be very large in this case, one can assume that the currents in the upper and lower arms \((i_U \text{ and } i_L)\) will be equal.

\[ 2L_s \frac{di}{dt} - V_{DC} = 0 \]

\[ L_s = \frac{V_{DC}}{2 \frac{di}{dt}} \]  

(B.19)

Thus, after selecting the maximum allowable current slope during transients, it is now possible to select the required inductor size.
B.2.4 Selection

Given the converter specification defined in Table 6.1, and using a maximum ripple of 10%, it is now possible to determine the required arm inductor value.

First, calculate the required ripple in amperes. The rated current can be calculated from the rated power and voltage.

\[
I_{DC} = \frac{1000\text{MW}}{640\text{kV}}
\]
\[
I_{DC} = 1.5625\text{kA}
\]

Based on a desired maximum ripple amplitude of 10%, the current ripple should be 156 A.

\[
L_s = \frac{N}{8V_{DC}\omega_0^2 C} \left( \frac{P_A}{3I_{2f}} + V_{DC} \right)
\]

\[
L_s = \frac{400}{8 \times 640000 \times 377^2 \times 0.0125} \left( \frac{1000000000}{3 \times 156} + 640000 \right)
\]

\[
L_s = \frac{9096256}{2776752.137}
\]

\[
L_s = 122.1\text{mH}
\] (B.20)

Which is in line with the value used in the system (50mH). The value in the system is smaller and would lead to circulating currents of approximate amplitude of 25%, this is not a problem in this case however, as the additional circulating current controls will easily be able to limit this value to a much smaller value.

Second, for the required fault current:

\[
L_s = \frac{V_{DC}}{\frac{2\pi}{\omega}}
\]
\[
50\text{mH} = \frac{640000}{\frac{2\pi}{\omega}}
\]
\[
\frac{di}{dt} = 6.4\text{MA/sec}
\] (B.21)

The selected value would thus allow for a fault current of 6.4 MA/sec. This value was apparently determined to be sufficient for this system. This, of course will vary depending on the individual systems.
Appendix C

Converter model including forward voltage drop in diodes and IGBTs

The model as implemented ignores the forward voltage drop of the diodes and IGBTs, instead representing them as fixed resistances based on their open or closed state. The forward voltage drop of Diodes and IGBTs is relatively small when compared to the overall voltages in the MMCs considered. However, simulations were performed to ensure that this simplification is valid. This was done by modifying the full converter models is described in 5, and adding forward voltage drop to the diode and IGBT models. The voltage drop was selected based on the characteristics of the CM1500HC-66R IGBT module by Mitsubishi electric, which is rated for 1500A and 3300V, both ratings reasonably close to the operating point of the converter studied in this thesis. The forward voltage drop for the IGBTs and diodes was thus set to 3V for this simulation.

The result of the simulation including the forward voltage drops was then compared to simulations performed ignoring it. The simulation was performed for 2 cases:

1. A change in DC voltage command from 0.9 to 1.1 pu

2. A single phase-to-ground fault on phase A at the point of connection of the converter with the AC system.

The results of these 2 simulations show the effect of the inclusion of the forward voltage drop in the system, it’s potential effects on the controls and and during fast transients.

C.0.5 Change in DC voltage reference

This first test scenario simulates a change in the DC voltage reference command. In this scenario, the reactive current command is set at 0 pu, while the DC voltage reference steps from 0.9 to 1.1 pu at t = 1sec. For this test, the circulating current controller is activated throughout. Important simulation parameters are shown in Table C.1, and results of the simulation in Figure C.1.

Simulation Results

The figure shows that the models produce equivalent results in this scenario. Some discrepancies are noticeable during the transient, most noticeably on the arm and AC currents, but their amplitude is
Table C.1: Information for the PSCAD simulations of a DC voltage reference step change, comparing the 12 levels MMC models including and omitting forward voltage drop

<table>
<thead>
<tr>
<th>Disturbance</th>
<th>Step change in DC voltage reference from 0.9 pu to 1.1 pu</th>
</tr>
</thead>
<tbody>
<tr>
<td>Disturbance Instant</td>
<td>1 sec</td>
</tr>
<tr>
<td>Reference Commands</td>
<td></td>
</tr>
<tr>
<td>Reactive Current Reference</td>
<td>0 pu</td>
</tr>
<tr>
<td>DC Voltage Reference</td>
<td>0.9 pu</td>
</tr>
<tr>
<td>Circulating Current Control</td>
<td>ON</td>
</tr>
</tbody>
</table>

Figure C.1: Comparison between the simulation results for models including and omitting forward voltage drop of the switching elements of a 12 levels MMC converter for a DC voltage reference step change
Appendix C. Converter model including forward voltage drop in diodes and IGBTs

limited.

The measured signals fluctuate more in the case including the forward voltage drop which is likely
the result of ignoring their effect in the control implementation, it is clear however, from looking at the
figure that the systems behave almost identically whether or not they are considered.

This scenario shows that the response of the system to a change in DC voltage reference is very
similar between the two models.

C.0.6 Single Phase Fault at the point of AC connection

Table C.2: Information for the PSCAD simulations of a 100ms single phase-to-ground AC fault at the
converter, comparing the 12 levels MMC models including and omitting forward voltage drop

<table>
<thead>
<tr>
<th>Disturbance</th>
<th>100m single phase-to-ground on phase A at the point of AC connection of the converter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Disturbance Instant</td>
<td>1 sec</td>
</tr>
<tr>
<td>Reference Commands</td>
<td>Before Disturbance</td>
</tr>
<tr>
<td>Reactive Current Reference</td>
<td>0 pu</td>
</tr>
<tr>
<td>DC Voltage Reference</td>
<td>1 pu</td>
</tr>
<tr>
<td>Circulating Current Control</td>
<td>ON</td>
</tr>
</tbody>
</table>

The second test scenario considers a 100ms line-to-ground fault, applied on phase A directly at the
point of connection of the AC system with the converter. This will generate asymmetric arm currents
and circulating currents as well as important fluctuations in the module capacitor voltages of phase
A. The reactive current and DC voltage command references are fixed throughout at 0 pu and 1 pu
respectively and the circulating current controls are active. Important simulation parameters are shown
in Table C.2, and results of the simulation in Figure C.2.

Simulation Results

The figure shows that both models yield almost identical simulation results, with very limited discrep-
ancies.
Figure C.2: Comparison between the simulation results for models including and omitting forward voltage drop of the switching elements of a 12 levels MMC converter during a 100ms single phase-to-ground AC fault at the converter
Appendix D

RTDS and FPGA Notes

This chapter contains general useful notes about RTDS.

- To display bit mapped variables to RTDS from the FPGA, the input type in RTDS has to be set to "INT" instead of "REAL". "REAL" variables usually truncate the lower bits so that information is lost in the display in RTDS if it is not set as an "INT". Even with an "INT", the display is rounded out (although with more precision).

D.1 Connection with FPGA Tests

- First test was default test at 100MHz. LEDs light up correctly, RTDS gives no errors. Signals are transmitted correctly.

- Tried to reduce all Rx and Tx clock speeds to 50MHz to see if the communications would still work. RTDS claims that 100MHz is the speed to use. The connection worked, both the FPGA and RTDS signalled that is was good, but the data was not correct.

D.1.1 RTDS Code to connect with FPGA

The code to connect with the FPGA from RTDS is relatively simple in its form. It is basically divided into 2 sections, receive and transmit. The sections are executed sequentially, that is, data is received in the FPGA first, then the FPGA completes its computations and transmits the data back. It must be done in this order or connection will not be established.

All the dip switches, push buttons and LEDs are connected to variables in code, while most are not used, some have specific functions:

- Push button S2 resets the code. Immediately after a reset, a LED chaser is run to indicate that the reset has been executed.

- LED 15 indicates that the card has a valid link to RTDS

- LED 14 indicates that the RTDS card is detected (this will not be lit up if the RTDS code is not running)

- LED 13 follows the internal clock. It is lit up, but an oscilloscope would allow to see it blinking.
D.2 RTDS Compile Faults

D.2.1 Download Error - See Telnet Session For Details

Sometimes during download, the error "rack 1: Download error, see Telnet session for details" appears. This issue prevents the download from finishing, and, as such, the program from running on RTDS.

There is a simple way to tell if the FPGA is detected by the RTDS rack. See subsection "GTFPGA X card not detected on Processor card X" below.

To get more information connect to RTDS using a telnet program, with windows XP, hyper terminal comes installed by default. It is located under "Accessories/Communications" in the start menu. The name of the connection is unimportant, but make sure to select "TCP/IP" under "Connect using:" when creating the connection. And enter the RTDS IP address under "Host address". Usually the RTDS IP address is "169.254.125.20". Once connected, when transferring the project HyperTerminal will display communications from RTDS, as shown in Figure D.1.

This particular screen shot shows the error "GTFPGA 1 card not detected on Processor card 2, GTIO1 TSPCMD_LOAD_FILE_TO_BP error" near the bottom of the image. The possible errors encountered are discussed in the subsections below.

GTFPGA X card not detected on Processor card X

This error is raised when the RTDS rack cannot find the FPGA device configured in the project. This can be caused by different factors.

The first factor (and most likely) is that the FPGA is not programmed correctly. It is not configured to keep the program when powered down. As such, it has to be re-programmed every time it is powered cycled. It is possible that the program be corrupted as well.

It also is possible that the rack hardware configuration needs to be refreshed. This can be done simply by going to "Tools/Config File Editor" in RSCAD, then select the rack in the list and click on "Get Selected Rack Configuration" in the top right of the screen. Once the process is complete, the rack should shown one "GTFPGA" for each FPGA connected to it. If this is not the case, check connections and programming on the FPGA’s themselves. This procedure will not work if RTDS is running a simulation.

There are a few other potential causes of this error:

- It seems that the presence of a .stp file (or signal tap from Quartus II) may also be a problem in certain cases. Some projects worked fine until a signal tap was setup. The exact cause of this issue is still not clear, but it seems like it is related to it.

- Modified the variables transmitted between RTDS and the FPGA also cause an error

D.2.2 Faults in small time step

The regular fault model is not available in the small time step functions of RTDS. Thus a the best way to simulate a fault in the small time step of the FPGA is to use a breaker and configure it to function like a fault. In RSCAD, a breaker is represented as a capacitor in series with a resistor when open, and by an inductor when closed. When a switch is activated, the energy stored in the capacitor \( (CV^2) \) or inductor \( (LI^2/2) \) is lost. To minimize the losses, a constraint that \( (CV^2 = LI^2/2) \) is added and limits the
choices of C and L. The formulas used for the selection are available in the RTDS manual in the "VSC Small Time-Step Modelling Manual" at page 1.4.

This also means that emulating the modelling of RTDS in PSCAD cannot be done simply by using a single fault function. The faults were modelled as two separate branches, one with capacitor and resistor and the other with an inductor, with only one of the two connected to the system at a time depending on if a fault is active or not.
## D.3 FPGA NOTES

### D.3.1 Implementation Notes

An overall diagram of the implementation is shown in Figure D.2.

![Figure D.2: Diagram representation of the code implementation in the Quartus software for MMC real-time simulation](image)

There was originally an issue with the model where, if the capacitor voltages were unlocked, one phase/arm would occasionally fail and the voltages would start growing uncontrollably, even when the model was holding well in steady-state for a extended period of time. This seemed to happen at random instants, and the model would hold for anywhere from a few minutes to a few hours before one of the phases would fail while the other 2 would continue to operate correctly.

After multiple test and to fix this issue, it was noticed that the calculation of the change of voltage through the capacitors which is done at each step and based on the equivalent capacitor resistor ($R_C$) and the arm current would sometime yield a very large number unexpectedly. This is most likely due to some overflow, but it was not simple to determine its precise origin.

So additional code was added to verify the change in voltage during a single time-step and if that change is more than a pre-determined value (the first 5 bits of the decimal part of the calculated change...
Appendix D. RTDS and FPGA Notes

in voltage must be 0 (that is nothing bigger than $2^{-6}$ or 0.015625 kV) for a single simulation time-step). Given the very small time-step used (2.5 µs), this still allows for very fast and accurate changes during transients, but discard any excessive changes caused by errors or overflows.

D.3.2 Input and Output Signals

The inputs to the FPGA platform from RTDS are:

- **AC Side currents (3):** Not used any more
- **Number of inserted modules (6):** Used to calculate the output voltage of the converter arm
- **Arm currents (6):** Used to calculate the change in module capacitor voltages
- **Capacitor Lock signal (1):** One signal to prevent capacitor voltage from being updated (used for testing/debugging)

The outputs of the FPGA platform to RTDS are:

- **MMC current on AC line (3):** Always 0, not used any more
- **MMC Voltage at PCC (6):** Always 0, not used any more
- **MMC Arm Voltages (6):** Sent back to RTDS for control
- **MMC Arm current for phase 1 (2):** Used for display/debugging
- **Capacitor voltages (upper arm, phase 1) (3):** Used for display/debugging
- **Switching signal for individual modules (upper arm, phase 1):** Used for display/debugging (on signals for first 32 modules (32-bit signal))
- **Calculate voltage change in arm capacitors (upper and lower arm, phase A) (2):** Used for display/debugging
- **Number of times the capacitor voltages were locked (phase 1):** Used as a marker for display and debugging in RTDS (10 bits, 5 LSBs show upper arm, 5 MSBs show lower arm)

D.3.3 Modifying converter size

Changing the size of the converter model simply requires resizing variables and arrays. The list below is intended to help finding variable and indexes to be modified, the value to be modified to depends on the size of the converter desired. The code can only easily accommodate modules in multiples of 20, any other number may required more changes.

- **Mytypes.vhd**
  - Variable: Volt_ArrayAll
  - Variable: Order_Array
  - Variable: SelectedMods
Appendix D. RTDS and FPGA Notes

- **AlteraSampleProject.vhd**
  - Variable:Upper gating (x3)
  - Variable:Lower gating (x3)
  - Variable:OnMods_U (x3)
  - Variable:OnMods_L (x3)

- **MMC_Circuit.vhd**
  - Definition:CONTROL_U
  - Definition:CONTROL_L

- **MMC_SM400.vhd**
  - Definition:CONTROL
  - Code:Calls of MMC_SM20.vhd commented out based on number of modules

- **ParallelSortNoPt.vhd**
  - Variable:Index
  - Code:Loop sizes
  - Code:Step Sizes (how many swaps per step)
  - Code:Max. Index (how many passes before the sorting is done)

- **BitAdder.vhd**
  - Definition:Vector
  - Definition:Sum
  - Code:Loop Sizes

- **ModSelect.vhd**
  - Definition:ModCmd
  - Variable:scanstate/scanIndex
  - Variable:sModCmds
  - Code:scanIndex limit (in state 1)

- **ModSwitch.vhd**
  - Definition:onMods/OnModCmd
  - Definition:ModCmds
  - Variable:sModCmds

### D.3.4 Important pins

The following pins are assigned to specific functions:
## Table D.1: Important pins on the FPGA

<table>
<thead>
<tr>
<th>Push Button</th>
<th>Dip Switches</th>
<th>LEDs</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td># Pin</td>
<td># Pin</td>
</tr>
<tr>
<td>S2</td>
<td>V34</td>
<td>1 AL35</td>
</tr>
<tr>
<td>S3</td>
<td>M34</td>
<td>2 AC35</td>
</tr>
<tr>
<td>S4</td>
<td>W32</td>
<td>3 J34</td>
</tr>
<tr>
<td>S5</td>
<td>AK35</td>
<td>4 AN35</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5 G33</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6 K35</td>
</tr>
<tr>
<td></td>
<td></td>
<td>7 AG34</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8 AG31</td>
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</tbody>
</table>
Appendix E

General Notes

This chapter contains any general notes that I took and consider may be useful.

Nov 1st 2012

The next notes a general notes about the tests I made for different modifications on the sorting algorithm. Tests were done with a much smaller MMC to speed up compilation times, but should transfer well to higher number of levels. The idea was to find out how modifications to the sorting algorithm would affect speed and space requirements on the FPGA. This was done at a point when I thought that fully sorting the array on every pass would take too long, so I was planning to sort the array and keep track of not only the order, but the voltage level of each module.

So instead of latching the voltage values at the beginning of the scan, and track only the module number and its voltage during the sorting, then starting over from scratch at the next iteration, this would link the ordered array with its respective module, so each scan could start from the result of the previous scan. This technique would work well in a conventional CPU, as each sorting pass would take much less time since it starts with a mostly sorted array and only has to deal with the recent changes in module voltages. This, however required much memory on the FPGA side as any of the positions of the voltage array could be linked to any of the positions of the sorted array on each cycle, which internally required a very high amount of resources.

The technique used (Odd-Even sort) was more efficient because it removes that link between the voltage array and the sorted array, which are not linked directly any more.

- Testing of a new selection algorithm
  - Sorting OK, Compsort (size 341)
  - ModCount OK, BitAdder640 (size 31)
  - HL.LV, Selection OK, ModSelectImp (size 132)
  - Switching OK, ModSw (size 146)

- Speed up the sorting
  - Initial Speed, 342 scans

- Swap 4 per scan
Appendix E. General Notes

- Sorting OK, BubbleSortImp (size 1149)
  - 78 Scans

  • Sorting from both ends (at the same time)
    - Sorting OK, BubbleSortImp (size 638)
      - 170 Scans
      - Does have the advantage of bubbling both min and max in one scan which is good to catch outlying values fast

  • Sorting once up, then in the other direction
    - Sorting OK, BubbleSortImp (size 598)
      - 358 Scans
      - No speed gain over standard technique, 174\% the size
      - Does have the advantage of bubbling both min and max in one scan which is good to catch outlying values fast

Table E.1: Sorting tests results

<table>
<thead>
<tr>
<th>Technique</th>
<th>Size</th>
<th>Speed (scans)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Regular Sort</td>
<td>344</td>
<td>342</td>
</tr>
<tr>
<td>Four at a Time</td>
<td>1149 (334%)</td>
<td>78 (438%)</td>
</tr>
<tr>
<td>Both Ways at Once</td>
<td>638 (185%)</td>
<td>170 (201%)</td>
</tr>
<tr>
<td>Changing Direction</td>
<td>598 (174%)</td>
<td>170 (96%)</td>
</tr>
</tbody>
</table>

Given no space limitations, multiple at a time is definitely best. Sorting both ways may be a good compromise.

LabView

Just a few notes on the LabView controller implementation.

- The PLL only seems to work in "LoopTimeInCalc" which is the time allow for execution of the loop doing calculations on the inputs (PLL, dq-transforms...) is set to at least 20\(\mu\)s. Not sure if it is because it is the same as "LoopTimeIn" which read the inputs, or because the calculated "stepsize" for the integrator is too small. In any case, 20\(\mu\)s seems to yield good results.

- Utilization at last compile
  - Slices 24\%
  - Registers 7\%
  - LUTs 16.8\%
  - DSP48s 43.9\%
  - RAM 0.0\%
Appendix F

System pictures
Figure F.1: Picture of the full real-time simulation platform showing two FPGA MMC simulators, the RTDS system and cRIO controller
Appendix F. System pictures

Figure F.2: Picture of the two FPGA MMC simulators, FPGA boards with attached fibre optic interface

Figure F.3: Picture of the cRIO controller with analog signals connected to RTDS