A 1.25GS/s 8-bit Time-Interleaved C-2C SAR ADC for Wireline Receiver Applications

by

Qiwei Wang

A thesis submitted in conformity with the requirements for the degree of Master of Applied Science
Graduate Department of Electrical and Computer Engineering
University of Toronto

© Copyright 2013 by Qiwei Wang
Abstract

A 1.25GS/s 8-bit Time-Interleaved C-2C SAR ADC for Wireline Receiver Applications

Qiwei Wang
Master of Applied Science
Graduate Department of Electrical and Computer Engineering
University of Toronto
2013

Many wireline communication systems are moving toward a digital based architecture for the receiver that requires a front-end high-speed ADC. This thesis proposes a two-level time-interleaving topology for realizing such an ADC, comprising front-end time-interleaved sub-rate track-and-holds each followed by a sub-ADC which is further time-interleaved to a slower clock frequency. The design, implementation and measurement of the 1.25GS/s sub-ADC fabricated in 65nm CMOS technology is presented. The SAR architecture is chosen for its low power and digital friendly nature along with an unconventional C-2C capacitive DAC implementation for higher bandwidth. The time-interleaved C-2C SAR ADC runs with a 1.0V supply, and it has a full input range of 1.0V_{pp} differential, while consuming 34mW. The SNDR is 39.4dB at low frequency and the FOM is 360fJ/conv-step and 428fJ/conv-step at low and Nyquist input frequencies respectively. The SNDR is 34dB at 4GHz input frequency, which is more than 6 times the Nyquist frequency.
Acknowledgements

I would like to thank my supervisor Professor Tony Chan Carusone for all of his guidance and support during my graduate study. And I look forward to spending another four years with him. I would also like to thank Professor David Johns, Professor Antonio Liscidini, and Professor Aleksandar Prodic for their participation in my MASc exam committee.

Second, I would like to thank my colleagues in BA5000 for all the fun interactions. My special thanks go to my "half-brother" Luke Wang, for all the discussions we had.

I would also like to thank my parents for their understanding and endless love through the duration of my studies and my life.

Finally, I would like to thank my beautiful wife Macy for always being there for me.
Contents

Table of Contents ................................................... iv
List of Figures ....................................................... v
List of Tables ......................................................... vii
List of Acronyms ..................................................... viii

1 Introduction ....................................................... 1
  1.1 Motivation ......................................................... 1
  1.2 Objective ........................................................ 2
  1.3 Thesis Organization ............................................. 2

2 Background ....................................................... 3
  2.1 ADC Architectures ............................................... 3
  2.2 Time-Interleaved ADC ......................................... 4
  2.3 SAR ADC ........................................................ 7
    2.3.1 Architecture and Operation ............................. 8
    2.3.2 Binary-Weighted DAC ................................. 10
    2.3.3 C-2C DAC ................................................. 12

3 System and Circuit Design .................................... 15
  3.1 System Overview .............................................. 15
  3.2 Architecture of the Individual C-2C SAR ADC ............ 18
  3.3 Operation of the Individual C-2C SAR ADC .............. 20
  3.4 Switch Design ................................................. 24
  3.5 Comparator Design ........................................... 27
  3.6 Time-Interleaving Architecture ............................ 30
  3.7 Calibration .................................................... 32

4 Experimental Results .......................................... 35
  4.1 Test Setup ..................................................... 35
4.1.1 Prototype .................................................. 35
4.1.2 Printed Circuit Board .................................. 35
4.1.3 Equipment Setup ...................................... 37
4.2 Measurement Results ..................................... 38
  4.2.1 Single SAR ADC Performance ...................... 39
  4.2.2 Time-Interleaved SAR ADC Performance .......... 40
  4.2.3 Performance Summary and Comparison .......... 48

5 Conclusion .................................................. 52
  5.1 Summary .................................................. 52
  5.2 Future Work ............................................. 52
List of Figures

2.1 Recent high-speed CMOS ADCs faster than or equal to 10GS/s . . . . . . . . . . 5
2.2 Time-interleaved ADC block diagram. . . . . . . . . . . . . . . . . . . . . . 6
2.3 SAR ADC block diagram. . . . . . . . . . . . . . . . . . . . . . . . . . . . 9
2.4 SAR algorithm chart for 3-bit conversion. . . . . . . . . . . . . . . . . . . . . 9
2.5 Charge redistribution SAR ADC with binary-weighted DAC. . . . . . . . . . . 10
2.6 Charge redistribution SAR ADC with C-2C DAC. . . . . . . . . . . . . . . . . 13

3.1 ENOB versus clock RMS jitter for a sinusoid with 5GHz input frequency. . . . 16
3.2 Top level block diagram of the proposed 10GS/s 8-bit two-level time-interleaved
ADC. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 17
3.3 Schematic of an individual C-2C SAR ADC. . . . . . . . . . . . . . . . . . . . 18
3.4 C-2C SAR ADC schematic during the sampling phase. . . . . . . . . . . . . . 20
3.5 C-2C SAR ADC schematic during MSB evaluation. . . . . . . . . . . . . . . 21
3.6 C-2C SAR ADC schematic during MSB-1 evaluation. . . . . . . . . . . . . . 22
3.7 C-2C SAR ADC schematic during MSB-2 evaluation. . . . . . . . . . . . . . 23
3.8 Detailed timing breakdown of the SAR ADC with a clock period of 800ps. . . 24
3.9 Schematic of the bootstrapped switch. . . . . . . . . . . . . . . . . . . . . . . 25
3.10 Switch resistance comparison between transmission gate and bootstrapping. . 26
3.11 Schematic of the comparator that consists of a pre-amplifier followed by a
double-tail latch. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 28
3.12 Block diagram of cross-coupled inverters. . . . . . . . . . . . . . . . . . . . . 28
3.13 Metastability error probability versus time constant with total comparator re-
solving time of 300ps. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 29
3.14 Top level diagram of the 1.25GS/s time-interleaved C-2C SAR ADC. . . . . . 31
3.15 Timing diagram of the time-interleaved SAR ADC with cycle numbers. . . . . 32
3.16 Detailed timing diagram of the front-end sampler and the input samplers in
each SAR ADC. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 33
3.17 Schematic of the PMOS source follower buffer, with 2.4mW power consumption. 33
3.18 Block diagram of the off-chip radix calibration performed in Matlab. 34

4.1 A die photo of the implemented time-interleaved C-2C SAR ADC. 36
4.2 Populated PCB photograph. 36
4.3 PCB block diagram. 37
4.4 External equipment setup block diagram. 38
4.5 External equipment setup photograph. 39
4.6 Offset histogram of 70 individual SAR ADCs. The measurement is conducted with a 92.75MHz sinusoidal input and 500 points are taken per individual SAR ADC. 40
4.7 Amplitude histogram of 70 individual SAR ADCs. The measurement is conducted with a 92.75MHz sinusoidal input and 500 points are taken per individual SAR ADC. 41
4.8 SNDR histogram of 70 individual SAR ADCs before and after radix calibration. The SNDR improved from 32dB to 38.8dB. 41
4.9 DNL for time-interleaved SAR ADC with 92.75MHz sinusoidal input before and after calibration. It improved from +6.2/-1.0 LSB to 1.9/-1.0 LSB. 42
4.10 INL for time-interleaved SAR ADC with 92.75MHz sinusoidal input before and after calibration. It improved from +5.6/-7.4 LSB to +2.2/-1.7 LSB. 43
4.11 Measured decimated output spectrum (5000 points) of the time-interleaved ADC with a Nyquist frequency input before and after calibration. SNDR improved from 27.1dB to 37.9dB. 45
4.12 Measured SNDR and SFDR, and channel loss versus input frequency up to 4GHz 46
4.13 SNDR versus input amplitude with 93MHz and 4GHz input frequencies. 47
4.14 SNDR versus sampling frequency for 1.0V, 1.1V and 1.2V supply voltages with an input frequency around 100MHz. 47
4.15 Power consumption of the time-interleaved C-2C SAR ADC versus sampling frequency. 48
4.16 Comparison with recent high-speed CMOS ADCs faster than or equal to 10GS/s, this work is denoted with a black star. 51
## List of Tables

<table>
<thead>
<tr>
<th>Table</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.1</td>
<td>Summary of time-interleaved mismatches for N sub-ADCs with input frequency of $F_{IN}$, $k = 1, 2, ..., N-1$</td>
<td>7</td>
</tr>
<tr>
<td>3.1</td>
<td>Design specification of the 1.25GS/s time-interleaved C-2C SAR ADC</td>
<td>16</td>
</tr>
<tr>
<td>3.2</td>
<td>Parasitic capacitance for different unit MIM capacitance values</td>
<td>19</td>
</tr>
<tr>
<td>3.3</td>
<td>Switch design summary</td>
<td>27</td>
</tr>
<tr>
<td>3.4</td>
<td>Comparator performance summary</td>
<td>30</td>
</tr>
<tr>
<td>4.1</td>
<td>List of key components on the PCB</td>
<td>37</td>
</tr>
<tr>
<td>4.2</td>
<td>List of external equipments used</td>
<td>38</td>
</tr>
<tr>
<td>4.3</td>
<td>Power consumption distribution of a single SAR ADC and the time-interleaved SAR ADC</td>
<td>49</td>
</tr>
<tr>
<td>4.4</td>
<td>Performance summary of the prototype ADC</td>
<td>50</td>
</tr>
<tr>
<td>4.5</td>
<td>ADC performance comparison with other published works</td>
<td>50</td>
</tr>
</tbody>
</table>
List of Acronyms

ADC  Analog-to-Digital Converter
BER  Bit Error Rate
CTLE  Continuous-Time Linear Equalization
DAC  Digital-to-Analog Converter
DFE  Decision-Feedback Equalization
DNL  Differential Non-Linearity
DSP  Digital Signal Processing (or Processor)
ENOB  Effective Number Of Bits
FIFO  First in, First out
FIR  Finite Impulse Response
FOM  Figure of Merit
Gb/s  Gbits/Second
INL  Integral Non-Linearity
I/O  Input/Output
LMS  Least Mean Squares
LSB  Least Significant Bit
MIM  Metal Insulator Metal
MMF  Multimode Fiber
**MOSFET**  Metal-Oxide-Semiconductor Field-Effect Transistor

**MSB**  Most Significant Bit

**NMOS**  N-Channel MOSFET

**PCB**  Printed Circuit Board

**PMOS**  P-Channel MOSFET

**SAR**  Successive Approximation Register

**SFDR**  Spurious-Free Dynamic Range

**SNDR**  Signal-to-Noise-and-Distortion Ratio

**SNR**  Signal-to-Noise Ratio

**T/H**  Track and Hold

**TI**  Time-Interleaved
Chapter 1

Introduction

Analog-to-digital conversion is the process of converting physical continuous signals into quantized values. A device that does this conversion is called an analog-to-digital converter (ADC). There are many performance metrics for ADC design such as speed, power dissipation, area, latency, input bandwidth, resolution, linearity, etc. As each application requires different constraints, many ADC architectures have been developed. The most popular ones are: flash, pipeline, integrating, successive approximation register (SAR), algorithmic, Delta-Sigma, interpolating (and folding), two-step, and time-interleaved converters [1]. In this thesis, a high-speed medium-resolution ADC is discussed for wireline receiver applications.

1.1 Motivation

Rising demand of bandwidth due to increasing on-chip processing speed and logic density have pushed serial input/output (I/O) data rates beyond 10Gbits/second (Gb/s). As the data rate rose, channel impairments such as dielectric loss, skin effect, crosstalk, and reflections became more severe and made transceiver design more challenging. Analog techniques including continuous-time linear equalization (CTLE), decision-feedback equalization (DFE), and finite impulse response (FIR) filtering have dominated in applications having low-medium attenuation ($<20\text{dB}$) at one-half the bit rate [2], [3] and at ultra high data rate ($\geq40\text{Gb/s}$) [4], [5]. Recently, for applications including backplane (KR) and multimode fiber (MMF), which have data rates of 10Gb/s, ADC-based receivers with digital signal processing (DSP) have become popular [6–11]. For MMF channels up to 300m, the receiver eye can be completely closed due to the complex and time-varying channel pulse response. In the case of copper backplanes (KR), high attenuation ($>20\text{dB}$) of the channel will also make equalization of the signal difficult. Under these severe channel impairments, ADC-based receivers with digital backend enable implementation of more sophisticated algorithms that offer potentially higher perfor-
mance. With technology scaling, digital solutions will also provide better portability between IC fabrication technologies and flexibility, and ultimately result in lower power and cost. Even though the ADC-based solution provides many benefits, it still faces a bottleneck which is the design of a high-speed low-medium-resolution ADC. Therefore this thesis will target the implementation of such an ADC.

1.2 Objective

The main objectives of this thesis are as follows

1. Provide a background of existing high-speed ADC designs for wireline systems and review different ADC architectures.

2. Propose a lower-speed ADC that can be time-interleaved to satisfy the application requirement.

3. Show test-chip simulation, implementation, and measurement results to validate the design.

1.3 Thesis Organization

This thesis is organized as follows:

**Chapter 2. Background** Background information on existing high-speed ADCs are presented. Time-interleaving and SAR ADC topologies are reviewed in details, and two different DAC implementations of the SAR ADC are compared.

**Chapter 3. System and Circuit Design** The architecture and operation of the individual C-2C SAR ADC are shown, system and transistor level design choices are explained, and time-interleaving topology and calibration methods are presented.

**Chapter 4. Experimental Results** Measurement results of the time-interleaved C-2C SAR ADC described in Chapter 3 are presented and compared with other similar designs.

**Chapter 5. Conclusion** This thesis is summarized and future work is discussed.
Chapter 2

Background

2.1 ADC Architectures

There are many analog-to-digital converter architectures, each one has its own benefits and disadvantages, and the right architecture is chosen for each application based on specifications and constraints. For example, most audio systems use delta-sigma ADCs and high-speed sampling oscilloscopes use time-interleaved ADCs. Based on speed, ADC architectures are roughly divided into three categories: low-medium speed, medium speed, and high speed [1].

Low-medium speed converters include integrating and delta-sigma ADCs, capable of very high resolution (12-24 bits). Integrating ADCs are ideal for digitizing low-bandwidth signals, and are used for example in digital multimeters. Delta-sigma converters utilize oversampling and noise shaping to obtain very high resolution at the expense of lower input bandwidth, and are popular for applications such as high-quality digital audio and narrowband wireless systems.

Medium speed converters include successive approximation register (SAR) and algorithmic converters. Both of these use a binary search algorithm to match a digital code with the input signal. They resolve one bit every cycle, making them intermediate in their speed. The only difference between them is that the SAR ADC refines the reference voltage each cycle to approach the sampled input voltage, whereas the algorithmic ADC generates an error voltage each cycle and iteratively moves it towards zero. Whereas algorithmic converters require an analog gain element, SAR ADCs do not, making them mostly digital in their implementation, so they have become one of the most popular ADC architectures, particularly in advanced CMOS process technologies where digital circuitry has very high performance and low power consumption.

High speed converters include flash, two-step, interpolating (and folding), pipeline, and time-interleaved ADCs. Flash converters are the fastest single-channel ADC architecture be-
cause they utilize parallel comparators and perform instantaneous comparison with all reference levels. Pipeline ADCs also perform iterative search to match a digital code with the input analog signal, however N different analog circuitries are used to process N iterations in parallel, therefore they are faster than algorithmic and SAR converters. Two-step converters are basically pipeline converters with two stages, and they offer a balance between flash and pipeline ADCs. Interpolating and folding ADCs also perform conversion in two steps similar to two-step converters, however two-steps are performed simultaneously due to the folding circuit. They have generally lost favour in modern CMOS due to their relative high analog circuit complexity. Lastly, time-interleaving is a technique to increase the throughput or conversion rate of a converter by using an array of parallel converters. It can be applied to all ADC topologies.

The application of interest is wireline communication systems, where a high-speed (10+GS/s) ADC with a low-medium resolution (4-8 bits) is needed [6–12]. Figure 2.1 shows recently published CMOS ADCs that are faster than or equal to 10GS/s [13]. Figure 2.1a and 2.1b show their power efficiency and ADC resolution, respectively, versus sampling frequency. There are several interesting observations. First, all of the shown ADCs are time-interleaved (TI), meaning that it is impossible or too power inefficient to achieve the target speed with only one ADC. In fact, some flash ADCs without time-interleaving have been reported, often in SiGe BiCMOS, but with much higher power consumption and at the lower-end of resolution (4-5 bits) [14], [15]. Second, the architecture of the constituent sub-ADCs within the time-interleaved converters is evenly distributed between SAR and flash topologies. It is not surprising that [8], [9], [11], [16], and [17] all use flash topology as it achieves the fastest speed out of all ADC architectures. Since SAR ADCs are slower than flash converters, they require more time-interleaving. For example, 160 time-interleaved SAR ADCs are used in [18] and [19], and 64 are used in [20]. Only 8 time-interleaved SAR ADCs are used in [12] to achieve 10GS/s because it uses techniques such as asynchronous logic and alternative comparators to increase the unit ADC speed. Even though flash converters require less time-interleaving, they are generally confined to a resolution of 6 bits or less simply because the number of comparators increases exponentially with resolution.

2.2 Time-Interleaved ADC

The concept of time-interleaved converters was first introduced in 1980 [21]. In this architecture, N sub-ADCs each running at $F_S/N$ achieve an overall conversion rate of $F_S$ as shown in Figure 2.2. The analog input multiplexer is responsible for distributing the input sample to each sub-ADC over time. And the digital output multiplexer combines all the digital outputs
Figure 2.1: Recent high-speed CMOS ADCs faster than or equal to 10GS/s
in the same order. Note that sometimes it is not necessary to multiplex the digital output as the DSP block operates directly on the lower speed parallel data, which is generally at a clock frequency nicely compatible with standard-cell CMOS logic.

Time-interleaved ADCs are very sensitive to mismatch between different sub-ADCs, unlike non-interleaved converters, where offset, gain, timing and bandwidth inaccuracies do not degrade performance as long as they are constant. The effects of mismatch in time-interleaved architectures has been studied extensively [16], [21–24] and a brief summary will be given below. For simplicity, a two-channel time-interleaved ADC (N=2) will be used for the following discussions.

**Offset Mismatch** is due to the variations in DC offset between different channels. In the output spectrum, it contributes a tone at DC and at half of the sampling frequency (FS/2). Intuitively, if there is no input, the two sub-ADCs will simply digitize their own offset. As a result, the multiplexed digital output will switch between two DC offsets at a rate of FS, which will produce a common mode offset at frequency = 0 and a differential offset at frequency = FS/2. The magnitude and location of this tone is static and does not depend on the input signal.

**Gain Mismatch** happens because the gain of each channel is different. In the output spectrum, it introduces a tone at FS/2-FIN for a time-interleaved ADC with two channels, and the magnitude of the tone depends on the input amplitude. Intuitively, gain mismatch is
Table 2.1: Summary of time-interleaved mismatches for N sub-ADCs with input frequency of $F_{IN}$, $k = 1, 2, ..., N-1$

<table>
<thead>
<tr>
<th>Type of Mismatch</th>
<th>Tone Frequency</th>
<th>Dependency on Input Magnitude</th>
<th>Dependency on Input Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offset</td>
<td>$\frac{k}{N} \times F_S$</td>
<td>Independent</td>
<td>Independent</td>
</tr>
<tr>
<td>Gain</td>
<td>$\frac{k}{N} \times F_S \pm F_{IN}$</td>
<td>Linearly dependent</td>
<td>Independent</td>
</tr>
<tr>
<td>Timing</td>
<td>$\frac{k}{N} \times F_S \pm F_{IN}$</td>
<td>Linearly dependent</td>
<td>Linearly dependent</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>$\frac{k}{N} \times F_S \pm F_{IN}$</td>
<td>Nonlinearly dependent</td>
<td>Nonlinearly dependent</td>
</tr>
</tbody>
</table>

like amplitude modulation. The input amplitude is modulated based on which channel is active, therefore the difference in magnitude of input signal can be thought of as the carrier signal, and it’s being modulated by a square wave with a frequency of $F_S/2$. Then the modulated signal has a tone at frequency $F_{mod} - F_{carrier} = F_S/2 - F_{IN}$.

**Timing Mismatch** or phase skew is due to the variations in the sampling instant of each sub-ADC. Ideally, each sampling instant should be spaced $1/F_S$ apart, any timing error will translate to magnitude error that’s dependent on the input amplitude as well as the input frequency. Timing mismatch is similar to phase modulation, where the timing error is modulated by a square wave with a frequency of $F_S/2$. This results in a tone at frequency $F_S/2 - F_{IN}$, the same as gain mismatch.

**Bandwidth Mismatch** is due to the bandwidth difference in the sampling networks of each sub-ADC. It is usually caused by the mismatch in switch resistance as capacitor matching in recent CMOS technologies is very good. Bandwidth mismatch wouldn’t be a problem if the sampling network bandwidth is much larger than the input frequency. If the bandwidth is comparable to the input frequency, this mismatch is similar to a combination of gain and timing mismatches. The main difference is that the gain error magnitude of bandwidth mismatch is dependent on the input frequency and the timing error is non-linear with respect to frequency.

For number of channels greater than 2, a very good analysis is given in [24] and a summary is shown in table 2.1.

### 2.3 SAR ADC

The first appearance of a successive approximation register (SAR) ADC dates back to 1946, in a patent filed by J. C. Schelleng of Bell Telephone Laboratories [25]. It is still one of the
most popular ADC architectures today. In fact, more than half of the Nyquist rate ADC papers presented at International Solid-State Circuits Conference 2013 are on SAR ADCs. And it is truly amazing that after almost 70 years, there are still many innovations on this topic.

The SAR ADC gained its popularity mainly thanks to CMOS technology scaling. Although it resolves only one bit per clock cycle (assuming a radix-2 search algorithm) and is therefore generally considered a medium-speed converter, with the help of time-interleaving, it becomes an attractive option for high-speed communication systems. Especially in sub-100nm technology, where scalability is a primary concern.

### 2.3.1 Architecture and Operation

SAR ADCs use a binary search algorithm to find the quantization level that most closely approximates the sampled input value. The binary search algorithm relies on the divide and conquer strategy and can be best understood through an example. Consider the number guessing game, where a person tries to guess a number from 1 to 64, and the only answers given are higher, lower, or yes. The first guess is 32, and if the answer is higher, the next guess will split the difference between 32 (a new lower-bound for the possible answer) and 64, resulting in 48. Similarly, if the answer to the first guess is lower, the second guess is 16, and so on. In general, each iteration divides the search space in half, and the desired data can be found with a maximum of N iterations given a data size of $2^N$.

Unlike the binary search example given above, SAR ADC quantizes continuous analog signals, therefore the answer “yes” is not possible. As a result, a conventional SAR ADC always needs N iterations to achieve a resolution of N bits. A generic simplified block diagram of a SAR ADC shown in Figure 2.3 consists of a track and hold (T/H) circuit, a comparator, the SAR logic and a digital-to-analog converter (DAC) that converts the digital output from SAR logic to an analog voltage $V_{\text{dac}}$. The T/H circuit holds the input voltage $V_{\text{in}}$ for the whole duration of the conversion. In each iteration, the comparator compares the input voltage with $V_{\text{dac}}$, and based on the decision, SAR logic updates $V_{\text{dac}}$. At the end of the conversion, $V_{\text{dac}}$ is within half least significant bit (LSB) of the input voltage. Since only 1 bit is resolved per cycle, and at least one clock cycle is dedicated to sampling, a N-bit conversion usually takes a total of N+1 clock cycles.

An example algorithm for a 3-bit SAR converter is shown in Figure 2.4. In the first cycle, sampling occurs which hold the input voltage for the rest of the conversion time. Then SAR logic and DAC generate $V_{\text{ref}}/2$ and compare it with $V_{\text{in}}$. Note that the dynamic range of the input signal is from 0 to $V_{\text{ref}}$. If $V_{\text{in}}$ is greater or equal to $V_{\text{ref}}/2$, the most significant bit (MSB) becomes 1, otherwise 0 is assigned to the MSB. Based on the MSB decision, DAC voltage
either goes up to $3V_{\text{ref}}/4$ or goes down to $V_{\text{ref}}/4$, and the MSB-1 bit is decided. Similarly, the LSB decision takes place based on the MSB-1 bit.

The most critical block in a SAR ADC is the DAC, because its performance directly impacts the overall linearity (resolution) of the whole system. There are many techniques for building the CMOS DAC, the most popular one being a charge redistribution DAC based on switched capacitor arrays [26]. This technique offers inherent T/H functionality. Also, the capacitors can be very well matched and do not dissipate static power. The most popular implementation for this technique is the capacitive binary-weighted DAC which will be explained in Section 2.3.2. Another implementation is the capacitive C-2C DAC which will be discussed in Section 2.3.3.
2.3.2 Binary-Weighted DAC

Figure 2.5 shows the schematic of a N-bit charge redistribution SAR ADC with the binary-weighted DAC. The capacitors are binary-weighted, and they range from unit capacitance $C$ to $2^{N-1}C$. An additional unit capacitance $C$ near the comparator is added to make the total capacitance equal to $2^NC$. No T/H circuit is needed because the capacitor array in the DAC also performs sampling. Based on the comparator decision, SAR logic controls the switches. The operation of this ADC is explained below:

1. The input voltage is sampled when the bottom plate of all capacitors are connected to $V_{in}$ and switch $S_{reset}$ shorts the top plate of the capacitor array ($V_X$) to ground. The total charge stored in the capacitors is

$$Q_{total} = V_{in} \cdot 2^N \cdot C$$

(2.1)

2. After sampling, switch $S_{reset}$ opens, making node $V_X$ float. Switches for bit 0 to N-2 connects to ground and bit N-1 switches to $V_{ref}$. Since the top plate is floating, there is no current path for the capacitors, and total charge is preserved. After settling, the value of $V_X$ can be solved by writing the charge conservation equation:

$$V_{in} \cdot 2^N \cdot C = (V_{ref} - V_X) \cdot 2^{N-1} \cdot C + (0 - V_X) \cdot (C + C + 2 \cdot C + \cdots + 2^{N-2} \cdot C)$$

(2.2)

Rearranging the equation

$$V_{in} \cdot 2^N \cdot C = V_{ref} \cdot 2^{N-1} \cdot C - V_X \cdot 2^N \cdot C$$

(2.3)
Solving for $V_X$ gives

$$V_X \cdot 2^N \cdot C = V_{\text{ref}} \cdot 2^{N-1} \cdot C - V_{\text{in}} \cdot 2^N \cdot C \Rightarrow V_X = \frac{V_{\text{ref}}}{2} - V_{\text{in}}$$  \hspace{1cm} (2.4)$$

Using the comparator to compare $V_X$ with ground is the same as comparing $V_{\text{in}}$ with $V_{\text{ref}}/2$. Based on the comparator decision, bit N-1 is resolved.

3. If $V_{\text{in}}$ is greater than $V_{\text{ref}}/2$, bit N-2 is switched to $V_{\text{ref}}$, and repeating the same analysis as for bit N-1 by writing the charge equation

$$V_{\text{in}} \cdot 2^N \cdot C = (V_{\text{ref}} - V_X) \cdot 3 \cdot 2^{N-2} \cdot C + (0 - V_X) \cdot 2^{N-2} \cdot C$$  \hspace{1cm} (2.5)$$

and solving for $V_X$ gives

$$V_X \cdot 2^N \cdot C = V_{\text{ref}} \cdot 3 \cdot 2^{N-2} \cdot C - V_{\text{in}} \cdot 2^N \cdot C \Rightarrow V_X = \frac{3V_{\text{ref}}}{4} - V_{\text{in}}$$  \hspace{1cm} (2.6)$$

Similarly, if bit N-1 is 0, it is not hard to show that the new $V_X = V_{\text{ref}}/4 - V_{\text{in}}$.

4. Using the same approach, all bits can be resolved and the conversion is complete.

One advantage of the binary-weighted DAC is that the node $V_X$ is insensitive to parasitic capacitance. If we assume the total parasitic capacitance at node $V_X$ to be $C_P$, and this includes parasitic capacitance from the comparator input and capacitor array top plate, the charge equation after sampling can be rewritten as

$$V_{\text{in}} \cdot 2^N \cdot C = (V_{\text{ref}} - V_X) \cdot 2^{N-1} \cdot C + (0 - V_X) \cdot (2^{N-1} \cdot C + C_P)$$  \hspace{1cm} (2.7)$$

Rearranging the equation gives

$$V_{\text{in}} \cdot 2^N \cdot C = V_{\text{ref}} \cdot 2^{N-1} \cdot C - V_X \cdot (2^N \cdot C + C_P)$$  \hspace{1cm} (2.8)$$

Solving for $V_X$ gives

$$V_X = \left( \frac{V_{\text{ref}}}{2} - V_{\text{in}} \right) \cdot \left( 1 - \frac{C_P}{2^N \cdot C + C_P} \right)$$  \hspace{1cm} (2.9)$$

$V_X$ gets attenuated compared to the case without parasitic capacitance, however that is okay since only sign of $V_X$ matters. It can be shown that the same attenuation applies to $V_X$ for all cycles. The parasitic insensitive feature of the binary-weighted DAC enables it to achieve high resolution.
In addition, the binary-weighted SAR ADC is well suited for sub-100nm CMOS processes. The SAR logic is purely digital, therefore benefits from technology scaling in both power and speed. The comparator speed depends on the transistor unity gain frequency which also benefits from technology scaling. The analog switches get smaller as the channel length shrinks, thus requiring less clocking power to drive. Moreover the capacitor matching gets better thanks to better photolithography.

Binary-weighted SAR ADCs seem like a very attractive option for high-speed communication systems, however it has severe bandwidth and speed limitations [27]. First of all, the DAC size increases exponentially with the number of bits assuming a fixed unit capacitor size. Moreover, during input sampling, the capacitance seen by the input switches is the total capacitance $2^N$ which also scales exponentially with the number of bits. For example, the minimum sized metal insulator metal (MIM) capacitor in the TSMC 65nm GP kit has 10fF capacitance, and for a resolution of 8 bits, the total capacitance is 2.56pF. And to achieve a input sampling bandwidth of 5GHz for 10Gb/s applications, the input sampling switch needs to have a resistance of 12.4 $\Omega$, which is very hard to build. And this even ignores any interconnect and termination resistances. Also the buffer driving this capacitance will burn a lot of power. Assuming a class-A buffer is used, and it shouldn’t slew at the input frequency of 5GHz, thus the bias current is given by

$$\frac{I_{bias}}{C_{load}} \geq \text{Amplitude} \cdot 2 \cdot \pi \cdot 5G$$  \hspace{1cm} (2.10)

Assuming the input peak to peak voltage is half VDD, the amplitude becomes $1/4 \ V$ for VDD = 1V, and the bias current is calculated to be 20mA, which is very likely larger than the total power consumption of the SAR ADC. Note that it is possible to design custom unit capacitors as small as 50aF [28], however this requires accurate knowledge and confidence in the process technology and/or fabrication and measurement of test structures, and capacitor mismatch becomes a problem.

### 2.3.3 C-2C DAC

An alternative to the binary-weighted capacitive DAC is the C-2C DAC for a SAR ADC [29–31]. The C-2C DAC is similar to the widely known R-2R DAC and the schematic of a N-bit charge redistribution SAR ADC with C-2C DAC is shown in Figure 2.6. There are only two capacitance sizes C and 2C. The series and parallel capacitors make the equivalent capacitance looking to the left always constant. The capacitor C on the leftmost of the array is there to properly terminate the network. The operation of this architecture is explained below:

1. The input voltage is sampled when the bottom plate of all capacitors are connected to $V_{in}$
and switch $S_{\text{reset}}$ shorts ($V_X$) to ground. Right now, the voltage at $V_X$ is 0.

2. Switch $S_{\text{reset}}$ opens and all the bottom plate connects to ground. The voltage at $V_X$ is now $-V_{\text{in}}$. Then the bottom plate of bit N-1 is switched to $V_{\text{ref}}$. Now the change in voltage at node $V_X$ is

$$\Delta V_X = (V_{\text{ref}} - 0) \cdot \frac{C}{C + C_{\text{eq1}}}$$

The nature of C-2C DAC makes $C_{\text{eq1}} = C$, resulting in

$$\Delta V_X = \frac{V_{\text{ref}}}{2}$$

Therefore the voltage at $V_X$ becomes $-V_{\text{in}} + V_{\text{ref}}/2$, the same as in the binary-weighted case.

3. For the next comparison, the bottom plate of bit N-2 is switched to $V_{\text{ref}}$, now the change in voltage at node $V_X$ is

$$\Delta V_X = \Delta V_2 \cdot \frac{2C}{2C + C}$$

where node $V_2$ is the capacitor top plate for bit N-2, and it is given by

$$\Delta V_2 = (V_{\text{ref}} - 0) \cdot \frac{C}{C + C_{\text{eq3}} + C_{\text{eq2}}} = \frac{3V_{\text{ref}}}{8}$$
substitute this into equation 2.13 to get

\[
\Delta V_x = \frac{V_{\text{ref}}}{4}
\]  

(2.15)

which is expected.

4. Using the same approach, all bits can be resolved and the conversion is complete.

One advantage of this C-2C DAC is that the DAC size increases linearly with the number of bit, thus it occupies less area compared to the binary-weighted architecture. Also during the sampling phase, the total capacitance seen by the input sampling switch is only 2C, which makes the switch design much easier.

Parasitic capacitance wasn’t a problem for the binary-weighted architecture, but it poses severe performance limitation to the C-2C DAC. Any parasitics on the capacitor top plate will change the capacitor ratio or the radix in the DAC. For example, if there is some parasitic capacitance \( C_P \) at node \( V_2 \), \( C_{eq1} \) becomes bigger than \( C \), causing an error when switching bit \( N-1 \) from 0 to \( V_{\text{ref}} \). Not only is the radix modified, it is different for each bit. This creates a limitation in the achievable resolution if not solved properly. Recent publications proposed calibration schemes either in analog or digital domain to solve this problem [29–32]. However due to the calibration complexity and mediocre performance, C-2C SAR ADCs are still limited to low-medium resolution, which is the main reason why they are not as popular as binary-weighted implementation, despite their potential bandwidth and speed advantages.
Chapter 3

System and Circuit Design

3.1 System Overview

An ADC for 10Gb/s wireline communication systems would have a sampling rate of 10GS/s. As stated in Section 2.1, for such a high-speed ADC, only a time-interleaved architecture is possible because one channel ADCs are too power inefficient. Therefore, a time-interleaved ADC is chosen as the starting point for the design.

Secondly, the ADC resolution is chosen to be 8 bits. Normally, there are three types of nonidealities that limit an ADC’s effective resolution. First, thermal noise, which is not likely a problem for a medium resolution converter accepting several hundred millivolt input amplitude. Second is nonlinearity due to mismatch, either within a sub-ADC or between different sub-ADCs which we assume will be ameliorated through careful design and calibrations. Finally, performance degradations can be caused by clock jitter [33]. Sampling time uncertainty causes a voltage noise that’s proportional to the input frequency and amplitude, and the maximum achievable signal-to-noise ratio (SNR) for a given random clock jitter standard deviation $\Delta t$ and input frequency $f_{in}$ is

$$\text{SNR}_{\text{max}} = -20\log_{10}(2\pi f_{in}\Delta t)$$  \hspace{1cm} (3.1)

And the effective number of bits (ENOB) can be related to SNR using the equation

$$\text{ENOB} \equiv \frac{\text{SNR}(\text{dB}) - 1.76}{6.02}.$$  \hspace{1cm} (3.2)

By making $f_{in} = 5\text{GHz}$, which is the Nyquist frequency for a 10GS/s ADC, ENOB vs clock jitter plot is generated as shown in Figure 3.1. A good on-chip clock generator will achieve 200 fs$_{\text{rms}}$ jitter, which corresponds to 7 ENOB. To make sure the system isn’t quantization noise limited, 8 bit is chosen for the time-interleaved ADC.


Figure 3.1: ENOB versus clock RMS jitter for a sinusoid with 5GHz input frequency.

Table 3.1: Design specification of the 1.25GS/s time-interleaved C-2C SAR ADC

<table>
<thead>
<tr>
<th>Sampling Rate</th>
<th>1.25GS/s</th>
<th>Preferred Bandwidth</th>
<th>5GHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>8 bit</td>
<td>Process</td>
<td>CMOS 65nm GP</td>
</tr>
<tr>
<td>Supply</td>
<td>1V</td>
<td>Power</td>
<td>&lt;40mW</td>
</tr>
</tbody>
</table>

For the sub-ADC topology, a SAR architecture is chosen since it offers the best combination of power and speed for converters with an effective resolution of approximately 7 bits. For the capacitive DAC implementation, the C-2C architecture is chosen over binary-weighted because of its superior bandwidth and speed, at the expense of higher distortion caused by parasitic capacitances. Roughly 80 time-interleaved SAR ADCs are required to achieve a total sampling rate of 10GS/s. If classical time-interleaving methodology is used, it would create a severe bandwidth limitation on the input due to interconnect parasitic capacitances. Also timing mismatch calibration will be difficult. Therefore a two-level time-interleaving architecture is proposed [18–20]. Instead of interleaving all 80 SAR ADCs in one hierarchy, they will be divided into 8 sub-ADCs each running at 1.25GS/s. Each sub-ADC further time interleaves 10 SAR ADCs running at 125MS/s each. The system block diagram is shown in Figure 3.2.

This thesis focuses on the design of the 1.25GS/s time-interleaved SAR sub-ADC. The design specification of the sub-ADC is shown in Table 3.1. Note that this sub-ADC is essentially a sub-sampling ADC where the maximum input frequency is 8 times its Nyquist frequency.

\footnote{Another student collaborated with me to integrate 8 sub-ADCs into a high-speed time-interleaved 8-bit ADC [34].}
Figure 3.2: Top level block diagram of the proposed 10GS/s 8-bit two-level time-interleaved ADC.
3.2 Architecture of the Individual C-2C SAR ADC

The schematic of the differential C-2C SAR ADC is shown in Figure 3.3. The differential inputs $V_{\text{inp}}$ and $V_{\text{inn}}$ are sampled by two bootstrapped switches. Bootstrapping is necessary for input switches to eliminate any signal dependent distortions caused by nonlinear switch resistance and signal dependent sampling instant. Switch charge injection is not a problem because with bootstrapping, $V_{\text{GS}}$ of the switches are constant, therefore leading to a constant charge injection voltage error which is canceled differentially. Input switch hold mode feedthrough is compensated by adding two dummy switches. Positive reference voltage $V_{\text{refp}}$ and negative reference voltage $V_{\text{refn}}$ define the ADC dynamic range, with $V_{\text{cm}}$ being the common mode voltage. The differential capacitor arrays contain switches at the bottom plate that connect to one of $V_{\text{refp}}$, $V_{\text{refn}}$ or $V_{\text{cm}}$. Note that these switches are not bootstrapped because they connect to DC voltages, which have deterministic charge injection that are canceled differentially. The SAR logic controls 21 switches (3/bit * 7 bit) on each side, and the decision is based on the preceding comparator output.

The unit capacitor $C$ is $40\text{fF}$, and $2C$ is $80\text{fF}$. The capacitance is chosen based on four factors: mismatch, parasitic capacitances, thermal noise, and input sampler bandwidth. First of
Table 3.2: Parasitic capacitance for different unit MIM capacitance values

<table>
<thead>
<tr>
<th>Unit MIM capacitance (fF)</th>
<th>20</th>
<th>40</th>
<th>80</th>
</tr>
</thead>
<tbody>
<tr>
<td>Top plate parasitic capacitance (fF)</td>
<td>0.48</td>
<td>0.64</td>
<td>0.93</td>
</tr>
<tr>
<td>Bottom plate parasitic capacitance (fF)</td>
<td>1.13</td>
<td>1.38</td>
<td>1.71</td>
</tr>
</tbody>
</table>

all, capacitor mismatch is inversely proportional to square root of the capacitor area. Therefore as unit capacitance gets smaller, mismatch gets worse which affects the DAC linearity. Second, the design rule requires a minimum extension distance for metal contacts connected to the MIM cap plates. And as the capacitor area gets smaller, the ratio of the parasitic capacitance to the actual capacitance gets bigger due to the overhead imposed by the design rule. The top and bottom plate parasitic capacitances for different unit MIM capacitance values are shown in Table 3.2. Moreover, for the C-2C SAR architecture, the input sampling capacitance is 2C, which leads to a differential thermal noise of $kT/C$. The thermal noise caused by the sampling capacitor, in addition to the comparator noise and the front-end time-interleaved sampler need to better than 8-bit resolution. The first three factors set a lower bound on the unit capacitance. For a fixed bandwidth and reasonable input switch size, the RC time constant sets the upper bound on the unit capacitance.

One difference of this differential implementation from the single ended implementation discussed in Section 2.3.3 is that the first comparison is free and there is no guessing needed. In the single-ended case, after the input is sampled, the MSB switch is connected to $V_{\text{ref}}$ for the DAC to generate the voltage $V_{\text{ref}}/2$ to compare with the input. If the input is less than $V_{\text{ref}}/2$, the MSB needs to switch back to ground. To know what the MSB value is, it has to be guessed first. The same also applies to all other bits including the LSB. Therefore for a 8-bit SAR ADC, the DAC also has to be 8-bit. For the differential implementation, since it is a signed ADC, the MSB can be determined by comparing the two differential inputs, and consequently the MSB-1 bit is determined by switching MSB, and the LSB is determined by switching LSB+1. Therefore the DAC does not need to use the LSB value, and it can be made 1 bit less than the ADC resolution. This is extremely advantageous to the binary-weighted architecture because 1 less bit halves the DAC size. Also since there is no guessing, the reference voltage power consumption is lower.

Normally for ADCs, bottom plate sampling is used to reduce signal dependent distortions. However for the C-2C SAR ADC discussed here, top plate sampling is used for three reasons. First, during sampling, top plates are connected to the input and bottom plates are connected to $V_{\text{cm}}$. When evaluating MSB, the input switches are open and the bottom plates are still connected to $V_{\text{cm}}$. Therefore the first comparison is free in the sense that no reference voltages need to be switched which saves power. Second, for the top plate sampling case, only one
3.3 Operation of the Individual C-2C SAR ADC

The operation of the proposed C-2C SAR ADC is explained below. For simplicity, assume \( V_{\text{refp}} = V_{\text{ref}}, V_{\text{refn}} = 0, \) and \( V_{\text{cm}} = V_{\text{ref}}/2. \)

1. Figure 3.4 shows the schematic during sampling phase. The differential input \( V_{\text{inp}} \) and \( V_{\text{inn}} \) are connected to nodes \( V_{\text{xp}} \) and \( V_{\text{xn}} \) through bootstrapped switches. The capacitor array bottom plates are connected to the common mode voltage \( V_{\text{ref}}/2. \)

2. The MSB evaluation phase is shown in Figure 3.5. The input bootstrapped switches are open and the bottom plates are still connected to \( V_{\text{ref}}/2. \) The voltage at nodes \( V_{\text{xp}} \) and
Figure 3.5: C-2C SAR ADC schematic during MSB evaluation.

\[ V_{xn} \text{ are unchanged and the differential input to the comparator is} \]

\[ V_{xp} - V_{xn} = V_{inp} - V_{inn} = V_{in,diff} \]  \hspace{1cm} (3.3)

Therefore the differential voltage \( V_{in,diff} \) is compared with 0 to evaluate the MSB value. Note that the full scale range for the differential input is from \(-V_{ref}\) to \(V_{ref}\).

3. Assume that \( V_{in,diff} > 0 \) and the MSB is 1. Knowing that \( V_{in,diff} \) is between 0 and \( V_{ref} \), the next step would be to compare it with \( V_{ref}/2 \), and the DAC configuration is shown in Figure 3.6. Bit 7 of the bottom capacitor array is connected to \( V_{ref} \) and bit 7 of the top capacitor array is connected to ground. Following the same procedure as the single-ended case discussed in Section 2.3.3 results in

\[ V_{xp} = V_{inp} + \Delta V_{xp} = V_{inp} + (0 - V_{ref}/2) \cdot \frac{C}{C+C} = V_{inp} - V_{ref}/4 \]  \hspace{1cm} (3.4)

and

\[ V_{xn} = V_{inn} + \Delta V_{xn} = V_{inn} + (V_{ref} - V_{ref}/2) \cdot \frac{C}{C+C} = V_{inn} + V_{ref}/4 \]  \hspace{1cm} (3.5)
Therefore the differential input to the comparator is
\[ V_{xp} - V_{xn} = (V_{inp} - V_{ref}/4) - (V_{inn} + V_{ref}/4) = V_{in,diff} - V_{ref}/2 \]  
(3.6)

which is expected.

4. Assume that \( V_{in,diff} < V_{ref}/2 \) and the MSB-1 is 0. Knowing that \( V_{in,diff} \) is between 0 and \( V_{ref}/2 \), the next step would be to compare it with \( V_{ref}/4 \), and the DAC configuration is shown in Figure 3.7. Bit 6 of the bottom capacitor array is connected to ground and bit 6 of the top capacitor array is connected to \( V_{ref} \). This results in

\[ V_{xp} = V_{inp} - V_{ref}/4 + \Delta V_{xp} = V_{inp} - V_{ref}/4 + V_{ref}/8 = V_{inp} - V_{ref}/8 \]  
(3.7)

and

\[ V_{xn} = V_{inn} + V_{ref}/4 + \Delta V_{xn} = V_{inn} + V_{ref}/4 - V_{ref}/8 = V_{inn} + V_{ref}/8 \]  
(3.8)

Note that some steps are skipped because the same analysis had been done in Section
2.3.3. The differential input to the comparator becomes

\[ V_{xp} - V_{xn} = (V_{inp} - V_{ref}/8) - (V_{inn} + V_{ref}/8) = V_{in,diff} - V_{ref}/4 \]  \hspace{1cm} (3.9)

which is expected.

5. Using the same approach, all bits can be resolved and the conversion is complete.

The C-2C SAR ADC takes 10 clock cycles to perform one conversion. Cycle 1 is dedicated to sampling of the input, cycles 2-9 are used to resolve 1 bit per cycle for a total of 8 bits, and cycle 10 latches the 8-bit ADC output. Since each SAR ADC has a sampling rate of 125MS/s and takes 10 cycles to finish, each cycle has 800ps, and the clock frequency is 1.25GHz. Each clock cycle has to tolerate the worst case loop delay, which is consisted of comparator resolving time, DAC settling time, and digital delay. The timing budget is shown in Figure 3.8. The digital logic clock clk\textsubscript{logic} and the comparator clock clk\textsubscript{cmp} are 400ps apart, which makes them complementary.
3.4 Switch Design

Even though a N-channel MOSFET (NMOS) switch is an attractive option for building the input switch, it suffers from voltage dependent resistance which makes the switch linearity a function of the input amplitude and the input common mode voltage [35]. A bootstrapped NMOS switch is implemented to improve resistor linearity by applying a constant $V_{GS}$ and it is shown in Figure 3.9 [36].

The clock multiplier is on the left side, it is consisted of M1, M2, C1, and C2. The complementary clock signals Clk and Clkb have a swing of 0 to Vdd, and the capacitors C1 and C2 are charged by M1 and M2 to have a voltage drop of Vdd. Therefore the gates of M1 and M2 swing from Vdd to 2Vdd, which is enough to open and close the NMOS switch M3. In the off state, M8 and M9 short the gate of the sampling switch M12 to ground to turn off the switch. M3 and M10 are used to charge capacitor C3 to have a voltage of Vdd. In the on state, M3 and M10 are shut off, and the capacitor C3 is applied directly across $V_{in}$ and $V_G$ of the sampling switch M12 by turning on transistors M7 and M11. Therefore the $V_{GS}$ of the sampling switch is the voltage of C3, which is charged to be Vdd. Since some node voltages exceed the supply voltage Vdd, this circuit is designed so no terminal-to-terminal voltage exceeds Vdd. Transistor M8 is cascaded with M9 to make sure the $V_{DS}$ of M9 is less than Vdd, and transistor M6 is included to make sure $V_{SG}$ of M7 does not exceed Vdd.

Ideally during the on state, the $V_{GS}$ of the sampling switch is Vdd, however any parasitic capacitances at the gate of M12 will attenuate that voltage. Assume the total parasitic capacitances at gate of M12 is $C_P$, we have the charge conservation equation

$$C_3 \cdot V_{dd} = C_3 \cdot (V_{G,M12} - V_{in}) + C_P \cdot V_{G,M12}$$ (3.10)
Figure 3.9: Schematic of the bootstrapped switch.
Figure 3.10: Switch resistance comparison between transmission gate and bootstrapping.

Rearranging the equation,

\[ V_{G,M12} = \frac{C_3}{C_3 + C_P} \cdot V_{dd} + \frac{C}{C_3 + C_P} \cdot V_{in} \]  \hspace{1cm} (3.11)

resulting in

\[ V_{GS,M12} = V_{G,M12} - V_{in} = \frac{C_3}{C_3 + C_P} \cdot V_{dd} - \frac{C}{C_3 + C_P} \cdot V_{in} \]  \hspace{1cm} (3.12)

The sampling switch \( V_{GS} \) is attenuated by a factor of \( C_3/(C_3+C_P) \) from \( V_{dd} \), it also has a loss term that’s proportional to the input voltage \( V_{in} \). Therefore it is better to have a large capacitor \( C_3 \) to minimize attenuation, however any parasitic capacitances of the bottom plate of an over-sized \( C_3 \) will directly load the input \( V_{in} \).

The switch resistance of the bootstrapped NMOS switch and a transmission gate is compared in Figure 3.10 over interested voltage range from 400mV to 900mV. Transmission gate is sized larger than the bootstrapped switch to have comparable resistance. It can be seen that the bootstrapped switch has a much linear resistance, and its increase in resistance at higher input voltage is due to parasitic capacitances as described in equation 3.12.

Bootstrapped switch is used for the input voltage, the other three reference voltages \( V_{refp} \), \( V_{refn} \), and \( V_{cm} \) all use simple NMOS or PMOS switches and the summary is shown in Table 3.3
Chapter 3. System and Circuit Design

Table 3.3: Switch design summary

<table>
<thead>
<tr>
<th>Type</th>
<th>Size</th>
<th>Voltage Range (mV)</th>
<th>Resistance (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{refp}$</td>
<td>PMOS</td>
<td>4 · 800n/60n</td>
<td>900</td>
</tr>
<tr>
<td>$V_{cm}$</td>
<td>PMOS</td>
<td>8 · 800n/60n</td>
<td>650</td>
</tr>
<tr>
<td>$V_{refn}$</td>
<td>NMOS</td>
<td>4 · 800n/60n</td>
<td>400</td>
</tr>
<tr>
<td>$V_{in}$</td>
<td>Bootstrapped NMOS</td>
<td>8 · 800n/60n</td>
<td>400 - 900</td>
</tr>
</tbody>
</table>

3.5 Comparator Design

The comparator is consisted of a pre-amplifier and a double-tail latch [37] and it is shown in Figure 3.11. The pre-amplifier draws 160μA and it has a DC gain of 3.3 and bandwidth of 3.6GHz at nominal condition. There are several advantages of using pre-amplification. First, the pre-amplifier reduces the input referred offset and thermal noise of the comparator. Second, it provides some common mode rejection of the input signal. Moreover, kickback noise of the latch is attenuated because the pre-amplifier is in the middle. The speed (metastability) of the comparator might be improved, assuming the pre-amplifier has enough bandwidth.

The double-tail latch [37] uses one tail for the input stage and another tail for latching. With this setup, three transistors are stacked instead of four in the conventional case, which is ideal for low supply voltage. In the reset phase, Clk is low and Clkb is high, therefore M5 is off to disable the bottom tail, and M16 is off to disable to the top tail. M8 and M9 charge the output of the bottom tail to Vdd, and M10 and M11 are turned on to discharge the output of the cross-coupled pair to ground. In the latch phase, Clk is high, and Clkb is low, the output of the bottom tail starts to drop from Vdd, with a rate of I/C. The imbalanced voltage at the gates of M10 and M11 will tilt the cross-coupled inverters formed by M12-M15, and the output is regenerated. The regenerative latch can be modeled as a cross-coupled negative gm block as shown in Figure 3.12, and the differential output voltage $V_d = V_1 - V_2$ is dependent on the initial condition $V_{d0} = V_{10} - V_{20}$ and the time $t$ given by

$$V_d = V_{d0} \cdot e^{t/\tau}$$  

where $\tau = C/g_m$. The comparator in the SAR ADC needs to resolve the output to full digital levels within time $T$, factoring in the pre-amplifier gain $A$, the minimum comparator input voltage is

$$V_{in,min} = \frac{V_{dd}}{A} \cdot e^{-T/\tau}$$  

And the comparator will be metastable if the input is smaller than $V_{in,min}$. Metastability is very bad for wireline communication systems because it will very likely lead to a bit error,
Figure 3.11: Schematic of the comparator that consists of a pre-amplifier followed by a double-tail latch.

Figure 3.12: Block diagram of cross-coupled inverters.
which increase the bit error rate (BER) of the system. In each conversion, the comparator will have one input less than \(1/2 \cdot \text{LSB}\), and assume that voltage magnitude is uniformly distributed between 0 and \(1/2 \cdot \text{LSB}\), the metastable probability is

\[
P(\text{metastable}) = \frac{V_{\text{in, min}}}{V_{\text{LSB}}/2} = \frac{V_{\text{dd}}/A \cdot e^{T/\tau}}{V_{\text{FS}}/2^{N+1}}
\]

(3.15)

where \(V_{\text{FS}}\) is the full scale input, and \(N\) is the number of bit. Plugging in the value \(V_{\text{dd}} = 1V\), \(T = 300\text{ps}\), \(V_{\text{FS}} = 500\text{mV}\), \(N = 8\), probability of a metastable event against time constant is plotted in Figure 3.13. For most wireline communication standards, a BER of \(10^{-12}\) is required, and assuming a metastability event leads to a bit error, it translates to a time constant of 8.4ps. Even though the above analysis ignores delay by pre-amplifier and digital logic after the regenerative latch such as SR latch, it still gives a good guideline to the comparator speed requirement.

Three simulation conditions are used, and the comparator performance is summarized in Table 3.4. Unfortunately the BER at SS corner and 0 degrees is higher than \(1e-12\). However there isn’t much room for improvement as the latch time constant simply depends on process parameter \(C/g_m\). The comparator resolving time can be increased if this becomes a problem.
Table 3.4: Comparator performance summary

<table>
<thead>
<tr>
<th>Simulation Corner</th>
<th>TT</th>
<th>FF</th>
<th>SS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature (Celsius)</td>
<td>27</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Pre-amp Gain (dB)</td>
<td>10.4</td>
<td>9.8</td>
<td>11.3</td>
</tr>
<tr>
<td>Pre-amp BW (GHz)</td>
<td>3.6</td>
<td>4.4</td>
<td>3</td>
</tr>
<tr>
<td>Latch time constant (ps)</td>
<td>8.1</td>
<td>6.8</td>
<td>10.9</td>
</tr>
<tr>
<td>BER</td>
<td>2.6e-14</td>
<td>2.1e-17</td>
<td>3.5e-10</td>
</tr>
<tr>
<td>Input Referred Noise (mV$_{\text{rms}}$)</td>
<td>0.9</td>
<td>0.9</td>
<td>0.8</td>
</tr>
<tr>
<td>Input Referred Offset (mV$_{\text{rms}}$)</td>
<td>7.4</td>
<td>7.4</td>
<td>7.2</td>
</tr>
</tbody>
</table>

The maximum input referred noise of the comparator is 0.9mV$_{\text{rms}}$, with a differential input amplitude of 500mV, the resulting SNR is

$$\text{SNR}_{\text{dB}}(\text{comparator}) = 10 \cdot \log \frac{0.5 \cdot (500\text{mV})^2}{(0.9\text{mV}_{\text{rms}})^2} = 51.9\text{dB}$$

which is below the quantization noise level. Unlike higher resolution ADCs such as delta-sigma and pipeline converters, a high-speed 8-bit SAR ADC is usually not thermal noise limited because of its lower resolution.

### 3.6 Time-Interleaving Architecture

The time-interleaved ADC uses 10 C-2C SAR ADCs to achieve an overall sampling rate of 1.25GS/s as shown in Figure 3.14. A front-end sampler is used, and it consists of a differential bootstrapped switch followed by a differential PMOS source follower. A 10 to 1 multiplexer is used to combine the ADC digital outputs from all 10 SAR ADCs. There are several advantages of using the front-end sampler. First, the buffer decouples the load of individual SAR ADCs from the input, thus improving the overall input bandwidth. Second, the front-end sampler outputs discrete time signal from subsampling a continuous time high frequency signal, therefore simplifying the switch design in individual SAR ADCs. Moreover, the true sampling for all 10 SAR ADCs is done by the front-end sampler, therefore there is minimal timing and bandwidth mismatch.

Since the input is sampled twice, first by the front-end sampler, then by the individual SAR ADC, kT/C thermal noise is doubled as well. With a front-end sampling capacitance of 100fF
and SAR sampling capacitance of 80fF, the resulting SNR is

$$\text{SNR}_{\text{dB}}(\text{sampling cap}) = 10 \cdot \log \frac{0.5 \cdot (500\text{mV})^2}{(kT/100\text{fF} + kT/80\text{fF}) \cdot 2} = 58.3\text{dB} \quad (3.17)$$

which is well below the quantization noise level.

The timing diagram of the time-interleaved SAR ADC is shown in Figure 3.15. The cycle numbers for all SAR ADCs are shown over time. Since 10 SAR ADCs are time-interleaved, and each SAR ADC requires 10 cycles to finish one conversion, in each cycle, there is exactly one SAR ADC in the sampling phase, and one SAR ADC outputing the result. This makes clock generation straightforward as a only a single 1.25GHz clock is needed for the whole time-interleaved ADC. Different reset conditions are provided for each SAR ADC to make sure they all start on a different cycle.

The sampler timing diagram is shown in Figure 3.16. The front-end sampler operates on a 1.25GHz sampling clock, which dedicates 400ps to track mode and 400ps to hold mode. The input samplers for individual SAR ADC are enabled one entire cycle every 10 cycles. It is important that the sampling instant which is the transition from track mode to hold mode for SAR ADC happens while the front-end sampler is in the hold phase. Hold mode is overlapped by 100ps as a safety margin over process and temperature variations. It is not necessary to generate non-overlap clocks to make sure two SAR samplers are not enabled at the same time, because it is faster to turn off a bootstrapped switch than to turn it on, which effective results in non-overlapping sampling even if the input clock to bootstrapped switches overlap due to
mismatch.

One disadvantage of using the front-end sampler is the difficulty in designing a high bandwidth and high linearity buffer. A simple PMOS source follower is used to achieve high bandwidth as shown in Figure 3.17. The input PMOS transistor M3 has its source and body shorted to eliminate any body effect. The total power consumption of the single-ended buffer is 2.4mW, which is comparable to the total power consumption of a SAR ADC. Also, it’s worth noting that with double sampling, the $kT/C$ noise adds up, but it’s fine in this case as the ADC is not thermal noise limited.

### 3.7 Calibration

As mentioned in Section 2.2, calibrations are needed for time-interleaved ADC to eliminate any performance degradations due to channel mismatch. Calibrations are performed individually for each SAR ADC and they are implemented off-chip. A sinusoid input with an arbitrary frequency is required for all calibrations. Offset calibration is carried out by first calculating the running mean of the ADC output and adjust the output digitally by removing the DC offset. Gain calibration is performed by detecting the output amplitude and add a multiplication factor such that all ADCs have the same amplitude. Bandwidth and timing mismatch calibrations are not needed because all SAR ADCs share the same front-end sampler.

The major disadvantage of the C-2C SAR ADC is that the linearity degrades heavily from

---

**Figure 3.15:** Timing diagram of the time-interleaved SAR ADC with cycle numbers.
Figure 3.16: Detailed timing diagram of the front-end sampler and the input samplers in each SAR ADC.

Figure 3.17: Schematic of the PMOS source follower buffer, with 2.4mW power consumption.
parasitic capacitances. Therefore radix calibration is used as shown in Figure 3.18 [29]. The ADC output is best fitted to a sinusoid signal, and a least mean squares (LMS) algorithm is performed to adjust the radix or weight of each bit such that the error is minimized.
Chapter 4

Experimental Results

The proposed time-interleaved C-2C SAR ADC was implemented in TSMC 65nm 1P9M GP process. This chapter covers the test setup and measurements results of the time-interleaved SAR ADC.

4.1 Test Setup

This section presents the detailed test setup of the prototype. The test setup consists of the prototype, the printed circuit board (PCB), external equipments used to supply differential input and clock signals, and a computer that retrieves the ADC digital output and performs calibrations.

4.1.1 Prototype

The prototype time-interleaved SAR ADC has an active area of 0.2mm$^2$. The die photo of the prototype is shown in Figure 4.1. The die was packaged in a QFN48 package.

4.1.2 Printed Circuit Board

A printed circuit board (PCB) was designed and fabricated to test the prototype. It provides supply voltages, reference voltages, common-mode voltage to differential input data and clock, and bias currents. The decimated ADC digital output is acquired by the FIFO. The microcontroller reads the FIFO content and transfers them to the PC via USB interface. A picture and block diagram of the PCB is shown in Figures 4.2 and 4.3 respectively. Note that the red microcontroller board is mounted on the right side of the PCB board via headers to avoid the use
Figure 4.1: A die photo of the implemented time-interleaved C-2C SAR ADC.

Figure 4.2: Populated PCB photograph.
Chapter 4. Experimental Results

Figure 4.3: PCB block diagram.

Table 4.1: List of key components on the PCB

<table>
<thead>
<tr>
<th>Item</th>
<th>Manufacturer</th>
<th>Part number</th>
<th>Part description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Microcontroller</td>
<td>Atmel</td>
<td>ATmega2560</td>
<td>8-bit microcontroller</td>
</tr>
<tr>
<td>Regulators</td>
<td>Linear Technology</td>
<td>LT3060ETS8</td>
<td>Linear voltage regulator</td>
</tr>
<tr>
<td></td>
<td>Analog Devices</td>
<td>ADP1715</td>
<td>Linear voltage regulator</td>
</tr>
<tr>
<td>Voltage reference</td>
<td>Linear Technology</td>
<td>LT1807CS8</td>
<td>Opamp</td>
</tr>
<tr>
<td>FIFO</td>
<td>Texas Instruments</td>
<td>SN74V293-7PZA</td>
<td>FIFO with 64K x 18 memory</td>
</tr>
<tr>
<td>Bias T</td>
<td>Mini-Circuits</td>
<td>TCBT-14+</td>
<td>Wideband bias tee</td>
</tr>
</tbody>
</table>

of ribbon cables. All the key components on the PCB are tabulated in Table 4.1. The PCB occupies an area of 291 mm x 97 mm.

4.1.3 Equipment Setup

External equipment was used to provide DC power, differential input data and clock, and communication to the PCB via USB interface. The computer sends configuration data to the PCB and receives the prototype digital outputs from the PCB. For the clock single-ended to differential conversion, a 4.0-8GHz 3dB hybrid coupler is used. For the data single-ended to differential conversion, a wideband balun board is used for frequency lower than 500MHz and a 180° hybrid coupler is used for frequency higher than 500MHz. HP 83712B signal generator is used as the data source for its large frequency range and high linearity. Centellax clock
synthesizer is used to provide a low jitter clock. A picture and block diagram of the equipment setup is shown in Figures 4.4 and 4.5 respectively. All equipment details are tabulated in Table 4.2.

### 4.2 Measurement Results

In this section, the static and dynamic performances of individual SAR ADCs are shown, before and after offset, gain, and radix calibrations. The DNL and INL results, as well as dynamic performance of the time-interleaved ADC are also presented, before and after calibrations. Additionally, the SNDR is shown as a function of input frequency, with calibrated input amplitude
based on channel loss. The SNDR versus input amplitude plot is also shown for low frequency and high frequency input signals. Furthermore, the SNDR is plotted versus sampling frequency, for different supply voltages. Finally, the ADC performance is summarized and compared with other published works. The sampling speed of the time-interleaved ADC is 1.25GS/s, with individual SAR ADC operating at one tenth of the sampling rate which is 125MS/s. Both the unit SAR ADC and the overall time-interleaved SAR ADC performances are measured at this speed unless otherwise stated.

### 4.2.1 Single SAR ADC Performance

The measured offset of 70 SAR ADCs is shown in Figure 4.6. The distribution looks like gaussian which is expected. The offset in mV is calculated by multiplying the offset in LSB by mV/LSB. There is a deterministic offset of 11.3mV, which might be caused by the mismatch in the input network, which is common to all SAR ADCs. The offset standard deviation is 10.9mV, which the majority is caused by the comparator, which is simulated to be 7.4mV\text{rms}.

The measured amplitude of 70 SAR ADCs is shown in Figure 4.7. The amplitude in dB is calculated based on the ADC full scale. The mean amplitude is -0.73 dBFS with a standard deviation of 0.14dB. The amplitude mismatch is mainly caused by the DC gain mismatch of the PMOS source follower amplifiers, because the mean amplitude standard deviation of individual
SAR ADCs sharing the same PMOS source follower amplifier is only 0.04dB.

By decimating the full rate output by a factor of 81, the FIFO with a memory depth of 64K stores output data from all 80 SAR ADCs, which means the maximum number of samples per individual SAR ADC is 819, which is not sufficient to measure INL and DNL with the histogram test. Therefore only SNDR results are shown for individual SAR ADCs and INL and DNL measurements are performed for time-interleaved SAR ADC. The measured SNDR of 70 SAR ADCs before and after radix calibration is shown in Figure 4.8. The SNDR improved from an average of 32dB to 38.8dB.

### 4.2.2 Time-Interleaved SAR ADC Performance

The INL and DNL are measured by applying a full scale low frequency sinusoidal input of 92.75MHz and collecting the output histogram. Offset, amplitude and radix calibrations are performed. Figures 4.9a and 4.10a show the DNL and INL, respectively, before the calibration. Figures 4.9b and 4.10b show the DNL and INL, respectively, after the calibration. As seen, the calibration improves DNL from +6.2/-1.0 LSB to +1.9/-1.0 LSB, and INL from +5.6/-7.4 LSB to +2.2/-1.7 LSB. Note that the maximum DNL happens when MSB transitions, which is due to the nature of C-2C DAC architecture of the SAR ADC. Even after calibration, there are two missing codes (DNL = -1) around output code 128.

The measured decimated output spectrum for a 617.75MHz (Nyquist) input is shown in Figure 4.11. Since there is a decimation by factor of 81, the frequency axis of the spectrum
Figure 4.7: Amplitude histogram of 70 individual SAR ADCs. The measurement is conducted with a 92.75MHz sinusoidal input and 500 points are taken per individual SAR ADC.

Figure 4.8: SNDR histogram of 70 individual SAR ADCs before and after radix calibration. The SNDR improved from 32dB to 38.8dB.
Figure 4.9: DNL for time-interleaved SAR ADC with 92.75MHz sinusoidal input before and after calibration. It improved from +6.2/-1.0 LSB to 1.9/-1.0 LSB.
Figure 4.10: INL for time-interleaved SAR ADC with 92.75MHz sinusoidal input before and after calibration. It improved from +5.6/-7.4 LSB to +2.2/-1.7 LSB.
scales down by a factor of 81 as well, however there is no loss of information as signal, harmonic distortions and noise all aliased back in-band. Figure 4.11a shows the decimated output spectrum before gain, offset and radix calibrations. At this point, the third harmonic denoted by the cross, caused by nonlinearities in the C-2C DAC, and the five spurs denoted by the diamonds, caused by gain mismatch between different SAR ADCs are limiting the overall time-interleaved ADC performance. Spurs caused by gain mismatch are denoted by circles, and they are not significant compared to the previous two nonidealities. When calibration is turned on, the spurs mentioned before all drop below -60dBc as shown in Figure 4.11b, and the SNDR and SFDR improves by 10.8dB and 17.7dB respectively.

The measured SNDR and SFDR after calibration are plotted versus input frequency up to 4GHz in Figure 4.12a. The SNDR is 39.4dB or 6.25 effective number of bits (ENOB) at low frequency, 37.9dB or 6 ENOB at Nyquist frequency, and the effective resolution bandwidth (ERBW) is 1GHz, which is larger than Nyquist frequency. At 4GHz input frequency, which is more than 6 times the Nyquist frequency, the SNDR is 34dB or 5.36 ENOB. The ENOB is calculated using the equation

$$\text{ENOB} = \frac{\text{SNDR}(\text{dB}) - 1.76}{6.02}.$$  \hspace{1cm} (4.1)

Note that in the above measurement, the signal amplitude is adjusted for each input frequency such that the ADC output amplitude is always around -1dBFS, and channel loss versus input frequency is shown in Figure 4.12b. This channel loss includes loss from bias tees, PCB trace, bond wires, on-chip transmission line and H-bridge distribution network.

The measured SNDR after calibration is plotted versus input amplitude with respect to full scale for 93MHz and 4GHz input in Figure 4.13. As seen, the SNDR increases linearly with amplitude for low frequency input which proves good linearity of the converter. For 4GHz input, the SNDR flattens near full scale which is likely caused by timing jitter. The total jitter is estimated to be 540 ps\text{rms}, which consists of the simulated 450 ps\text{rms} from the on-chip clock generator and the measured 300 ps\text{rms} from the reference clock. The noise contributed by jitter is calculated to be -37dBc, and the point denoted by x in Figure 4.13 is the SNDR for 4GHz input by removing performance degradation caused by jitter. It can be seen that now SNDR increases almost linearly for 4GHz input as well.

Figure 4.14 shows the SNDR versus sampling frequency with 100MHz input for different supply voltages. Note that the nominal supply voltage is 1.0V and the sampling speed is 1.25GS/s. The SNDR is independent of sampling frequency until the cycle time gets too short and the SAR ADC starts to make mistakes on some cycles. The ADC can operate up to 1.55GS/s for 1.1V supply and 1.7GS/s for 1.2V supply without performance degradations.
Figure 4.11: Measured decimated output spectrum (5000 points) of the time-interleaved ADC with a Nyquist frequency input before and after calibration. SNDR improved from 27.1dB to 37.9dB.
Figure 4.12: Measured SNDR and SFDR, and channel loss versus input frequency up to 4GHz
Figure 4.13: SNDR versus input amplitude with 93MHz and 4GHz input frequencies.

Figure 4.14: SNDR versus sampling frequency for 1.0V, 1.1V and 1.2V supply voltages with an input frequency around 100MHz.
Figure 4.15 shows the power consumption versus the sampling frequency. The time-interleaved ADC consumes 34.2mW at 1.25GS/s and the static power is 14mW based on extrapolation. The CML-based clock generation and buffers, and the input PMOS source follower buffers contribute to majority of the static power. The power breakdown for a single ADC and the time-interleaved ADC is shown in Table 4.3. A single SAR ADC consumes 2.3mW, 25% comes from the analog blocks mainly by the comparator whereas 75% is consumed by the digital blocks. This is primarily because the digital blocks have custom logics optimized for maximum speed and these custom designs are power hungry. Note that the voltage reference power is only 0.05mW per SAR ADC because there is no on-chip active reference buffer, instead passive decoupling capacitors around 3pF per reference supply per SAR ADC are used to stabilize the reference voltage. The overall ADC consumes 34.2mW, 67% comes from 10 SAR ADCs, 14% is consumed by the input buffer, and the rest is mainly dissipated by clocking.

4.2.3 Performance Summary and Comparison

The ADC performance is summarized in Table 4.4. The main characteristics of this ADC is that it is implemented in TSMC65nm GP process, runs with 1.0V supply, and has a sampling rate of 1.25GS/s. It has an input full scale range of 1.0V_{pp} differential and the power consumption is 34.2mW. The SNDR is 34dB even at 4GHz input, which is more than 6 times the Nyquist
Table 4.3: Power consumption distribution of a single SAR ADC and the time-interleaved SAR ADC

<table>
<thead>
<tr>
<th>Single ADC power consumption (Total = 2.3mW)</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Comparator and analog blocks 0.53mW</td>
<td>23%</td>
</tr>
<tr>
<td>Digital logic 1.72mW</td>
<td>75%</td>
</tr>
<tr>
<td>Voltage reference 0.05mW</td>
<td>2%</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Overall ADC power consumption (Total = 34.2mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 SAR ADCs 23mW</td>
</tr>
<tr>
<td>Input buffer 4.7mW</td>
</tr>
<tr>
<td>Clock generation and buffer + peripheral blocks 6.5mW</td>
</tr>
</tbody>
</table>

The Walden figure-of-merit (FOM) is calculated with equation

\[
FOM \equiv \frac{\text{Power}}{f_s \times 2^{\text{ENOB}}}
\]  

(4.2)

And it is 360fJ/conv-step and 428fJ/conv-step for low and Nyquist input frequencies respectively.

Table 4.5 shows the comparison of this work with other published time-interleaved C-2C SAR ADCs. It can be seen that this work has the best SNDR even though it doesn’t have the best FOM or sampling rate. It is also interesting to compare this work with other recently published >10GS/s ADC, this work is denoted with a black star as shown in Figure 4.16. Even though time-interleaving eight 1.25GS/s ADC will have performance degradation due to timing and bandwidth mismatch, and the ADC only works well up to 4GHz input, it is good to know that this work’s performance is comparable to other published ADCs.
Table 4.4: Performance summary of the prototype ADC

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>TSMC 65nm 1P9M GP</td>
</tr>
<tr>
<td>Active area</td>
<td>0.2mm²</td>
</tr>
<tr>
<td>Resolution</td>
<td>8 bits</td>
</tr>
<tr>
<td>Sample rate</td>
<td>1.25GS/s</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>1.0V</td>
</tr>
<tr>
<td>$V_{\text{ref, max}}$</td>
<td>900mV</td>
</tr>
<tr>
<td>$V_{\text{ref, min}}$</td>
<td>400mV</td>
</tr>
<tr>
<td>Input range</td>
<td>1.0V&lt;sub&gt;pp&lt;/sub&gt; differential</td>
</tr>
<tr>
<td>Power consumption</td>
<td>34.2mW</td>
</tr>
<tr>
<td>DNL</td>
<td>+1.9/-1.0</td>
</tr>
<tr>
<td>INL</td>
<td>+2.2/-1.7</td>
</tr>
<tr>
<td>$f_{\text{in}} = 93\text{MHz}$</td>
<td>$f_{\text{in}} = 617\text{MHz}$</td>
</tr>
<tr>
<td>SNDR</td>
<td>39.4dB</td>
</tr>
<tr>
<td>ENOB</td>
<td>6.25 bits</td>
</tr>
<tr>
<td>FOM</td>
<td>360fJ/conv-step</td>
</tr>
</tbody>
</table>

Table 4.5: ADC performance comparison with other published works

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>[29]</td>
<td>6</td>
<td>0.6</td>
<td>5.3</td>
<td>34</td>
<td>220</td>
<td>0.13μm</td>
</tr>
<tr>
<td>[30]</td>
<td>6</td>
<td>1</td>
<td>6.27</td>
<td>31.5</td>
<td>210</td>
<td>65nm</td>
</tr>
<tr>
<td>[31]</td>
<td>7</td>
<td>2.5</td>
<td>50</td>
<td>34</td>
<td>480</td>
<td>45nm</td>
</tr>
<tr>
<td>This work</td>
<td>8</td>
<td>1.25</td>
<td>34.2</td>
<td>37.9</td>
<td>428</td>
<td>65nm</td>
</tr>
</tbody>
</table>
Figure 4.16: Comparison with recent high-speed CMOS ADCs faster than or equal to 10GS/s, this work is denoted with a black star.
Chapter 5

Conclusion

5.1 Summary

Recently, wireline communication systems start to favour ADC-based receivers with digital backend that enable implementation of more sophisticated algorithms that offer potentially higher performance. The ADC design is the bottleneck, which needs to have a speed of 10GS/s and low-medium resolution. This thesis proposed a two-level time-interleaving architecture for realizing such an ADC, and presented the design, implementation and measurement of the 1.25GS/s 8-bit sub-ADC. A SAR topology is used for its digital friendly nature and bandwidth enhancement is enabled by using the C-2C capacitive DAC architecture. The test-chip was fabricated in 65nm CMOS technology to validate the design. The time-interleaved C-2C SAR ADC operates on a 1.0V supply and consumes 34mW. The DNL is 1.9/-1.0 LSB and the INL is 2.2/-1.7 LSB. The SNDR is 39.4dB at low frequency, 37.9dB at Nyquist frequency, and 34dB at 4GHz. The Walden FOM is 428fF/conv-step at Nyquist frequency.

5.2 Future Work

The time-interleaved C-2C SAR ADC measurement results show poor performance over 4GHz input frequency. The input passive network might be the reason and it should be investigated. The digital SAR logic consumes a majority of the ADC power consumption as shown in Table 4.3. Redesign of the digital logic which focuses on power efficiency could significantly reduce the dynamic power dissipation. Also digital logic efficiency benefits from technology scaling.

Moreover, smaller custom capacitors can be designed to reduce area and parasitic capacitances. With a smaller sized unit capacitor, binary-weighted DAC architecture could be ex-
explored to achieve higher linearity and avoid radix calibrations.

Finally, the speed of individual SAR ADCs can be increased by using techniques such as asynchronous logic and 2-bit/cycle. Synchronous SAR converters like the one used in this thesis rely on a high-speed clock to divide the conversion phase into equally timed slots. Even though an individual SAR ADC operates at 125MS/s, it requires a clock frequency of 1.25GHz. Whereas for asynchronous SAR converters [12, 29, 30], the comparison from MSB to LSB is triggered like dominoes by the asynchronous logic, and only a low frequency clock equal to the sampling rate is needed to start each conversion. In addition to the reduced clocking power due to lower clock frequencies, asynchronous SAR ADCs are able to allocate different comparator resolving time for each cycle, which theoretically could reduce the total comparator resolving time by up to 50% [29]. Moreover, instead of resolving only 1 bit per cycle, two additional comparators can be added to achieve 2-bit/cycle [38], [39]. This technique almost doubles the sampling rate of the SAR converter, however many errors sources such as mismatches between comparators, and the signal dependent errors such as comparator kickback noise make it difficult to achieve high resolution.
Bibliography


