Practical Volume-Reduction Strategies for Low-Power High-Frequency Switch Mode Power Supplies

by

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A thesis submitted in conformity with the requirements for the degree of Doctor of Philosophy

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The miniaturization of dc–dc switch-mode power supplies (SMPS) is of a key importance in volume-sensitive portable devices, such as cell phones, tablet computers, and digital cameras. In these systems, multiple SMPS are required to provide well regulated voltage and power to various electronic components such as the central processing unit (CPU) and random-access memory (RAM). The combined volume, weight, and surface area footprint of these SMPS is usually the largest component.

Traditionally, SMPS volume reduction has been achieved through increased switching frequencies; however, for power-sensitive applications this is undesirable due to the increased switching losses. This thesis presents two alternative, power-efficient, SMPS miniaturization methods: one control and one topology based.

The presented controller recovers from load transients with virtually minimum possible output voltage deviation, reducing the reactive component size. The controller utilizes a simple algorithm, requiring no knowledge of the converter parameters and virtually no processing
power. The simplicity of the control concept enabled the design of an area and power efficient integrated circuit (IC) implementation.

The entire IC is implemented in a CMOS 0.18μm process on a 0.26 mm² silicon area, which is comparable to the state-of-the-art analog solutions. For the experimental system the deviation (output capacitor size) is about four times smaller than that of a fast PID compensator having a 1/10th of the switching frequency bandwidth.

The second solution is a complementary converter topology that has a smaller output filter volume, improved dynamic response, and lower switching losses compared to the state-of-the-art solutions. To reduce the volume and switching losses, the input-to-output voltage difference is decreased with a capacitive attenuator that replaces the input filter capacitor and has approximately the same volume. Both the attenuator and the downstream buck converter share the same set of switches, minimizing conduction losses. A single multi-mode digital controller governs operation of both stages, seamlessly regulating the output and input center-tap voltages. Experiments with a 5–1.5-V, 2.5-A, 1-MHz prototype show that, compared to the conventional buck, the merged topology has 43% smaller inductor, 36% smaller output capacitor, up to 30% lower power losses, and a 25% faster transient response.
ACKNOWLEDGMENTS

I offer my deepest thanks to the faculty, staff and fellow students at the University of Toronto, without whom many of the ideas presented in this thesis would have never been developed. Financial support from the Energy System Department and the Ontario Graduate Scholarship program are gratefully acknowledged.

I owe particular thanks to Prof. Aleksandar Prodić for his wise advice, direction and financial support. He consistently went beyond the ‘call-of-duty’ of a supervisor, and for that I am deeply grateful. I appreciate the thoughtful feedback from my supervisory committee members Prof. Peter Lehn and Prof. Joseph Tate. I am also thankful for the feedback from Prof. Reza Iravani and Prof. Francisco J. Azcondo Sánchez during the final oral examination.

I thank Robert de Nie, from NXP Semiconductors, for his mentor-ship and wise advice. I am grateful to Dr. Zdravko Lukić for his invaluable help during our many IC design projects. My thanks also go out to all of my lab colleagues (SM Ahsanuzzaman, Amir Parayandeh, Behzad Mahdavikhah, Massimo Tarulli, Jurgen Alico, SC Huerta, Adrian Straka and Mor Peretz) who made the entire experience an enjoyable one.
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<td>BCMCA</td>
<td>Buck Converter with Merged Capacitive Attenuator</td>
</tr>
<tr>
<td>CPM</td>
<td>Current Programmed-Mode</td>
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<tr>
<td>CPU</td>
<td>Central Processing Unit</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital-to-Analog Converter</td>
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<tr>
<td>DPWM</td>
<td>Digital Pulse-Width Modulator</td>
</tr>
<tr>
<td>EMI</td>
<td>Electro-magnetic Interference</td>
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<tr>
<td>ESR</td>
<td>Equivalent Series Resistance</td>
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<td>HDL</td>
<td>Hardware Description Language</td>
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<td>NLC</td>
<td>Non-Linear Control</td>
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<td>PID</td>
<td>Proportional-Integral-Derivative</td>
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<tr>
<td>PWM</td>
<td>Pulse Width Modulation</td>
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<td>RAM</td>
<td>Random Access Memory</td>
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<td>SAR</td>
<td>Successive Approximation Register</td>
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SMPS Switch-Mode Power Supplies
Chapter 1

Introduction

Modern consumer electronics rely on multiple distributed dc-dc power supplies to provide regulated power to one or more functional blocks for proper operation [1, 2]. While functionally adequate, the state-of-the-art power supply solutions consume significant area, weight, and volume, and contribute to the overall cost of the price-sensitive electronic devices [3, 4]. The extent of the problem can be fully appreciated by, for example, examining a typical mobile device, a 2012 Microsoft Surface Tablet motherboard, shown in Fig. 1.

Figure 1. Microsoft Surface Tablet motherboard with the power supplies shaded in red. [4]

The power supply components, shaded in red in Fig. 1, take up 17% of the surface area; more than the central processing unit (CPU) and random access memory (RAM) combined. In addition, the SMPS inductive components introduce a height constraint, 7 mm [87], which limits the overall device thickness and volume (thickness of the tablet is 9mm). Furthermore, the power supplies contribute 10% of the price of the motherboard [4], and are among the largest contributors to the overall weight of the device. From these values, it is clear that the
miniaturization of the power supplies reactive components can result in a significant reduction of the overall cost and size of portable applications.

In order to achieve practical SMPS miniaturization, the tight regulation of the supply voltages cannot be affected [1]. Also, a relatively in-expensive and power efficient topology and controller implementation are required. To this end, two blocks have been helpful in effectively meeting these constraints while achieving meaningful volume reduction: switch-mode power conversion and negative-feedback control.

1.1 Switch-Mode Power Conversion

Before the emergence of the switch-mode power conversion concept, linear voltage regulators (LVR) dominated dc-dc power conversion applications. However, due to the inherently poor power processing efficiency of LVR, high current and large voltage conversion ratio solutions were impractical [5, 6].

The switch-mode power conversion process, shown in Fig. 2, overcame LVRs poor power processing efficiency through the replacement of the lossy resistor with a low-loss switching network and low-pass filter.
Figure 2. Switch-mode power conversion principle of operation (feedback controller not shown).

The switching network is utilized to generate a pulsed voltage waveform, denoted \( v_x \) in Fig. 2, with an average voltage value equal to the product of the input voltage, \( v_{in} \), and a controllable duty ratio value, \( d \). The \( v_x \) averaged value is extracted by the low-pass filter, generating a dc output voltage, \( v_{out} = dv_{in} \), where \( v_{in} \) is the input voltage. In such a manner, a desired input-to-output voltage conversion ratio can be achieved using power efficient switching and reactive components.

The following subsection is devoted to further discussion of duty ratio control.

1.2 Negative-Feedback Control

Negative-feedback control is one of the fundamental concepts of any modern power conversion system. It facilitates robust regulation of one or more system variables, usually the output voltage, using its measurement and comparison to a desired reference value [7]. As a result, system disturbances and system uncertainties are effectively dealt with and the desired operating conditions maintained. A top-level diagram of a typical SMPS system utilizing negative-feedback control is shown in Fig. 3.

![Diagram of a dc-dc converter](image)

Figure 3. Negative feedback control of a dc-dc converter.
The output voltage is measured and compared to a reference voltage, $v_{\text{ref}}$, yielding the error signal, $e$. Depending on the error value the controller generates a pulse-width modulated control signal, $c$, modifying the switch network on/off positions. The speed and accuracy of the controller in large part determines the required volume of the capacitive components, i.e. their energy requirements [7]. The next two subsections discuss the small-signal compensator, most commonly used in current SMPS and the advanced large-signal compensators. The following sections also explain the role of compensators in minimizing the passive component size requirements and address the advantages and drawbacks of those systems.

1.2.1 Small-Signal Control

Small-signal modeling, usually used in conventional designs, is based on the assumption that the system variable and control signal changes are small and gradual [7]. This approximation simplifies modeling and compensator design. It also allows closed-form stability analysis, in spite of the non-linear and time-variant nature of SMPS converters. Because of these advantages, small-signal control is used almost exclusively in commonly used controller solutions, such as the one shown in Fig. 1.

The main drawback of the small-signal controllers, whose typical top-level diagram is shown in Fig. 4, is the limited bandwidth of the feedback loop. The bandwidth is limited to nearly one order of magnitude less than the switching frequency [9], resulting in oversized reactive components [7]. In essence, the ease of controller design is traded-off for the size of converter reactive components.
The previous discussion indicates that practical SMPS miniaturization using small-signal control is limited by the unfavorable coupling between switching frequency and reactive component size.

1.2.2 Large-Signal Control

Large-signal control [10, 11, 12] relies on *non-linear control actions* to minimize system delays, such as the one switching cycle delay, and/or to maximize the dynamics of system variable changes. As a result, the energy storage requirements of the SMPS reactive components can be reduced [10].

A typical digital large-signal controller system is shown in Fig. 5. Compared to the small-signal controller of Fig. 4, the large-signal controller is usually more challenging to implement due to the relatively high complexity of its control laws and hardware requirements.

For digital controller implementations, the increased requirements are due to the need for a high-speed high-resolution analog-to-digital converter (ADC) and a powerful processing unit. [11, 12]. These ADC specifications translate into significant increased power and silicon area consumption demands [11, 12] and make potential integrated circuit (IC) implementations difficult, if not impractical.
Furthermore, the non-linear compensator control laws are usually composed of a set of division, multiplication and square root functions [10], requiring relatively powerful processing units and silicon area requirements.

In order to make the large-signal controllers practical, the ADC and non-linear compensator, i.e. processing unit, require simplification. Once these problems are resolved, the fundamental limits of control-based SMPS miniaturization can be reached, and any further SMPS volume reductions can only be achieved through topological modifications.

The following subsection addresses the topology-based limitations related to the inductor current and capacitor voltage slew-rates. The most popular step-down converter topology, the buck converter, is analyzed and its theoretical limits defined. Furthermore, potential strategies for further improvement are described.

1.3 SMPS Topology Limits

The reactive components of the buck converter, shown in Fig. 6, are usually chosen to limit the output voltage ripple, $\Delta v_{out}$, and inductor steady-state current ripple, $I_{ripple}$, under all operating conditions. As such, it is useful to define the reactive components in terms of these two constraints and operating conditions.
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Given these constraints, the minimum inductance value is equal to [7]

$$L = \frac{1}{2I_{\text{ripple}}} \cdot V_{\text{out}} (1 - \frac{V_{\text{out}}}{V_{\text{in}}}) \cdot \frac{1}{f_{\text{sw}}},$$  \hspace{1cm} (1)

where $V_{\text{out}}$ is the output voltage, $V_{\text{in}}$ is the input voltage, and $f_{\text{sw}}$ is the converter steady-state switching frequency. While the minimum capacitance value is equal to [7]

$$C = \frac{I_{\text{load}}^2}{2V_{\text{ripple}}} \cdot \frac{1}{V_{\text{out}}} \cdot L,$$  \hspace{1cm} (2)

where $I_{\text{load}}$ is the maximum output load current.

From (1) and (2) it can be seen that the reactive component values (size) can be reduced by increasing the switching frequency or reducing the input-to-output voltage ratio. The first option, on which most traditional methods for minimization are based, introduces increased switching losses and is limited by semiconductor process capabilities. The reduction of the input-to-output voltage ratio does not suffer from these two limitations and a minimization method based on the principle is presented in this thesis.
1.4 Thesis Objectives

The main thesis objective is to reduce the overall volume of SMPS, by reducing the reactive components size. This goal is achieved using a two-step process: development of a practical integrated circuit large-signal mixed-signal controller and a topology modification. This general goal is achieved by:

- Addressing the shortcomings of state-of-the-art large-signal controllers through development of hardware-efficient solutions for
  - fast and accurate detection of load transients
  - accurate detection of peak/valley points
  - smooth mode transition between linear and non-linear modes of operation
- Introducing topology modifications which reduce the input-to-output voltage difference, further minimizing the reactive component energy storage requirements.

1.5 Thesis Outline

The organization of this thesis is as follows:

Chapter 2 reviews the existing analog and digital controller architectures, as well as the state-of-the-art topological modifications which are utilized to minimize SMPS reactive component size. Special attention is given to the potential areas of improvement for each solution.

Chapter 3 presents the first major thesis contribution: a hardware efficient minimum-deviation response controller IC. The control concept is presented in a comparative manner, illustrating the reduced sensitivity and low-hardware complexity of the new method. Furthermore, a power and silicon size efficient ADC architecture is presented and its IC implementation described. Experimental results are provided, showing minimum-deviation response for a wide range of operating-conditions.
Chapter 4 presents the second major thesis contribution: a merged capacitive-attenuator topology. The fundamental concept is described and the reactive component reduction characterized for a wide range of operating conditions. A practical implementation, utilizing a unified control loop and minimal external components, is also described. Experimental results showing reduced reactive component size, improved power processing efficiency, and faster transient response, are also shown.

Chapter 5 concludes the thesis, reviewing the main results and suggests future research topics.
Chapter 2

Previous Art and Motivations

The literature review is organized in three main sections and follows the thesis objective. The first two sections review the state-of-the-art analog and digital control architectures. The advantages and shortcomings are described in detail; laying a foundation for the proposed mixed-signal solution. The third subsection reviews various reduced input-to-output voltage ratio topologies, specifically illustrating areas for improvement.

2.1 Analog Control

Conventional commercial SMPS ICs most frequently utilize analog voltage [13-15] or current-mode controllers [16-18]. In large part, the predominance of analog solutions is due to their low power consumption and hardware simplicity. The two major drawbacks of these solutions are i) relatively low loop bandwidth due to component variations resulting from external influences (temperature, humidity and aging) and ii) nontransferable IC design [19, 20].

2.1.1 Voltage-Mode PWM

A constant-frequency voltage-mode controller [13-15], shown in Fig. 7, utilizes a linear PID compensator to provide accurate output voltage regulation and system robustness over a wide range of operating conditions. To obtain relatively fast dynamic response and, consequently, small output voltage deviations a high bandwidth control loop is usually designed. However, since the validity of the averaged converter models used in compensator designs is constrained to frequencies significantly lower than the switching frequency [7], the bandwidth of the feedback loop is limited. As discussed previously, this limitation results in oversized reactive components and is a major disadvantage of the voltage-mode PWM control.
The high bandwidth control loop can be implemented using a small number of components and is made up of two main building blocks, the PID compensator and the pulse-width modulator (PWM). The PID compensator is implemented using only one high-bandwidth operational amplifier, two impedance elements and a voltage reference generator. The PWM requires only one high-speed comparator and a saw-tooth voltage waveform generator.

As mentioned previously, this controller can be implemented with a small numbers of components but it needs to be redesigned each time semiconductor process changes. This increases the time to market and the product development cost. Furthermore, the advance in semiconductor technology is accompanied with lower voltage rating of components, imposing novel design challenges in the analog domain. Those include reduction of operational amplifier and comparator dynamic range, input common-mode range, signal-to-noise ratio attenuation and various other issues [21].

Figure 7. Top-level diagram of an analog voltage-mode PWM controller.
2.1.2 Current Programmed Control

A constant-frequency current programmed-mode (CPM) controller [16-18], shown in Fig. 8, is a useful and widely used control method in applications requiring over-current protection.

![Diagram of Current Programmed Control](image)

Figure 8. Current programmed control of a buck converter.

The main disadvantage of the CPM is the need for inductor current measurement or estimation. This usually requires the inclusion of a lossy current-sensor and power hungry high-bandwidth amplifier in the power path for best performance. While it is possible to estimate the inductor current using a lossless RC circuit [22], inherent estimation errors limit the achievable loop bandwidth. Furthermore, for operation of converters with duty ratio values greater than 0.5, an additional stabilizing ramp is required in order to maintain system stability [7]. In addition, CPM
control does not eliminate the significant delays associated with the switching period. As such, the worst case response of the controller to voltage disturbances is defined by this delay, and is an inherent drawback of fixed switching frequency controllers.

2.1.3 Ripple-Based Control

A ripple-based analog controller [23-25], whose general structure is shown in Fig. 9, builds upon the CPM control concept, by operating at a variable switching frequency. As a result, control delays are minimized resulting in faster control actions, reducing reactive component energy requirements.

![Ripple-based control of a buck converter.](image)

Figure 9. Ripple-based control of a buck converter.

However, for noise-sensitive applications (the targeted low-power devices) the variable steady-state switching frequency can cause unacceptable electromagnetic interference (EMI). To offset the EMI problems, the introduction of an additional frequency stabilizing loop (controls $v_{band}$) is required [24, 25], coincidently increasing system complexity and/or resulting in slower transient
response. Furthermore, in these systems, great care is required to mitigate stability problems, such as jitter, high noise sensitivity, and fast-scale instability [24]. Also, during load transients the switching components and the inductor are often exposed to currents significantly larger than the nominal [25]. As a consequence, an overdesign of the power stage is usually required.

2.2 Digital Control

While analog control can tightly regulate the output voltage using a hardware efficient implementation, great care and expertise are required for its proper integration using a low-voltage process. The capacitive and resistive elements, required for the compensator feedback system consume significant silicon area and do not follow process scaling [19, 20]. Furthermore, parameter matching becomes more difficult with each iterative process, i.e. IC technology, requiring reduction of the loop bandwidth. As a result, time-consuming design work is required for each specific process implementation.

Digital control overcomes these difficulties by allowing the design to be performed at a higher-level. The digital portion of integrated circuit can be synthesized automatically using a hardware description language (HDL) based design. This design is easily transferable from one process to another, meaning that an identical HDL design can be integrated in any process technology with a general digital toolkit [19].

Furthermore, digital implementations scale down with process more efficiently than the analog implementations. An added advantage of a higher-level design procedure is the ability to implement advanced control laws. As a result, improvements in transient response, health monitoring, process identification, and power processing efficiency [20] are made possible.

One of the main difficulties with digital control implementations arises from the analog-to-digital interface. The analog voltages and currents of interest (output voltage, inductor current, etc) first need to be digitized using analog-to-digital converters (ADC), before they can be processed and control signals calculated. As a result, significantly larger controller power budget and silicon size are required, compared to analog solutions. These issues are further addressed in the next three subsections.
The first subsection reviews a state-of-the-art digital voltage-mode PWM controller, discussing each component in detail, and where applicable, comparing to the analog counter-part. The second sub-section describes an oversampled dual-mode digital controller with improved output voltage regulation compared to the state-of-the-art analog solutions. Finally, in the last subsection, the dual-mode time-optimal digital control concept, in ideal case achieving the fastest possible transient response is illustrated. The main drawbacks of the time-optimal controller are analyzed in terms of the practical implementation difficulties, and the crucial areas needing improvements identified. These improvements are the main topic of the first part of this thesis.

2.2.1 Voltage-Mode Digital PWM Controller

The digital and analog voltage-mode PWM controllers share the same block-level structure. Both
\( i) \) measure the output voltage with respect to a reference value; \( ii) \) based on the resulting error calculate a duty ratio control value for each switching period, using a compensator, and \( iii) \) generate main switch and synchronous switch control signals using a PWM and dead-time generator. The differences arise in the implementations of the functional blocks and are reviewed in detail in the next three subsections.
2.2.1.1 Analog-to-Digital Converter

As can be seen from Fig. 10, the first component of a digital controller is an ADC. Its task is to digitize an analog voltage waveform, with a sufficient resolution and speed to maintain loop stability and tight output voltage regulation [8, 26]. The resolution is usually selected such that the zero-error bin is less than 0.5% of the reference voltage [1]. For the targeted IC applications, it is highly desirable that the ADC digitizes the output voltage while consuming minimal power and silicon area. This is necessary in order to be competitive with the analog implementations.

The rest of this subsection is solely devoted to the critical analysis of the three main ADC architectures utilized by digital controllers today: i) flash, ii) delay-line and iii) successive-approximation register (SAR) architectures. It will be shown that they are not well suited for the targeted application space and that an alternative hybrid structure is required.
2.2.1.1.1 Flash ADC

The flash ADC architecture (general structure shown in Fig. 11) is able to digitize a wide range of analog signals with the highest resolution and sampling rate among the three architectures [27, 28]. In order to achieve high performance, significant silicon area and power are required. To generate an $N$-bit digital error value, $2^N-1$ comparators are needed, where $N$ is chosen to achieve a given resolution/range. As a result, when implemented on silicon for a wide range application, (for example 7-bit resolution), the area consumption can reach 0.5 mm$^2$ [11, 12]. This area is comparable to the size of an entire analog controller [28-33], and is a major deterrent for the use of flash ADCs in low-power price sensitive IC controller solutions with wide and high resolution voltage and or current digitization requirements.

![Flash ADC architecture top-level diagram.](image)

Figure 11. Flash ADC architecture top-level diagram.

2.2.1.1.2 Delay-Line ADC

The delay-line based ADC architecture [34] (general structure shown in Fig. 12) is a hardware efficient alternative to the flash ADC. It utilizes a reference and measurement voltage-controlled delay-lines. The ADC measures the propagation time of a clock pulse for each voltage controlled
delay time; calculates the time difference; and \textit{iii}) decodes this time value into a digital representation of the error signal. An important benefit of the design is the lack of true analog components, like a differential amplifier, simplifying the implementation for low-voltage applications [35].

Figure 12. Delay-line ADC architecture top-level diagram showing the reference delay-line bank and the measurement delay-line bank feeding into a snapshot register and error decoder.

The range of the ADC is dependant on the number of delay-lines while the resolution is dependant on their propagation times. Improvement of either of these metrics requires additional delay-lines, negatively affecting component matching and linearity of the decoded error signal. As a result, a high linearity delay-line ADC can only be designed with either \textit{i}) a relatively slow sampling rate and high-resolution/wide range or \textit{ii}) a fast sampling rate and low-resolution/low range. The first design optimization is well suited for small-signal based digital controller applications (voltage-mode PWM); however, for applications where both high sampling rate and resolution are required (ripple-based control), the large quantization errors may result in stability problems [26]. For such applications the SAR ADC is a more appropriate choice and is reviewed in the next subsection.
2.2.1.1.3 SAR ADC

The SAR ADC architecture [27], whose general structure and typical operating waveforms are shown in Fig. 13, is a hybrid structure closely resembling a merged voltage-based (flash) and time-based (delay-line) ADC. The SAR block iteratively estimates the digital equivalent value, $v_{out^*}[n]$ using a feedback loop to generate subsequent estimates. The analog-to-digital conversion is reduced to an ordered array search problem [36].

![SAR ADC Architecture](image)

Figure 13. Successive approximation register (SAR) ADC architecture top-level diagram (right) and typical waveforms during operation (left).

The feedback loop is implemented using an $N$-bit DAC, which generates an analog representation of the digital estimate $v_{out^*}(t)$, and a single comparator. Based on the feedback comparator output, $cmp$, and prediction algorithm, i.e. quick search [36], a subsequent estimation is made. In this way, after $N$ estimation steps a digital value with $N$-bit accuracy is achieved [27, 36, 37]. As such, the achievable sampling rate is limited by this multi-step estimation procedure, making the SAR ADC suitable for applications requiring high resolution and moderate sampling rates.
2.2.1.2 PID Compensator

The digital PID compensator block, shown in Fig. 10, generates the PWM duty-ratio control signal, \(d[n]\), based on the previous duty-ratio and error signal values. The relationship can be given by the difference equation

\[
d[n] = a_1d[n-1] + a_2d[n-2] + \ldots + b_1e[n] + b_2e[n-2] + \ldots
\]  

(3)

The coefficients \(\{a_i, b_i\}\) are determined using well known digital compensation design principles [8, 9], ensuring satisfactory phase margin, disturbance rejection, and loop bandwidth.

A hardware and power efficient LUT-based implementation of a modified Eq. 3 is shown in Fig. 14. The all-digital implementation eliminates the resistive and/or capacitive elements found in the analog counterpart, resulting in smaller parameter variations [9].

![Diagram](image)

Figure 14. LUT based PID implementation.

Using the structure of Fig. 14 it is possible to calculate the duty-ratio with a small delay, making it attractive for high switching frequency applications. In addition, the number of toggling gates is minimized compared to a multiplication-based PID, maintaining low dynamic power losses.
2.2.1.3 Digital Pulse Width Modulator (DPWM)

The basic digital pulse width modulator [38], whose structure and main waveforms are shown in Fig. 15, only differs from the analog PWM counter-part in the implementation of the ramp signal. While an analog generator is usually constructed with a dc current source, switch network and a small capacitor [39], the digital ramp generator is implemented with a counter.

![](image)

**Figure 15. Conventional N-bit DPWM architecture.**

The resolution of the counter limits the output voltage regulation. The resolution needs to be sufficiently high not to cause output voltage limit-cycle oscillations (LCO) [38].

Under certain conditions, the DPWM resolution required for LCO-free operation can be significant, in ns range [40], requiring a fast system clock (GHz range) causing large power losses.

An addition of a 2nd-order sigma delta front-end [40], as shown in Fig. 16, effectively reduces the core DPWM clk frequency requirement for a given DPWM resolution, allowing for ultra high frequency operation within acceptable power budgets.
From the previous analysis, it can be seen that effective state-of-the-art solutions for the digital voltage-mode PWM controller blocks exist. In many instances the digital implementations are superior to the analog counter-parts, providing ease of implementation, low parameter variation sensitivity, and superior process scaling.

The next two subsections review advanced control laws, made possible by the digital design flow.

2.2.2 Oversampled Control

An oversampled digital controller [41], whose top-level structure is shown in Fig. 17, can be utilized to improve the output voltage regulation, and accordingly the reactive components size. By using a variable switching frequency, $f_{sw}$, the controller reaction time can be improved during load transients, while reduced switching losses and low-frequency EMI maintained during steady-state.
Figure 17. Oversampled control of a buck converter.

However, due to the relatively large ADC hardware complexity, required by higher sampling rate, the maximum achievable oversampling frequency is limited. Furthermore, during the oversampled mode of operation, the power processing efficiency of the SMPS is negatively affected. In order to improve the output voltage regulation without increasing the switching losses, the authors of [41] modified the oversampled digital controller, gluing together PWM pulses. This resulted in reduction of the maximum switching frequency by one-half and the output capacitor size by two-times (compared to voltage-mode PID compensator).

It should be noted that this variable frequency controller is not suitable for applications with highly dynamic loads, due to the increased switching losses during load transients. The next subsection is devoted to a class of advanced digital controllers, which do not suffer from this limitation.
2.2.3 Dual-Mode Optimal Control

Recently emerged dual-mode digital controllers for high-frequency dc-dc converters [11, 12], whose generalized structure is shown in Fig. 18, have created possibilities of superior transient response. They utilize conventional fixed-frequency voltage-mode PID control during steady-state and non-linear control (NLC) during load or input voltage transients.

![Digital dual-mode optimal control of a buck converter](image)

Figure 18. Digital dual-mode optimal control of a buck converter.

Among the most promising examples are time-optimal [10, 11],[42-49] and digital hysteretic [12], [50-55] controllers. For a given power stage, these solutions achieve virtually the fastest possible recovery time and, consequently, the smallest deviation. The reduction in output voltage deviation allows for an equal miniaturization of the output capacitor size.
These advantages are most often demonstrated with large-scale prototypes consisting of discrete components and general-purpose digital logic. However, on-chip implementation of these controllers has not been widely adopted. This is mainly due to the challenges related to the complexity of the hardware needed for their implementation. The controllers require fairly demanding computational algorithms, to calculate the optimum switching sequence, and use complex analog-to-digital converters (ADC) consuming relatively large power and silicon area (flash ADC) [11, 12]. Furthermore, their operation is significantly affected by the imperfections of the converter circuit, i.e. converter losses and parasitic resistances, as well as by the system delays. All of these make the implementation of the on-chip dual-mode optimal controllers challenging and overly expensive for the targeted cost-sensitive applications. A more power efficient ADC and less parameter sensitive NLC are required before the full benefits of the control concepts can be practically implemented. Chapter 3 is devoted to the solutions to these problems.

The next section reviews the state-of-the-art topologies and topological modifications which can be utilized to further reduce the SMPS reactive components size, including inductance elements size, beyond controller improvements.

### 2.3 Topology Variations

After the limits of controller-based volume miniaturization are reached, and increase in switching frequency is unacceptable, further reduction in the components volume can only be achieved through topology modifications. In the following subsections three promising DC-DC step-down topological solutions are reviewed: i) *inductor-less switched-capacitor converter*, ii) *negative input-voltage buck converter* and iii) *three-level buck converter*. The review is used to lay the foundation for a modified three-level buck converter which merges parts of the three solutions and is the second major contribution of this thesis.
2.3.1 Switched-Capacitor Converter

The inductor-less switch-capacitor converters (SCC) [56-61], such as the step-down flying capacitor topology shown in Fig. 19, are interesting alternatives to conventional inductor-based solutions. Compared to a conventional SMPS, the SCC requires smaller reactive components and offers improved efficiency over a certain conversion range [57, 58]. However, the absence of the inductor that stores energy during voltage variations [61] causes voltage regulation difficulties preventing a wider adoption of SCC converters. To tightly regulate the output while maintaining high efficiency over a wide operating range, variable frequency control and/or multiple power stages increasing the system size are proposed in [57].

![Switched-capacitor step-down topology with variable frequency control](image)

Figure 19. Switched-capacitor step-down topology with variable frequency control.

In [62] and [63], a SCC and a buck converter are combined to minimize the size of filtering components without facing the voltage regulation difficulties. In addition to minimizing the buck output filter, lower buck converter switching losses are achieved, due to reduced blocking voltages of the switches [7]. These solutions consist of a straightforward serial connection of an SCC stage and a downstream buck converter that are regulated with two separate controllers.
Besides increasing the controller complexity, those two-stage solutions also introduce a significant number of extra switches in the conduction path compared to the conventional buck. As a result, the overall implementation is comparable in size and power processing efficiency to a standalone singled-stage buck converter solution [62], limiting the wide adoption of the concept.

2.3.2 Negative Input Voltage Buck Converter

SMPS with mismatched positive and negative inductor slew-rates, ie. buck converter, suffer from asymmetrical voltage deviations during load transients [64]. For the targeted application space the maximum voltage deviation usually occurs during heavy-to-light transients, for which the absolute inductor slew-rate is minimum. As a result, topological modifications which increase the negative inductor slew-rate can be utilized to reduce the voltage deviations during heavy-to-light load transients, allowing for a miniaturization of the output capacitor size.

One such modification is shown in Fig. 20 and is based on the principle of variable positive and negative input voltage, allowing for a symmetrical load-transient response [64].

Figure 20. Negative duty-ratio value control of a buck converter.
During heavy-to-light transients the input capacitor $C_{in}$ is flipped, using the $SW_{1,2,3}$ switch network, and connected to the output filter. As a result, during transients the inductor current slew-rate, $\frac{v_{L_{out}}}{L_{out}}$, is increased by a factor $m_i$ resulting in equal reduction of the output voltage deviation or output capacitor size.

$$m_i = \frac{v_{in}}{v_{out}} + 1. \quad (4)$$

However, in order to be able to achieve these gains three additional MOSFETs and gate drivers are required, significantly increasing the hardware complexity. Furthermore, the addition of $SW_3$ MOSFET in the current conduction path results in increased conduction power losses, negatively affecting SMPS power processing efficiency.

It should be noted that the inductor size is unaffected by the proposed topological modification, resulting in modest total SMPS reactive component size reduction. The three-level buck converter, reviewed in the next subsection, can be utilized to minimize the output inductor and capacitor size, making it an attractive topology for the targeted low-power integrated application space.

### 2.3.3 Three-Level Buck Converter

The three-level buck converter [65, 66], shown in Fig. 21, achieves miniaturization of the output filter with the introduction of a voltage attenuating capacitor, $C_x$. The $C_x$ capacitor reduces the input-to-output voltage difference as seen by the output inductor, allowing for a significant reduction of the inductor value and size as discussed in section 1.3.
Figure 21. Three-level buck converter being controlled by basic voltage-mode PID compensator.

The topology is operated such that the voltage across the capacitor $C_x$ is maintained at one-half of the input voltage. As a result, the switching node peak voltage value is reduced by the same amount and the benefits of a reduced inductor input-to-output voltage difference made possible.

The main drawbacks of the proposed converter are the need for two additional MOSFETs, $SW_2$ and $SW_3$, which significantly increase the conduction and switching losses of the converter. Furthermore, due to gate driver circuit imperfections and converter non-linearity an additional control loop is required in order to tightly regulate the $C_x$ voltage, equal to one-half the input voltage [65].

Chapter 4 is devoted to further development of this concept.
Chapter 3

Minimum-Deviation Controller $^{1,2,3}$

Even though the dual-mode control methods described in Section 2 have demonstrated superior performance compared to conventional solutions, they have not been widely adopted due to one or more of the following four problems: i) *Instability caused by transitions between steady state and dynamic modes*, i.e. chattering; ii) *High sensitivity to quantization effects and converter parameter variations*, iii) *Overly complex hardware requiring a large silicon area for implementation*; and iv) *Inability to react to consecutive load steps occurring during the dynamic mode*.

The main goal of this section is to introduce a simple minimum-deviation digital controller IC for single and two-phase dc-dc converters that does not suffer from the previously mentioned drawbacks and can be integrated on-chip with fairly simple hardware.

Similar to solutions presented in [10, 11, 42] the controller IC of Fig. 22 has two distinctive modes of operation. In steady state the IC operates as a conventional constant frequency pulse-width modulated voltage-mode controller. It uses a PID compensator to provide robust operation over a wide range of operating conditions. During transients, the controller provides recovery from load step changes with virtually minimum possible output deviation.

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Figure 22. A dual-phase buck converter regulated by minimum deviation controller IC.

The entire controller is implemented on a silicon area that is comparable to conventional state-of-the-art single-phase solutions [28-33]. The cost-effective IC implementation is obtained by combining new minimum-deviation transient mode control with a novel track-and-hold architecture of the ADC. The minimum-deviation controller utilizes a very simple algorithm that does not require any knowledge of the converter output filter parameters and virtually requires no processing power. It makes use of readily available data from the PID compensator and can be practically implemented through a single binary shifting operation, with no additional calculations. The asynchronous sampling track-and-hold ADC utilizes only four comparators and a low-gain pre-amplifier, to accurately acquire information about the output voltage. The ADC also has a self-calibrating feature that automatically clears any accumulated error during its operation.
Furthermore, the new IC includes two elements for minimizing effects of the converter losses and system delays, allowing this chip to be used with realistic converters. Namely, the IC has a dynamic duty ratio correction block, which compensates for effects of duty ratio variations due to converter losses, and it also incorporates a dual valley/point detection mechanism for reducing the effects of system delays. The controller IC is designed for applications where the frequent load changes occur and the input voltage variations are relatively slow. The targeted applications include point of load supplies and battery powered systems.

The section is organized as follows: In the next section, principles of the controller operation are described. Section 3.1 describes the analog-to-digital converter architecture. In Section 3.2, practical implementation problems related to the mode transitions and fast detection of the transients are addressed. Solutions for the above mentioned problems are also presented. In particular, the operation of the duty ratio correction logic and dual extreme point detection method are described. That section also addresses effects of multiple transients and capacitor equivalent series resistance (ESR) on the controller operation and gives solutions for their minimization. Details of the on-chip implementation and experimental results verifying performance of the new controller IC are given in Section 3.3.

### 3.1 Control Law Principle of Operation

The controller IC of Fig.22 has two modes of operation, named *steady state* and *transient suppression* modes. In steady state, for output voltage variations smaller than a predefined threshold value $v_{th}$, the IC operates as a conventional voltage-mode digital pulse-width modulation regulator. The *self-calibrating track and hold analog-to-digital converter* (ADC) compares the output voltage with a reference $V_{ref}$ and produces a digital equivalent of the error signal $e[n]$. This value is then passed to the *steady-state PID compensator*, i.e. conventional compensator, which calculates an input value for the *digital pulse-width modulator* (DPWM), labeled as $d[n]$. After a load transient is detected the controller enters the *suppression mode*. In this mode, the *inductor current reconstruction logic* reverses effects of the transient and
seamlessly puts the system back into the steady-state mode of operation by only using information about the transient time instant and the steady state duty ratio value before the transient.

The principle of operation of the minimum-deviation controller is explained with the help of diagrams shown in Fig.23, through a comparison with the operation of well-known time-optimal systems [10, 11],[42-49]. For simplicity, an ideal, i.e. lossless low-ESR single-phase power stage is initially considered. Later on, implementations for a two-phase power stage and a realistic lossy converter will be described. The diagrams are also used to address the challenges of practical IC implementation of the conventional time-optimal systems.

Operation of a time-optimal controller for a light-to-heavy load transient (from a load value $I_{load1}$ to $I_{load2}$) is shown in Fig.23. The control is commonly performed with two different functional blocks. Before the transient, i.e. in steady state, the output is usually regulated with a conventional PID compensator. After a voltage drop larger than the threshold value, $v_{thresh1}$ is detected, the transient suppression logic is activated. To eliminate the delay between the load transient instant and activation of the controller (labeled as $t_d$ in Fig.23), the transient logic is activated after a large current in the output capacitor is detected. Such solutions require either a fast current sensor or, as discussed in Subsection 3.3.3, a well-matched RC estimation circuit.
The time-optimal logic usually performs output voltage recovery through a two phase process. In the first phase, i.e. the inductor current ramping phase, it brings the inductor current to the new load value, by keeping the main switch ($SW_1$ of Fig.22) in on state. During the second phase, the suppression logic recovers the lost capacitor charge, $Q$, through a single on-off switching action. This, ideally, results in a seamless transition into the new steady state, where the conventional compensation mode is reactivated. In Fig.23.a the off and on times, calculated during charge recovery phase, are labeled as $t_{on,d}$ and $t_{off,d}$, respectively. These times are usually computed based on the value and/or location of the maximum voltage deviation at the peak or valley point $[10, 11, 42]$, $\Delta v_{peaks}$, and on measurement (or estimation) of the capacitor current during transients $[10, 44, 45]$.

The main challenge in implementing the time-optimal algorithms is related to charge recovery phase. It requires a fairly accurate calculation of the $t_{on,d}$ and $t_{off,d}$ times and timely generation of the switching sequence, to avoid severe mode transition stability problems. As addressed in [10,
11], and shown in the sensitivity analysis of the following sections, even small inaccuracies in the timing sequence cause a large mismatch between the new load and the inductor current values at the end of the recovery phase and undesirable mode toggling.

In the practical sense, the need for an accurate optimal sequence generation transfers into requirements for a fast high-resolution processing unit and, as described in the following section, a very fast and accurate ADC for the output voltage measurement. The time-optimal algorithms often require a processing unit or a large look-up table (LUT), to perform divisions or calculations of square root values, which are fairly demanding tasks [10]. All of these make on-chip implementation of the proposed solutions challenging in the targeted cost-sensitive applications.

To achieve the minimum possible deviation, in the controller of Fig.22 the tasks between the transient suppression logic and the conventional compensator are divided differently compared to the time-optimal solutions. The transient suppression logic, here named inductor current recovery logic, only brings the current to its new steady state and the charge recovery task is passed to a conventional PID compensator. As it will be shown throughout the paper, for realistic systems, this rearrangement drastically decrease computational requirements, as well as complexity of the ADC, allowing cost-effective implementation, at the price of a slight increase of the full-voltage recovery time. By looking at Fig.23 it can be noticed that this increase in the recovery time can actually be beneficial in some cases, since it reduces the peak inductor current value exposing components to a lower stress.

It should be noted that the problem of large current stress in the time-optimal solutions was addressed in [49, 67] and a theoretical solution for current limiting, based on the state-trajectory control was proposed. In [49] the authors performed detailed analysis of the current overshoot problem and stressed its significance in high step-down ratio converters. Also, a multi-pulse solution for limiting the current that does not require knowledge of LC parameters was proposed. However, such a solution assumes that accurate information about instantaneous capacitor current during transients is available and requires a very fast and accurate measurement of the output voltage value during transients. Both of these requirements make the implementation of the previously proposed solution challenging in the targeted applications. As it will be described in the following sections, the minimum-deviation controller introduced here does not require
current sensing and does not use the output voltage deviation value in determining the transient switching sequence.

### 3.1.1 Inductor Current Reconstruction

During transients, the minimum deviation controller performs very simple actions to create an inductor current wave-shape corresponding to that of the new steady state. In this case, an accurate reconstruction of the entire current waveform, i.e. both the dc and ripple components, is very important. This is because, in modern converters, the ripple component can be as large as 40% of the maximum load current value [68, 69] and, consequently, any ripple mismatch can have the same effect as a large load transient.

The operation of the controller during a sudden light-to-heavy load change can be explained by looking at the waveforms of Fig. 24. As soon as the output voltage drop exceeds the threshold value, i.e. a transient is detected, the controller turns on the converter main switch (SW₁ of Fig. 22) causing the inductor current to ramp up. This process continues until the output voltage valley point is detected, by the track-and-hold ADC of Fig. 22. At this point, the initial on-time of the transistor control signal, \(c(t)\), is extended by the time interval

\[
t_{on} = \frac{D \cdot T_{sw}}{2},
\]

followed by a turn off period

\[
t_{off} = (1 - D) \cdot T_{sw},
\]
where $D$ is the steady-state duty ratio value and $T_{sw}$ is the switching period. Figure 24 demonstrates that this switching sequence results in a current waveform practically identical to that of the new steady state. As soon as this current reconstruction period is completed, the PID compensator is reactivated, to perform charge recovery bringing the output voltage to the reference value.

It should be noted that the new operating conditions are well-suited for the PID compensators, since the converter operates close to the steady state, where the small-signal assumption [7] is valid.

![Figure 24. Operation of the large-small signal digital controller during the light-to-heavy load transient with a single-phase buck converter.](image)

Equations (5) and (6) show that the transient suppression can be performed with very simple
hardware, practically requiring no additional calculations or any knowledge of the converter LC parameters. For an ideal, lossless system, the digital equivalent of the duty ratio value $D$ can be obtained by capturing the PID compensator output $d[n]$ prior to the transient. Subsequently, the division by two can be accomplished with virtually no processing power, through a right shift of the captured digital value.

It should also be noted that, unlike time-optimal and digital hysteretic solutions, the transient logic of the minimum deviation controller requires no knowledge of the output voltage value and, thus, has reduced ADC requirements as well.

Operation of the minimum deviation controller during a heavy-to-light load transient is shown in Fig. 25. It is based on the same principle of the inductor current reconstruction and is more straightforward than for the opposite transient. As soon as a transient is detected, i.e. the output voltage exceeds a pre-defined threshold voltage $V_{HiLo}$, the controller turns on $SW_2$ and turns off $SW_1$ (Fig. 22) causing the inductor current to slope down.
Figure 25. Operation of the minimum-deviation digital controller during a heavy-to-light load transient with a single-phase buck converter.

After the inductor current reaches the new load value, i.e. the peak voltage is detected; the transistor off time is extended by the time

\[ t_{\text{off}} = \frac{(1-D)T_{\text{sw}}}{2} \]  

(7)

and, at the end of this interval, the PID compensator is immediately reactivated. As demonstrated in Fig. 25, in this case, a simple extension of the off-interval is sufficient to reconstruct the new steady state current waveform.
3.1.2 Extension to the Two-Phase Interleaved Buck Operation

The minimum deviation controller IC is also designed to regulate the operation of 2-phase interleaved buck converters with identical phases, allowing the power stage rating to be doubled. In the two phase mode the same suppression logic is used, and the current reconstruction algorithm is slightly modified. In steady state, a single PID compensator regulates both phases through pulse-width modulated control signals $c_1(t)$ and $c_2(t)$ (Fig. 22). The current sharing is implemented passively, by issuing the same $d[n]$ value to the both phases, to ensure the highest power processing efficiency [70].

The dual-phase operation of the controller during a transient is illustrated in Fig. 26. In this case, the sum of two phase currents is shaped by the transient suppression logic. The logic creates a sum whose dc and ripple values are identical to the sum of the two phase currents in the new steady state, as shown in Fig. 26.

After the transient is detected, the main switches of both phases are turned on and kept in this state until the sum of the two phase currents becomes equal to the new load value. At this point, to reconstruct the sum, the on-time of the leading phase (known in digital implementations) is extended by $t_{\text{on}}$, defined by (5) and the lagging current is phase shifted, by applying $t_{\text{off}}$ time equal to (6). As shown in Fig. 26, such a simple action results in the desired wave shapes.
Figure 26. Operation of the minimum-deviation controller during the heavy-to-light load transient with a dual-phase buck converter.
3.1.3 Sensitivity Analysis

This subsection explains why the minimum deviation controller is less sensitive to system non-idealities than the time-optimal counterpart. As discussed previously, the time-optimal controllers require either knowledge of the LC parameters \([10, 44, 48, 49]\) and the input voltage value \([10, 43, 47]\) and/or an extremely fast load transient detection circuit \([10, 11]\). Fairly complex multiple calculations steps are also contributing to sensitivity, where each step is a source of potential error in the switching sequence timing.

The following analysis shows how these timing errors affect the output voltage, potentially, causing undesirable mode transitions and stability problems. The worst-case analysis can be performed using the diagrams of Fig. 27, showing a light-to-heavy load transient response in the presence of a delay, for a time-optimal and the minimum-deviation controllers. To simplify the analysis, all timing errors are lumped into a single parameter \(t_{\text{delay}}\), shown in the diagrams. It is also assumed that the total delay in both systems is the same.

Figure 27. Typical light-to-heavy transient of the time-optimal (left) and minimum-deviation (right) controllers illustrating the effects of non-idealities on the voltage overshoot.
The output voltage mismatch due to a delay can be calculated based on the extra capacitor charge, from diagrams in Fig. 27. It can be seen that, for the time-optimal system, the delay results in extra charge $\Delta Q_{to}$, and consequently a voltage mismatch

$$\Delta V_{to} = \frac{\Delta Q_{to}}{C} = \frac{V_{in} - V_{out}}{LC} \cdot t_{delay} \cdot \left( \frac{t_{delay}}{2D} + \frac{t_{on-to}}{D} \right),$$  \hspace{1cm}(8)$$

where $V_{in}$ is the input voltage of the buck converter, $V_{out}$ is its output voltage, and $t_{on-to}$ is the main switch on time during charge recovery phase (Fig. 27).

For the minimum deviation case, the delay results in extra charge $\Delta Q_{md}$ and the output voltage change of

$$\Delta V_{md} = \frac{\Delta Q_{md}}{C} = \frac{V_{in} - V_{out}}{LC} \cdot t_{delay} \cdot \left( \frac{t_{delay}}{2D} + \frac{t_{on-md}}{D} \right),$$  \hspace{1cm}(9)$$

where $t_{on-md} = DT_{sw}/2$.

By comparing the principles of operation of both systems and looking at (5) and (6), it can be noticed that $t_{on1}$ is significantly larger than $t_{on2}$ causing a larger absolute voltage. It should also be noticed that, for $\Delta V_{md}$ smaller than the deviation at the valley point $\Delta V_{vp}$, the time delay actually brings the voltage closer to the desired reference, decreasing the output voltage error, while for the time-optimal cases the error is increased. This effect is worsened by the subsequent PID activation. As demonstrated in Fig. 27, the following synchronized action of the PID further increases the voltage error of the time-optimal controller causing potential stability problems. On the other hand, in the minimum-deviation case, the PID reduces the output voltage error bringing it closer to the desired reference.
3.1.3.1 Quantization effect of the ADC

Accurate detection of the valley point is important for both time-optimal and minimum-deviation controllers. In systems where an ADC is used to detect extreme points, finite quantization steps introduce additional delays that can potentially affect the system stability. The following analysis relates a quantization step of the ADC, $V_q$, to the valley point detection time delay. Fig. 28 shows zoomed-in waveforms of the output voltage, inductor current and load current around the valley point. To detect the valley/peak point, the output of the ADC is usually monitored, and the point where the derivative of the error value changes sign sensed. In the case when the valley/peak point happens inside a quantization bin (as shown in Fig.28), a delay in the detection occurs [10].

![Figure 28. Zoomed-in waveform of the valley point, illustrating the effect of the ADC quantization.](image)

Utilizing graphical analysis of the waveforms of Fig.28, the worst case valley point detection delay, $t_{\text{delay}}$, can be calculated by combining the following equations:
\[ \Delta i_{\text{delay}} = \frac{V_{\text{in}} - V_{\text{out}}}{L} \cdot t_{\text{delay}}, \quad (10) \]

\[ \Delta Q_{\text{delay}} = \frac{\Delta i_{\text{delay}} \cdot t_{\text{delay}}}{2} = \frac{V_{\text{in}} - V_{\text{out}}}{2L} \cdot t_{\text{delay}}^2, \quad \text{and} \quad (11) \]

\[ V_q = \frac{\Delta Q_{\text{delay}}}{C} = \frac{V_{\text{in}} - V_{\text{out}}}{2LC} \cdot t_{\text{delay}}^2, \quad (12) \]

resulting in

\[ t_{\text{delay}} = \sqrt{\frac{2LCV_q}{V_{\text{in}} - V_{\text{out}}}}. \quad (13) \]
Figure 29. Worst-case inductor-current matching error ($\Delta i_{\text{delay}}$) and valley/peak point detection delay ($t_{\text{delay}}$) for a range of ADC quantization voltages (example system is 12-to-1.6V 500kHz buck converter with 470 nH inductor and 400 $\mu$F capacitor).

For the targeted applications [68, 69] the effect of quantization voltage on the inductor-current matching is shown in Fig. 29.

### 3.2 Self-Calibrating Asynchronous Track and Hold ADC

The previous analysis indicates that fast transient response digital controllers require fast and accurate analog-to-digital conversion, to ensure prompt transient detection and seamless mode transitions. In [11], an application specific 6-bit Flash ADC was presented, as a part of an optimal-time controller. The presented ADC provides fast conversion time and small quantization steps. However, it also consumes relatively large power and takes a significant silicon area, of about 0.5 mm$^2$, which is comparable to the size of an entire analog controller.
[33]. By looking at the operation of that ADC, as well as at other flash architectures, it can be noticed that comparators are poorly utilized, since only one of them is toggling during valley/peak point detection. Generally, as described in Section 2.2.1.1.3, the successive approximation register based ADCs (SAR-DAC) are more cost effective. However, for the targeted applications they are too slow and/or inaccurate. The self-calibrating asynchronous track-and-hold ADC architecture introduced in this section combines the flash ADC and SAR ADC concepts to obtain high accuracy, fast conversion time, and implementation on a small silicon area. As described later, the ADC also incorporates self-calibration, for reducing accumulated quantization errors.

The block diagram of the new ADC and its key waveforms are shown in Figures 30 and 31, respectively. The ADC consists of a static error generator that produces an error signal during steady state operation, a dynamic error generator creating the error during transients, a differential amplifier with a gain factor $k$, and error decoding logic. As shown in the figures, the complete ADC is implemented with only 4 comparators, a low-gain pre-amplifier, a voltage divider, and simple digital logic. The role of the differential stage is to amplify the output voltage error, i.e. $v_{\text{error}}(t) = v_{\text{out}}(t) - V_{\text{ref}}$, and, in that way, reduce the accuracy requirements of the comparators.

For small output voltage variations, the ADC behaves as a simple 3-level asynchronous flash ADC, with effective quantization step $V_{q2}$ (step seen at the input of the ADC). During transients, a digital error value $e_T[n]$ is formed by comparing the amplified analog error signal, $kv_{\text{error}}(t)$, with a tracking window that is formed around it, as shown in Fig.31. The window is created by a dynamic voltage reference generator and two sample and hold circuits $S/H$. 
Figure 30. Functional block diagram of the self-calibrated track-and-hold ADC.

Figure 31. Key waveforms of the asynchronous track and hold ADC.
The dynamic voltage generator adds a positive and a negative offset to the signal $k v_{\text{error}}(t)$ producing two outputs, whose values are $k(v_{\text{error}}(t)+V_{q1})$ and $k(v_{\text{error}}(t)-V_{q1})$, respectively. Where, $V_{q1}$ is the effective quantization step at the input of the ADC during the dynamic mode of operation. In this implementation, the steady state and dynamic quantization steps are intentionally sized differently, so that $V_{q1} < V_{q2}$, i.e. the steady-state step is larger. As described in [40], such a selection improves voltage sensing during transients and, at the same time, eliminates potential limit cycling problems caused by overly small quantization steps around the reference point.

The staircase shaped reference window around the measured signal is created by the dynamic comparators and the sample and hold circuits. As shown in Fig.31, each time the measured signal crosses the reference window, the sample and hold circuits are triggered and the outputs of the dynamic voltage generator captured. This results in an asynchronous change of the reference step by a value $+/-$ $kV_{q1}$. At the same time, the error value is updated. As shown in Fig.30, the value is changed depending on the type of transient. If $k v_{\text{error}}(t)$ exceeds the window $e_T[n]$ is increased by one and if it drops below it is reduced. In this way a fast and accurate measurement with simple hardware is achieved. To eliminate potential metastability problems, the asynchronously captured error $e_T[n]$ is represented using a thermal code. This value is then converted to the binary-weighted equivalent $e[n]$ and synchronized with the rest of the system using bit pipelining [72].

3.2.1 Dynamic Error Generator

Figure 32 shows a circuit level diagram of the dynamic error generator. It can be seen that the circuit implementation is very simple. The dynamic voltage reference generator consists of only four transistors forming a current mirror and an adder [27]. The dynamic quantization steps are adjusted by the biasing circuit and the sample and hold blocks, composed of transmission gates and capacitors.
3.2.2 Quantization, Delay Effect and Self-Calibration

The operation of the track and hold ADC can be affected by the delays in the circuit. These effects can be described with the diagrams of Fig. 3.3, showing zoomed in ADC waveforms around a transient point for a realistic non-zero delay system. The diagrams show both the effects of the comparator delay, $t_{d_{-cmp}}$, and the latency caused by a finite rise/fall time from one step level to another, labeled as $t_{d_{-tsh}}$. By looking at the waveforms we can see that the delay-caused error in quantization step to $\Delta V_q$, can be approximated as

\[
\Delta V_q = \frac{dk V_{error}}{dt} (t_{d_{-cmp}} + t_{d_{-tsh}}).
\] (15)
This equation indicates that the error is proportional to the rate of change of the error signal and linearly increases with the delays. In the targeted application, where the input signal can change at a fairly high rate, the error could accumulate and, consequently, affect the controller operation. To minimize this accumulative effect two techniques are applied. First, high-frequency noise, resulting in the high derivative of the error signal, is eliminated with the differential amplifier of Fig.30. It is designed as a two-stage operational transconductance amplifier [27] that also acts as low-pass filter for the high-frequency noise.

![Diagram](image)

Figure 33. Key waveforms of the realistic non-zero delay asynchronous track and hold ADC.

The second technique is self-calibration. For this purpose, the static error generator from Fig. 30 is used. The self-calibration is based on the detection of zero-error bin crossing. Whenever the analog input signal enters the zero-error bin of the static comparators, the dynamic error generator is reset to zero and any accumulated error eliminated.
3.3 Practical Implementation

This section describes how the converter losses and the equivalent series resistance of the output capacitor affect the operation of the presented controller, as well as of the other fast response solutions. It also shows new methods and circuits that minimize the effects of these non-idealities. The delay in the peak/valley point detection is also further discussed and a dual detection method for reducing this negative effect introduced. Accordingly, a modification of the originally presented control algorithm that incorporates a correction method is also shown.

3.3.1.1 Dual extreme point detection

In Section 3.1 it was indicated that the operation of the presented controller and other solutions relying on the detection of the peak/valley point is sensitive to delays. As shown in the example of Fig.34, for a buck converter with a high step down ratio, this problem is quite significant during light-to-heavy load transients.
Figure 34. Light-to-heavy load transient waveforms of a high-step down buck converter when the dual-extreme point based delay compensation is applied.

Even a small delay in the detection of the extreme point, $t_{delay1}$, causes a significant mismatch in the inductor current, $\Delta i_1$, due to a high inductor current slew rate, $m_r$.

To minimize this effect, a double extreme point detection algorithm is applied. For the case of Fig. 34, in addition to detecting the valley point, the peak output voltage during the main switch off-time is also detected. The switching sequence is then slightly modified. In this case, after the peak point is detected, the main switch off-time is extended by $(1-D)T_s/2$. It can be seen that, now, the same delay results in a much smaller current mismatch at the end of the current reconstruction phase, $\Delta i_2$, due to the drastically lower current slew rate $m_f$.

The reduction in the current mismatch for a general case can be calculated from the following expression:
where \( t_{delay1} \) and \( t_{delay2} \) are delays in the detection of the valley and peak point, respectively. This equation indicates as long as \( t_{delay2} \) is not larger than \((m_r/m_f)*t_{delay1}\), the dual point detection results in a smaller current mismatch. For most targeted applications this condition is easily satisfied.

### 3.3.1.2 Self-adjusting duty ratio corrector

In realistic, i.e. lossy, converters the steady state duty ratio value changes with load conditions. For a buck converter operating in a closed loop this dependence can be calculated from the dc steady state model \( [7] \) and described with the following equation:

\[
D_{steady} = \frac{V_{out}}{V_{in}} \cdot \left( 1 + \frac{R_{eq} \cdot I_{load}}{V_{out}} \right),
\]  

(16)

where \( D_{steady} \) is the steady state duty ratio value, \( I_{load} \) is the load current, and \( R_{eq} \) a lumped sum of converter losses, obtained from the dc averaged model.

For this system, as well as for other fast transient response solutions where the generation of the optimal switching sequence relies on the information about the steady state duty ratio value \([10, 11, 44]\), this dependence can cause potential stability problems. Since the duty ratio values before and after a load transient are not the same, mode transient problems can occur due to an erroneous calculation of the optimal switching sequence.

To compensate for the duty ratio variations, systems shown in \([10, 11, 44]\) use a high bandwidth compensator. However, such solutions require accurate knowledge of the converter parameters,
and as will be demonstrated in the experimental section, are still are not able to fully suppress subsequent voltage overshoots and undershoots. This is because, even though it is relatively fast, the PID compensator is not able to change the duty ratio to the new steady value in a single switching cycle.

To reduce the influence of the converter losses and allow the use of a slower compensator covering a wide range of the output filter component values, an on-line self-tuning duty ratio correction system is developed. The correction is performed through a repetitive two-step process. In the first step, a small look-up table (LUT) that relates changes in the load current, i.e. inductor current rise/fall time, and the corresponding loss-related duty ratio value increments are updated. In the second step, the stored values are used to instantaneously correct the duty ratio value. The operation of the duty ratio corrector can be explained with the help of Figs. 23.b and 35.

![Figure 35. Simplified block diagram of the duty ratio correction logic.](image)

To estimate the increase in the inductor, i.e. load current, for light-to-heavy load transients, the on-time of the converter main switch is measured during the inductor current ramp time. This time is labeled as $t_{cr}$, in Fig.23.b. The obtained digital equivalent $t_{cr}[n]$ is then used as the address input for the look up table of Fig.35 producing a corresponding duty ratio correction factor $\Delta d[n]$. The correction factor is added to the old steady state duty ratio $D_{old}[n]$. This value, as described in Section 3.1, is obtained by capturing the output of the PID compensator (Fig.22) before the suppression logic is activated. In this way an estimate of the new duty ratio value
\( d_{\text{est}}[n] \) is formed. This estimate, which takes into account converter losses, is now used during the current reconstruction phase to create the switching sequence, i.e. generate transistor on and off times. Once the system has returned back to the steady state and the output voltage is fully recovered, the correction factor in the look up table is updated. As shown in Fig.35, the update is performed by comparing the actual new duty ratio value \( D_{\text{new}}[n] \) with the \( D_{\text{old}}[n] \) and storing the difference in the table. Again, the true duty ratio value is obtained by capturing the output of the PID compensator after the transient is completed.

For heavy-to-light load transients the correction is performed in a similar manner. Now to estimate the current drop, the inductor current fall time is measured and the resulting digital value \( t_{\text{cf}}[n] \) used for calibration. The indication of the type of transient is provided through \( h/l \) signal provided by the transient detection logic (Fig.22).

In order to minimize the size of the correction logic, a small LUT with only few entries is created. The number of entries, i.e. input values to the table, is reduced through a truncation of the values \( t_{\text{cr}}[n] \) and \( t_{\text{cf}}[n] \). As it will be shown in the following section, this truncation does not have a significant effect on the performance of the correction logic and still provides seamless mode transitions. For the start up, the LUT can be initially populated with data obtained from data sheets, simulations, or from experimental testing.

### 3.3.2 Detection of successive transients

In fast transient response controllers having two modes of operation, successive transients can cause toggling between the dynamic and steady state modes. To prevent the undesirable toggling, the control IC logic is slightly modified, as described with the state diagram of Fig.36. In this case, during transients, the threshold value for activating the suppression logic is dynamically adjusted. As soon as the inductor current ramping/falling phase (labeled as \( HL1/LH1 \) states in Fig.36) is completed, the error captured at the peak/valley point, \( \Delta v_{\text{peak}} \), is set as the new triggering threshold. At the same time instant, the current reconstruction phase is initiated (states \( HL2/LH2 \)). After the reconstruction is completed, the control task is passed to the PID compensator, which now operates with shifted threshold (state S2). In this state, consecutive small transients are not able to create a sufficiently large output voltage variation to reactivate
suppression logic. Thus, the PID compensator remains active (stays in S2). For large load steps, the error value overpasses the new threshold and the suppression logic is activated again. In this way toggle-free successive transient handling is performed. Once the voltage returns back to the steady state, the threshold is set back to its nominal value, and the PID returns to its regular state (state S1).

Figure 36. The minimum-deviation controller state diagram.

3.3.3 Transient Detector for Converters with Large Output Capacitor ESR

For the converters with relatively large output capacitor equivalent series resistance (ESR) the detection of the zero capacitor current through a valley/peak point detection can be erroneous
In the presence of ESR the output voltage of the converter might not coincide with that of the ideal capacitor and a premature detection of the valley/peak points can occur, as demonstrated in Fig. 37. To compensate for this and, at the same time, improve the detection of the transient instant through the output capacitor estimation, solutions based on the utilization of a matched RC network have been proposed in [10, 44, 52]. A simple detection circuit introduced in this subsection utilizes the same principle as the previous solutions. However, in addition to minimizing the ESR effects, the circuit of Fig. 38 also provides improved detection of load transients and the peak/valley points.

Figure 37. Light-to-heavy load transient waveform of a buck converter with large output capacitor ESR.
Figure 38. Transient and valley point detection circuit for SMPS utilizing output capacitors with large ESR.

The operation of the detector is based on the generation of two thresholds, i.e. a threshold window, around a waveform identical to the $v_c(t)$ portion of the output capacitor (Fig.37) and their comparison with the actual output voltage $v_{out}(t)$. As soon as the output voltage exceeds one of the thresholds a load transient is detected. The peak/valley points are detected at the point where the output voltage and $v_c(t)$ are the same. This point corresponds to the time instant at which the voltage drop across the ESR is zero, i.e. the output capacitor current is zero.

The detector consists of only three comparators, an $RC$ circuit, and several transistors forming a threshold generator block. The capacitor $C_1$ and the resistor $R_1$ are selected such that, ideally, their time constant matches that of the large ESR capacitor, i.e. $CR_{esr}=C_1R_1$, where $R_{esr}$ is the ESR value. As shown in Fig.39, for such a selection, the voltage across capacitor $C_1$, $v_{c1}(t)$, is identical to the $v_c(t)$ portion of the output capacitor. The threshold generation circuit operates in the same manner as the one for the track and hold ADC of Section 3.2. It generates a threshold window around $v_{c1}(t)$, where the size of the threshold $\Delta V_{th_d}=R_{th}I_{bus_d}$, can be adjusted with the bias circuit. In this case the threshold steps are selected to be slightly larger than the steady-state
voltage ripple, to eliminate undesirable mode transitions and, at the same time, allow a fast transient detection. The comparators detect load transients, when the output voltage exceeds a threshold point. They also detect the point where $v_{c1}(t)$ and $v_{out}(t)$ are the same.

In this case the peak/valley point detection signals from the ADC are blanked. This is done because the presented detector does not suffer from quantization problems and, consequently, offers a better accuracy.

![Figure 39. Key waveforms of the large ESR transient detector.](image)

3.3.4 Stability Discussion

The main stability concern of the minimum deviation controller is related to the steady-state and transient mode transitions. For ideally operating transition logic the overall stability of the system can be assumed if the PID compensator provides stable operation during steady state.
This is because the current reconstruction logic used during transients reconstructs the new inductor current steady-state value. The output voltage deviation is the only remnant the PID needs to manage. For such a case the small-signal assumptions are valid and stability is maintained [7].

However, as discussed through the paper, in a realistic converter system delays and converter losses affect operation of the controller causing inductor current and duty ratio value mismatches at the end of the current reconstruction phase and possible stability problems. From the PID compensator point of view, these mismatches have the same effect as load transients, causing undesirable additional transient logic activation, as shown in [71] for near-optimal control. To eliminate these problems, the PID should be fast enough to limit the mismatch-caused voltage variation to a lower than the threshold value. In this way undesirable toggling between the modes can be eliminated. This practically means that the accuracy of the current reconstruction logic determines the bandwidth requirement of the controller and that for well-behaved transient logic the PID bandwidth can be reduced.

The effect of errors in the current reconstruction is demonstrated in waveforms of Fig. 40. They are showing load transient response simulations of a lossy buck converter that is regulated with a minimum-deviation controller prior to the activation of the duty ratio correction logic.
Figure 40. Closed loop simulations of an 80% efficient, 12 V to 1.6 V buck without duty ratio correction for a 5A to 30 A load transient. Top: output voltage. Bottom: inductor and output capacitor currents.

It can be seen that a mismatch in the duty ratio values causes multiple transients even in the case when the adaptive threshold adjustment (described in Subsection 3.3.2) is applied. Such a scenario can be envisioned right after the start-up of the converter before the LUT of the duty ratio correction logic is populated or if the table is not populated with correct values. The influences of other elements affecting the operation of the current reconstruction logic described in previous sections can have similar effects and hence affect the system stability.
3.3.5 Integrated Circuit

Based on the diagrams of Figs. 22, 30, 32, and 36, a minimum deviation digital controller IC was designed and fabricated in a 0.18µm CMOS process. The PID compensator and the dual output digital pulse-width modulator (DPWM) of Fig 22 utilize a hybrid architecture, whose detailed description is found in [40]. The complete digital logic takes about 4500 gates and is fully implemented through the Verilog hardware description language (HDL) using automated design tools. Besides the previously described controller, the digital logic of the prototype IC also includes additional testing and debugging blocks that, out of the total number, take about 500 digital gates. A photograph of the prototype IC and an oversampled digital controller IC [41] are shown in Fig. 41 and their characteristics compared in Table I.

![Figure 41. A photograph of the oversampled digital control IC (left) and minimum-deviation digital controller IC (right).]
Table 1 Minimum-Deviation Digital Controller IC Summary and Comparison to Oversampled Digital Controller IC

<table>
<thead>
<tr>
<th>Controller type</th>
<th>Minimum-Deviation</th>
<th>Oversampled [41]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>TSMC 0.18μm CMOS</td>
<td>TSMC 0.18μm CMOS</td>
</tr>
<tr>
<td>Supply Voltage (Digital / Analog)</td>
<td>1.8 V / 3.3 V</td>
<td>1.8 V / 3.3 V</td>
</tr>
<tr>
<td>DPWM resolution</td>
<td>13 bits</td>
<td>8 bits</td>
</tr>
<tr>
<td>DPWM nominal frequency (oversampling)</td>
<td>500 kHz</td>
<td>500 kHz (x4)</td>
</tr>
<tr>
<td>ADC area</td>
<td>0.02 mm$^2$</td>
<td>0.22 mm$^2$</td>
</tr>
<tr>
<td>ADC current consumption</td>
<td>0.24 mA</td>
<td>2 mA</td>
</tr>
<tr>
<td>ADC quantization voltage</td>
<td>4 mV</td>
<td>4 mV</td>
</tr>
<tr>
<td>ADC resolution</td>
<td>NA</td>
<td>7 bits</td>
</tr>
<tr>
<td>Digital logic area</td>
<td>0.22 mm$^2$</td>
<td>0.31 mm$^2$</td>
</tr>
<tr>
<td>Digital logic current consumption</td>
<td>0.2 mA</td>
<td>~0.3 mA</td>
</tr>
<tr>
<td>Total area</td>
<td>0.24 mm$^2$</td>
<td>0.53 mm$^2$</td>
</tr>
</tbody>
</table>

It can be seen that, even with the extra digital logic occupying about 11% of the digital part, the IC takes only 0.24 mm$^2$ of the silicon area, which is comparable to state of the art analog solutions [33] and is 55% smaller than a digital oversampled control IC solution.

The track-and-hold ADC contributes significantly to the reduced silicon area utilization. In fact, it is 9 times smaller than a 7-bit Flash ADC commonly found in digital controller ICs, such as the oversampled controller IC shown in Fig. 41. In the following subsection, the experimental verification results of the chip are presented.
3.4 Experimental Results

The closed loop verification of the minimum-deviation controller IC was performed with a state-of-the-art industrial two-phase, 12 V to 1.8 V, 500 kHz, buck converter module, providing 35 A per phase [73]. The ESR of the 400 µF output capacitor is just 0.5 mΩ and each phase has a 0.47 µH inductor. The performances of the IC are tested for the case when one of the phases is disabled and in the two-phase interleaved modes of operation.

3.4.1 Load transient response and comparison with a conventional high-bandwidth controller

To verify transient performance of the minimum-deviation controller, its response is compared to that of a conventional wide-bandwidth controller, where both systems regulate operation of the single phase buck. To create a conventional controller, the same fabricated IC was used. In this case, the transient suppression logic was disabled and the PID compensator designed to have the bandwidth of a $1/10^{th}$ of the switching frequency. The tests were performed with an ultra fast load transient circuit reaching the maximum load current of 35 A in 20ns, i.e. having the current slew rate of 1.75 A/ns.

The experimental waveforms of Fig. 42 show the transient response results of the conventional controller. In Fig.43 the suppression logic is active. In this case, the duty ratio correction logic is not employed.
Figure 42. Transient response waveforms for a 0 A to 30 A load step (wide-bandwidth conventional compensator): Ch1: Output converter voltage (200mV/div); Ch2: actual inductor current $i_L(t)$ 30 A/div; D0: load transient triggering signal; D1: pulse-width modulated control signal; D2: main switch control signal created by suppression logic; D3: synchronous rectifier control signal created by the suppression logic; D4: peak valley point detection; Time scale is 5μs/div.
Figure 43. Transient response waveforms for a 0 A to 30 A load step (minimum deviation controller IC): Ch1: output voltage (200mV/div); Ch2: inductor current $i_L(t)$ 30A/div; D0: load transient triggering signal; D1: pulse-width modulated control signal; D2: main switch control signal created by suppression logic; D3: synchronous rectifier control signal created by the suppression logic; D4: peak/valley point detection; Time scale is 5μs/div.

The results demonstrate that the activation of the suppression logic results in about three times smaller deviation, allowing for a proportional reduction of the output capacitor. Fig. 44 shows operation of the minimum-deviation controller IC during a heavy-to-light load step.
Figure 44. Transient response waveforms of the minimum deviation controller IC for a 30 A to 0 A load heavy-to-light load transient: Ch1: output voltage (500mV/div); Ch2: inductor current $i_L(t)$ 30 A/div; D0: load transient triggering signal; D1: pulse-width modulated control signal; D2: main switch control signal created by suppression logic; D3: synchronous rectifier control signal created by the suppression logic; D4: peak valley/point detection signal; Time scale is 5μs/div.

### 3.4.2 Consecutive Load Transients

The minimum-deviation controller behavior in the presence of two consecutive load transients, a 0 A to 12 A followed by a 12 A to 30 A, is shown in Fig. 45. It can be seen that the controller seamlessly moves between the transient suppression and PID modes of operation.
Figure 45. Consecutive light-to-heavy load transients: Ch1: output voltage (100mV/div); Ch2: inductor current $i_L(t)$ 30 A/div; D0, D1: load transient triggering signals; D2: pulse-width modulated control signal; D3: main switch control signal created by suppression logic; D4: synchronous rectifier control signal created by the suppression logic; D5: peak valley/point detection signal; Time scale is 10 μs/div.

3.4.3 Operation with a dual-phase buck

The waveforms of Fig.46 show the response of the controller with the 2-phase buck. It can be seen that the minimum voltage deviation is obtained with a very low inductor current overshoot, i.e. low current stress.
3.4.4 Duty ratio corrector and parameter insensitive operation

The experimental results shown in the previous subsections are obtained with the utilization of a high-bandwidth PID compensator, which partially compensates for the loss-related duty ratio variations. As mentioned in Subsection 3.3.1.2, such an approach requires a fairly accurate knowledge of the converter LC parameters and, as can be seen from the experimental waveforms of Figs. 43 and 45, still causes a slight undershoot after the current reconstruction phase. The experimental results shown in this subsection demonstrate that, by utilizing duty ratio correction logic, the requirements for the PID compensator bandwidth can be drastically reduced. This allows for a slower and more robust compensator design that can operate with a very wide range of the output filter LC values, practically allowing parameter-insensitive operation.
To demonstrate the effectiveness of the duty ratio corrector, the bandwidth of the PID compensator is set to be about a $1/50^{th}$ of the switching frequency, i.e. reduced five times, and the performance of the IC are compared with and without duty ratio correction logic. Fig. 47 shows the transient response of the controller IC for a load step from 0 A to a half of the nominal load current without correction logic. It can be seen that, even at this load level, a subsequent voltage undershoot larger than the one caused by the original transient occurs.

![Graph showing transient response](image)

Figure 47. Transient response for a 0 A to 16 A load step for the case when a slow PID compensator without duty ratio correction logic is used. Ch1: output voltage (100mV/div); Ch2: inductor current $i_L(t)$ 30 A/div; Digital channels: load transient triggering and key controller signals; Time scale is 5μs/div.

Fig. 48 shows operation with the slow PID compensator when the duty ratio corrector is active. It can be seen that the correction logic not only eliminates the subsequent transient but also results
in virtually seamless mode transition. Even though a slow PID compensator is utilized, the consequent undershoot existing in the previous case is eliminated.

Figure 48. Transient response of the controller IC for a 0 A to 16 A load step with a slow PID compensator when the duty ratio correction logic is active. Ch1: output voltage (100mV/div); Ch2: inductor current $i_L(t)$ 30 A/div; Digital channels: load transient triggering and key controller signals; Time scale is 5μs/div.

Figures 49 and 50 demonstrate operation of the system with the same slow PID compensator for a load step from 0 A to a 90% of the full load. In this case, the low ESR output capacitor is replaced with a one that has four times larger ESR value and, to compensate for that, an off-chip transient detector, which was described in Section 3.3.3, was used. The performances are again verified through a comparison of the operation with and without the duty ratio corrector.
Figure 49. Transient response for a 0 A to 32 A load step for the case when a slow PID compensator without duty ratio correction logic is used. Ch1: output voltage (100mV/div); Ch2: inductor current $i_L(t)$ 30 A/div; Digital channels: load transient triggering and key controller signals; Time scale is 5μs/div.
Figure 50. Transient response for a 0 A to 32 A with a slow PID compensator when the duty ratio correction logic is active. Ch1: output voltage (100mV/div); Ch2: inductor current $i_L(t)$ 30 A/div; Digital channels: load transient triggering and key controller signals; Time scale is 5μs/div.

It can be seen that the duty ratio correction logic eliminates subsequent transients caused by the duty ratio variations. Also, a comparison with the waveforms of Fig.43 shows that the detection circuit further reduces voltage deviation, even when the output capacitor with a much larger ESR is used. This is because of the reduction of the delay in the detection of the transient instant. In this case, for triggering estimate of the output capacitor current is used and, as discussed in Section 3.1, the delay existing in the voltage-threshold triggered systems is practically eliminated. A wider adoption of this detection method, and consequent practical on-chip implementation, will probably depend on solving the problems related to the mismatch in the time constants, which is characteristic for all RC-based methods [10]. A potential solution is presented in Appendix A.
Chapter 4

Chapter 4: Buck Converter with Merged Capacitive Attenuator

The main goal of this section is to introduce a buck converter with merged capacitive attenuator (BCMCA) and a complementary digital controller, shown in Fig. 51. Compared to the other two-stage solutions described in Section 2.3 [62, 63, 65, 66], the BCMCA has a smaller number/area of switches, a simpler unified controller, and/or a faster transient response, allowing further filter reduction.

The BCMCA has some resemblance with the previously presented two-stage structures. However, unlike the other systems, the converter in Fig. 51 does not require an extra flying or output capacitor. Furthermore, the proposed converter shares the same set of switches between the two stages, minimizing their total number to four compared to at least six required for the previous solutions. A single digital controller regulates the output voltage and keeps the attenuator output constant, through a novel active-charge algorithm executed by the Charge-sharing regulator. The steady-state output regulation is performed with an analog-to-digital converter, a PID regulator, and a digital pulse-width modulator. To suppress transients, the controller employs the minimum-deviation method using Minimum-deviation logic. During transients, it also increases the slew rate of the inductor voltage, by bypassing the attenuator, largely improving dynamic performance.

---

4.1 Principle of Operation

The main purpose of the charge-controlled attenuator in Fig. 51 is to reduce the difference between the input and output voltage of the downstream buck converter and, in that way, reduce the output filter. Quantitatively, this effect can be described by looking at the expression for the inductor current ripple of a buck converter [7]

\[
\Delta I_{\text{ripple}} \approx \frac{V_{\text{out}} (1 - D)}{2 L f_{\text{sw}}} = \frac{V_{\text{out}}}{2 L} \cdot \left(1 - \frac{V_{\text{out}}}{V_{\text{in}}} \right) \cdot \frac{1}{f_{\text{sw}}},
\]

where \( V_{\text{in}} \) and \( V_{\text{out}} \) are the input and output voltage, respectively, \( f_{\text{sw}} \) is the switching frequency, 
\( D \) is the steady-state duty ratio, and \( L \) is the inductor value. A similar expression for the capacitor voltage ripple can also be derived. In conventional designs, the inductor is usually sized based on
the minimum allowable ripple for the worst case operating condition, corresponding to the largest *difference between the input and the output* voltages. There, to minimize the filter while maintaining small ripple, operation at higher switching frequencies is usually targeted. The system in Fig. 51 operates on the fundamental principles introduced in [65, 66]. Instead of increasing the frequency, the *voltage difference between the input and output of the buck is reduced* allowing filter minimization and, concurrent, reduction of switching losses. In this implementation, a digitally controlled attenuator reduces the voltage difference. It is controlled such that the switching node voltage, \( v_{Lx}(t) \), is regulated to a value that is closer to the output voltage \( V_{\text{out}} \). Utilizing the input capacitor attenuator of Fig. 51, the inductor current ripple takes on the characteristics given by (18) and (19).

\[
\Delta I_{\text{ripple}} \approx \frac{V_{\text{out}}}{2L} \cdot (1 - \frac{2V_{\text{out}}}{V_{\text{in}}}) \cdot \frac{1}{f_{\text{sw}}}, \quad (v_g > 2V_{\text{out}}) \quad (18)
\]

\[
\Delta I_{\text{ripple}} \approx \frac{V_{\text{out}}}{2L} \cdot \frac{2V_{\text{out}}}{V_{\text{in}}} - 1 \cdot \frac{V_{\text{in}}}{V_{\text{out}}} - 1 \cdot \frac{1}{f_{\text{sw}}}, \quad (v_g < 2V_{\text{out}}) \quad (19)
\]

The above equations are plotted in Fig. 52, illustrating inductor-value reduction potential.
Figure 52. Normalized inductor current ripple values of the conventional buck converter and proposed BCMCA for a wide range of input-to-output voltage ratios. The switching node voltages are noted for the BCMCA in brackets.

Furthermore, compared to the conventional buck and other two-stage solutions, the converter in Fig. 51 practically does not increase the input filter volume. The charge controlled attenuator is constructed by replacing the input filter capacitor $C_{in}$, with two serially connected capacitors with a half of the voltage rating and $2C_{in}$ capacitance value. Since the volume of the capacitors is primarily determined by its energy storage capability [74], $W_E = 1/2 CV^2$, and the total energy in both cases is the same. Hence, ideally, this modification virtually has no influence on the input filter size.
4.1.1 Steady-State Operation

In the system in Fig. 51, during steady state for $V_g > 2V_{out}$, the attenuated supply voltage $V_{in} = V_g/2$ is provided to the downstream buck converter, and for $V_g < 2V_{out}$ the full input voltage $V_{in} = V_g$ and the attenuated supply voltage $V_{in} = V_g/2$ are supplied. This minimizes the maximum difference between the filter input and output voltages during all modes of operation, allowing for the output filter minimization. For the sake of simplicity, in the following analysis the steady-state input voltage is assumed to always be greater than $2V_{out}$.

The attenuator operation for a high-supply voltage can be visualized with the help of Fig. 53 showing its simplified circuit over two consecutive switching periods, where the conduction path is highlighted. During the first period (mode a), $SW_1$ and $SW_4$ in Fig. 51 are turned ON and the top capacitor is connected to the input of the downstream converter. During the next mode, (b/d) $SW_3$ and $SW_4$ are turned ON and $SW_1$ and $SW_2$ are turned OFF, providing a path for the inductor current $i_L(t)$ (equivalent to the operation of a synchronous rectifier (SR) in the conventional buck). Over the following period (mode c), $SW_2$ and $SW_3$ are conducting and the bottom capacitor provides the current for the converter. Finally, mode b/d is reactivated and the entire process is repeated.
Figure 53. Steady-state modes of operation of the two-capacitor BCMCA of Fig. 50 for the case when $V_g > 2V_{out}$.

In this way, the voltage balance of the input capacitive attenuator is maintained using only the buck inductor current. A consequence of this implementation is a decoupled input and output ground. However, as discussed in the following section, due to a smaller number of switches and their reduced voltage rating, the conduction losses of the BCMCA are more comparable to that of a conventional buck.

1) Center-Tap Voltage Regulation: By operating as previously described, ideally, equal average current over the same period of time, i.e., equal charge, is taken from the both attenuator capacitors, resulting in a stable center-tap voltage. However, in practice, this is usually not the case. Due to different losses of the two current loops, mismatches of components, the tap voltages $v_{in1}(t)$ and $v_{in2}(t)$ (see Figs. 51 and 53) might diverge in time resulting in unbalanced operating conditions, affecting the output voltage regulation. To compensate for this, a practical charge control-based algorithm is applied. The algorithm is described with the state diagram of Fig. 53. During each cycle, the center-tap voltage $v_{in2}(t)$ is compared to one-half of the input
voltage using the comparator in Fig. 51. When a significant difference between the two voltages is detected, Charge-sharing regulator, i.e., state machine in Fig. 54, alters the previously described steady-state operation sequence. Instead of following the regular capacitor discharging pattern, the switching sequence is changed, such that more charge is taken from the capacitor with a higher voltage. In particular, instead of taking the current from the capacitors in alternating fashion, the inductor discharges only the higher voltage capacitor for several cycles, until the voltages are equalized. When the balance is achieved, the regular sequence is resumed. This control scheme simplifies regulation of the center-tap voltage, eliminating the need for a fully dedicated front stage controller existing in other two-stage systems.

![State-diagram describing operation of the active charge controlled attenuator.](image)

Figure 54. State-diagram describing operation of the active charge controlled attenuator.

4.1.2 Transient Operation

Lowering the input voltage of a conventional buck generally reduces the inductor current slew rate during light-to-heavy load transients, negatively affecting the dynamic performance. In the topology of Fig. 51, a comparatively smaller inductor minimizes this effect and, at the same time, improves heavy-to-light load transient response. To further improve dynamics, during light-to-heavy transients, the controller directly connects the input port of the buck stage to \( V_g \), by turning ON SW1 and SW2. Thus, compared to the conventional buck, the inductor slew rate is increased by the ratio proportional to the reduction in the inductance value. This is demonstrated in Fig. 55, where the inductances of the conventional buck and the introduced two
stage converter are labeled as $L_{\text{buck}}$ and $L_{2s}$, respectively. To fully utilize the advantages of the reduced inductor, the minimum deviation control method is utilized.

![Figure 55. Idealized transient response waveforms of a conventional buck and the BCMCA (2s).](image)

(Top) AC components of the output voltages. (Bottom) Load and inductor currents.

1) **Output Capacitor Reduction in the Ideal System:** In modern supplies, the output capacitor value is determined based on the voltage deviation during transients rather than on the ripple [1]. For such requirements, the size reduction can be found by comparing the responses of an optimum controller to a step load change, for a conventional buck and the proposed topology, as shown in Fig. 55.

In both cases, the output capacitors are selected such that the same maximum allowable voltage deviation $\Delta v_{\text{max}}$ occurs during a maximum load step change, $\Delta I_{\text{max}}$. The value of the output capacitance $C$ resulting in a $\Delta v_{\text{max}}$ voltage deviation during transient can be approximately calculated as

$$ C \approx \frac{Q}{\Delta v_{\text{max}}} = \frac{\Delta I_{\text{max}}^2 L}{2\Delta v_{\text{max}}(V_{\text{in}} - V_{\text{out}})} $$.  

(20)
where \( V_{\text{in}} \) and \( V_{\text{out}} \) are dc values of the buck stage input and output voltages, respectively, and \( Q \) is the lost capacitor charge during transient (for the two-stage converter labeled as \( Q2s \) in Fig. 55). This equation shows that, ideally, possible reduction of the output capacitor is directly proportional to that of the inductor resulting in a squared minimization of the output filter \( LC \) product.

### 4.2 Practical Implementation

In a practical two-stage converter of Fig. 51, the maximum allowable reduction of the output capacitor is smaller than what the previously analyzed ideal case predicts. This section gives a more realistic estimate of the output capacitor reduction and also discusses the tradeoff between switching and conduction losses.

#### 4.2.1 Selection of the Output Filter Capacitor

Delays between the occurrence of a load transient and the controller reaction contribute to increased output voltage deviations, and the required output capacitor energy storage requirements (size). In the presence of the delay, \( t_d \), the output voltage, inductor current and load current waveforms resemble those of Fig. 56.
Figure 56. Realistic transient response waveforms of the BCMCA. (Top) AC component of the output voltage. (Bottom) Load and inductor currents.

The maximum voltage deviation of a realistic system controlled by a near-optimal controller can be approximated as

\[
\Delta V_{\text{max}} = \frac{Q_d}{C} + \frac{Q_1}{C} \approx \frac{\Delta I_{\text{max}} t_d}{C} + \frac{\Delta I_{\text{max}}^2 L}{2C(V_{\text{in}} - V_{\text{out}})},
\]  

(21)

where the first term on the right-hand side is contribution of the delay, during which the maximum difference between the load and the inductor current is taken from the capacitor. The second term, obtained from (20), is due to the lost capacitor charge. From (21), it can be seen that the delay in the controller reaction has a larger influence on the power stage with a smaller output capacitor not allowing a reduction in \( C \) directly proportional to that of \( L \), predicted by the ideal case analysis. Still, as shown in a later section, for realistic delays, a significant reduction in the output capacitor value is achievable.
4.2.2 High Attenuation Merged-Capacitive Input-Stage

For converters with a large input-to-output voltage conversion ratio, the reactive component size reduction, achievable by the one-half capacitive-attenuator of Fig. 51, is quite limited. Therefore, a modified input-stage with a larger attenuation factor is desired. It can be achieved with a one-third attenuation input-stage shown in Fig. 57a and one-quarter attenuation input-stage shown in Fig. 57b, for example.

Figure 57. Input capacitive-attenuator stages with maximum attenuation factor of 3 (a) and 4 (b). Transistor blocking voltages are shown through color.

Unlike the one-half capacitive-attenuator, the solutions presented in Fig. 57 do not result in transistor blocking voltage reductions proportional to the SCC conversion ratios. As a result, the transistor conduction losses are higher for a given silicon area budget. However, if the active charge controller is designed to toggle only two transistors during each mode transition, the conduction losses can be partially offset with decreased switching losses. An example of a
power efficient active charge control algorithm is illustrated in Fig. 58, for the one-third capacitive-attenuator circuit (Fig. 57a).

Figure 58. State-diagram describing operation of the one-third capacitive-attenuator (middle left) and steady-state mode diagrams.
The mode transition algorithm ensures that only two switches are toggled during each mode transition, consequently reducing the switching-losses by three compared to a conventional buck converter. In order to accurately implement the algorithm, at least two capacitor divider node voltage values are needed. A power and silicon size efficient ADC architecture suitable for input voltage measurement is described in Appendix B [75].

The normalized inductor current ripple values of the two capacitive-attenuators are illustrated in Fig. 59.

Figure 59. Normalized inductor current ripple values of the conventional buck converter and proposed BCMCA for a wide-range of input-to-output voltage ratios. The switching node voltages used for a given input-to-output voltage ratio are noted in brackets.
The inductor current-ripple is significantly smaller, compared to a conventional buck converter, for all operating conditions, allowing for equal reduction of the inductor value. Furthermore, for variable input voltage applications the inherent reduction of current-ripple can be exploited to improve the power processing efficiency, through reduced steady-state switching frequency [76].

### 4.2.3 Efficiency Analysis and Design Tradeoffs

To find losses of the BCMCA and compare them to the conventional buck, the analysis presented in [77] and [78], giving detailed expressions for conduction and switching losses of similar two-stage and single-stage topologies, is used. The FET turn-on and turn-off switching losses are modeled using piece-wise linear approximations, while the conduction losses are modeled using conventional lumped equivalent resistance.

Compared to the conventional buck, the BCMCA has lower switching losses, because of reduced transistor blocking voltages, as seen from Figs. 53, 56 and 57. This reduction comes at the expense of an increased number of switches in the conduction path. However, in an optimized design, where the transistors are constructed to safely sustain only the maximum blocking voltage, the extra switches do not cause a twofold increase in the conduction losses. Since the transistor ON-resistance per unit silicon area is

\[
R_{on_{sp}} = \alpha \cdot V_B^2, \tag{22}
\]

where \(\alpha\) is process-dependant constant and \(V_B\) is the breakdown voltage, in optimized design, a two times smaller blocking voltage results in the four times smaller resistance for the same area [79].

For the BCMCA of Fig. 51, this practically means that \(SW3\) and \(SW4\) can be designed such that each of them has a half of the ON resistance of the conventional buck SR and that their total silicon area is the same as that of the SR. Consequently, the mode b/d (see Fig. 53) of the
BCMCA does not increase the conduction losses. As far as SW1 and SW2 are concerned, in practice, they need to sustain a higher than $1/2v_g(t)$ voltage and, consequently, have a higher total resistance than the main switch (MS) of the buck. This is due to a possible temporary conduction of the body diodes of SW3 and SW4 during mode transitions, causing up to 1.2V [80] increase in the blocking voltage. As a result, during modes a/b the conduction losses are slightly increased.

For the BCMCA of Fig. 57a and Fig. 57b, similar conclusions can be reached. Namely, during the synchronous rectification modes (mode b/d) the total on-resistance of the optimized switches (SW5,6,7,8) are comparable to that of a single-phase buck converter SR. However, during the main switch modes (mode a/c/e) the total transistor on-resistance is increased compared to a buck converter MS. The normalized approximate on-resistance, assuming fixed silicon area budget, is given in Table 2.

<table>
<thead>
<tr>
<th>Mode</th>
<th>$R_{on}$ – Fig. 55a (Fig. 55b)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Charging from top/bottom $C_{in}$</td>
<td>5/3 MS (2 MS)</td>
</tr>
<tr>
<td>Charging from middle $C_{in}$</td>
<td>4/3 MS (5/4 MS)</td>
</tr>
<tr>
<td>Dis-charging</td>
<td>SR</td>
</tr>
</tbody>
</table>

Due to the decreased switching losses improved power processing efficiency at the low-to-medium load level should be expected, compared to a buck converter. While at the high load level comparable efficiency is attainable for optimized switch designs, as will be shown in the experimental results.
4.3 Experimental Results

To characterize the system, a 5V-to-1.5 V, 2.5 A, 1 MHz experimental prototype was created based on Figs. 51 and 54. The performance of the prototype was compared to a conventional buck prototype having the same switching frequency and power ratings. The power stages of both prototypes are formed of discrete transistors, gate drivers, and filter components. The controller is based on a field-programmable gate array system and discrete components. To compare the inductor volumes, the inductors from the same production line are selected, such that the current ripple is about a 20% of the rated current. This results in a 1.0-μH (5.1A/24mΩ, 3.6mm×3.0mm×2.0 mm) inductor for the buck and a 0.56 μH (5 A/22mΩ, 3.6mm× 3.0mm × 1.2 mm) for the BCMCA, i.e., about 40% reduction. The output capacitors are selected using Eq. 21, such that for the maximum load step ΔI_max = 1.5A (exceeding common testing requirements of 50% I_max [81]), the voltage deviation is no larger than 50 mV. The capacitances of 14 and 9 μF for the conventional buck and the BCMCA, respectively, are obtained taking into account system delays, which are about 400 ns. The reactive component characteristics are compared in-depth in Table 3.

Table 3 Output filter characteristics of the BCMCA and buck converter experimental prototypes

<table>
<thead>
<tr>
<th>Converter</th>
<th>BCMCA</th>
<th>Buck</th>
<th>Diff (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inductor value</td>
<td>0.56 μH</td>
<td>1.0 μH</td>
<td>-44%</td>
</tr>
<tr>
<td>Inductor volume</td>
<td>13 mm³</td>
<td>21.6 mm³</td>
<td>-40%</td>
</tr>
<tr>
<td>Inductor height</td>
<td>1.2 mm</td>
<td>2.0 mm</td>
<td>-40%</td>
</tr>
<tr>
<td>Inductor resistance</td>
<td>22 mΩ</td>
<td>24 mΩ</td>
<td>-8%</td>
</tr>
<tr>
<td>Inductor cost</td>
<td>$0.718⁵</td>
<td>$0.838⁶</td>
<td>-14.3%</td>
</tr>
</tbody>
</table>

⁵ Calculated using www.digikey.ca online price database, assuming 6,000 unit price break, for component 541-1326-1-ND on 7/22/2013

⁶ Calculated using www.digikey.ca online price database, assuming 6,000 unit price break, for component 541-1319-1-ND on 7/22/2013
As discussed in the previous section, the BCMCA switches SW₃ and SW₄ are rated for a half of the conventional buck SR blocking voltage. The blocking voltages of SW₁ and SW₂ are larger than optimal \( \frac{1}{2} v_g(t) + \text{forward voltage drops of the body diodes} \), due to limited availability of discrete components. The MS of the conventional buck and SW₁/₂ are identical, blocking the full input voltage.

### 4.3.1 Steady-State and Dynamic Operation

Fig. 59, showing steady-state waveforms of both converters, verifies that the reduction of the inductor has no influence on the current ripple. It can be seen that the ripples of both converters are approximately the same, even though the BCMCA inductor is 44% smaller. It can also be seen that the BCMCA has a larger output voltage ripple, due to the smaller output capacitor. The rms value of this ripple is still significantly smaller than a 1% of the rated output, commonly seen in state-of-the-art solutions [81].

---

\[<\text{Table: Output capacitor values}>\]

<table>
<thead>
<tr>
<th></th>
<th>9 ( \mu F )</th>
<th>14 ( \mu F )</th>
<th>-36%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output capacitor value</td>
<td>2.5 mm³</td>
<td>3.6 mm³</td>
<td>-31%</td>
</tr>
<tr>
<td>Output capacitor volume</td>
<td>$0.0352\text{\textsuperscript{7}}$</td>
<td>$0.156\text{\textsuperscript{8}}$</td>
<td>-77.4%</td>
</tr>
<tr>
<td>Output capacitor height</td>
<td>1 mm</td>
<td>1.45 mm</td>
<td>-31%</td>
</tr>
<tr>
<td>LC volume</td>
<td>17.3 mm³</td>
<td>30.6 mm³</td>
<td>-43%</td>
</tr>
<tr>
<td>LC height</td>
<td>1.2 mm</td>
<td>2 mm</td>
<td>-40%</td>
</tr>
<tr>
<td>LC cost</td>
<td>$0.753$</td>
<td>$0.994$</td>
<td>-24.3%</td>
</tr>
</tbody>
</table>

\[<\text{Notes:}>\]

\textsuperscript{7} Calculated using www.digikey.ca online price database, assuming 100,000 unit price break, for component 445-14554-1-ND on 7/22/2013

\textsuperscript{8} Calculated using www.digikey.ca online price database, assuming 100,000 unit price break, for component 445-14555-1-ND on 7/22/2013
Fig. 60 also confirms proper operation of the unified controller (see Fig. 51). Both the center-tap voltage of the capacitive attenuator and the output of the buck are tightly regulated. The figure also demonstrates operation of the charge balance algorithm described in Section 4.1.1. It can be seen how the switching pattern of \( SW_1 \) and \( SW_2 \) is varied to maintain a constant center-tap voltage. To eliminate a possible jitter in duty ratio, the center tap voltage comparator with a relatively small hysteresis is used. As a result, the voltages of both attenuator capacitors are kept approximately the same and, consequently, no significant difference in the duty ratio during mode transitions (see Figs. 53 and 54) occurs.

In Fig. 61, the responses to a 1.5-A light-to-heavy load step of both systems are compared. In both cases, minimum-deviation response control method is applied. It can be seen that the inductor current slew rate of the two-stage converter is increased by applying the full input voltage, i.e., bypassing the attenuator, as described in Section 4.1. The results demonstrate that, although a much smaller output capacitor is used, the BCMCA has the same voltage deviation as the conventional buck and about a 25% faster response.
Figure 61. Response to a 1.5-A light-to-heavy load step of (left) the conventional buck and (right) BCMCA. Ch.1: Inductor current $i_L(t)$, 1A/div; Ch. 2: Buck converter switching node voltage $v_{Lx}(t)$, 5V/div; Ch. 4: Output voltage $v_{out}(t)$, 50 mV/div-ac; The time scale is 5 $\mu$s/div.

4.3.2 Efficiency Comparison

Fig. 62 shows comparison of the efficiency for both converters over the full operating load range as well as a breakdown of the losses.

Figure 62. Efficiency curves and breakdowns of the losses for the conventional buck and the BCMCA (experimental and optimized); $P_{sw}$ indicates switching losses, $P_{drc}$ conduction losses of the inductor, and $P_{rdson}$ conduction losses of the switches.
At light-to-medium loads, where the switching losses are dominant, the BCMCA has up to 15% better efficiency. At heavier loads, the reduction in switching losses is partially canceled by increased conduction losses. The increased conduction losses are mostly caused by discrete implementation and, consequent, suboptimal voltage ratings of the transistors $SW_1$ and $SW_2$. Still, at the full load, the efficiency of both converters is the same and the higher efficiency of the BCMCA is maintained throughout the entire operating range. The suboptimal discrete implementation also has influence on the other losses of both converters resulting in lower efficiency than that of the integrated solutions [82]. To compare the efficiencies for optimized case, the efficiency of the BCMCA is calculated and plotted in Fig. 62 as well (red dotted line and box). The calculation is based on the analysis given in [77] and [78] assuming that $SW_1$ and $SW_2$ are rated for the optimal blocking voltage of 3.7V, as described in the previous section. The combined resistance of $SW_1$ and $SW_2$ case is 42% larger than that of the buck MS [calculated from (22)] for the same silicon area. This can further improve efficiency, as shown in the diagram, and reduce the size of the suboptimal BCMCA prototype, for which both the resistance and silicon area of $SW_1$ and $SW_2$ are two times larger than that of the buck MS.
Conclusions and Future Work

This thesis presents two new practical volume-reduction strategies for low-power high-frequency SMPS. Compared to traditional solutions, the control-based and topology-based strategies, achieve reduced SMPS volume without sacrificing power processing efficiency or hardware simplicity.

5.1 Minimum-Deviation Controller

A practical minimum-deviation digital controller IC for single and dual-phase high-frequency dc-dc switching converters is introduced. The IC combines a very simple parameter insensitive transient suppression algorithm with a novel architecture of the ADC to obtain a cost-effective implementation.

In steady-state the IC operates as a conventional digital pulse-width modulated voltage-mode controller. During transients it activates the suppression logic. The suppression logic reconstructs the inductor current such that both its dc and ripple components match those in the new steady state. The full voltage recovery task is then passed to the steady-state compensator. Such an arrangement results in a very simple hardware implementation. The suppression logic only utilizes a readily available duty ratio value and performs a single division by two, through binary shifting.

The self-calibrating asynchronous ADC only uses four comparators, a low-gain amplifier, and several transistors. Its operation is based on the track-and-hold principle and the construction of a moveable comparison window around the amplified error signal. To cancel any accumulated error, the ADC utilizes a self-calibration process that is performed during the input signal zero voltage crossings.
The IC also incorporates two new elements that minimize effects of the power stage losses and system delays. The first is adaptive duty ratio correction logic. The corrector compensates for the duty ratio variations due to the converter losses, which can cause mode transition-related stability problems. It uses a simple dynamically updatable look-up table to estimate changes in the duty ratio value, based on the size of the current step, and, accordingly, corrects the switching sequence. The second element is a dual peak/valley detection block. It minimizes the effects of system delays during transients. The detection block captures the capacitor current zero crossings when the inductor current slew is the lowest and, consequently, the effect of the system delays minimized.

Also in the chapter a circuit that reduces the effects of the output capacitor ESR and, at the same time, improves detection of the load transient and peak/valley point is proposed.

The IC is implemented in a 0.18 µm CMOS process, on a silicon area no large than that of the state-of-the-art analog solutions. Experimental results obtained with the IC verify minimum deviation response and stable mode transitions for various operating conditions. The voltage deviation is about four times smaller than that of a fast PID compensator having a 1/10th of the switching frequency bandwidth, allowing for a four-fold reduction of the output capacitor.

5.1.1 Future Work

The minimum-deviation controller concept can be further improved through three branches of research. The first could be directed towards hardware efficient integration of the ESR estimation circuit. The expected difficulties will be due to analog component variations and their effect on system operation. The second branch of research could investigate modifications required for the minimum-deviation response in case of input voltage disturbances. Finally, the third branch of research could investigate application of this concept for converters with indirect energy transfer. Due to the indirect energy transfer accurate detection of the ‘peak/valley’ points become be more challenging and worthy of investigation.
5.2 Merged-Capacitive Attenuator

The BCMCA introduced in Chapter 4 has a smaller output filter and lower switching losses than the conventional buck. The savings are obtained by reducing the difference between the input and output voltage with a capacitive attenuator, whose center-tap voltage is regulated with the buck inductor current and a simple digital controller. Consequently, an extra capacitor existing in other systems combining a capacitive converter and an inductor-based power stage is eliminated. The attenuator controller, which is merged with that of the buck, implements a charge-control algorithm where the center-tap voltage is regulated by redirecting the current of the buck inductor. Also, to minimize conduction losses, the switching components of the attenuator and the buck converter are shared and advantages of transistor operating at lower blocking voltages utilized. Experimental results comparing the BCMCA with a conventional buck show 43% smaller reactive component volume, 25% faster settling time, and significantly improved light-to-medium load efficiency.

5.2.1 Future Work

In order to fully realize the benefits of the BCMCA architecture, IC integration is required such that optimized transistor design can be achieved. As such, future research could attempt to implement and characterize the performance of an IC with optimized BCMCA. Furthermore, variable capacitive-attenuation factor input stages can potentially be analyzed, and satisfactory performance under a wider ultra-wide input-to-output voltage conversion ratios confirmed.

A longer-term research could focus on the extension of concept to common ground and/or multiphase interleaved implementations. Such research would require the development of a different downstream stage and mode selection algorithm. However, the benefits of a successful design would be far-reaching and as such worthy of investigation.
A. NONINVASIVE SELF-TUNING OUTPUT CAPACITOR TIME CONSTANT ESTIMATOR FOR LOW POWER DIGITALLY CONTROLLED DC-DC CONVERTERS

A1. INTRODUCTION

In realistic dc-dc converters the output capacitors often have a non-negligible equivalent series resistance that, together with the capacitance value, form the output capacitor time constant [10, 44, 52]. An accurate estimation of that constant and/or emulation of the realistic capacitor behavior is of a key importance for fast transient response control methods, as was shown throughout Chapter 3. However, the non-invasive estimators usually utilized in these applications can exhibit significant estimation errors during operating conditions changes.

The main goal of this appendix is to propose a hardware-efficient self-tuning passive estimator that does not suffer from the estimation errors. The new solution which is labeled as $R_{eq}C$ estimator in Fig.63, builds upon the non-invasive estimator used in [10, 44, 52], where a small high-impedance RC circuit is placed in parallel with the output capacitor. In this case, to provide self-tuning capability, this RC circuit has an adjustable resistor, $R_{adj}$, which is tuned continuously using only the knowledge of the two steady-state capacitor zero-current crossing points and synchronization with the digital pulse width modulator.

In the following section, the operation of the introduced output capacitor time-constant estimator is presented. Section A3 discusses issues related to the practical implementation. Section A4 presents experimental verification.

---

A2. PRINCIPLE OF OPERATION

The self-tuning time constant estimator of Fig. 63 operates on the well-known time constants matching principle utilized in non-invasive estimation methods and in the RC based inductor current estimation methods [83, 84]. In these systems, an RC filter is placed in parallel with a non-ideal element whose current is estimated. For the case when the time constants of the output capacitor and the filter are the same, the currents going through both elements have the same wave shapes and no delay between them can be noticed.

The system of Fig. 63 utilizes a miniature filter consisting of a capacitor $C_{adj}$, which is much smaller than the power stage capacitor $C$, and a variable resistor $R_{adj}$ whose value is much larger than the equivalent series $R_{esr}$. This estimator periodically adjusts the $R_{adj}$ value, such that $C_{adj}R_{adj} = CR_{esr}$. The estimation is performed during converter steady state only. During transients the operation of the estimator is suspended, i.e. it is placed in a sleep mode.
In order to match the $C_{adj}R_{adj}$ and $CR_{esr}$ time-constants, this estimator takes advantage of the buck converter steady-state capacitor current waveform. Namely, the fact that during steady-state the capacitor current, $i_c(t)$, shown in Fig. 64, has a triangular waveform with two well-defined zero crossing points. The first zero crossing occurs at $dT_{sw}/2$ and the second at $(1+d)T_{sw}/2$, with respect to the beginning of the switching cycle [7], where $d$ is the duty ratio value and $T_{sw} = 1/f_{sw}$ the switching period. For the case when $C_{adj}R_{adj} = CR_{esr}$, the small current going through the filter, $i_\ell(t)$, will have the same wave-shape and zero crossing points. This also means that the voltage drop across $R_{adj}$ ($v_{Radj}$ in Fig. 62) will only have the zero crossing points at $dT_{sw}/2$ and $(1+d)T_{sw}/2$ when the two time constants are matched.
Figure 64. Key waveforms of the digital controller and the self-tuning estimator. Top-to-bottom: \( v_{Radj} \) - voltage across the estimator resistor, \( i_{c}(t) \) – the output capacitor current and \( c(t) \) – signal produced by the DPWM.
This observation is used in the self-tuning process of the estimator shown in Fig. 62. It has a synchronous comparator that monitors the voltage drop across $R_{adj}$. This comparator is triggered by the digital pulse-width modulator (DPWM), at one of the output capacitor zero crossing points, and, accordingly, the $R_{adj}$ is adjusted until the zero value at the input of the comparator, i.e. time constants matched condition, is detected. In this way, the need for costly capacitor current sensing and actual comparison of $i_c(t)$ and $v_{Radj}$ is eliminated.

When the two time-constants are not equal the resistor voltage $v_{Radj}$ takes one of the two forms shown in Fig. 62. For the case when $R_{adj}C_{adj} < R_{esr}C$, the zero crossing of $v_{Radj}$ occurs before the output capacitor current zero crossing and for $R_{adj}C_{adj} > R_{esr}C$ it happens later.

Therefore, by simply measuring the polarity of the $v_{Radj}$ value at one of the two zero crossing points, the time-constant can be adjusted such that it converges to a value equal to the output capacitor.

A3. PRACTICAL IMPLEMENTATION

A practical realization of the estimator is shown in Fig. 65. It consists of an operational amplifier, a binary-weighted resistive network, four small transistors, a comparator, a sample and hold circuit S/H, and simple digital logic.
The amplifier with a relatively low-gain and a low-bandwidth is used to eliminate the high frequency switching noise and increase the estimator input when operating with low output voltage converters. This amplification improves the zero crossing point detection, reducing comparator speed and, consequently, power requirements.

The polarity of $v_{\text{Radj}}$ at the zero capacitor crossing points is determined through the sampled comparator value $\text{comps}$. The comparator is sampled once per cycle, using information about the digital equivalent of the duty-ratio value, $d[n]$, from the control loop (Fig.62). Accordingly, the equivalent $R_{\text{adj}}$ value is adjusted using the binary-weighted resistive network and the estimator logic of Fig. 65 [85].
In order to minimize any switching noise effects, the second sampling point, \(((1+d)T_{sw}/2)\), is used when the duty ratio is less than 0.5. In most of the targeted applications the duty ratio is significantly smaller than 0.5. Therefore, for the following analysis the second sampling point is used.

When \(\text{comp}_s\) is low, the \(R_{adj}\) is increased and when \(\text{comp}_s\) is high, the \(R_{adj}\) value is reduced. In order to speed up the tuning process during the start-up, when a large initial time-constant error is likely, a binary search algorithm is utilized [36]. The binary search algorithm changes the resistance in larger steps, significantly reducing the worst case tuning time, from 15 cycles, needed for the linear search, to 4 cycles. Once the start-up mode is finished a linear, finer, search algorithm is applied until the time-constants are matched. This condition is indicated by hi-lo or lo-hi transition of the S/H output. At this point the estimator enters sleep mode and only occasionally is re-engaged upon the exit of a transient or after a pre-defined wait time.

In order to minimize the estimation error due to the gate driver transmission delay a simple delay measuring circuit, shown in Fig. 66, can be utilized. It counts the number of clock cycles, \(t_{clk}\), between the DPWM control signal, \(c(t)\), and the switching node rising edge, \(v_x(t)\). The digital representation of the total gate driver and converter turn-on time delay, \(t_{delay}[n]\), is then added to the nominal sampling point, thus eliminating its effect.

Figure 66. Circuit for estimating gate driver and converter turn-on delay.
A4. EXPERIMENTAL RESULTS

To verify the operation of the estimator a 5V-to-1V, 5A, 500 kHz, digitally controlled, buck converter prototype was built based on the diagrams of Figs. 63 and 64. The converter has a 1.5µH output filter inductor and a 100 µF ceramic output capacitor with Resr ≈ 25mΩ. To form the estimator filter, a small 2 nF capacitor and a resistive network covering 640 to 9600 Ω range of values are used.

This network allows for variation of the estimator time constant over the full range of expected CR_{esr} variations. The results of experimental system verification are shown in Figs. 67 and 68. Figure 67 illustrates how the R_{adj}[n] control value, described in the previous section, is changing during the auto tuning process. It can be seen that, unlike invasive solutions, this estimation method does not affect the output voltage regulation and that the system stability is maintained throughout the full operating range. Figure 68 shows zoomed-in capacitor current and the estimator voltage before and after the tuning, respectively.

![Figure 67. Key waveforms of the digital controller and the self-tuning estimator. Top-to-bottom: i_c(t) (10 A/div), v_{Radj} (200 mV/div), output voltage of the converter v_{out} (500 mV/div), comp_s -](image-url)
sampled comparator output, enable- estimator enable bit, and $R_{adj}[n]$ binary resistor control value. Time-scale (20μs/div).

The results demonstrate the effectiveness of the estimator. It can be seen that the delay between zero crossings of $i_c(t)$ and $v_{adj}(t)$ has been reduced from 500 ns, indicating a large mismatch in time constants, to 40 ns, corresponding to practically tuned filter.

Figure 68. Actual and estimated output capacitor ESR voltage before (left) and after (right) the tuning process. Top-to-bottom: $i_c(t)$ – the output capacitor current (2.5 A/div), $v_{Radj}$ - voltage across the estimator resistor (50 mV/div), comp – sampled comparator output, $R_{adj}[n]$ – binary-weighted representation of the resistor. Time-scale – 500ns/div.

A5. CONCLUSION

A hardware-efficient noninvasive output capacitor time-constant estimator for low-power digitally controlled dc-dc converters is presented. The estimator operates on a simple principle of detecting the mismatch between the estimator output and the output capacitor zero value crossings. To eliminate the need for costly capacitor current sensing, the mismatch detection is performed through synchronization with the digital pulse-width modulator. Experimental results verify accurate on-line tuning that is not affecting the output voltage regulation.
B. ANALOG-TO-DIGITAL CONVERTER FOR INPUT VOLTAGE MEASUREMENTS IN LOW-POWER DIGITALLY CONTROLLED SWITCH-MODE POWER SUPPLY CONVERTERS

B1. INTRODUCTION

To obtain a digital equivalent of the input voltage, which can vary over a wide range, conventional general-purpose ADCs [86] are not the most suitable solution. The silicon size and power consumption of these systems are often significantly larger than those of the entire application specific controller [33] and, as such, prohibitive in the targeted low-power cost-sensitive application.

Hardware-efficient application specific ADCs for the SMPS output voltage measurement consuming low power and taking a very small fraction of the controller silicon area [34, 70] are also not suitable for this application. They operate around a confined output voltage reference window and cannot cover the much wider range of the input voltage variations. Therefore, alternative hardware-efficient architectures of the input voltage acquisition are needed.

The main goal of this Appendix is to introduce a simple and accurate ADC architecture suitable for digitizing a wide range of input voltages. The ADC, shown in Fig.69, obtains information about the input voltage from an RC based circuit mimicking fine operation of an ideal buck converter.

---

In the following section operation of the new ADC architecture is described. A practical implementation of the ADC is shown in Section B3. In this section, an estimation of the silicon size needed for on-chip implementation is given as well.

Figure 69. Proposed ADC architecture (outlined in red) used.
Section B4 describes an experimental system implementation and presents results showing a fast and accurate ADC operation.

**B2. Principle of Operation**

Ideally, in a lossless buck converter operating with a feedback loop containing an integrator the input voltage $V_{in}$ can be estimated based on the steady state duty ratio value $D$ and the reference voltage $V_{ref}$, as

$$V_{in} = \frac{V_{ref}}{D}. \quad (23)$$

For a realistic converter of Fig. 69, containing switching and conduction losses that affect the duty ratio value, such a simple estimation of the input voltage cannot be achieved. The duty ratio of the realistic converter changes with the load current and cannot be directly used for an accurate input voltage measurement.

To overcome this problem in the system of Fig. 69, an RC-based circuit mimicking the dc operation of an ideal closed-loop buck converter, from the conversion ratio perspective, is placed next to the main feedback loop of the buck converter. The RC circuit is driven with a set of small complementary transistors $SW_1$ and $SW_2$ and their operation is controlled with a digital feedback loop containing a small windowed based ADC ($ADC_2$), an integrator, and one port of a dual $DPWM$. All of these elements and a look up table of Fig. 69 form the new ADC architecture for the input voltage measurement.

The feedback loop of the input voltage ADC produces the duty ratio control value $d_2[n]$ that regulates the operation of the switches. The switches are controlled such that the output voltage of the $RC$ filter has the same dc value as the main buck stage, i.e. $<V_{RC}(t)> = V_{ref} = d_2V_{in}$, as shown in Fig. 70 that also demonstrates other key waveforms of the $RC$ filter.
Then, the digital equivalent of the analog input value $V_{in}[n]$ is found by mapping $d_2[n]$ through the look up table implementing the following nonlinear equation:

$$V_{in}[n] = \frac{V_{ref}}{d_2[n]}.$$  \hspace{1cm} (24)

**B3. Practical Implementation**

Quantization effects can play a significant role in the proper and accurate operation of digital systems. For that reason they are analyzed in this section. From (24) we can see that the accuracy of the input voltage estimates is inversely proportional to the digital duty value resolution. Further insights can be gained by analyzing the small-signal properties of (24), giving us

$$\left(V_{in} + \Delta V_{in}\right) \cdot \left(d_2 - \Delta d\right) = \left(V_{ref} \pm \frac{\Delta V_q}{2}\right)$$  \hspace{1cm} (25)

where $\Delta V_{in}$ is an input voltage change, $\Delta d$ is the resulting duty cycle change, and $\Delta V_q$ is the Windowed ADC$_2$ quantization voltage. If we treat the $\Delta d$ as the minimum duty cycle variation (DPWM resolution), then we can ensure limit-cycle free operation [38] as long as the quantization voltage $\Delta V_q$ is greater than
\[ \Delta V_q = \Delta d \cdot V_{in}^{MAX} \]  

(26)

where \( V_{in}^{MAX} \) is the maximum input voltage. By combining (24), (25) and (26) we can derive the relationship between the maximum input voltage estimate error and the DPWM resolution, given by

\[
\text{error} = \frac{\Delta V_{in}}{V_{in}} = \frac{V_{in}^{MAX}}{2V_{in}} \cdot \frac{1}{V_{ref}} \cdot \frac{1}{\Delta d} - 1 \approx \frac{\Delta d}{V_{ref}} \cdot \left( \frac{V_{in}^{MAX}}{2} + V_{in} \right).
\]

(27)

The worst-case error will occur when the input voltage is the largest, and is illustrated in Fig. 71 for a system with maximum input voltage equal to 3.3V and reference voltage equal to 1.5V.
B4. EXPERIMENTAL RESULTS

In order to verify the operation of the proposed system a 3W, 500 kHz 3.3V-1.8V input voltage to 1.5V output voltage dc-dc buck converter, discrete input voltage ADC and FPGA based controller prototype were implemented with discrete components. The Dual output DPWM resolution has an 8-bit effective resolution for both channels. To quantify the accuracy of the proposed system two separate load conditions were applied while varying the input voltage in the range of 1.8V to 3.3V. The results are compared to the input voltage estimate obtained using only the SMPS steady-state duty ratio value, $d[n]$, referred to as passive.

Figure 72 illustrates the input voltage estimate under zero-load current condition, both methods exhibit worst case 1.5% error.
Figure 72. Input voltage estimates for zero-load current condition.

Figure 73 shows the case for the maximum load condition, 2.15A. Due to the increase in conduction losses, the input voltage estimation obtained using the SMPS steady state duty ratio value \(d_{[n]}\) exhibits a 20% worst-case error. On the other hand, the proposed method input voltage estimate maintains accuracy within 1.5%.
To verify the dynamic performance of the proposed system, the input voltage of the converter was changed abruptly from 3V to 1.5V, the minimum possible input voltage. Then the output of the proposed ADC was fed into a DAC to demonstrate the analog comparison. As is shown in Fig. 74, the proposed input voltage ADC accurately tracks the change in input voltage and reaches the correct value within 260 us.
Figure 74. Input voltage tracking for the proposed ADC. The digital values are represented in HEX format for integer and fractional parts separately.

Figure 75 presents the dynamic response for a more practical input voltage step. The input voltage ADC is able to accurately track the signal at all points.
B5. CONCLUSION

A simple yet accurate implementation of an input voltage ADC for digitally controlled SMPS converters is proposed. The accuracy of the system is experimentally characterized using a discrete buck converter over the wide operating range of input voltage and load current variation, exhibiting worst-case measured error of 1.5%.
[1] “Voltage regulator module (VRM) and enterprise voltage regulator-down (EVRD) 11.0,” Intel Corp., Oregon, USA.


[14] “ISL6545 data sheet,” Intersil Corporation, Milpitas, USA.


[17] “LTC3851 data sheet,” Linear Technology Corporation, Milpitas, USA.

[18] “TPS40180 data sheet,” Texas Instruments, Dallas, USA.


[24] “MIC2130 data sheet,” Micrel Incorporated, San Jose, USA


[69] “FDMF8700 data sheet,” Fairchild Semiconductors, San Jose, USA.


[81] DELPHI DNT04 2.4-5.5Vin/0.75-3.63Vo/3 A non-isolated point of load datasheet, Delta Electronics Inc., Taipei, Taiwan, 2008.


[86] 1 MSPS 10-bit ADCs, AD7477 Data Sheet 2006 , Analog Devices