Design and Optimization of Power MOSFET Output Stage for High-Frequency Integrated DC-DC Converters

by

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A thesis submitted in conformity with the requirements for the degree of Master of Applied Science

Graduate Department of Electrical and Computer Engineering
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Abstract

Switching device power losses place critical limits on the design and performance of high-frequency integrated DC-DC converters. Especially, the layout of metal interconnects in lateral power MOSFETs has a profound effect on their on-resistances and conduction power losses. This thesis presents an analytical interconnect modeling and layout optimization technique for large-area power MOSFETs. The layout optimization of 24V LDMOS transistors in the area of 1 mm² has achieved an improvement of 55% in its on-resistance. The simulation result has been verified by experimental measurements on a test chip fabricated in TSMC 0.25 μm HV CMOS technology. In addition, this thesis presents an optimized output stage design methodology for the implementation of a 4 MHz, 12V to 1V integrated DC-DC converter. A segmented output stage scheme is employed to increase the converter efficiency at light load conditions. The peak efficiency of 84% was achieved at load current of 2 A.
Acknowledgments

Firstly, I would like to express my sincere gratitude towards my research supervisor, Professor Wai Tung Ng. This thesis would not have been possible without his guidance, encouragement and patience, not to mention his wide-ranging expertise in power electronics and fabrication technologies. His vision in the area of power devices and smart power applications has been invaluable in shaping my passion and career choices. In times of struggle, he has provided me with insightful suggestions and was always open to my frequent drop-in visit discussions. I have very much enjoyed working in the Smart Power Integration & Semiconductor Devices Research Group under his strong leadership.

Next, I would like to thank my fellow graduate students and researchers for creating a unique and enjoyable work environment as well as their companionship along the way, namely; Abraham Yoo, Jing Wang, April Zhao, Ke Cao, Andrew Shorten, Shuang Xie, Gang Xie, Masahiro Sasaki, Jingshu Yu, Jingxuan Chen, and Ning Yang. In particular, I would like to express my appreciation to Abraham Yoo who provided me with numerous rich discussions and feedbacks during my initial stage of research.

I would also like to thank TSMC for providing me with various IC fabrication support, and also Silicon Frontline for an academic license and technical support in using their R3D, resistive 3D extraction and analysis simulation tools.

Lastly, the completion of this thesis will not only leave a deep impression on myself, but my parents also. They watched me from a distance as I worked towards my degree. Thus, I would like to convey a special thanks to my loving parents, Seungmyoung Lee and Jungsook Lee.
Table of Contents

Acknowledgments........................................................................................................ iii

Table of Contents......................................................................................................... iv

List of Tables ................................................................................................................ vi

List of Figures ............................................................................................................... vii

List of Glossary............................................................................................................. xi

List of Symbols ............................................................................................................ xiii

Chapter 1  Introduction ................................................................................................ 1

  1.1 Trends and Challenges in Power MOSFETs Technology ............................... 1

  1.2 Trends and Challenges in Integrated DC-DC Converters ............................ 4

  1.3 Research Objectives............................................................................................ 5

  1.4 Thesis Organization ............................................................................................ 5

Chapter 2  Power MOSFETs in Synchronous DC-DC Converters ......................... 7

  2.1 Power MOSFET Fundamentals ........................................................................ 7

  2.2 Power MOSFET Requirements for Integrated DC-DC Converters ............... 12

  2.2.1 Basic Operation of Synchronous Buck Converters .................................... 12

  2.2.2 Sources of Power Loss in Synchronous Buck Converters ........................ 14

  2.2.3 Performance of Power MOSFETs (Figure of Merit) .............................. 16

  2.3 Types of Power MOSFETs .............................................................................. 17

  2.3.1 Vertical Discrete Power MOSFETs ............................................................ 17

  2.3.2 Lateral Power MOSFETs .......................................................................... 18

  2.4 Parasitic Resistances in Lateral Power MOSFETs ......................................... 22

  2.5 Summary ............................................................................................................ 24

Chapter 3  Analysis and Optimization of Metal Interconnects in Large-Area Power

  MOSFETs..................................................................................................................... 26
3.1 Physics of Current Flow in Interconnects .......................................................... 27
3.2 SPICE Lumped-Element Layout Modeling ......................................................... 30
3.3 R3D Resistive Extraction and Analysis .............................................................. 36
3.4 Layout Optimization of HV 24V LDMOS in 1mm$^2$ .......................................... 42
  3.4.1 HV 24V LDMOS Test Device ...................................................................... 42
  3.4.2 Layout Optimization Variables ..................................................................... 45
  3.4.3 Layout Optimization Summary ..................................................................... 54
  3.4.4 Experimental Verification of Optimized Layout ........................................... 56
3.5 Summary ............................................................................................................. 58

Chapter 4  Design of Integrated Output Stage for High-Frequency DC-DC Converters ..... 60
  4.1 Switching Device Size Optimization ................................................................. 62
  4.2 Segmented Output Stage Design ...................................................................... 65
  4.3 Layout and Simulation Results ......................................................................... 66
  4.4 Summary ........................................................................................................... 71

Chapter 5  Conclusion and Future Work ................................................................. 72
  5.1 Conclusion ....................................................................................................... 72
  5.2 Future Work .................................................................................................... 72

References .............................................................................................................. 74
List of Tables

Table 3.1 Resistivity and Conductivity of Materials Used in Metal Interconnects ............. 27

Table 3.2 Comparisons of 5V Power MOSFETs in Multi-finger and Hybrid-waffle Layouts .................................................................................................................. 37

Table 3.3 Summary of the HV 24 V LDMOS Test Device...................................................... 42

Table 3.4 Physical Properties of the Test Devices................................................................... 57

Table 3.5 Comparison of Measured and Simulated $R_{ds,on}$ of Three Different Layout Designs .......................................................................................................................... 58

Table 4.1 Operating Conditions of the DC-DC converter for the output stage design........... 61

Table 4.2 SPICE extracted values of $R_{ds,on}$, $Q_G$ and $Q_{SW}$ of 24V LDMOS transistors........ 64

Table 4.3 Properties of segmented output stage power MOSFETs...................................... 68
# List of Figures

Figure 1.1 Evolution of power MOSFETs ................................................................. 2

Figure 1.2 Modern LDMOS technology benchmark: $R_{on,sp}$ vs. $BV_{DSS}$ ...................... 3

Figure 2.1 Ideal switching waveforms of a power switch device.................................... 7

Figure 2.2 Instantaneous power loss waveforms ($V_{DS} \times I_{DS}$) of power MOSFETs in switching applications........................................................................................................ 8

Figure 2.3 An equivalent circuit model for n-type MOSFET showing the parasitic capacitances and resistances ................................................................. 10

Figure 2.4 Turn-on and turn-off waveforms of power MOSFETs........................................ 10

Figure 2.5 Schematic of a synchronous buck converter. ................................................... 12

Figure 2.6 Ideal operating waveforms of a buck converter. .............................................. 13

Figure 2.7 Cross-sectional diagrams of (a) UMOS and (b) VDMOS.................................. 18

Figure 2.8 Low-voltage and high-voltage MOSFETs in modern HV CMOS technology [9]................................................................................................................ 19

Figure 2.9 Different layout styles of CMOS power MOSFETs: (a) Multi-finger, (b) Waffle, (c) Hybrid-waffle ................................................................................. 21

Figure 2.10 Lateral scaling limitation: (a) $R_{ds,on}$ vs. gate width (b) $R_{on,sp}$ vs. gate width... 23

Figure 3.1 Resistance of a straight piece of metal. ............................................................ 27

Figure 3.2 Current crowding effect near the contacts......................................................... 28

Figure 3.3 3D mesh of a metal interconnect (generated by Synopsys TCAD tools).......... 29

Figure 3.4 (a) Single MOS finger layout (b) Basic MOS multi-finger layout.................... 30
Figure 3.5 SPICE lumped-element model for a MOS finger with parasitic resistive components. .................................................................31

Figure 3.6 (a) Simulation results of $R_{\text{on,device}}$, $R_{\text{ds,on}}$, and $R_{\text{parasitic}}$ of a standard 5 V MOS finger using SPICE lumped-element model (b) Layout of a standard 5 V MOS finger. .................................................................................................32

Figure 3.7 (a) Simulation results of $R_{\text{on,device}}$, $R_{\text{ds,on}}$, and $R_{\text{parasitic}}$ of HV 24 V LDMOS finger using SPICE lumped-element model (b) Layout of a HV 24 V LDMOS finger. .................................................................................................32

Figure 3.8 (a) TCAD structure of basic metal interconnects (b) TCAD simulation results of the current density distribution in metal interconnects. .................34

Figure 3.9 (a) SPICE lumped-element model of a cornered metal interconnect (b) Current density distribution of a cornered metal interconnect (simulated using R3D). .................................................................................................35

Figure 3.10 R3D simulation flow diagram. .................................................................36

Figure 3.11 Multi-finger structure within 60,000 $\mu$m$^2$: (a) Potential distribution in the top metal (b) Current density distribution in the top metal (c) $V_{DS}$ distribution of the device cells. .................................................................................................39

Figure 3.12 Hybrid-waffle structure within 60,000 $\mu$m$^2$: (a) Potential distribution in the top metal (b) Current density distribution in the top metal (c) $V_{DS}$ distribution of the device cells. .................................................................................................40

Figure 3.13 HV 24V LDMOS test device: (a) schematic (b) layout. .........................43

Figure 3.14 Basic arrangement of metal interconnect layers in multi-finger structure: (a) metal 3 to metal 2 interconnect (b) metal 2 to metal 1 interconnect. ............44

Figure 3.15 Potential distribution and current flow in metal 3 with three different source and drain terminations: (a) type A, (b) type B, (c) type C. ..........................46
Figure 3.16 $V_{DS}$ distribution with three different source and drain terminations: (a) type A, (b) type B, (c) type C. ................................................................. 46

Figure 3.17 Metal 1 optimization: (a) $R_{ds,on}$ vs. $W_{M1,source}$ (b) metal 1 geometry. ............... 48

Figure 3.18 Current density distribution in metal 2 source runners: (a) equally distributed metal 2 source runners (b) asymmetrical metal 2 source runners. 49

Figure 3.19 Current density distribution in metal 3 source runners: (a) equally distributed metal 3 source runners (b) asymmetrical metal 3 source runners. 50

Figure 3.20 Current density distribution in metal 3 source runners: (a) equally distributed metal 3 source runners (b) asymmetrical metal 3 source runners. 51

Figure 3.21 Current density distribution in the top metal with CUP design: (a) 1 to 1 aspect ratio (b) 1.9 to 1 aspect ratio (c) 4 to 1 aspect ratio. ......................... 53

Figure 3.22 $V_{DS}$ distribution with CUP design: (a) 1 to 1 aspect ratio (b) 1.9 to 1 aspect ratio (c) 4 to 1 aspect ratio. ................................................................. 53

Figure 3.23 Effects of metal interconnect resistance on $R_{ds,on}$ after the cumulative optimization at 25°C. .................................................................................. 54

Figure 3.24 Effects of metal interconnect resistance on $R_{ds,on}$ after the cumulative optimization at 85°C .................................................................................. 55

Figure 3.25 Die photo of the test chip fabricated in TSMC 0.25µm HV CMOS process. . 56

Figure 3.26 (a) Diagram of $R_{ds,on}$ measurement setup (b) Four-terminal sensing technique. ............................................................................................... 57

Figure 4.1 Simplified block diagram of the output stage IC for a 4 MHz, 12 V to 1.2 V DC-DC converter ............................................................................................ 60

Figure 4.2 Simulated gate charge characteristics of a 24 V LDMOS transistor ($W$ = 283000 µm)........................................................................................................... 63
Figure 4.3 Calculated efficiency of a 12 V to 1.2 V DC-DC converter with different HS and LS device sizes at 4 MHz switching frequency. ........................................... 64

Figure 4.4 Simulated efficiency of the 12 V to 1.2 V DC-DC converter with the optimum size switches at 4 MHz switching frequency. ........................................... 65

Figure 4.5 Ideal efficiency curves for increasing transistor size, \( W_1 < W_2 < W_3 \) ........... 66

Figure 4.6 Layout of the output stage IC fabricated in TSMC 0.25 HV CMOS process. ..67

Figure 4.7 Layout of top metal and locations of CUP pads................................................. 67

Figure 4.8 R3D simulation results of current density distributions in the top metal (LS switch)....................................................................................................................... 68

Figure 4.9 Simulated switching waveform of the DC-DC converter at 2 A load current (all segments enabled)......................................................................................... 69

Figure 4.10 Segmented output stage efficiency at 4 MHz switching frequency. ............... 70

Figure 4.11 Output stage efficiency with optimum number of enabled segments depending on load current................................................................. 70
### List of Glossary

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMOS</td>
<td>Complementary Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>CUP</td>
<td>Circuits Under Pads</td>
</tr>
<tr>
<td>DMOS</td>
<td>Double Diffused MOS</td>
</tr>
<tr>
<td>EDA</td>
<td>Electronic Design Automation</td>
</tr>
<tr>
<td>EDMOS</td>
<td>Extended Drain MOS</td>
</tr>
<tr>
<td>FOM</td>
<td>Figure of Merit</td>
</tr>
<tr>
<td>HS</td>
<td>High Side (Output Switch)</td>
</tr>
<tr>
<td>HVNW</td>
<td>High Voltage N-Well</td>
</tr>
<tr>
<td>HVPW</td>
<td>High Voltage P-Well</td>
</tr>
<tr>
<td>LDMOS</td>
<td>Lateral Double Diffused MOS</td>
</tr>
<tr>
<td>LS</td>
<td>Low Side (Output Switch)</td>
</tr>
<tr>
<td>MOS</td>
<td>Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal Oxide Semiconductor Field Effect Transistor</td>
</tr>
<tr>
<td>RESURF</td>
<td>Reduced Surface Field</td>
</tr>
<tr>
<td>SMPS</td>
<td>Switched Mode Power Supplies</td>
</tr>
<tr>
<td>SOA</td>
<td>Safe Operating Area</td>
</tr>
<tr>
<td>TCAD</td>
<td>Technology Computer Aided Design</td>
</tr>
<tr>
<td>UMOS</td>
<td>U-shaped Gate MOS</td>
</tr>
<tr>
<td>UTM</td>
<td>Ultra Thick Metal</td>
</tr>
<tr>
<td>Abbreviation</td>
<td>Description</td>
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<td>--------------</td>
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<tr>
<td>VDMOS</td>
<td>Vertical DMOS</td>
</tr>
<tr>
<td>VMOS</td>
<td>V-shaped Gate MOS</td>
</tr>
</tbody>
</table>
List of Symbols

$B V_{D S S}$: Saturated-Drain-Source Breakdown Voltage

$C_{G D}$: Gate to Drain Capacitance

$C_{G S}$: Gate to Source Capacitance

$C_{D S}$: Drain to Source Capacitance

$C_{i s s}$: Input Capacitance

$C_{o s s}$: Output Capacitance

$C_{r s s}$: Reverse Transfer Capacitance

D: Duty Ratio

$f_{s w}$: Switching Frequency

$I_{D S}$: Drain to Source Current

$I_{G}$: Gate Current

$I_{l o a d}$: DC Value of the Converter Load Current

M: Conversion Ratio

$\eta$: Efficiency

$P_{c o n d}$: Conduction Power Loss

$P_{g a t e}$: Gate-Drive Power Loss

$P_{l o s s}$: Total Power Loss

$P_{s w}$: Switching Power Loss

$Q_{G}$: Gate Charge
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Q_{GD}$</td>
<td>Gate to Drain Charge</td>
</tr>
<tr>
<td>$R_{ds,on}$</td>
<td>On-resistance (of Power MOSFETs)</td>
</tr>
<tr>
<td>$R_{on,sp}$</td>
<td>Specific On-resistance</td>
</tr>
<tr>
<td>$\tau_{off}$</td>
<td>Turn-off Time</td>
</tr>
<tr>
<td>$\tau_{on}$</td>
<td>Turn-on Time</td>
</tr>
<tr>
<td>$T_s$</td>
<td>Switching Period</td>
</tr>
<tr>
<td>$V_{DS}$</td>
<td>Drain to Source Voltage</td>
</tr>
<tr>
<td>$V_{DS,max}$</td>
<td>Maximum Drain to Source Voltage</td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>Gate to Source Voltage</td>
</tr>
<tr>
<td>$V_{IN}$</td>
<td>Input Supply Voltage</td>
</tr>
<tr>
<td>$V_{OUT}$</td>
<td>Output Voltage</td>
</tr>
<tr>
<td>$V_{TH}$</td>
<td>Threshold Voltage</td>
</tr>
<tr>
<td>$W$</td>
<td>Gate Width</td>
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</tbody>
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Chapter 1 Introduction

Over the last few decades, demand for energy efficient power integrated circuits has continued to increase for various electronic applications. Especially, with the popularity of portable electronic products, integrated DC-DC converters have become one of the most imperative ICs for maximum battery run-time. Integrated DC-DC converters consist of many different analog and digital functional blocks; however, power output stages typically occupy the largest silicon area, and play the most critical role in providing efficient power delivery.

Monolithic integration of power output stages with digital and analog control circuitries not only provides a reduction in the number of circuit components and physical size, but also improvement in efficiency, performance and reliability of the overall system [1]. As complementary metal-oxide-semiconductor (CMOS) technology has continued to be the dominant technology for fabricating integrated circuits, lateral power MOSFETs, which are CMOS process compatible, are widely used as the switching devices in portable power applications. In addition to the CMOS process compatibility, lateral power MOSFETs offer significant efficiency improvement in high frequency DC-DC converters due to their low gate charge \( Q_G \) [2]. Nevertheless, there exist practical limitations due to parasitic resistances in the metal interconnect in minimizing on-resistance of lateral power MOSFETs. This has been one of the major limiting factors in further improving performance of high-frequency integrated DC-DC converters.

In this thesis, performance improvements of lateral power MOSFETs by optimizing metal interconnect layout are effectively modeled, simulated and experimentally verified. Furthermore, a design methodology of an optimized power MOSFET output stage is demonstrated for the implementation of a high-frequency integrated DC-DC converter.

1.1 Trends and Challenges in Power MOSFETs Technology

Since the introduction of power MOSFETs in the late 1970s, there have been two distinct directions for the development of power MOSFET technologies. The first direction involves the development of discrete vertical power MOSFETs for medium to high voltage applications. These applications include automotive electronics, industrial power supplies, and motor controls.
The process technology for these high voltage applications has shifted from VMOS (V-shaped gate MOSFET) in the early 1970s, DMOS (Double-diffused MOSFET) in the 1980s, and to UMOS (U-shaped gate MOSFET) technology in the 1990s [4]. In the last decade, discrete vertical power MOSFETs have benefited from the improvements achieved in the trench technology and the implementation of vertical super-junction drift layers [5]. These efforts were aimed at improving the performance of MOSFETs by minimizing specific on-resistance \((R_{on,sp})\) while maintaining their voltage blocking capability \((BV_{DSS})\).

The second direction involves the development of lateral power MOSFETs for low voltage (less than 100 V) and smart power applications. LDMOS (Lateral Double-diffused MOS), RESURF (Reduced Surface Field) LDMOS, and sub-micron CMOS power MOSFETs belong to these lateral power MOSFETs, and their applications include DC-DC converters, low drop-out regulators, and power management ICs. The development of lateral power MOSFETs provided a monolithic integration of power devices and control circuits in CMOS technology. Therefore, power electronic systems have greatly benefited from the monolithic integration as it has offered efficient protection circuits, simple drive circuits, and various smart controls for efficiency improvements. Significant improvements in the performance of lateral power MOSFETs have been made by using RESURF techniques, source/drain engineering, and isolation engineering, as well as advances in CMOS lithography scaling.

![Diagram of power MOSFETs evolution](image)

Figure 1.1 Evolution of power MOSFETs [1] [6].
Modern LDMOS process technologies are benchmarked in Figure 1.2 by comparing the most discussed figure of merits (FOM) in power devices, \( R_{\text{on,sp}} \) and \( BV_{\text{DSS}} \). As shown in Figure 1.2, there are many competitive process technologies with similar FOM. There has been an about 20 percent improvement in \( R_{\text{on,sp}} \) within each generation every two to three years; however, they are reaching their intrinsic silicon limitations. Therefore, today’s LDMOS process foundries tend to differentiate themselves by focusing on characteristics such as robustness, and reliability.

In particular, metal interconnect processes have become as equally important as the silicon device. This is because lateral devices possess a significant resistive voltage drop in the metal interconnects while accommodating the lateral current flow. This affects not only the resistive power loss, but also the transistor operating condition in terms of “de-biasing”. The metal interconnect process and the characterization of its parasitic resistance has become one of the major challenges today, as very low on-resistance lateral power MOSFETs are needed for high efficiency power systems.

![Figure 1.2 Modern LDMOS technology benchmark: \( R_{\text{on,sp}} \) vs. \( BV_{\text{DSS}} \) [7] [8] [9] [10].](image-url)
1.2 Trends and Challenges in Integrated DC-DC Converters

In the past several years, consumer demands for portable electronic products such as cell phones, laptops, GPS, and tablet PCs have been rapidly increasing. In a portable electronic system, a battery is used as a central power source. In order to generate low-voltage power supplies for various digital and analog ICs in the system, high-efficient step-down and step-up DC-DC conversions are required from a single battery source. Since the battery capacity is limited in any portable electronic products, efficient power delivery from the battery to the system is very crucial to maximize the battery run-time. Due to their highly efficient power conversion, switch-mode DC-DC converters are widely used in mobile electronic products.

There has been a steady driving force within the industry towards higher switching frequency DC-DC converters due to two main benefits: smaller passive components and faster dynamic responses [11] [12]. However, operating at a higher switching frequency also means degradation on the efficiency of a DC-DC converter due to its higher switching and gate-drive losses. At higher switching frequencies, power devices need to be monolithically integrated with their gate drivers in order to minimize parasitic inductances at gate terminals. Monolithic integration also provides the designer with higher degrees of freedom in optimizing the size and layout of power devices and their gate-drive circuit design.

Lateral power MOSFETs are the best candidates for switch devices in the output stages of high frequency DC-DC converters. Their lower gate charge, in comparison to that of vertical power MOSFETs, allows DC-DC converters to operate at a higher switching frequency. Currently, the switching frequency is approaching to 2 to 3 MHz. However, in order to minimize conduction loss, the on-resistance of power MOSFETs needs to be very low (a few tens of mΩ). This means the size of power MOSFETs needs to be very large, and the parasitic resistance, which exists in the metal interconnects, contribute more to resistive conduction power loss. Moreover, large-area power MOSFETs exhibit higher switching and gate-drive losses due to their higher gate charge. Therefore, there exist complicated trade-offs which makes designing a high-frequency and high-efficient DC-DC converter very challenging.

The most important design consideration for a high-frequency DC-DC converter is simply the efficiency of power conversion. This requires an understanding of various power loss
mechanisms and an effective use of a collection of techniques to minimize these power losses. There are device-related design techniques such as device size optimization and interconnect layout optimization. There are also circuit-related design techniques such as gate-driver optimization and segmented output-stages. This thesis presents the design and optimization of a LDMOS power MOSFET output stage that can switch at 4 MHz for the implementation of 12 V to 1.2 V DC-DC converters.

1.3 Research Objectives

The objective of this research is to design and optimize power MOSFET output stages for high-frequency integrated DC-DC converters. This includes the development and demonstration of metal layout optimization techniques for large lateral power MOSFETs, and an optimized output stage design methodology to maximize the efficiency of DC-DC converters. Key research contributions which address these goals are highlighted below:

- Development of analytical layout modeling and systematic layout optimization techniques for minimizing parasitic resistance in a large-area lateral power MOSFETs using R3D simulation tools
- Successful demonstration of an optimized and segmented output stage for the implementation of a 12 V to 1.2 V DC-DC converter output stage switchable at 4 MHz

1.4 Thesis Organization

Chapter 2 provides an introduction to power MOSFET fundamentals and an expectation on its performance for hard-switching synchronous DC-DC converter applications.

Chapter 3 describes the analytical layout modeling of metal interconnects and layout optimization techniques for minimizing parasitic resistance in large-area lateral power MOSFETs. The experimental verification through a test-chip fabrication in TSMC 0.25 μm HV CMOS technology is also presented.

In Chapter 4, an optimized output stage design methodology for the implementation of a 4 MHz, 12 V to 1.2 V DC-DC converter is presented. An efficiency calculation method for selecting...
optimum sizes of switching devices and output stage segmentation for light load conditions are applied in order to maximize efficiency of the converter. The implementation and post layout simulation results of the output stage are also presented.

Finally, in Chapter 5, conclusion and suggestions for future work are presented.
Chapter 2  Power MOSFETs in Synchronous DC-DC Converters

The key component of integrated DC-DC converters is the output stage. The design of the output stage requires thorough understanding of the power devices’ breakdown voltage, current handling capability, switching speed and process compatibility. This chapter offers an introduction to power MOSFET fundamentals and describes the expectations on the performance of power MOSFETs in synchronous DC-DC converter applications. Special attention is made to CMOS compatible lateral power MOSFETs.

2.1  Power MOSFET Fundamentals

MOSFETs have been used as the basis of today’s integrated circuits. MOS transistors, which are specifically designed for high current, low on-resistance and high blocking voltage applications, are called power MOSFETs to distinguish them from their low-power, or small-signal transistor counterparts [13]. The basic operating principle of power MOSFETs is similar to that of low-power MOS transistors. Since most textbooks offer a relatively complete discussion of the MOS transistor operation, this section discusses the properties and operations of power MOSFETs from a power IC designer’s perspective.

![Ideal switching waveform of a power switch device.](image)

Figure 2.1  Ideal switching waveforms of a power switch device.
Power MOSFETs usually operate as switches. Figure 2.1 shows the ideal voltage and current waveforms for a simple power delivery. For an ideal power switch, the voltage drop during the on-state and the leakage current during the off-state are both zero, resulting in zero power dissipation. In addition, the power required for the transition between the on and off-state is also zero. However, in reality, power MOSFETs exhibit finite power losses with various different mechanisms. The instantaneous power loss waveform of power MOSFETs in switching applications is illustrated in Figure 2.2. More detailed analysis of different power loss mechanisms will be discussed later.

Figure 2.2 Instantaneous power loss waveforms (V_{DS} \times I_{DS}) of power MOSFETs in switching applications.

The turn-on and turn-off operation of power MOSFETs relies on the control of an inversion layer induced underneath the gate. For n-type MOSFETs, applying a positive bias to the gate drives positive mobile charges (holes) away from the silicon/oxide interface underneath the gate. If the gate bias is strong enough, negative mobile charges (electrons) gather at the silicon/oxide
interface, and an inversion layer (channel) is formed. The gate voltage, at this stage, is called threshold voltage ($V_{TH}$). The threshold voltage of a MOS transistor depends on several factors, including the gate electrode material, the doping of the backgate, the thickness of the gate oxide, the surface state charge density, and the oxide charge density [13]. The value of the threshold voltage can be calculated using theoretical equations describing the energy bending at the MOS interface [14]. However, a more accurate and empirical value of $V_{TH}$ is provided by the silicon foundries for everyday IC designers’ use.

During the on-state, power MOSFETs can conduct a large current between the drain and the source with a low drain to source voltage ($V_{DS}$). The power MOSFETs under these conditions are operating in the linear region and their behaviour can be explained by the Shichman-Hodges Theory [15]. The theory implies, the transistors behave like resistors by providing a linear relationship between $V_{DS}$ and $I_{DS}$. Therefore, the on-resistance ($R_{ds,on}$) is one of the most important properties of power MOSFETs as it is the direct source of conducting power loss through Joule heating. In theory, the on-resistance of power MOSFETs can be reduced to arbitrarily small values by increasing the gate width of the MOSFETs, for a given gate length. However, it requires a large silicon area. Therefore, the specific on-resistance, $R_{on,sp}$ ($R_{ds,on} \times Area$), is another important property to estimate the die cost, which is directly proportional to its area. In practice, the typical values of $R_{ds,on}$ for large power transistors varies from 50 to 500mΩ and are limited by parasitic resistances of the metallization system and bond wires [13].

During the off-state, power MOSFETs are required to withstand a large drain to source potential difference. The blocking capability of power MOSFETs is defined by the maximum allowable drain voltage ($V_{DS,max}$). However, the actual breakdown voltage of the device ($BV_{DSS}$), has to be higher than $V_{DS,max}$ in order to provide some design margin for unwanted voltage spikes during switching. All possible breakdown conditions in power MOSFETs have to be carefully studied by a designer, as they can lead to destructive triggering of the parasitic bipolar transistor and latch-up.
Switching performance of power MOSFETs is dictated by the value of gate and parasitic capacitances. The input capacitance ($C_{\text{iss}}$) of power MOSFETs is defined by the sum of the gate-to-drain capacitance ($C_{GD}$) and the gate-to-source capacitance ($C_{GS}$). The input capacitance governs the amount of charge that has to be transferred into the gate terminal in order to achieve the desired gate voltage ($V_{GS}$) level. The output capacitance ($C_{oss}$) is the sum of the gate-to-drain capacitance and the drain-to-source capacitance ($C_{DS}$), which governs the speed of the output transition. The gate to drain capacitance is also called reverse transfer capacitance ($C_{rss}$) which determines the amount of feedback from the drain to gate terminal during transition.
Figure 2.4 describes the turn-on and turn-off switching behaviour of power MOSFETs. During the turn-on, the drain current ($I_{DS}$) start to flow as the gate voltage exceeds $V_{TH}$. After that, $V_{GS}$ goes through the Miller plateau as it charges the Miller capacitance ($C_{GD}$). Once the Miller capacitance is fully charged, $V_{GS}$ increases again to the desired gate voltage. During the turn-off, the device goes through a reverse sequence of the turn-on event. The overlap of the drain current ($I_{DS}$) and the drain voltage ($V_{DS}$) produces switching power loss during both turn-on and off transitions. In both transitions, the Miller capacitance is particularly important as smaller $C_{GD}$ results in faster transition with less switching power loss.

Due to nonlinearity of the parasitic capacitances of power MOSFETs over the full range of relevant voltage and temperature, the gate charge ($Q_G$) is more useful when designing a gate driver. This is because the gate charge is relatively insensitive to the drain current and is quite independent of temperature [16]. The gate charge is defined as the amount of charge needed to be transferred at the gate terminal in order to reach a pre-defined $V_{GS}$ level to turn on the device. It provides a relatively simple design methodology for obtaining the desired switching time by using the following current and charge relationship [17],

$$Q_G = \int_{t_b}^{t_e} i_G \cdot dt ,$$  
Eq. 2.1

where $t_b$ is the initial time of switching, $t_e$ is the end time of switching, and $i_G$ is the current entering the gate terminal.

When a constant gate current ($I_G$) is employed, the equation can be further simplified as,

$$I_G = \frac{Q_G}{t_s} ,$$  
Eq. 2.2

where $t_s$ is the switching time period ($t_e - t_b$).

Another gate charge parameter ($Q_{GD}$), which is often called the Miller charge, is the amount of charge correlated with the Miller plateau. This is particularly important to estimate switching power loss because the overlap of $I_{DS}$ and $V_{DS}$ occurs mostly during the Miller plateau.
2.2 Power MOSFET Requirements for Integrated DC-DC Converters

This section provides the expectation on MOSFET performance for integrated DC-DC converter applications. It describes the basic operation of synchronous buck converters and three major power loss mechanisms associated with switching devices in the output stages. The parasitic effects due to metal interconnects in lateral power MOSFETs are also addressed.

2.2.1 Basic Operation of Synchronous Buck Converters

The synchronous buck converter is the most popular topology of Switched Mode Power Supply (SMPS) systems for low-voltage DC-DC conversion [18]. Figure 2.5 shows the schematic of a synchronous buck converter.

![Figure 2.5 Schematic of a synchronous buck converter.](image-url)

The high-side (HS) switch and the low-side (LS) switch are implemented using power MOSFETs and are labeled as M1 and M2 respectively. The synchronous buck converter operates
by periodically connecting the switching node ($V_{SW}$) to either the input power source ($V_{IN}$) or ground by controlling the switches M1 and M2. This produces a rectangular wave at the switching node ($V_{SW}$) with a duty cycle ($D$) and a period ($T_s$). The second-order low-pass LC filter provides an averaging function to produce the desired DC voltage to the output node ($V_{OUT}$). The ideal conversion ratio of this topology is defined as:

$$M = \frac{V_{OUT}}{V_{IN}} = D$$  \hspace{1cm} (Eq. 2.3) [18]

The ideal operating waveforms are as shown in Figure 2.6.

To ensure a fast dynamic response to any instant changes in power demand of the load, high switching frequency is required. At the same time, high switching frequency allows a reduction of the LC filter size, making the converter less expensive. The LC values required to achieve an output voltage ($V_{OUT}$) with a tolerance of $\Delta V_c$, and load current variation of $\Delta i_L$, are shown in the following equations [18].
2.2.2 Sources of Power Loss in Synchronous Buck Converters

There are a number of non-idealities in power MOSFETs that account for various power losses in a synchronous buck converter [19] [20] [21]. In this section, three major power loss mechanisms in power MOSFETs are discussed: conduction loss, switching loss, and gate charge loss.

**Conduction Loss**

The conduction loss of the converter resulted from the on-resistance, $R_{ds,on}$, of HS and LS power MOSFET switches during the load current ($I_L$) conduction. The conduction loss of HS and LS power MOSFETs can be calculated as follows:

$$P_{\text{cond}(HS)} = I_L^2 \cdot R_{ds,on(HS)} \cdot D \quad \text{(Eq. 2.6)}$$

$$P_{\text{cond}(LS)} = I_L^2 \cdot R_{ds,on(LS)} \cdot (1 - D) \quad \text{(Eq. 2.7)}$$

Conduction loss is directly proportional to $R_{ds,on}$ of the HS and LS switches. When designing a buck converter within a given cost and thermal limits, $R_{ds,on}$ of power MOSFETs is the primary variable that designers must consider. By increasing the gate width of power MOSFETs, $R_{ds,on}$ can be reduced to a few tens of milliohms. However, increasing the gate width requires a larger silicon area. Moreover, there exist diminishing returns in further increasing the size of power MOSFETs at some point due to the increase in gate capacitance and parasitic resistances in the metal interconnect.
In addition, temperature has a strong effect on $R_{ds,on}$ of power MOSFETs. As shown in Figure 2.7, $R_{ds,on}$ approximately increases 40% from 25°C to 85°C. The positive temperature coefficient compounds the conduction loss as temperature increases.

![Figure 2.7 Typical $R_{ds,on}$ versus temperature.](image)

**Switching Loss**

As shown in the turn-on and turn-off switching waveforms of the power MOSFETs in Figure 2.4, the HS and LS switches do not switch on and off instantaneously. There exist finite turn-on time ($\tau_{on}$) and turn-off time ($\tau_{off}$) that depend on the gate charge of power MOSFETs and the current slew rate of the gate drivers. During the turn-on and turn-off time, the overlap of drain-to-source current ($I_{DS}$) and drain-to-source voltage ($V_{DS}$) produces switching power loss. By using first order approximation of $I_{DS}$ and $V_{DS}$ waveforms, the switching power loss ($P_{sw}$) can be expressed as follows:

$$P_{SW} = f_{SW} \cdot V_{DS} \cdot I_{L} \cdot \frac{(\tau_{on} + \tau_{off})}{2}$$  \hspace{1cm} (Eq. 2.8)

where $f_{sw}$ is the switching frequency. The switching loss of the HS and LS transistors should be calculated separately if the sizes of HS and LS switches are different. Eq. 2.8 shows that the
switching loss is linearly proportional to the switching frequency and both the turn-on and turn-off times. As there is a push towards higher switching frequency, smaller gate charge of power MOSFETs, which ensures faster turn-on and turn-off transition, is necessary to minimize the switching power loss.

**Gate Drive Loss**

The gate drive loss is generated from the charging and discharging of input capacitance of the MOSFET switches at every switching cycle. The gate drive loss \( P_{gate} \) is modeled as shown in Eq. 2.9 [19].

\[
P_{gate} = f_{sw} \cdot V_{gs} \cdot (Q_{G(HS)} + Q_{G(LS)}) \quad \text{(Eq. 2.9)}
\]

Similar to switching loss, the gate drive loss also increases proportionally when the switching frequency increases. Therefore, power MOSFETs with smaller gate charge is necessary for higher frequency switching.

### 2.2.3 Performance of Power MOSFETs (Figure of Merit)

To evaluate various power MOSFETs, two figure of merits (FOM) have been introduced [22] [23]:

\[
FOM_1 = R_{ds,on} \cdot Q_G \quad \text{(Eq. 2.10)}
\]

\[
FOM_2 = R_{on,sp} \cdot Q_G \quad \text{(Eq. 2.11)}
\]

\( FOM_1 \) is a good indicator of general performance and efficiency, as it includes \( R_{ds,on} \) and \( Q_G \), which are two major contributors to conduction, switching, and gate drive losses. Since the specific on-resistance, \( R_{on,sp} \), is the product of multiplication of the silicon area and \( R_{ds,on} \), \( FOM_2 \) allows the implication of the die cost into \( FOM_1 \). Thus, \( FOM_1 \) and \( FOM_2 \) provide a direct comparison of different process technologies.
2.3 Types of Power MOSFETs

As discussed in previous sections, the efficiency of DC-DC converters largely depends on the performance of power MOSFETs. Therefore, appropriate choice of power MOSFETs is required to implement the output stage of a DC-DC converter. There are various types of power MOSFETs which are divided into two categories: vertical discrete power MOSFETs and lateral power MOSFETs.

2.3.1 Vertical Discrete Power MOSFETs

Vertical power MOSFETs are constructed with their source and drain on the top and bottom side of the silicon substrate, respectively. Examples of vertical power MOSFETs include UMOS (U-shaped gate MOS), and VDMOS (vertical double-diffused MOS). Structure of UMOS and VDMOS are as shown in Figure 2.8 [24]. While UMOS have a vertical channel formed by a trench etching technique for the U-shaped gate, VDMOS has a lateral channel underneath the gate formed through a double diffusion process [25]. Both UMOS and VDMOS have a drift region inside the substrate to support high breakdown voltage and to allow vertical current flows from the top source electrode to the bottom drain electrode.

Due to the efficient use of area using the vertical current flow, the specific on-resistance ($R_{on,sp}$) of vertical power MOSFETs is generally smaller than that of lateral power MOSFETs with similar voltage rating. On the other hand, vertical power MOSFETs have a larger gate-to-drain overlapping area, which leads to a larger gate-to-drain capacitance and gate charge. Thus, in comparison to lateral power MOSFETs, vertical power MOSFETs exhibit smaller conduction loss but higher switching and gate-charge loss under the same operating condition. In addition to a higher $Q_G$, there exist monolithic integration issues with the current CMOS technology due to the bottom drain electrode. Therefore, vertical power MOSFETs are not widely adopted for high-frequency and low voltage applications, unless more complicated up-drain connections are incorporated into the fabrication process.
2.3.2 Lateral Power MOSFETs

Lateral power MOSFETs include EDMOS (extended drain MOS), LDMOS (laterally diffused MOS) and sub-micron CMOS-based power MOSFETs. Lateral power MOSFETs have both source and drain terminals on the top surface of the silicon substrate, thereby producing lateral current flow [26]. Figure 2.9 shows the cross-sectional diagram of CMOS standard transistors and high voltage LDMOS transistors in a CMOS compatible technology [9]. The blocking capability ($BV_{DSS}$) of lateral power MOSFETs is generally related to its on-resistance ($R_{on,sp}$) by the following trade-off relationship:

$$R_{on,sp} \propto BV_{DSS}^{2.5} \cdot \Omega \cdot cm^2$$  \hspace{1cm} (Eq. 2.12) [27]

In order to enhance $BV_{DSS}$, the n-drift region length should be increased while its doping concentration is decreased. However, this contradicts with the effort to lower the $R_{on,sp}$ of power MOSFETs. Therefore, in lateral power MOSFETs, the silicon area efficiency is quite low and the specific on-resistance is relatively high for high voltage applications. In vertical power MOSFETs, the n-drift region is located vertically inside the silicon substrate; therefore elongating the drift region does not sacrifice the silicon area.
Even though $R_{on,sp}$ of lateral power MOSFETs are generally higher than vertical power MOSFETs, there are a few distinctive advantages in using lateral power MOSFETs for high-frequency and low-voltage applications such as integrated DC-DC converters. The first advantage is its monolithic integration. The monolithic integration of the gate drivers and the power MOSFETs on the same die allows higher switching frequency by minimizing the parasitic inductance and resistance associated with the gate terminals of power MOSFETs. In addition, monolithic integration provides a higher degree of freedom in optimizing the size and layout of power devices and their gate-drive circuit design depending on their applications.

![Diagram of 5V n-MOS and HV n-LDMOS](image)

Figure 2.9 Low-voltage and high-voltage MOSFETs in modern HV CMOS technology [9].

The second advantage is its lower gate capacitance and gate charge due to less gate-to-drain and gate-to-source overlapping area as shown in Figure 2.9. This enables the power MOSFETs to switch at a higher frequency without incurring significant switching and gate charge power losses.

However, when large size power MOSFETs are needed for low $R_{ds,on}$ and conduction loss, the lateral current flow introduces a significant resistive voltage drop due to parasitic resistances in the metal interconnects. The parasitic resistance is the fundamental reason for the lower limit of $R_{ds,on}$ of lateral power MOSFETs. The parasitic resistance of the metal interconnect affects not just the resistive conducting power loss, but also the transistor operating condition in terms of “de-biasing”. The “de-biasing” effect occurs because $V_{GS}$ of the transistor is reduced due to the
voltage drop along the source metal line and further reduces the $R_{ds,on}$ of the transistor. The metal interconnect process and the characterization of its parasitic resistance has become a major challenge in today’s industry, as very low on-resistance lateral power MOSFETs are in need for high efficiency power systems.

Previous research by Katayama et al. demonstrated that simple power device models, which do not consider the effects of metal resistance, can produce more than 50% variation in the $R_{ds,on}$ simulation for large power MOSFETs [28]. The impact of parasitic resistances is strongly dependent on the metallization process and layout style of power MOSFETs. Three examples of different layout styles using CMOS-based power MOSFETs are shown in Figure 2.10 [6].
Figure 2.10 Different layout styles of CMOS power MOSFETs: (a) Multi-finger, (b) Waffle, (c) Hybrid-waffle (Source: [6])
The multi-finger layout in Figure 2.10 (a) is the most popular method to implement large gate width MOSFETs for a given area. Generally, multi-finger power MOSFETs provide relatively good $R_{ds,on}$ and low $Q_G$ with an efficient use of the silicon area. The source and drain junctions are shared between the adjacent transistors in parallel, thus, reducing the junction capacitances.

The waffle layout in Figure 2.10 (b) was introduced to further increase the gate width for a given area, by sharing each source and drain junctions with four surrounding transistors. The packing density of multi-finger, $\left(\frac{W}{L}\right)_{MF}$, and waffle layout, $\left(\frac{W}{L}\right)_{WA}$, are shown below:

$$\frac{\left(\frac{W}{L}\right)_{WA}}{\left(\frac{W}{L}\right)_{MF}} = \frac{2S_{gate}}{L_{gate}+S_{gate}},$$

(Eq. 2.13) [13]

where $S_{gate}$ is the spacing between the gates and $L_{gate}$ is the gate length. This equation reveals that a waffle layout offers a better packing density than the multi-finger layout as long as the spacing between the gates exceeds the gate length. However, the minimum design rule of metal and contact restricts the use of a waffle layout in most CMOS technologies. In a waffle layout, the width of the diagonal source and drain metal lines are limited by the size of the unit cell transistor. Therefore, the metal interconnect resistance contribute significantly to $R_{ds,on}$. In order to minimize the metal parasitic resistance in a waffle layout, the hybrid-waffle layout was proposed as shown in Figure 2.10 (c) [6]. The hybrid-waffle layout allows wider interconnections at the expense of reduced total gate width. For detailed explanations of the hybrid-waffle layout, refer to Abraham Yoo’s PhD dissertation [6].

### 2.4 Parasitic Resistances in Lateral Power MOSFETs

The power semiconductor industry has made tremendous progress in reducing specific on-resistance of integrated lateral power MOSFETs [29] [30]. With the rapid progress in power MOSFETs technology, the silicon-contributed $R_{ds,on}$ of lateral power MOSFETs can easily be a few tens of mΩ by increasing the chip size. However, the total $R_{ds,on}$ of lateral power MOSFETs has yet to decrease with increasing the chip size as expected due to the parasitic resistance of metal interconnects. This effect is known as “lateral scaling limitation” [31] [32]. It is common that the metal interconnects contribute to $R_{ds,on}$ two to three times more than the silicon in LDMOS transistors [33]. The lateral scaling limitation is illustrated in Figure 2.11.
In Figure 2.11 (a), $R_{ds,on}$ initially drops at a fast rate as the gate width increases and then saturates due to metal parasitic resistances. This is also reflected in Figure 2.11 (b) which illustrates the behaviour of $R_{on,sp}$ with respect to the gate width. When the metal contribution is not considered, $R_{on,sp}$ should not change because it is a constant parameter, which is defined by the process technology. However, when metal interconnect resistances are taken into account, $R_{on,sp}$ gradually increases with the increase of gate width. The amount of metal contribution to the total $R_{ds,on}$ depends on the size of power MOSFETs, the material and thickness of metal layers, and the layout of metal interconnects.

The metal interconnect of power MOSFETs consists of aluminum layers with different thicknesses. These metal layers conduct current from thousands of parallel connected device cells to the bond wires. Contacts and vias are also part of the metal interconnect, and provide vertical current flow between different metal layers. Currently, there are strong industrial interests to adopt thicker aluminum layers and different materials with higher conductivity such as copper for their power process technology. However, this process changes are limited by the wafer fabrication throughput, and more importantly by the photolithography requirement after the metal deposition [34].

For a power IC designer, changing the metal interconnect process is not always a viable solution for minimizing the parasitic resistance. Therefore, the design of a metal interconnect layout
should be optimized such that the resistive contribution of the metal interconnect is minimized. However, the optimization of an interconnect layout is a very challenging and time-consuming process because there are no standard systematic procedures or design tools available. Due to a large number of components and complex geometry, the design of an optimized metal interconnect requires a 3-dimensional computer aided modeling. A SPICE lumped-element modeling approach is often reported in the literature [35]. However, its use and accuracy are very limited in complex multi-metal power IC layout design. Moreover, commercial Technology Computer-Aided Design (TCAD) tools and parasitic extraction tools such as Assura QRC are not suitable for power IC layouts due to the size and complexity of geometry and the three-dimensional nature of current flow. Therefore, more customized layout modeling methods and optimization procedures need to be developed. In Chapter 3, analytic modeling methods of the metal interconnect and layout optimization techniques will be discussed in detail.

2.5 Summary

One of the most important performance indicators, efficiency of DC-DC converters, is largely dependent on the output stage design. In synchronous buck topology, two switches in the output stage is implemented by power MOSFETs, and the conduction and switching performance of power MOSFETs dictates the efficiency of DC-DC converters. Even though switching at a higher frequency is beneficial for cost reduction and fast dynamic response, it degrades the efficiency due to higher switching and gate charge losses. Therefore, lateral power MOSFETs which exhibits low $Q_G$ and easy monolithic integration, are the most adequate choices for high-frequency integrated DC-DC converters.

When designing large-area lateral power MOSFETs, optimization of the metal interconnect is very critical because the metal contribution to its $R_{ds,on}$ can be two to three times larger than the silicon. However, the optimization of the metal interconnect is very challenging and time-consuming because standard systematic procedures or appropriate design tools are not available. Currently available simulation tools such as SPICE, TCAD, and RCX are limited in their use and accuracy for modeling the large and complicated power metal interconnects.
In conclusion, designing an output stage requires a thorough understanding of all power loss mechanisms and effective optimization of the power MOSFETs. From the designer’s perspective, the following MOSFET variables have to be considered:

- small $R_{ds,on}$ for reducing conduction loss
- small $Q_G$ for reducing gate-charge loss
- small $Q_{GD}$ for reducing switching loss
- gate width of HS and LS switches for optimized efficiency
- optimized layout for minimized parasitic effects

The analytical layout modeling of interconnects and layout optimization techniques for minimizing parasitic effects are presented in Chapter 3. In Chapter 4, an optimized output stage design methodology for high-frequency integrated DC-DC converters by effective trade-offs among major power losses in power MOSFETs is presented.
Chapter 3  Analysis and Optimization of Metal Interconnects in Large-Area Power MOSFETs

The layout of a power device contains a huge number of small components such as metal lines, vias, contacts, bond-pads, wirebonds and devices. Since there exist series and distributed resistive components in the interconnects between the silicon and its package, a power device will experience undesired parasitic effects as it carries high current. These parasitic effects are $I \times R$ voltage drop, current crowding, metal debiasing effect, and high on-resistance ($R_{ds,on}$) [31] [34] [36]. Furthermore, the uneven current distribution in a power device can result in localized heating, electromigration, and other reliability concerns [32]. The parasitic resistances in the interconnect becomes more critical in a large-area power device, which is designed to carry a large amount of current with a very low $R_{ds,on}$ value.

In standard IC design, SPICE device models provided by fabrication foundries are essential to simulating circuit behavior. However, SPICE device models cannot be solely used when simulating a large-area power device because the parasitic resistances in the interconnect are not included in the device models. There exist commercial tools for RC parasitic extractions for post-layout simulations, such as Assura QRC, Calibre PEX and Star RCX. Nevertheless, they are not capable of handling the layout of power interconnects due to complexities of size and geometry of the layout, and multi-dimensional nature of the current flow [37]. There are also Technology Computer-Aided Design (TCAD) tools which are widely used to develop and optimize semiconductor processing technologies and devices. Although some commercial TCAD simulation tools support the simulation of interconnects, their role is limited in computing the mechanical stress in the interconnect resulting from thermal processing and externally applied forces in a small defined structure. The size and the complexity of geometry in the power interconnects make the TCAD simulation tools unsuitable for large-area power device simulations. Therefore, the performance degradation due to parasitic effects should be thoroughly analyzed by using customized layout modeling methods in the case of designing a large-area power device.
3.1 Physics of Current Flow in Interconnects

The physics of current flow in interconnects simply follows the Ohm’s law. In linear media, the conduction current density is proportional to the applied electric field:

\[ \vec{j} = \sigma \cdot \vec{E} = \frac{E}{\rho} \quad [A/m^2] . \]  

(Eq. 3.1) [38]

where \( \vec{j} \) is the current density, \( E \) is the electric field, \( \sigma = 1/\rho \) is the conductivity and \( \rho \) is the resistivity of the material. A table of resistivity and conductivity of most common materials used in metal interconnects are as listed in Table 3.1.

<table>
<thead>
<tr>
<th>Material</th>
<th>( \rho ) [( \Omega \cdot \text{m} )]</th>
<th>( \sigma ) [S/m]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aluminum</td>
<td>( 2.83 \times 10^{-8} )</td>
<td>( 3.53 \times 10^{7} )</td>
</tr>
<tr>
<td>Copper</td>
<td>( 1.69 \times 10^{-8} )</td>
<td>( 5.8 \times 10^{7} )</td>
</tr>
<tr>
<td>Nickel</td>
<td>( 7.24 \times 10^{-8} )</td>
<td>( 1.38 \times 10^{7} )</td>
</tr>
</tbody>
</table>

Consider a straight piece of metal with a cross section area, \( A \) (\( w \times h \)), and length, \( l \), as shown in Figure 3.1. If a voltage, \( V \), is applied between the ends of the metal, a uniform electric field of \( E \)
= \frac{Vl}{\rho}\) exists in the conducting material and generates a current density, \(j = \frac{E}{\rho}\). Then, the total current, \(I\), through the material is:

\[
I = \int_A \vec{j} \cdot ds = j \cdot w \cdot h = \frac{V \cdot w \cdot h}{\rho \cdot l} \quad \text{(Eq. 3.2)}
\]

Also, the resistance is defined as follows:

\[
R = \rho \cdot \frac{l}{w \cdot h}, \quad \text{(Eq. 3.3)}
\]

where \(R\) is the resistance of the metal piece.

Calculating the resistance of a metal piece is trivial, when the assumption of uniform current flow is made as seen in Eq. 3.2. However, the geometrical complexity of the metal interconnects introduces difficulties in accurately modeling the parasitic resistances. Moreover, the uniform current density assumption cannot be applied to a large piece of metal due to the current crowding effect. For example, when the current exits from the metal to a contact, current crowding around the contact occurs. The current then bends upward to exit through the surface of the metal, and it crowds toward the inside edges of the contact (see Figure 3.2). This current crowding produces a slight increase in the overall resistance. Therefore, when modeling the metal interconnects, the assumption of uniform current density should be made only for small pieces of metals.

![Current crowding effect near the contacts.](image)

**Figure 3.2** Current crowding effect near the contacts.
For more accurate modeling of current flow in the metal interconnects, finite element analysis should be used for solving the basic charge conservation equation:

\[ \nabla \cdot \left( \sigma(x, y, z) \nabla V(x, y, z) \right) = 0, \quad \text{(Eq. 3.4)} \]

where \( \sigma \) is the conductivity of the media, and \( V \) is the electrostatic potential at location \((x, y, z)\). In order to apply finite element analysis, the device regions must be divided into units (elements) using a 3D mesh (or grid). Figure 3.3 shows a 3D mesh of a metal interconnect generated by Synopsys TCAD tools. The potential values at the nodes of each element are approximated with an elemental interpolation and a user-specified potential as a boundary condition [39]. The current density at each node of elements is then solved by using finite difference method with the aid of a computer program.

Figure 3.3 3D mesh of a metal interconnect (generated by Synopsys TCAD tools).
3.2 SPICE Lumped-Element Layout Modeling

Although power MOSFETs are specifically designed for carrying a large amount of power, the same finger layouts used to construct small-signal transistors serve equally well for power applications [13]. Figure 3.4 shows a MOS finger and a basic MOS multi-finger layout that are most frequently used to construct a large gate width transistor. Scalable SPICE models for MOS transistors are typically provided by fabrication foundries, but the parasitic resistances and capacitances from the interconnect are not included in the models. Because the automatic parasitic extraction followed by the post-layout SPICE simulation is not a viable solution for designing large-area power MOSFETs, the parasitic resistances of the interconnects should be identified manually with an assumption of uniform current flow in a small piece of metal. Then, the resistance value for each parasitic component can be calculated by using the sheet resistance table, which is provided by the foundry.

Figure 3.4 (a) Single MOS finger layout (b) Basic MOS multi-finger layout.
Figure 3.5 shows an example of a SPICE lumped-element model with parasitic resistances in its contacts and metal 1 source/drain runners. A MOS transistor finger is partitioned into many small unit transistors with one contact for each source and drain. Then, the resistive parasitic components are manually inserted into the SPICE netlist.

![Diagram of MOS finger with parasitic resistances](image)

**Figure 3.5 SPICE lumped-element model for a MOS finger with parasitic resistive components.**

Using this SPICE lumped-element model, several different circuit simulations have been performed to understand the effects of parasitic interconnect resistances. In this thesis, TSMC’s 0.25 µm HV CMOS technology is used, and standard 5 V MOS transistors and HV 24 V LDMOS transistor device models are used in the simulations.
Figure 3.6 (a) Simulation results of $R_{\text{on,device}}$, $R_{\text{ds,on}}$, and $R_{\text{parasitic}}$ of a standard 5 V MOS finger using SPICE lumped-element model (b) Layout of a standard 5 V MOS finger.

Figure 3.7 (a) Simulation results of $R_{\text{on,device}}$, $R_{\text{ds,on}}$, and $R_{\text{parasitic}}$ of HV 24 V LDMOS finger using SPICE lumped-element model (b) Layout of a HV 24 V LDMOS finger.
Figure 3.6 shows the contribution of parasitic resistance due to contacts and metal-1 source drain runners in a 5 V MOS finger layout. As the gate width increases, the intrinsic device on-resistance \((R_{\text{on,device}})\) and the total on-resistance \((R_{\text{ds,on}})\) decrease because the intrinsic channel resistance are inversely proportional to the gate width \([40]\). The parasitic interconnect resistance \((R_{\text{parasitic}})\) corresponds to the difference between \(R_{\text{ds,on}}\) and \(R_{\text{on,device}}\). When the gate length is below 100 µm, the plot of \(R_{\text{ds,on}}\) and \(R_{\text{on,device}}\) are almost identical because \(R_{\text{parasitic}}\) is relatively small compared to \(R_{\text{on,device}}\). However, when the gate length increases beyond 100 µm, \(R_{\text{ds,on}}\) starts to increase gradually while \(R_{\text{on,device}}\) continues to decrease. This indicates that the parasitic resistance begins contributing more to \(R_{\text{ds,on}}\). The domination of \(R_{\text{parasitic}}\) is more pronounced in the longer gate width region. Figure 3.7 also exhibits the same trend, although the simulation was performed with a HV 24 V LDMOS finger layout. However, the intrinsic device on-resistance of a HV 24 V LDMOS transistor is much higher than that of the 5V transistor due to the longer drift region. Thus, the percentage of \(R_{\text{parasitic}}\) contributing to \(R_{\text{ds,on}}\) in the LDMOS finger layout is much smaller.

SPICE lumped-element layout modeling had been used to simulate power MOSFET layouts such as multi-finger layouts and hybrid-waffle layouts \([32]\) \([35]\). However, this method requires designers to manually identify the resistive components in the layout and insert them to the SPICE netlist. Since the width of a power MOSFET can be as large as 100,000 µm or larger depending on applications, the SPICE netlist can easily involve millions of components. Therefore, the simulation time and the accuracy of this simulation largely depend on clever optimization of the SPICE netlist by its designers. This modeling method can be effective when the size of power MOSFETs is small with a few metal layers. Otherwise, it requires a very long and tedious process of setting up the simulation, which can take up to several days. In addition, SPICE is not optimized for handling such a huge number of components interconnected in a 3-dimensional mesh, thus, the simulation can often result in convergence failures.

The other disadvantage of this method is its incapability to accurately model and visualize the current crowding effect. In order to understand the current crowding effect, the current behavior in a small power MOSFET with 2 metal layers was simulated by Crosslight’s 3D TCAD simulator. In Figure 3.8, the non-homogeneous distribution of current density, which is known for current crowding effect, is clearly shown in the contacts, vias, and the metal layers.
Figure 3.8 (a) TCAD structure of basic metal interconnects (b) TCAD simulation results of the current density distribution in metal interconnects.
Figure 3.9 shows another example of the current crowding effect in a cornered metal layout. In SPICE-based layout modeling, a corner is normally represented with two resistors connected in series. However, due to the current crowding effect, the current density tends to concentrate in the sharp corner which is shown in red in Figure 3.9 (b). This produces a slightly higher value of resistance than the simple SPICE model. In addition to the discrepancies in the resistance value due to simplified models, identifying the high current density regions is very important because they are common sources of serious reliability issues. As shown in Figure 3.9 (c), the high current density at the corners can be mitigated by using diagonally cornered interconnect. Moreover, the output data of SPICE simulations do not allow easy visualization of the current and voltage information at each node. This visualization is particularly important because it allows the designers to optimize the interconnect layout for more even distributions of the current density over the device area.

![Figure 3.9](image)

Figure 3.9 (a) SPICE lumped-element model of a cornered metal interconnect (b) Current density distribution of a cornered metal interconnect (c) Current density distribution of a diagonally cornered metal interconnect.

SPICE-based layout modeling had been previously used in some academic literature because it was the only available approach to analytically investigate the parasitic effects in different power device layouts. However, it encompasses many handicaps, such as the complexity in the process of setting up the simulation, the time and accuracy of simulation, which largely depend on the designer’s clever optimization of the SPICE netlist, and the difficulty in processing and visualizing the output data. Therefore, this method is not adopted widely for industrial use.
3.3 R3D Resistive Extraction and Analysis

R3D is a resistance extraction and analysis software developed by Silicon Frontline in 2009. This tool is equipped with a highly efficient iterative matrix solver, which is specifically designed for extraction, simulation, analysis, and optimization of metal interconnects of power semiconductor devices [37]. Figure 3.10 is an illustration of the simulation flow of R3D. R3D reads in a standard layout file (GDSII), process technology files, and generates a 3D model representing all resistive elements of the structure (metal layers, vias/contacts, wire bonds/balls, and device cells) [37]. R3D’s capability to read GDSII standard data files speeds up the process of setting up the simulation, while the SPICE-based layout modeling requires a large amount of the designer’s effort to setup the simulation. R3D also helps minimize human errors which can be possibly associated with the process of setting up the simulation [41].

![R3D simulation flow diagram](source: [37]).

The layout in the GDSII file is then sub-divided using a 3-dimentional mesh, and current transport equations are solved at each point in the mesh using a finite difference method. The user-specified voltages applied to wire bonds or bond pads are used as boundary conditions in the calculations [41]. R3D is capable of computing the distributions of potential and current...
densities in all metal layers, vias, contacts, and devices. In addition, it provides an effective 2D and 3D visualization of the simulated data, and $R_{ds, on}$ value of the power device as the final result.

The usefulness and effectiveness of the R3D simulator has been demonstrated by comparing two different power MOSFET layout structures within two given silicon areas. First, 5 V nMOS transistors were placed within the area of 10,000 $\mu$m$^2$ and 60,000 $\mu$m$^2$, and both multi-finger layout and hybrid-waffle layout techniques were employed to design the metal interconnect. The standard metal process option and total three metal layers were used. Then, R3D simulations were performed on both designs in order to investigate the difference in the contribution of parasitic resistances on $R_{ds, on}$ due to their structural differences. Since the R3D simulator produces $R_{ds, on}$ values as the final result of simulation from the input GDSII layout files, comparisons between the two layout techniques can be easily made (see Table 3.2).

| Table 3.2 Comparisons of 5V Power MOSFETs in Multi-finger and Hybrid-waffle Layouts |
|---------------------------------|-----------------|-----------------|-----------------|-----------------|
|                                 | Within 10,000 $\mu$m$^2$ | Within 60,000 $\mu$m$^2$ |
|                                 | Multi-finger | Hybrid-waffle | Multi-finger | Hybrid-waffle |
| Total gate width [$\mu$m]       | 7,767        | 2,100          | 45,802        | 11,900          |
| Total area [$\mu$m$^2$]         | 9,752        | 9,497          | 57,200        | 60,025          |
| $R_{ds, on}$ [$\Omega$]         | 0.389        | 1.991          | 0.222         | 0.447           |
| $R_{on, sp}$ [m$\Omega$ $\cdot$ mm$^2$] | 3.794 | 18.91 | 12.70 | 26.83 |
| % of $R_{parasitic}$            | 40.1         | 57.2           | 82.4          | 67.0            |
| $Q_G$ [nC] (SPICE simulated)    | 0.069        | 0.016          | 0.375         | 0.096           |
| FOM$_1$ ($R_{ds, on} \times Q_G$) [nC$\cdot$m$\Omega$] | 26.8 | 31.9 | 83.3 | 42.9 |
| FOM$_2$ ($R_{on, sp} \times Q_G$) [nC$\cdot$m$\Omega$ $\cdot$ mm$^2$] | 0.261 | 0.303 | 4.762 | 2.575 |

In both multi-finger and hybrid-waffle structures within the area of 10,000 $\mu$m$^2$, the percentage of $R_{parasitic}$ contributing to $R_{ds, on}$ is larger than 40 %. The percentage of $R_{parasitic}$ contributing to $R_{ds, on}$ in the multi-finger structures increases up to 82.4 % when the given area increases to
60,000 µm². This clearly shows the difficulty in designing a power MOSFET with a very low \( R_{ds,on} \) due to the parasitic resistance in the interconnects.

In both given areas, the multi-finger structures exhibit higher \( Q_G \) values than the hybrid-waffle structures. This is because \( Q_G \) is proportional to the gate width of the power MOSFETs for a given length and the multi-finger structures have higher cell density than the hybrid waffle structures as shown in the Table 3.2. \( R_{ds,on} \) values of the multi-finger structures in both given areas are also lower than the hybrid waffle structures. However, for the given area of 60,000 µm², the hybrid-waffle structure demonstrates smaller \( FOM_1 \) and \( FOM_2 \) even though its \( R_{ds,on} \) is higher than that of the multi-finger structure. This is due to the smaller \( Q_G \) value as the hybrid-waffle structure contains about one-fourth fewer transistor gates and smaller percentage of \( R_{parasitic} \) contributing to its \( R_{ds,on} \).

As shown above, there exist complicated trade-offs for the performance of power MOSFETs depending on the layout of power MOSFETs, the metal interconnects and the size of the devices. In particular, the effects of parasitic resistances in the interconnects vary greatly depending on the layout techniques, thickness of metal layers, the number of metal layers, termination of source and drain pads, and so on. Therefore, when designing power MOSFETs, the effect of interconnects has to be thoroughly analyzed and optimized. R3D simulation tools also provide visual aid to analyze and optimize metal interconnect layouts.
Figure 3.11 Multi-finger structure within 60,000 µm²: (a) Potential distribution in the top metal (b) Current density distribution in the top metal (c) VDS distribution of the device cells.
Figure 3.12 Hybrid-waffle structure within 60,000 \( \mu \text{m}^2 \): (a) Potential distribution in the top metal (b) Current density distribution in the top metal (c) \( V_{DS} \) distribution of the device cells.
Figure 3.11 and Figure 3.12 show the colour contour maps generated by R3D for visualization of the potential distribution, the current density distribution, and $V_{DS}$ distribution in the two different layouts. Analysis of these distributions provides a better understanding of the device operation and visual aid to explore and optimize interconnect layouts for the designer. For example, the source terminal and the drain terminal in the top metal are connected to 0V and 0.1V respectively. This is a typical $R_{ds,on}$ measurement condition. However, as shown in Figure 3.11, the multi-finger layout exhibits excessive potential drop in the top metal interconnect. Thus, in the multi-finger layout, the individual MOS transistor cells in the silicon are only applied to $V_{DS}$ potential ranging from 0.014V to 0.024V. This is a lot less than the actual voltage applied to the source and drain net of the device. In addition, due to the voltage drops on the source metal, $V_{GS}$ values also reduced, resulting in “de-biasing” effect. On the other hand, in Figure 3.12, the hybrid-waffle layout shows less potential drops in the top metal and higher $V_{DS}$ distributions ranging from 0.55V to 0.8V, and less “de-biasing” effect.

These $V_{DS}$ distributions allow the designer to know how much potential drops occur due to the metal interconnect and provides a quick estimate of the design’s balance. The current density can be used to immediately identify regions vulnerable to electromigration and thermo-mechanical problems. Furthermore, this information can be used to optimize the layout by evenly distributing the current over the device area. The optimization technique will be discussed in the next section.

In comparison to SPICE lumped-element layout modeling, R3D extraction and analysis exhibits the distinct benefits, such as fast handling of large and complex designs, powerful visualization of potential and current distributions in the interconnect, and enabling possibility of further optimization of layouts. Therefore, R3D extraction and analysis was used throughout the research for the layout optimization of a large-area power device.
3.4 Layout Optimization of HV 24V LDMOS in 1mm²

In previous sections, different layout modeling and analysis methods to investigate the parasitic effects of a power device were discussed. The R3D simulator offers effective visualization aid for the designer to identify and minimize the parasitic resistances in the interconnect of a power device. In this section, a systematic approach to optimize the layout of TSMC’s HV 24 V LDMOS transistors in the area of 1mm² is demonstrated by using R3D extraction and analysis tools. The goal of this layout optimization is to accomplish a minimum value of $R_{ds,on}$ at room temperature.

3.4.1 HV 24V LDMOS Test Device

Figure 3.13 illustrates the layout and schematic of the test device. In order to maximize the cell density within the area of 1 mm², the conventional multi-finger layout was used. A thorough study had been performed on the possibility of using the hybrid-waffle layout; however, the design rule restrictions on the HVNW and HVPW spacing, reliability issues associated with 45° angled metal layers, and much lower cell density due to the longer drift region length did not provide any advantages over multi-finger layout in the case of LDMOS power transistors. Therefore, the multi-finger layout was the most adequate choice for optimizing the layout for a minimum $R_{ds,on}$ in a given area. Table 3.3 summarizes the test device. This device was designed using the three metal layer process with an ultra-thick (3 µm) top metal layer option.

<table>
<thead>
<tr>
<th>$W$ of a finger [µm]</th>
<th>No. of fingers in a row</th>
<th>No. of rows</th>
<th>Total $W$ [µm]</th>
<th>Size [mm x mm]</th>
<th>$R_{on,device}$ [mΩ]</th>
</tr>
</thead>
<tbody>
<tr>
<td>234</td>
<td>290</td>
<td>4</td>
<td>271,440</td>
<td>1.005 x 0.998</td>
<td>25.3</td>
</tr>
</tbody>
</table>

Table 3.3 Summary of the HV 24 V LDMOS Test Device
Figure 3.13 HV 24V LDMOS test device: (a) schematic (b) layout.
Figure 3.14 Basic arrangement of metal interconnect layers in multi-finger structure: (a) metal 3 to metal 2 interconnect (b) metal 2 to metal 1 interconnect.
3.4.2 Layout Optimization Variables

Since searching the entire range of possible metal interconnect layouts was impractical, the metal interconnect layers, which are designed by using the guidelines from the foundry, was used as a starting point. The basic arrangement of metal interconnect layers are illustrated in Figure 3.14. Metal 1 runners are placed parallel to the poly gates to provide connectivity to the source and drain device terminals. Metal 2 runners are placed perpendicular to metal 1 runners, and connected to metal 1 by via 1 in a checkerboard pattern to provide separate connectivity to metal 1 source/drain runners. The top metal, metal 3, source/drain runners are laid out perpendicular to metal 2 runners, and connected to the metal 3 source/drain bus which delivers current to bond wires. The impact on the $R_{ds, on}$ of the power MOSFETs, due to number of geometric variables, were studied.

Source and Drain Termination Locations

The locations of the source and drain pads, where the current flows in and out, are very important for designing power MOSFETs. This is because the termination location determines the length of the current path and the current crowding effect occurs near the terminations. A variety of different termination arrangements are possible, some of which, perform better than others. Figure 3.15 and Figure 3.16 show the potential distributions of the top metal layer and $V_{DS}$ distributions in three different termination layouts.
Figure 3.15 Potential distribution and current flow in metal 3 with three different source and drain terminations: (a) type A, (b) type B, (c) type C.

![Potential distribution and current flow in metal 3 with different source and drain terminations](image)

Figure 3.16 $V_{DS}$ distribution with three different source and drain terminations: (a) type A, (b) type B, (c) type C.

Type A is a common arrangement in which both terminations lie on the same end of the transistor. This type of design is common when the locations of bond pads are already determined. However, this layout produces excessive voltage drops in the top metal and an uneven distribution of $V_{DS}$ over the device. The skewed $V_{DS}$ distribution is clearly shown in Figure 3.16 (a). Type B layout has the source and drain terminations at opposite ends of the power device. Type B layout produces the most even distribution of $V_{DS}$, but not the lowest $R_{ds,on}$ because of the longest current path between the terminations. Unlike type A and type B, type C
layout has terminations in the midway along the source and drain buses, so the current does not flow through its full length. Therefore, it produces minimum voltage drops in the top metal and lowest $R_{ds,on}$.

**Metal 1**

Metal 1 source runners retrieve current from the source of the transistor, and delivers to the metal 2 source runners through via 1. Metal 2 drain runners share the same purpose but the current flow is opposite. The length of the current path in the metal 1 source/drain runners is fixed by the distance between two adjacent metal 2 source/drain runners placed perpendicularly on top of metal 1. Therefore, in order to minimize the parasitic resistance in metal 1 source/drain runners, the width of the metal 1 runners need to be maximized. The maximum width of metal 1 source/drain runners are restricted by the spacing between the adjacent gates as shown below:

$$2S_{gate} = W_{M1, source} + W_{M1, drain} + 2S_{M1} \quad \text{(Eq. 3.5)}$$

where $S_{gate}$ is the spacing between adjacent gates, $W_{M1, source}$ is the width of metal 1 source runner, $W_{M1, drain}$ is the width of metal 1 drain runner, and $S_{M1}$ is the minimum spacing between any two metal 1 defined in the design rule. Figure 3.17 (b) illustrates the design restriction by its geometry.
Figure 3.17 Metal 1 optimization: (a) $R_{ds, on}$ vs. $W_{M1, source}$ (b) metal 1 geometry.

Since $S_{gate}$ and $S_{M1}$ are determined by the design rule, increasing $W_{M1, source}$ results in decreasing $W_{M1, drain}$ and vice versa. As $W_{M1, source}$ is increased, the magnitude of the voltage drop in the metal 1 drain runner is increased, and the magnitude of the voltage drop in the metal 1 drain runner is decreased. Because of this trade-off relationship, the lowest $R_{ds, on}$ was observed when $W_{M1, source}$ was equal to $W_{M1, drain}$ as shown in Figure 3.17 (a).

**Metal 2**

The metal 2 runners are the only metal layers that allow perpendicular current flow in the device, except the metal 3 bus attached to the pads. In order to minimize $R_{ds, on}$, the width of metal 2 source/drain runners is maximized until the upper limit is reached by the metal slot design rule. The metal slots are required in order to release the mechanical stress if the width of a metal is greater than the value defined by the design rule. When the metal slots are inserted, the current flow in the metal is greatly disturbed by the metal slots.

Figure 3.18 (a) shows the metal 2 design with equally distributed metal 2 source runners with the maximum width. This is the most common arrangement of metal 2 runners with the maximum metal 2 density in a given area. However, since the current density accumulates as it reaches the source pad, the current density in the metal 2 source runners near the source pad is much higher.
than in the metal 2 source runners near the drain pad. Similarly, the current density in the metal 2 drain runners near the drain pad is much higher than in the metal 2 drain runners near the source pad. Therefore, the number of source runners near the source termination was increased while sacrificing the number of drain runners. The same modification was also performed on the drain runners near the drain termination. Since the thickness and density of metal 2 runners are already constrained, the only method to minimize $R_{ds, on}$ is the effective trade-off between the metal 2 layers for source and drain runners.

![Current density distribution in metal 2 source runners](image)

**Figure 3.18** Current density distribution in metal 2 source runners: (a) equally distributed metal 2 source runners (b) asymmetrical metal 2 source runners.

This asymmetrical design, as shown in Figure 3.18 (b), was very effective in minimizing the voltage drops near the pads where the high current density was observed. This modification produced 6% reduction in the total $R_{ds, on}$.

**Metal 3**

Metal 3 is the top metal layer which delivers the current between the wirebonds in the pads and the metal 2 layers. The top metal layer in this process is also called the ultra-thick metal (UTM) layer. The ultra-thick metal layer is about 7 times thicker than the other metal layers; thus, the sheet resistance is about 7 times smaller. Therefore, it is important to effectively design the top
metal layer such that this metal layer is in charge of delivering most of the lateral current flows over the device. Figure 3.19 (a) shows the conventional top metal layers. Even though this design is most commonly used, it exhibits excessive voltage drops near the source and drain pads. There are two major weaknesses with this conventional design. First, the metal 3 bus attached to the pad is not wide enough. Second, the equal width of the metal 3 runners is not effective for distributing the current density evenly in the entire area. In Figure 3.19 (b), the width of the metal 3 bus attached to the pad is twice the width, and the width of metal 3 runners near the pad is 3 times wider than the width of the runners near the drain pad. To achieve this design, a portion of the drain runners near the source pad were sacrificed and attached to the adjacent source runners. Thus, the density of metal 3 source runners near the source pad was increased, while the density of metal 3 drain runners was decreased. The same modification was performed on the metal 3 drain bus and runners.

![Figure 3.19](image)

**Figure 3.19** Current density distribution in metal 3 source runners: (a) equally distributed metal 3 source runners (b) asymmetrical metal 3 source runners.

**Number of Bond Pads**

Since the current crowding effect occurs near the pads, dividing the current path by increasing the number of pads is the effective solution to minimize voltage drops near the pads. As shown in Figure 3.20 (a), current has to converge to the single bond pad in the middle of the
source/drain bus. This leads to a long current path and subsequently a large voltage drop across the top metal layer. Moreover, due to the current concentration near the bond pads, a large voltage drop occurs near the bond pads. Figure 3.20 clearly shows how this effect is mitigated as the number of pads increase. However, this is only possible when the locations and the number of pads are not restricted by other reasons.

![Figure 3.20 Current density distribution in metal 3 source runners](image)

Figure 3.20 Current density distribution in metal 3 source runners: (a) equally distributed metal 3 source runners (b) asymmetrical metal 3 source runners.

**Circuits Under Pads (CUP) and Different Aspect Ratio**

In some processes, placing transistors under the pads are allowed in order to maximize the use of silicon area. The circuit under pads (CUP) design effectively reduces the die cost by minimizing the total silicon area. Moreover, CUP enables the bond wires to be attached to the pads inside the active area while reducing the length of the total current path.

Another method to reduce the current path length is to change the shape of the device. Instead of using a square-like layout, the width is decreased and the length is increased to produce a rectangular shape without changing the device area. The current density in the top metal and the \( V_{DS} \) distribution with the three different aspect ratios, all including the CUP design, are shown in Figure 3.21 and Figure 3.22.
As shown in Figure 3.21 (c), a 4 to 1 aspect ratio design with CUP shows the most even current density distributed over the top metal. It also exhibits the highest average $V_{DS}$ value and most even $V_{DS}$ distribution as shown in Figure 3.22 (c). Most importantly, the metal layout with a 4 to 1 aspect ratio and CUP design resulted in the lowest $R_{ds,on}$. 
Figure 3.21 Current density distribution in the top metal with CUP design: (a) 1 to 1 aspect ratio (b) 1.9 to 1 aspect ratio (c) 4 to 1 aspect ratio.

Figure 3.22 $V_{DS}$ distribution with CUP design: (a) 1 to 1 aspect ratio (b) 1.9 to 1 aspect ratio (c) 4 to 1 aspect ratio.
3.4.3 Layout Optimization Summary

The influence of metal interconnect layout on $R_{ds,on}$ was quantitatively studied by using the R3D simulation tools. Since searching the entire range of possible metal interconnect layouts was impractical, a test device within the area of 1 mm$^2$ was designed and optimized by simulating it with different pad locations, metal 1 to 3 layer optimization, different number of pads, CUP design, and different aspect ratio of the device. The current density, potential, and $V_{DS}$ distributions were investigated in order to identify bottlenecks of each layout design. Then, each geometric variables were optimized for minimum $R_{ds,on}$. Figure 3.23 summarizes the changes in $R_{ds,on}$ after cumulative optimization of each geometric variable.

![Figure 3.23 Effects of metal interconnect resistance on $R_{ds,on}$ after the cumulative optimization at 25°C.](image)

After the final optimization process, the layout with 4 to1 aspect ratio and CUP design produced the minimum value of $R_{ds,on}$, which is 31.04 mΩ. The metal contribution was reduced to 11.08%
of the $R_{ds,on}$ whilst the metal contribution prior to the optimization was almost 60.2% of the $R_{ds,on}$. The metal interconnection resistance was reduced from 41.73 mΩ to 18.11 mΩ by optimizing the layout of metal 1-to-3 runners and buses without changing the number of bond pads. The metal interconnect resistance was further reduced from 18.11 mΩ to 3.44 mΩ by increasing the number of bond pads and employing CUP designs.

When temperature was increased to 85°C, the metal and silicon contribution was changed as shown in Figure 3.24. After the final optimization process, the metal contribution was reduced to 10.4% of $R_{ds,on}$ whilst the metal contribution prior to the optimization was 58.5%. In comparison to the simulation result at 25°C, the percentage of metal contribution to $R_{ds,on}$ was slightly reduced due to smaller temperature coefficient of resistivity in metal (0.003 to 0.004 parts per °C as defined by TSMC’s design rules) than the power MOSFETs.

![Figure 3.24 Effects of metal interconnect resistance on $R_{ds,on}$ after the cumulative optimization at 85°C.](image-url)
3.4.4 Experimental Verification of Optimized Layout

The simulation results were verified by fabricating a test chip in TSMC 0.25 µm HV CMOS technology. The test chip occupies an area of 2.3 mm × 2.8 mm, and the die photo of the test chip is shown in Figure 3.25. Three metal layers with Ultra Thick Metal option and Circuit Under Pads option were employed in the fabrication process. The test chip was packaged into Kyocera 18 lead side brazed packages with 1.1 mil bondwires.

Figure 3.25 Die photo of the test chip fabricated in TSMC 0.25µm HV CMOS process.

The test chip includes four test devices which utilize 24 V LDMOS transistors with 5 V gate oxide (NLD24G5 device). Device 1 includes the total gate width of 257,400 µm, which is divided into 4 rows of multi-fingers with a 1 to 1 aspect ratio. Device 2 includes the total gate width of 267,300 µm, which is divided into 3 rows of multi-fingers with a 1.9 to 1 aspect ratio. Device 3 and Device 4 are exactly the same design, and they include the total gate width of 268,200 µm which is divided into 2 rows of multi-fingers with a 4 to 1 aspect ratio. Each of the devices was placed within an area of 1mm², and all metal layers were optimized as discussed in Section 3.4.3. Table 3.4 summarizes the physical properties of test devices.
Table 3.4 Physical Properties of the Test Devices

<table>
<thead>
<tr>
<th>Device</th>
<th>Size [µm × µm]</th>
<th>Aspect Ratio</th>
<th>No. of Rows</th>
<th>No. of fingers in a row</th>
<th>Width of a finger [µm]</th>
<th>Total Width [µm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device 1</td>
<td>992 × 964</td>
<td>1:1</td>
<td>4</td>
<td>286</td>
<td>225</td>
<td>257,400</td>
</tr>
<tr>
<td>Device 2</td>
<td>1369 × 723</td>
<td>1.9:1</td>
<td>3</td>
<td>396</td>
<td>225</td>
<td>267,300</td>
</tr>
<tr>
<td>Device 3</td>
<td>2015 × 488</td>
<td>4:1</td>
<td>2</td>
<td>596</td>
<td>225</td>
<td>268,200</td>
</tr>
</tbody>
</table>

The $R_{ds,\text{on}}$ measurement was performed on the test devices by using the Tektronix 371A curve tracer at room temperature. Figure 3.26 (a) describes the measurement setup, and Figure 3.26 (b) describes the four-terminal sensing technique used in order to minimize any equipment resistances. The pulse measurement mode was used with the pulse width of 250 µs and the repetition rate of 30 Hz. The pulse mode effectively minimized the self-heating of the test devices, which could cause discrepancies on $R_{ds,\text{on}}$ measurements. In addition, the resistances of the package and bondwires were separately measured with the same equipment, and eliminated from the measured resistance for accurate measurements of $R_{ds,\text{on}}$.

Figure 3.26 (a) Diagram of $R_{ds,\text{on}}$ measurement setup (b) Four-terminal sensing technique.
Table 3.5 shows the comparison between the measured $R_{ds, on}$ and simulated $R_{ds, on}$. Even though the calibration of the R3D simulation solely relied on the physical properties provided in the design rule documents provided by the fabrication foundry, there is a good agreement between the measured $R_{ds, on}$ and simulated $R_{ds, on}$. In comparison to the unoptimized layout, significant performance gain was obtained without additional processing step or changes in the device structure. This implies that the layout optimization is a very effective and attractive solution for maximizing the performance of power MOSFETs without extra process costs.

<table>
<thead>
<tr>
<th></th>
<th>Simulated $R_{ds, on}$ [mΩ]</th>
<th>Measured $R_{ds, on}$ [mΩ]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device 1</td>
<td>37.2</td>
<td>42.5</td>
</tr>
<tr>
<td>Device 2</td>
<td>32.6</td>
<td>35.8</td>
</tr>
<tr>
<td>Device 3 / Device 4</td>
<td>31.0</td>
<td>31.4</td>
</tr>
</tbody>
</table>

### 3.5 Summary

This chapter presented the SPICE lumped-element modeling method and the R3D resistive extraction method for analyzing the parasitic resistances of metal interconnects. The SPICE lumped-element modeling can be sufficient when the size of power MOSFETs is small with a few metal layers. However, it encompasses many handicaps, such as the complexity in the process of setting up the simulation, the ineffective time and accuracy of the simulation, and the difficulty in processing and visualizing the output data. As an alternative, the R3D resistive extraction and analysis, which was developed by Silicon Frontline in 2009, was investigated. By using R3D simulation tools, an effective comparison between the multi-finger and hybrid-waffle structures in two different given areas was presented. It was also verified that the metal interconnect resistance contribution strongly depends on the layout structures and arrangements of bond pads. Furthermore, a layout optimization technique for 24 V LDMOS transistors in 1mm$^2$ was demonstrated and experimentally verified through a test chip fabricated in TSMC 0.25 μm HV CMOS technology. After the cumulative optimization of the layout in terms of
termination locations, number of pads, metal layers, aspect ratios, and CUP designs, an improvement of 55% in its on-resistance had been achieved. This performance gain was obtained without any additional processing steps or changes in the device structure.
Chapter 4  Design of Integrated Output Stage for High-Frequency DC-DC Converters

The efficiency of DC-DC converters is highly dependent on the output stage design. In Chapter 2 and 3, the requirements of power MOSFETs and the metal interconnect layout optimization technique were presented. The focus of this chapter is to take advantage of the improved performance of power MOSFETs in order to design a 12 V to 1.2 V DC-DC converter output stage, operating with a switching frequency of 4 MHz. In this chapter, the optimized size of power MOSFETs for HS and LS switches are determined by a power loss calculation procedure [28] [42]. The segmented output stage design technique to improve efficiency in light load conditions is then presented. The layout optimization technique discussed in Chapter 3 is also applied to each segment of the output stage. Finally, the simulation results and IC implementation of the DC-DC converter are presented.

Figure 4.1 Simplified block diagram of the output stage IC for a 4 MHz, 12 V to 1.2 V DC-DC converter.
Figure 4.1 shows a simplified block diagram of the output stage IC for a 4 MHz, 12 V to 1V DC-DC converter, which is designed and implemented in TSMC 0.25 \( \mu \)m HV CMOS technology. In the field of low voltage and high frequency monolithic converters, most of the available literatures focus on low \( V_{IN} \) (less than 5 V) and low \( I_{LOAD} \) (less than 1 A) converters [6] [12] [43] [44]. In this thesis, consideration is given to mid-range point of load applications with the 2 A load current and 12 V input voltage. Although discrete power MOSFETs are more popular in this application field, discrete switched-mode power supplies cannot be switched as quickly as their integrated counterparts, due to their parasitic capacitance [12].

The significance of the term, high switching frequency, is relative to a synchronous buck converter application, which depends on the power range and the amount of the voltage conversion. With a low input voltage around 3 to 5 V and a power range less than 1 W, a switching frequency up to 10 MHz can be reasonably achieved. On the other hand, delivering load current of 2 A from \( V_{IN} \) of 12 V down to 1.2 V with a switching frequency of 4 MHz, is very challenging if about 90% efficiency is expected. In addition, a duty cycle of 10 % means that the on-cycle interval has to be accomplished within 25 ns. This requires very fast and effective gate drivers and optimization of the output stage. The target operating conditions of the DC-DC converter for the output stage design is listed in Table 4.1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IN} )</td>
<td>12 V</td>
</tr>
<tr>
<td>( V_{OUT} )</td>
<td>1.2 V</td>
</tr>
<tr>
<td>( C )</td>
<td>4.7 ( \mu )F</td>
</tr>
<tr>
<td>( L )</td>
<td>1 ( \mu )H</td>
</tr>
<tr>
<td>( I_{LOAD} )</td>
<td>2 A</td>
</tr>
<tr>
<td>( f_{SW} )</td>
<td>4 MHz</td>
</tr>
</tbody>
</table>
4.1 Switching Device Size Optimization

In order to maximize the efficiency of the DC-DC converter, the size of the HS and LS switches are optimized after assessing different power losses associated with power MOSFETs. The efficiency of the DC-DC converter is estimated by a calculation method with an aid of spreadsheet modeling and SPICE parameter extraction at temperature of 25°C. In his paper [19], Mitter established the following loss contribution equations.

\[ P_{loss} = P_{cond(HS)} + P_{cond(LS)} + P_{gate} + P_{sw} \]  \hspace{1cm} (Eq. 4.1)

The total power loss \( P_{loss} \) includes conduction, gate-drive and switching losses of power MOSFET switches, and each component of power loss is calculated as follows:

\[ P_{cond(HS)} = I_L^2 \cdot R_{ds,on(HS)} \cdot D \]  \hspace{1cm} (Eq. 4.2)

\[ P_{cond(LS)} = I_L^2 \cdot R_{ds,on(LS)} \cdot (1 - D) \]  \hspace{1cm} (Eq. 4.3)

\[ P_{gate} = f_{sw} \cdot V_{gs} \cdot (Q_{G(HS)} + Q_{G(LS)}) \]  \hspace{1cm} (Eq. 4.4)

\[ P_{sw} = f_{sw} \cdot V_{DS} \cdot I_L \cdot \frac{(\tau_{on} + \tau_{off})}{2} \]  \hspace{1cm} (Eq. 4.5)

The efficiency of the converter is expressed as:

\[ \eta = \frac{(V_{OUT} \times I_{LOAD})}{(V_{OUT} \times I_{LOAD}) + P_{loss}} \times 100 \]  \hspace{1cm} (Eq. 4.6)

In order to determine the optimum size of HS and LS switches, which maximizes the efficiency at the given condition, \( R_{ds,on} \) and \( Q_G \) values of 20 different sizes of power MOSFETs are extracted from SPICE simulations as shown in Table 4.2. Figure 4.2 shows the simulated gate charge characteristic of a 24 V LDMOS transistor with \( W = 283000 \) µm. For calculation of the switching power loss \( P_{sw} \), the switching gate charge \( Q_{SW} \) is determined as the sum of \( Q_{GD} \) and \( Q_{GS2} \) as shown in Figure 4.2. Then, the switching turn-on and turn-off times are estimated by using Eq. 4.7 and 4.8.
Figure 4.2 Simulated gate charge characteristics of a 24 V LDMOS transistor ($W = 283000 \, \mu m$).

\[
\tau_{on} = \frac{Q_{SW}}{I_{driver(\text{pull-up})}} \quad \text{(Eq. 4.7)}
\]

\[
\tau_{off} = \frac{Q_{SW}}{I_{driver(\text{pull-down})}} \quad \text{(Eq. 4.8)}
\]

With an aid of spreadsheet modeling, efficiency of the DC-DC converter for the given operating condition was calculated with 20 different sizes for both HS and LS switches. As shown in Figure 4.3, the maximum efficiency is achieved when the HS device number is 4 and the LS device number is 16. From Table 4.2, the optimum size of the HS and LS switches are determined to be $W_{\text{total(HS)}} = 70800 \, \mu m$ and $W_{\text{total(LS)}} = 283000 \, \mu m$. After that, the efficiency of the DC-DC converter with optimum size is simulated by using SPICE and plotted in Figure 4.4. Peak efficiency of 85.8 % was achieved at load current of 2 A.
Table 4.2 SPICE extracted values of $R_{ds,on}$, $Q_G$ and $Q_{sw}$ of 24V LDMOS transistors

<table>
<thead>
<tr>
<th>Device No.</th>
<th>$W_{total}$ [µm]</th>
<th>$R_{ds,on}$ [Ω]</th>
<th>$Q_G$ [nC]</th>
<th>$Q_{sw}$ [nC]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>17694.6</td>
<td>0.429</td>
<td>0.352</td>
<td>0.115</td>
</tr>
<tr>
<td>2</td>
<td>35389.2</td>
<td>0.214</td>
<td>0.727</td>
<td>0.215</td>
</tr>
<tr>
<td>3</td>
<td>53083.8</td>
<td>0.143</td>
<td>1.102</td>
<td>0.263</td>
</tr>
<tr>
<td>4</td>
<td>70778.4</td>
<td>0.107</td>
<td>1.474</td>
<td>0.329</td>
</tr>
<tr>
<td>5</td>
<td>88473</td>
<td>0.086</td>
<td>1.949</td>
<td>0.402</td>
</tr>
<tr>
<td>6</td>
<td>106167.6</td>
<td>0.071</td>
<td>2.220</td>
<td>0.471</td>
</tr>
<tr>
<td>7</td>
<td>123862.2</td>
<td>0.061</td>
<td>2.594</td>
<td>0.562</td>
</tr>
<tr>
<td>8</td>
<td>141556.8</td>
<td>0.054</td>
<td>2.969</td>
<td>0.620</td>
</tr>
<tr>
<td>9</td>
<td>159251.4</td>
<td>0.048</td>
<td>3.343</td>
<td>0.682</td>
</tr>
<tr>
<td>10</td>
<td>176946</td>
<td>0.043</td>
<td>3.713</td>
<td>0.731</td>
</tr>
<tr>
<td>11</td>
<td>194640.6</td>
<td>0.039</td>
<td>4.088</td>
<td>0.820</td>
</tr>
<tr>
<td>12</td>
<td>212335.2</td>
<td>0.036</td>
<td>4.460</td>
<td>0.892</td>
</tr>
<tr>
<td>13</td>
<td>230029.8</td>
<td>0.033</td>
<td>4.834</td>
<td>0.941</td>
</tr>
<tr>
<td>14</td>
<td>247724.4</td>
<td>0.031</td>
<td>5.210</td>
<td>1.030</td>
</tr>
<tr>
<td>15</td>
<td>265419</td>
<td>0.029</td>
<td>5.580</td>
<td>1.120</td>
</tr>
<tr>
<td>16</td>
<td>283113.6</td>
<td>0.027</td>
<td>5.950</td>
<td>1.170</td>
</tr>
<tr>
<td>17</td>
<td>300808.2</td>
<td>0.025</td>
<td>6.330</td>
<td>1.270</td>
</tr>
<tr>
<td>18</td>
<td>318502.8</td>
<td>0.024</td>
<td>6.710</td>
<td>1.320</td>
</tr>
<tr>
<td>19</td>
<td>336197.4</td>
<td>0.023</td>
<td>7.080</td>
<td>1.380</td>
</tr>
<tr>
<td>20</td>
<td>353892</td>
<td>0.021</td>
<td>7.450</td>
<td>1.450</td>
</tr>
</tbody>
</table>

Figure 4.3 Calculated efficiency of a 12 V to 1.2 V DC-DC converter with different HS and LS device sizes at 4 MHz switching frequency.
4.2 Segmented Output Stage Design

In Section 4.1, the power MOSFETs in the DC-DC converter are sized to achieve the maximum efficiency at the nominal load condition of 2 A. Since the figure of merit, $R_{ds,on} \times Q_G$, is imposed by the process technology, efficiency degradation occurs in the light load range with a fixed frequency operation. Figure 4.4 clearly shows the degraded efficiency in the light load condition where the current is below 0.5 A. However, this limitation can be mitigated by using a segmented output stage, where the power MOSFET’s effective width ($W_{eff}$) is changed depending on the load current [45] [46]. As shown in Figure 4.5, the gate-drive and switching losses dominate in the light load range. With a segmented output stage, enabling and disabling each segment changes the effective width of the power transistors. Changing $W_{eff}$ on the fly depending on the load current can lead to an effective trade-off between the gate-drive loss and conduction loss over a wider load range for efficiency optimization.
Figure 4.5 Ideal efficiency curves for increasing transistor size, $W_1 < W_2 < W_3$ [47].

Unlike the gate-drive loss, the switching loss does not scale linearly with the size of power transistors. Regardless of whether the transistor segment is enabled or not, the parasitic capacitances of all transistor segments are present at the switching node. As a result, both the rise and fall times of the switching node are increased as $W_{\text{eff}}$ is reduced. Likewise, due to a number of high order effects, $W_{\text{eff}}$ cannot be exactly predicted from the calculation method as in Section 4.1. Therefore, the optimum effective width, which decreases with the load current, is determined by simulations and measurements.

In this output stage design, the LS switch is divided into 4 segments, and the HS switch remains the same. With the segmentation scheme, one segment of the LS switch is identical to the HS switch. This is intentionally designed so that the identical segmented gate driver design can be applied for both of the LS and HS switches. The design of segmented gate-drivers is out of the scope of this thesis.

### 4.3 Layout and Simulation Results

The output stage described in the previous sections had been implemented into an IC using TSMC 0.25 µm HV CMOS process. It occupies an area of $1280 \times 1930 \, \mu\text{m}^2$ and the layout of the output stage IC is as shown in Figure 4.6.
Figure 4.6 Layout of the output stage IC fabricated in TSMC 0.25 HV CMOS process.

Since the interconnect resistance contribution strongly depends on the layout and bond pad arrangements, the metal layout design was thoroughly analyzed and optimized by using R3D simulation tools as presented in Chapter 3. In order to minimize the metal parasitic resistances, the 3 µm ultra-thick top metal layer and circuit under pad designs are employed. The optimized layout of the top metal and locations of the pads are as shown in Figure 4.7.

Figure 4.7 Layout of top metal and locations of CUP pads.
In order to minimize the current path lengths as much as possible, 3 CUP bond pads for each source and drain terminals are placed in each segment. After the metal layer optimization, $R_{ds, on}$ of the HS and LS switches with the segmentation scheme are simulated and the contribution of the parasitic resistances are identified. Table 4.3 shows the properties of the segmented output stage power MOSFETs.

Table 4.3 Properties of segmented output stage power MOSFETs

<table>
<thead>
<tr>
<th>No. of enabled segments</th>
<th>HS switch</th>
<th>LS switch</th>
</tr>
</thead>
<tbody>
<tr>
<td>No. of enabled segments</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>$R_{ds, on}$ [mΩ]</td>
<td>112.2</td>
<td>112.1</td>
</tr>
<tr>
<td>% of $R_{parasitic}$</td>
<td>4.6</td>
<td>4.5</td>
</tr>
<tr>
<td>$Q_G$ [nC]</td>
<td>1.474</td>
<td>1.47</td>
</tr>
<tr>
<td>$FOM_1$ [nC·mΩ]</td>
<td>165.4</td>
<td>165.2</td>
</tr>
</tbody>
</table>

Figure 4.8 R3D simulation results of current density distributions in the top metal (LS switch).
As shown in Table 4.3, the contribution of metal resistances on $R_{ds,on}$ are maintained under 4.6% for all segment variations.

The switching characteristics of the output stage are verified through post-layout simulations by using HSPICE. Since the conventional parasitic extraction tools such as Assuara QRC or Calibre PEX cannot be used for power MOSFETs, the parasitic resistances extracted from R3D simulation tools are inserted to the SPICE models for post-layout simulations. Figure 4.9 shows the simulated switching waveforms of the DC-DC converter at 2 A load current with all segments enabled. The rise time and fall time of the switching node is determined to be 0.72 ns and 1.10 ns respectively. The rise time and fall time of the switching node is increased to 0.86 ns and 1.20 ns respectively as the number of enabled segments is decreased to 1.

![Simulated switching waveform of the DC-DC converter at 2 A load current (all segments enabled).](image)

As the total number of enabled segments decreases, $R_{ds,on}$ of the LS switch increases and $Q_G$ decreases as shown in Table 4.3. The efficiency versus load current with different number of enabled segments is shown in Figure 4.10. Each data point is obtained from a post layout transient simulation using HSPICE.
Figure 4.10 Segmented output stage efficiency at 4MHz switching frequency.

Figure 4.11 Output stage efficiency with optimum number of enabled segments depending on load current.
With all segments enabled, the peak efficiency of 84% was achieved at load current of 2 A. In addition, Figure 4.10 also shows higher efficiency when operating with a smaller number of segments at light load condition. This is due to the effective trade-off between the gate-drive loss and the conduction loss. By changing the number of enabled segments on the fly depending on the load current, the overall efficiency can be improved as shown in Figure 4.11. This shows a clear advantage in improving the overall efficiency with output stage segmentation. For example, at light load condition, the efficiency was increased from 68% to 72% at load current of 0.4 A by changing from the 4 segment operation to 1 segment operation.

4.4 Summary

A segmented output stage containing 24V LDMOS transistors with optimum widths was designed for the implementation of a 4 MHz, 12 V to 1.2V DC-DC converter. The optimum sizes of HS and LS switches are determined by calculating the efficiency with 20 different sizes of power MOSFETs for the HS and LS switches. In order to assess the various power losses in the power MOSFETs, SPICE parameter extractions and power loss calculation methods are employed. In order to improve the light load efficiency, the LS switch is divided into 4 segments. The effect of the segmentation is verified through post-layout simulations. The layout of the output stage was thoroughly analyzed by R3D simulation tools. The metal interconnect layout was optimized such that the parasitic resistance contribution was maintained under 4.6% of $R_{ds,on}$. The peak efficiency of 84% was achieved at load current of 2 A and the light load efficiency was increased from 68% to 72% at load current of 0.4 A by changing from the 4 segment operation to 1 segment operation. The output stage IC was fabricated by TSMC 0.25 μm HV CMOS process with 4 metal layers, Ultra Thick Metal and Circuit Under Pads options. The experimental results are not yet available by the time of the completion of this thesis.
Chapter 5  Conclusion and Future Work

This thesis presents the design and optimization of the output stage in high-frequency integrated DC-DC converters for minimum power loss and the highest efficiency. In this chapter, a brief summary of the thesis and suggestions for future work are presented.

5.1 Conclusion

Switching device power losses place critical limits on the design and performance of high frequency integrated DC-DC converters. Therefore, designing an output stage requires a thorough understanding of all power loss mechanisms and effective optimization of power MOSFETs. In this thesis, the effect of the metal interconnect layout in lateral power MOSFETs is thoroughly analyzed. It is shown that the interconnect resistance contribution strongly depends on the layout and bond pad arrangements. Furthermore, a layout optimization technique by using R3D simulation tools was demonstrated with 24 V LDMOS transistors in 1 mm². The optimization includes quantitative studies on \( R_{ds,on} \) due to termination locations, metal layers, aspect ratios, number of pads, and CUP designs. After the optimization, an improvement of 55% in its on-resistance was achieved. This performance gain was obtained without any additional processing steps or changes in the device structure. Therefore, the layout optimization technique is an effective solution for improving the performance of power MOSFETs without extra processing cost. In addition, this thesis presented an optimized output stage design methodology for the implementation of a 4 MHz, 12 V to 1 V integrated DC-DC converter. The optimum width of power MOSFETs were selected from the power loss calculation method and segmentation of the power MOSFETs was implemented to increase the light-load efficiency. The peak efficiency of 84% was achieved at load current of 2 A and an improvement of 4% in light-load efficiency was achieved at a load current of 0.4 A by changing from the 4 segment operation to 1 segment operation. The segmented output stage technique is effective in reducing the gate-drive loss at light load condition and improves the overall efficiency.

5.2 Future Work

In relation to this thesis, below are some suggestions for future work.
**Safe Operating Area (SOA) characterization:** Optimizing metal interconnects not only minimizes the contribution of metal parasitic resistance on $R_{ds, on}$, but also changes the transistor operating condition in terms of “de-biasing”. Since SOA primarily depends on $V_{DS}$ and $V_{GS}$ of power MOSFETs, characterizing SOA of metal optimized power MOSFETs is necessary in order to design the output stage for robustness.

**New interconnect and contact processes:** Future work may take advantage of new developments in power interconnect and contact process. Aside from Thick Al process used in this thesis, Thick Plated CuNiPd and Thick Cu Damascene processes are recently available in a few foundries. Since Cu provides lower sheet resistance, further reduction in the contribution of parasitic resistance on $R_{ds, on}$ may be achieved.
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