HIGH-DENSITY POWER MANAGEMENT ARCHITECTURE FOR PORTABLE APPLICATIONS

by

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A thesis submitted in conformity with the requirements for the degree of Doctor of Philosophy Graduate Department of Electrical and Computer Engineering University of Toronto

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ABSTRACT

This thesis introduces a power management architecture (PMA) and its on-chip implementation, designed for battery-powered portable applications. Compared to conventional two-stage PMA architectures, consisting of a front-end inductive converter followed by a set of point-of-load (PoL) buck converters, the presented PMA has improved power density. The new architecture, named MSC-DB, is based on a hybrid converter topology that combines a fixed ratio multi-output switched capacitor converter (MSC) and a set of differential-input buck (DB) converters, to achieve low volume and high power processing efficiency. The front-end switched capacitor stage has a higher power density than the conventionally used inductive converters. The downstream differential-input buck converters enable tight output voltage regulation, and allow for a drastic reduction of output filter inductors without the need for increasing switching frequency, hence limiting switching losses and improving the efficiency of the system. Furthermore, the new PMA provides battery cells balancing feature, not existing in conventional systems.
The PMA architecture is implemented both as a discrete prototype and as an application-specific integrated circuit (IC) module. The on-chip implemented architecture is fabricated in a standard 0.13 $\mu$m CMOS process and operates at 9.3 MHz switching frequency. Experimental comparisons with a conventional two-cell battery input architecture, providing 15 W of total power in three different voltage outputs, demonstrate up to a 50% reduction in the inductances of the downstream converter stages and up to a 53% reduction in losses, equivalent to the improvement of the power processing efficiency of a 12%. Moreover, the fabricated IC module is co-packaged with low-profile thin-film inductors, to demonstrate the effectiveness of the introduced architecture in reducing the volume of PMAs for portable applications and possibly providing complete on-chip implementation of PMAs in near future.
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List of Acronyms

PMA  Power Management Architecture
SMPS  Switch-Mode Power Supply
SOC   State-of-Charge
SC    Switched-Capacitor
ASIC  Application Specific Integrated Circuits
PWM   Pulse Width Modulator
DPWM  Digital Pulse Width Modulator
DC    Direct Current
ADC   Analog-to-Digital Converter
DAC   Digital-to-Analog Converter
CCM   Continuous Conduction Mode
CPM   Current Program Mode
CPU   Central Processing Unit
USB   Universal Serial Bus
DCR   DC resistance
FSM   Finite State Machine
IC    Integrated Circuits
PMIC  Power Management IC
MSC Multi-Output Switched-capacitor Converter

DB Differential Buck

SCB Switched-Capacitor Buck

PCB Printed Circuit Board

PI Proportional Integrator

PID Proportional Integral Derivative

AC Alternating Current
Chapter 1

Introduction

This thesis presents the design and practical implementation of a high power density integrated power management architecture (PMA) for portable applications, such as cell phones, smart phones, tablets, and laptop computers. In the following sections, common design requirements of power management architectures in such applications are examined, implementation challenges are identified, and thesis objectives are formulated accordingly.
1.1 Design Requirement of Power Management Architectures in Modern Portable Applications

In modern portable electronic devices, power management architectures (PMA) play the essential role of delivering power from the input battery source to different components of the devices. As shown in Fig. 1.1, these components include display, memory, connectivity components, CPU and GPU, peripherals etc. Design specifications in portable electronics, require PMAs to:

![Fig. 1.1 Power management architecture (PMA) in modern portable electronic devices](image)
• provide multiple regulated output voltages, regardless of input battery state-of-the-charge (SOC)
• demonstrate high power processing efficiency to improve battery life and to decrease heat generation, reducing cooling requirements
• maintain high light-load operating efficiency, as these devices spend significant portion of the their life time in idle/sleep mode
• result in low volume implementation, with the possibility of on-chip integration, to minimize discrete component count, due to limited area and small form factors of such portable devices
• perform tight dynamic regulation of output voltages, providing fast transient response, to minimize the size of energy storage components
• implement simple controllers with additional features, such as over-current protection and dynamic efficiency optimization

Furthermore, for applications utilizing multiple Li-ion cells, cell-balancing is a highly desirable feature for PMAs, to extend battery life of the device. As pointed out above, significant challenges exist in both design and implementation of power management solutions for modern battery powered portable electronic devices. This is mainly due to the limited battery life and the compact, light-weight design of these devices. Furthermore, looking forward as more and more features are being included in these miniaturized computers, including larger display, faster processing speed etc., the power management solution is proven to be one of the major challenges in portable applications [1].
1.2 Research Motivation

Portable electronic devices, such as tablets and smartphones, are one of the largest and fastest growing markets of the current time, with more than 1 billion smartphones being sold worldwide in both 2013 and 2014 as well as an astonishing growth in tablet sales, forecasted 5 times increase between 2013 and 2017. Fig. 1.2 and 1.3 show global sales and forecasts for smartphones and tablets, respectively.

Fig. 1.2 Global smartphone shipments forecast from 2010 to 2018 (in million units) (source: statista.com)
In tablets, smartphones, and other more conventional portable devices such as cell phones, laptop/notebook and ultra book computers, PMAs are considered key components, as they power up various functional blocks, including digital processors, I/O interfaces, and memory devices. As a result in these portable devices, PMAs are required to provide different voltage levels, utilizing as many as 30 separate dc-dc converters, consisting of switch mode power supplies (SMPS) and linear low-dropout regulators (LDO) [2]. As shown in Table I, the cost of power management solution is quite significant (up to 8%) considering the bill of materials (BOM) of these devices (excluding mechanical parts, packaging and licensing fees).
Table I: BOM breakdown of smartphones and tablets

<table>
<thead>
<tr>
<th>Type</th>
<th>Smartphone (iPhone5) $</th>
<th>(%)</th>
<th>Tablet (Nexus7) $</th>
<th>(%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory</td>
<td>20.85 (18.15%)</td>
<td></td>
<td>21.00 (26.67%)</td>
<td></td>
</tr>
<tr>
<td>Processor</td>
<td>17.50 (15.24%)</td>
<td></td>
<td>21.00 (26.67%)</td>
<td></td>
</tr>
<tr>
<td>Sensors</td>
<td>6.50 (5.66%)</td>
<td></td>
<td>11.00 (13.97%)</td>
<td></td>
</tr>
<tr>
<td>Camera</td>
<td>18.00 (15.67%)</td>
<td></td>
<td>2.50 (3.17%)</td>
<td></td>
</tr>
<tr>
<td>Cellular Radio</td>
<td>34.00 (29.60%)</td>
<td></td>
<td>N/A</td>
<td></td>
</tr>
<tr>
<td>Wireless Radio</td>
<td>5.00 (4.35%)</td>
<td></td>
<td>5.00 (6.35%)</td>
<td></td>
</tr>
<tr>
<td>Battery</td>
<td>4.50 (3.92%)</td>
<td></td>
<td>12.75 (16.19%)</td>
<td></td>
</tr>
<tr>
<td><strong>Power Management</strong></td>
<td><strong>8.50 (7.40%)</strong></td>
<td></td>
<td><strong>5.50 (6.98%)</strong></td>
<td></td>
</tr>
<tr>
<td>Total Cost</td>
<td>114.85</td>
<td></td>
<td>78.75</td>
<td></td>
</tr>
</tbody>
</table>

(sources: digitaltrends.com (iPhone5), technology.ihs.com (Nexus7))

One of the major challenges related to the implementation of the traditional power management architectures is their overall size and cost. In numerous portable devices they take up a large portion of the overall volume [3], [4] and significant contributor to the overall BOM (Table I). This is largely due to the bulky and costly reactive components of the SMPS output filters. In
portable applications, PMAs are often implemented in integrated circuits (IC), also known as power management ICs (PMICs), due to the strict limitation of available space. A typical PMIC consists of semiconductor switches, along with gate drivers, controller and sensing circuitries, packaged on the same silicon die. However, bulky reactive components, such as inductors and capacitors, often cannot be integrated in PMICs [5], [6]. As a result, the overall volume of the existing power management solution is largely contributed by the output filter reactive components, where inductors are most dominant [7].

Fig. 1.4 and 1.5 show the existing power management solutions for Nexus 5 smartphone and Apple Ipad Air tablet, respectively. As shown in these figures, significant portion of the PCB area and device volumes is consumed by off-chip reactive components, particularly inductors.
Integration in the form of PMIC allows minimizing number of discrete components, and results in improved performance due to reduction in parasitics. As a result, a significant growth in PMIC market is forecasted (Fig. 1.6) to meet the ever increasing demand for the volume reduction of PMAs. This is particularly important for portable applications, where the future demands of such devices are expected to grow drastically and the devices are becoming smaller and thinner, while boosting their performance.

Fig. 1.5 Power management solution in Apple Ipad Air (source: ifixit.com)
Furthermore, as in existing portable electronics market segment, power management solutions are mostly designed and implemented by semiconductor companies. Integration reduces the amount of off-shelf discrete components, saving their associated costs. Fig. 1.7 shows the current market share of PMIC in portable applications.
However, reactive components, particularly inductors, in the existing power management solutions, are often difficult to integrate with PMICs [5], [6], due to their large volume, resulting in increased cost of implementation. As a result, off-chip discrete inductors are the most commonly used, contributing to a significant portion of the PCB area and overall implementation volume for PMAs [7].
1.3 Thesis Objectives

The goal of this thesis is to reduce the volume requirement of PMAs in portable applications. This is presented in three steps as follows:

1. Introducing novel power management architecture, with the following two advantages over conventional solutions:
   
   i. Reduced number of inductors, and
   
   ii. Significantly smaller size of the inductors.

2. Design and fabricate custom power management IC (PMIC) to verify effectiveness of the introduced solution, in reducing the volume of the PMA.

3. Finally, combine the introduced PMIC with integrated inductors, to demonstrate a complete on-chip solution for PMA.

In addition to the development of novel power management architecture and its IC implementation, this thesis also focuses on developing associated controllers. The complete solution proposed in this thesis is suitable for a wide range of applications, beyond portable devices. In addition to the volume reduction, the introduced PMA also allows improved efficiency for power conversion, increasing battery life of the portable devices. As shown in this thesis, the introduced architecture increases the level of integration in power management solutions, by significantly reducing inductance volumes, and creating the possibility of integrating them on the same silicon die as PMICs.
1.4 Thesis Outline

The thesis is organized as follows:

Chapter 2 reviews the background and prior art of the presented research work. It presents a big picture of how power management is done in existing solutions along with the major challenges for low volume implementation. A brief summary of state-of-the-art solution and prior art is also given, along with a discussion of their limitations.

Chapter 3 presents the novel power management solution targeted for low volume power management implementation in portable applications. Details of operation principles, practical implementation and comparison with existing architecture are presented.

Chapter 4 is focused on the integration of the introduced architecture in Power Management IC (PMIC). Design details and implementation challenges are addressed. Furthermore, this chapter also shows how the introduced power management architecture can combine PMIC with integrated inductors, to create fully integrated power management solutions.

Chapter 5 presents a wide range of applications, beyond portable applications, where the implemented IC can be useful. The range of application is from energy harvesting dc-ac multi-level inverters to differential power processing in dc-dc power converter applications.

Finally, this thesis is concluded in Chapter 6, summarizing the main contributions of the presented work, as well as exploring the directions for possible future research.
Appendix A shows a low-power accurate current sensing technique, suitable for IC implementation. This technique can be incorporated in existing PMAs to acquire current information, without compromising efficiency and accuracy. Appendix B presents power management architecture for universal input ac-dc adapter support in battery powered laptop/notebook and ultra-book applications. The presented solution allows combining several power processing stages into one, reducing component count and implementation volume in the targeted applications. Materials presented in the appendices are not essential components of this thesis, but associated with existing power management solutions for portable applications.

1.5 References


Chapter 2

Background and Prior Art

2.1 Power Management Architecture in Portable Applications

In modern battery powered portable applications, such as cell phones, laptop, or tablet computers, power management systems provide multiple voltage levels using many different dc-dc converters [1]. These voltages are supplied to various functional blocks, including digital processors, I/O interfaces, and memory devices. A conventional power management architecture
(PMA) is shown in Fig. 2.1. It consists of a front-end dc-dc converter, connecting the input voltage source (typically a battery pack) and creating a stable intermediate bus voltage. As the Li-ion battery cells are commonly used in these applications, the input voltage varies depending on the battery state-of-charge (SOC). The front end bus regulator maintains the intermediate bus voltage at a fixed voltage level, typically at 5V, regardless of the SOC.

A number of downstream dc-dc conversion stages, consisting of switch-mode power supplies (SMPS) and/or low-dropout (LDO) linear regulators, while connected to the intermediate bus voltage, provide multiple output voltages. These downstream stages are required to meet specific steady state and dynamic voltage requirements [1]-[3] of various functional blocks. In a typical
portable application, these voltage levels include 5V for USB and other peripherals, 3.3V for analog circuitry, such as power amplifiers, memory units and 1V for digital processors and chipsets. In order to minimize the power losses and to extend battery life of the device, both stages in this two-stage conversion process are required to be very efficient.

### 2.2 Switched Mode Power Supply: Topology Limitation

Switch mode power supplies (SMPS) are widely used in electronic devices to provided dc-dc voltage conversions. Depending on the application and power rating, a wide range of SMPS topologies are utilized. The switching stage (i.e. power stage) of a SMPS consists of two major building blocks as shown in Fig. 2.2. First, the switching network, consisting of semiconductor components, such as switches and diodes and the second is input and output filter, consisting of reactive components, such as inductors and capacitors.
As mentioned in Chapter 1, in the targeted low power portable applications, semiconductor components can often be integrated on integrated circuits (IC), allowing low implementation volume. However, the filter components, being bulky and mostly off-chip discrete elements, consume a large volume of the SMPS implementation. Fig. 2.3 shows the switching network and output filter of a conventional buck converter. The input and output voltages of the buck converter is denoted as $V_{in}$ and $v_{out}$, respectively. As shown by the waveforms of Fig. 2.3, the complementary gating signals of switches, $SW_1$ and $SW_2$, results in a voltage swing of $V_{in}$ at the switching node, $v_{s}(t)$. As a result, for a conventional buck converter, the switching node has a voltage swing of the full input voltage, $V_{in}$. The output filter, consisting of inductor, $L$ and capacitor $C_{out}$, works as a low pass filter. Due to the voltage swing at the switching node, the inductor and capacitor have associated current and voltage ripples as shown by the waveforms. Hence, the size of the output filter for given ripple requirement of a dc-dc converter, is

Fig. 2.2 Switch mode power supplies (SMPS) building blocks
determined by two major components of the SMPS implementation, i) voltage swing at the switching node and ii) switching frequency.

![Conventional buck converter topology and steady state waveforms](image)

Fig. 2.3 Conventional buck converter topology and steady state waveforms

The ever increasing demand for lower volume power management solutions in battery powered portable electronics has commonly been met by switching at higher frequencies, up to several hundred megahertz [4], allowing smaller filter size. However, a higher switching frequency
comes with a penalty of increased switching [5] and magnetic [6] losses, negatively affecting power processing efficiency and, therefore, reducing the battery life of portable devices. Furthermore, the reduced efficiency combined with a smaller volume of converter results in significantly higher heat density, creating a bottle-neck for further miniaturization of PMAs. The higher heat density can result in the overheating of the entire device or put a requirement for an additional cooling system, completely nullifying the obtained volume and weight savings.

2.3 Integrated Magnetics: State-of-the-art Solutions and Trade-offs

In order to solve the issue of large volume requirement for inductor implementation, new technologies focused on integrated magnetics are also being developed in both industry and academia. Although integrated inductors are more feasible and practical for RF applications [7], in power converters they are not yet widely adopted for poor efficiency, large on-chip area requirements for unconventional and costly IC implementation technologies etc [8]. In a more recent work, Tyndall institute from Ireland, developed on-chip integrated inductors, compatible with CMOS technology. The race track shaped inductor, shown in Fig. 2.4, has several advantages, making it closer to the real application need. These include good frequency response of up to 100 MHz, relatively high inductance density of up to 100nH/mm² and high efficiency (above 85%).
Fig. 2.4 Racetrack shaped integrated inductors from Tyndall National Institute, Ireland

Fig. 2.5 shows integrated inductor efficiencies with respect to their inductance values and on-chip implementation area. Inductor efficiency is defined by Eq. 2.1, and only includes inductor losses. Power converter losses, i.e. conduction and switching, are not included here.

\[ Efficiency_{inductor} = \frac{P_{out}}{P_{out} + P_{loss\_inductor}} \]

where, \( P_{out} \) is total output power and \( P_{loss\_inductor} \) is inductor losses, including core loss (i.e. eddy currents, hysteresis) and winding losses (i.e. ac and dc currents).
The trade-offs between the inductance value and the efficiency of these inductors, impose a practical challenge for incorporating them in conventional power management topologies. As shown in Fig. 2.5, for a given area for on-chip implementation, the inductors become more efficient as their values decrease. In other words, high efficiency of these inductors can only be achieved by operating the conventional converters at very high switching frequency, requiring minimal filter inductance. However, as already mentioned, this would create additional switching losses in the converter, negatively affecting the power conversion efficiency. As a result, the conventional power management architectures do not result in practical low volume solutions, incorporating on-chip inductors.
2.4 Step-Down Conversion in Portable Applications

This section reviews different step-down conversion techniques in portable applications. In addition to the brief description of each of the approaches, associate advantages and disadvantages are also mentioned.

2.4.1 Buck converter

Buck converters are widely used as step-down dc-dc converters in portable applications, for both front-end and downstream dc-dc conversion, due to several advantages. These include low component count, tight output voltage regulation including good dynamic response, relatively flat efficiency characteristics for variations in operating conditions, such as changes in load current and input/output voltages. However, in portable applications as shown in Fig. 2.1, downstream SMPS buck converters operate from fixed intermediate bus voltage. This often creates a non-optimal voltage swings for the output filters of the downstream stage buck converters, resulting in bulky reactive components. As the reactive components, i.e. inductors and capacitors are difficult to integrate, and hence, commonly placed as off-chip discrete components, buck converters result in a relatively large volume for implementation when compared to switched-capacitor converters, discussed next.

2.4.2 Switched-capacitor converters

Switched-capacitor (SC) converters, consisting of only switches and capacitors, have higher energy density, compared to inductor based converters. The key advantage of SC converters is
the ability to meet the strict volume requirement of the modern portable devices [9], [10], [11], as
they don’t need bulky inductors. Hence, these converters can be implemented in a significantly
smaller volume, possibly integrating on ICs [10], [11]. Fig. 2.6 shows a simple SC active voltage
divider circuit, which provides half of the input voltage to the output.

Furthermore, SC converters show very high efficiency for fixed input-to-output voltage ratios
[10]-[12]. However, SC converters suffer from several practical challenges when considered for
portable applications. Those include sharp efficiency drop when operating away from their ideal
conversion ratios [12]-[14] and inadequate dynamic regulation [15], [16] to satisfy the demand of
modern processors.

Fig. 2.6 Operation of switched-capacitor voltage divider circuit
Chapter 2: Background and Prior Art

2.5 Combining SC with Inductor Based Topologies

A combined SC voltage divider and inductor based architecture was proposed in [17], to minimize the volume of the power management system. In that architecture, two inductors are connected to intermediate nodes of a SC voltage divider, to provide three separate output voltages of $3/4^{th}$, $1/2^{nd}$ and $1/4^{th}$ of the input voltage. The architecture shown there reduces the volume of the filtering inductors, and is very effective in fixed input voltage applications, i.e. where the input is provided from a tightly regulated voltage source. However, the output voltages are correlated due to their fixed input-to-output voltage ratios and, hence, cannot be controlled independently. In portable applications that architecture does not provide a complete solution, without introducing an additional front-end stage, since the battery voltage varies as the state-of-charge (SOC) changes.

To provide tight output voltage regulation under the input voltage variation, in [18]-[20] two-stage compact and power efficient solutions are presented (Fig. 2.7). In these solutions, a SC fixed-ratio front-end stage performs a large portion of voltage conversion at the peak efficiency, and provides a bus voltage that is loosely regulated. The inductor-based downstream stage then provides final regulation, while connected to this bus and dealing with small conversion ratio. This arrangement reduces the voltage swing at the switching node of the inductor based stage, relaxing the requirement of the filter inductor, while improving the efficiency at the same time, due to a lower input-to-output voltage conversion ratio [5], [21]. However, for applications where multiple regulated output voltages are required, this concept of single unregulated bus voltage does not result in optimum voltage swings for all the downstream stages, and hence cannot easily be extended.
Novel converters merging switched-capacitor and inductor based topologies are proposed in [22]-[24]. These topologies, while sharing semiconductor components, reduces component count compared to two-stage solutions. Although these solutions can be attractive for providing a well regulated output voltage, they cannot be simply extended as a complete power management system for portable applications, where multiple regulated voltages are required. Moreover, single output solution of [22], suffers from isolated ground between the input and output voltages, limiting its adoptability in low power applications where common ground is required. The multi-phase solution of [23] has comparable component count compared to two-stage systems and results in additional controller complexity. The solution presented in [24], is more
suitable for high power applications and has limited use in low power portable applications due to significant implementations challenges, including start-up, gate driver implementation, transient response etc.

2.5 References


Chapter 3

LOW-VOLUME POWER MANAGEMENT SOLUTION FOR PORTABLE APPLICATIONS

3.1 Introduction

In this chapter the concept of combined switched-capacitor and inductor based power processing is utilized, where both front-end and downstream stages of the conventional architecture of Fig. 2.2 are completely redesigned, to obtain further improvements in both size reduction and power processing efficiency. The goal of the introduced architecture is to combine the advantages of
Chapter 3: Low-Volume Power Management Solution for Portable Applications

the switched capacitors converters, such as high efficiency, low volume, together with the benefits of the inductor based topologies, including tight regulation and fast transient response.

In the introduced architecture, named MSC-DB and shown in Fig. 3.1, the front-end converter is replaced with a multiple-output SC (MSC) stage and, instead of operating at the full bus voltage, the downstream 2-input dc-dc converters, are stacked up across the intermediate capacitor network. This stacked up 2-input configuration can be considered as differential input for the downstream stages and hence, referred to as differential buck (DB) converters. It will be shown here, this arrangement results in minimization of the inductors of downstream stages, through reductions of the voltage swings at switching nodes and in further efficiency improvement, through reduction of switching losses. Moreover, the new PMA incorporates battery cell balancing, usually not present in conventional systems, allowing for extension of battery operating times. An additional advantage of this architecture is that, unlike conventional two-stage solutions, it can be implemented with a fairly simple single controller regulating operation of both power conversion stages.

Fig. 3.1 Multi-output SC (MSC) based introduced power management architecture
This chapter is organized as follows: details of principle of operation are explained in Section 3.2. Section 3.3 describes the practical implementation of a digital and a mixed-signal controller for the introduced power management architecture. Section 3.4 shows a simple implementation of the battery cell balancing feature that further improves power processing efficiency. Section 3.5 describes experimental prototype and results verifying advantages of the introduced PMA. The final Section 3.6 provides summary of this chapter.

### 3.2 Principle of Operation

In low-power applications switched-capacitor (SC) converters are preferred over conventional switch-mode power supplies (SMPS) as they do not require bulky inductors, and hence can easily be implemented on integrated circuits [1], [2]. Such SC networks operate most efficiently (up to 97% [3]) at fixed input-to-output voltage ratios. However, they demonstrate significant efficiency degradation when they are required to provide a fixed output voltage as the input voltage varies [4]. The transient response of SC circuits is also inferior compared to conventional SMPS alternatives [5], making them unsuitable for applications where strict voltage regulation and transient response requirements need to be met. On the other hand, SMPS requires bulky inductors, especially in the cases when relatively large conversion ratios are required [6].

The MSC-DB power management architecture introduced in this chapter (Fig. 3.1) combines a multi-output switch-capacitor (MSC) with a set of modified differential-input buck (DB) converters [7]. The front-end MSC stage operates with a fixed conversion ratio at the peak power processing efficiency. The downstream DB converters providing tight regulation are connected
across the individual output capacitors of the MSC stage, to minimize the voltages across the converters’ components, resulting in volume and loss reductions. In the following subsections, advantages of this design over the conventional solutions are further elaborated and more details on the principle of operation of MSC-DB architecture are provided, followed by a comparison with the conventional solution.

3.2.1 Multi-output fixed ratio switched-capacitor converter

The multi-output switched-capacitor (MSC) front-end stage replaces the inductor-based converter of the conventional solution (Fig. 2.1), increasing the power density of the front-end part of the converter. SC converters can be significantly more cost and area effective compared to their inductive counterparts [8], due to several reasons. First, in contrast to the conventional buck or a boost converter, which requires a bulky inductor, the SC dc-dc converter requires only capacitors. In the applications of interest inductors are much larger than capacitors for the same energy and power handling capability. According to [8], the capacitors have up to three orders of magnitude higher energy density for all practical frequencies of interest, allowing SC converters to have higher power density without sacrificing efficiency. The significantly lower energy density of the inductors makes them much more difficult to integrate than capacitors, due to area and associated cost constraints of the IC processes. Also, SC converters demonstrate higher power density and improved efficiency as the IC technology is gradually scaling down [9], making them more suitable for integrated dc-dc converters. In addition, more recent development of advanced implementation technique of on-chip capacitor, such as trench technology, is further improving the performance of SC converters [10]. This means that, the MSC front-end stage not
only improves power density but also opens a possibility for a full-on chip in the future without introducing any additional cost, area and/or efficiency penalty compared to conventional buck converters. More importantly, as shown in the following subsection, the MSC stage contributes to a drastic improvement in the power density of the downstream stages.

The multi-output switched-capacitor converter (MSC) [9] stage is shown in Fig. 3.2. In this MSC stage, six switches ($SW_{1-6}$) and two flying capacitors ($C_{s1,2}$) are utilized to provide 2/3 and 1/3 of the battery pack voltage, $V_{batt}$ across the intermediate capacitor network, consisting of three capacitors ($C_{mid1-3}$). This stage is a modified version of the well-known single output switched-capacitor voltage divider [11]. Compared to the single-output topology, this MSC stage has two additional switches and an extra shuttling capacitor, to accommodate multiple outputs.

To maintain constant $V_{batt}/3$ voltage across all intermediate capacitors, the shuttling capacitors redistribute the charge difference through a two-phase switching sequence. In phase 1 (labeled with dashed lines $\Phi_1$ in Fig. 3.2), $SW_1$, $SW_3$, and $SW_5$ are turned on, to connect 3 capacitors $C_{s1}$, $C_{s2}$ and $C_{mid3}$ in series with equal voltages, $V_{batt}/3$ across each of them. Similarly in phase 2 (marked with solid line $\Phi_2$ in Fig. 3.2), $C_{mid1}$, $C_{s1}$ and $C_{s2}$ are connected in series with equal voltages, $V_{batt}/3$ across each of them, through $SW_2$, $SW_4$ and $SW_6$. In order to maintain high conversion efficiency the MSC operates with equal duty ratios of 50%, for both the phases [9].

It is important to mention here that, even though, the MSC converter has higher number of switches than the conventional buck, the smaller volt-ampere (V-A) product of these switches [12] yields to a lower conduction and switching losses. This is due to the fact that the SC switches block only a portion of the input voltages. Also, most switches carry a significantly smaller current than those of the buck converter.
Fig. 3.2 Triple output front-end multi-output switched capacitor (MSC) stage
3.2.2 Modified downstream buck converters

One of the main problems of SC converters operating in a closed loop is that they demonstrate significant efficiency degradation when the input voltage varies [13]. The transient response of SC circuits is also inferior compared to conventional SMPS alternatives [14], making them unsuitable for applications where strict voltage regulation and transient response requirements need to be met. The front-end MSC stage of the introduced architecture shares the same drawback. For that reason it is not required to provide regulation of the output tap voltages, in case of input battery voltage variations. As the battery cell voltages vary, the intermediate voltages also vary, maintaining the desired fixed input-to-output ratio and peak efficiency. In the targeted applications, this change is slow and fairly constrained, due to the limited variation exhibited by the battery pack voltage, imposed by inside-the-pack integrated protection preventing full discharge [15]. To compensate for the battery’s state-of-charge (SOC) dependent voltage variations, the MSC stage is connected to a string of modified buck converters providing regulated output voltages, as shown in Fig. 3.3.

Each of these downstream differential buck (DB) converters is based on the dual-input buck converters, originally introduced in [16] for higher power ac-dc and dc-dc applications. In those applications dual-input buck converter provides a single output voltage from two input voltages provided by a flyback converter. It was shown that the dual-input buck, i.e. differentially connected buck, results in a drastic reduction of the output filter inductance value and minimization of the switching losses, significantly improving conversion efficiency. Furthermore, as explained in [16], dual-input converter reduces voltage stress across the transistors and can be controlled utilizing conventional control techniques.
In the architecture introduced in this thesis, the concept of dual-input buck is extended to multiple regulated outputs, while maintaining all the above-mentioned advantages. Also, the bulky dual-output flyback converter, earlier used to provide two input voltages, is replaced with low-volume and high-efficiency fixed-ratio MSC stage, as described in the previous subsection.

Fig. 3.3 Differentially connected buck (DB) downstream stages
In MSC-DB, the inductors are drastically minimized through reduction of their voltage swings. The voltage-swing based reduction principle and the size of reduction can be described through the following analysis, based on the constant current ripple criteria. The current ripple, \( \Delta i_L \) and duty ratio, \( D \) equations for a general single inductor-based converter in continuous conduction mode are:

\[
\Delta i_L = \frac{V_{L_{on}} \cdot D}{2 \cdot L \cdot f_{sw}} = \frac{V_{L_{off}} \cdot (1 - D)}{2 \cdot L \cdot f_{sw}}, \tag{3.1}
\]

\[
D = \frac{V_{L_{off}}}{V_{L_{on}} + V_{L_{off}}}, \tag{3.2}
\]

where \( L \) is the inductance value, \( f_{sw} \) is the switching frequency, \( V_{L_{on}} \) and \( V_{L_{off}} \) are the voltages across the inductor during on and off states of the main switch, respectively. Substituting (3.2) in (3.1) gives:

\[
\Delta i_L = \frac{1}{2 \cdot L \cdot f_{sw}} \cdot \left( \frac{V_{L_{on}} \cdot V_{L_{off}}}{V_{L_{on}} + V_{L_{off}}} \right), \tag{3.3}
\]

In the conventional buck converter \( V_{L_{on}} = (V_{in} - V_{out}) \) and \( V_{L_{off}} = V_{out} \), where \( V_{in} \) and \( V_{out} \) are the input and output voltages of the converter, respectively. As a result, by manipulating (3.3) the expression for the inductor value of a conventional buck can be written as:

\[
L_{buck} = \frac{1}{2 \cdot \Delta i_L \cdot f_{sw}} \cdot \left( \frac{(V_{in} - V_{out}) \cdot V_{out}}{V_{in}} \right), \tag{3.4}
\]
The most common approach to minimize the inductor value, while maintaining the same current ripple, is to increase the switching frequency \([17]\). However, this approach results in increased switching losses \([18]\) and therefore, poses a fundamental limit on the inductor size reduction. In the modified buck converters of Fig. 3.3, the inductors are reduced by minimizing \(V_{L, on}\) and \(V_{L, off}\) values of (3.1). This is achieved by setting the two possible switching node (\(v_x\) of Fig. 3.3) voltage values, \(V_{high}\) and \(V_{low}\), to be about \(V_{bat}/6\) larger and smaller than the desired converter output voltage, respectively.

The resulting reduction of the inductor values can be found by comparing their expressions. For the differential-input buck, (or 2-input buck converter), the equation for its inductance value can be found from (3.3) and written as:

\[
L_{2-input} = \frac{1}{2.\Delta f_{sw}} \frac{(V_{high} - V_{out})(V_{out} - V_{low})}{V_{high} - V_{low}}, \quad (3.5)
\]

By dividing (3.5) by (3.4), we get:

\[
\frac{L_{2-input}}{L_{buck}} = \frac{(V_{high} - V_{out})(V_{out} - V_{low})}{(V_{high} - V_{low})} \cdot \frac{V_{in}}{(V_{in} - V_{out})V_{out}}, \quad (3.6)
\]

which can be simplified as,

\[
\frac{L_{2-input}}{L_{buck}} = \frac{(1 - \frac{V_{out}}{V_{high}})}{(1 - \frac{V_{out}}{V_{in}})} \cdot \frac{(1 - \frac{V_{low}}{V_{out}})}{(1 - \frac{V_{low}}{V_{high}})}, \quad (3.7)
\]

Equation (3.7) proves that the differential buck has a smaller inductor, since \(V_{high} \leq V_{in}\) and \(V_{out} \leq V_{high}\) (Fig. 3.3) and considering both parts of (3.7)

\[
\frac{(1 - \frac{V_{out}}{V_{high}})}{(1 - \frac{V_{out}}{V_{in}})} \leq 1 \quad \text{and} \quad \frac{(1 - \frac{V_{low}}{V_{out}})}{(1 - \frac{V_{low}}{V_{high}})} \leq 1
\]
and, even more importantly, gives analytical expression for the reduction in the inductance value. In the following subsection, this equation is used to quantitatively determine the reductions in the output filter inductors in a standard power management system of the interest.

### 3.2.3 Comparison with conventional architecture

In this subsection a comparison between MSC-DB and the conventional power management architecture is provided. Typical PMA for portable applications is considered in this case, where two series-connected standard 3.3V lithium-ion cells (whose voltage varies between 2.7V and 3.6V [20], [21]) are used. The standard output voltages are 1 V for the digital processors, 3.3V for analog components, and 5V for USB ports and other peripherals. Applications for such architectures include tablet computers and a number of other mobile devices. Fig. 3.4 shows the complete architecture, including MSC stage and differentially connected downstream buck converters as well as the types of transistors used for this implementation. One key point to note here is although the downstream buck converters are connected differentially in MSC-DB architecture, all three outputs are referred to the same ground, which is also the ground of the MSC stage.
In order to compare the advantages of MSC-DB, the conventional system of Fig. 2.1 is considered. The conventional system operates under the same conditions, where a front-end bus converter [22] provides a well-regulated 5V intermediate bus voltage over the entire range of the battery pack voltage variations.

Eq. (3.7) is used to calculate the normalized inductance values of MSC-DB with respect to the conventional architecture. For the differential buck $buck_2$, providing 3.3V output in Fig. 3.4, the normalized value for the inductor ($L_2$) is plotted on a 3-dimensional surface, shown in Fig. 3.5.
this plot, $V_{\text{high}}$ and $V_{\text{low}}$ of the 2-input $\text{buck}_2$ converter is represented by x and y-axis respectively and z-axis shows the normalized value of inductance, $L_2$ (Fig. 3.4). $V_{\text{in}}$ and $V_{\text{out}}$ in eq. (3.7) is 5V and 3.3V respectively, since in the conventional architecture, the buck providing 3.3V operates from the 5V bus. The results are shown for the sweep of $V_{\text{low}}$ from 0V (corresponding to conventional buck) to 3.3V (its maximum value) while, similarly, $V_{\text{high}}$ ranges from 3.3V to 5V, and the range of voltage variations for a realistic system is labeled with points B and C in the diagram.

The diagram shows that, the MSC-DB allows for a drastic reduction of the inductance value, while operating at the same switching frequency and under the same ripple requirement. This is demonstrated by points A, B and C in Fig. 3.5. Point A corresponds to the conventional topology where 5V bus voltage results in the normalized value of inductance to be 1, as the plot is normalized with respect to this particular operating condition. Depending on the battery SOC $V_{\text{high}}$ of 2-input $\text{buck}_2$, i.e. the high value of the node $v_{x2}(t)$ in Fig. 3.4, can vary between 4.8V and 3.6V ($2/3$rd of $V_{\text{batt}}$) and its $V_{\text{low}}$ value can vary between 2.4V and 1.8V ($1/3$rd of $V_{\text{batt}}$). These two extreme operating points are labeled as B and C on Fig. 3.5. The line joining these two points shows the range of inductance reduction for 2-input $\text{buck}_2$ providing 3.3V output, depending on battery SOC. As shown by point B, which is the worst-case operating condition, MSC-DB has about a 50% smaller inductor of the buck proving 3.3V output.
Chapter 3: Low-Volume Power Management Solution for Portable Applications

Fig. 3.5 Normalized value of the inductance for the differentially connected 3.3V buck converter of the MSC-DB PDA

Similarly, in order to compare the inductance values of the bottom downstream buck, i.e. buck3 of Fig. 3.4, to that of the conventional system, eq. (3.7) can be used again. However, since in this case $V_{low} = 0V$ (ground), Eq. (3.7) can be simplified as:

$$
\frac{L_3}{L_{buck}} = \frac{1 - \frac{V_{out}}{V_{high}}}{(1 - \frac{V_{out}}{V_{in}})}, \quad (3.8)
$$

As a result of this simplification, for buck3, providing 1V output, the normalized inductor value can be shown on a 2-dimensional graph (Fig. 3.6), where x and y-axis represent $V_{high}$ and normalized value of inductance, $L_3$, respectively.
For the system under the consideration $V_{in}$ and $V_{out}$ in eq. (3.8) are 5V and 1V, respectively, as in the conventional architecture of Fig. 2.1, 1V buck operates from a 5V bus. Again, MSC-DB allows a significant reduction of inductance, while operating at the same switching frequency and under the same ripple requirement.

The quantitative reduction is demonstrated by points D, E and F of Fig. 3.6. Here, point D represents conventional topology having the normalized value of inductance 1. Like in the previous case, two extreme values of reduction in $L_3$, depending on the battery SOC are labeled with points E and F. As shown by point E, the worst-case condition, MSC-DB results in more than 27% reduction of the inductance value, $L_3$.

Fig. 3.6 Normalized value of the inductance for differentially connected 1V buck converter
3.2.3.1 Comparison of 5V outputs

In comparison with the conventional architecture of Fig. 2.1, where the front-end dc-dc converter provides a fixed 5V bus voltage, the front-end MSC stage of the MSC-DB PMA does not provide a regulated 5V supply. As a result, in order to provide power to the peripheral loads, such as USB, differentially connected buck\_1 is used (Fig. 3.4). As it will be shown here, the inductor of this additional 2-input converter is much smaller than that of the front-stage of the conventional architecture.

Comparison of the front-end buck converter of the conventional architecture and the differential buck buck\_1, both providing 5V, is similar to the previous 1V output case. Since for this case, \( V_{\text{high}} = V_{\text{in}} = V_{\text{batt}} \), eq. (3.7) becomes:

\[
\frac{L_1}{L_{\text{buck}}} = \frac{\left(1 - \frac{V_{\text{low}}}{V_{\text{out}}}ight)}{\left(1 - \frac{V_{\text{low}}}{V_{\text{high}}}ight)} , \quad (3.9)
\]

Using the analysis shown in previous cases, it can be calculated that for 6.6V nominal battery input, the required inductance of the MSC-DB 5V output is about 64% smaller. However, the actual reduction of the inductor is even bigger, since the 5V MSC-DB buck processes only a small portion of the power compared to that of the conventional front-end stage. By taking into account both (3.9) and the fact that the volume of an inductor is proportional to the energy it stores, i.e. \( 0.5(L.I)^2 \), inductor volume reduction in buck\_1 can be calculated. For a 6.6 V input, this inductor reduction is proportional to approximately \( 0.36(I_{\text{load}}/I_{\text{bus}})^2 \), where \( I_{\text{bus}} \) and \( I_{\text{load}} \) are
nominal bus and load currents respectively, for the system of Fig. 2.1. Since, the current requirement of peripherals, such as USB, is only small portion (10%-20%) of the total load current [23], the size of this inductor is practically negligible compared to that of the front-end inductor in the conventional topology. Furthermore, this comparison assumes the same switching frequencies and current ripples. However, since the 5 V downstream stage of the MSC processes less power, it can potentially operate at a higher switching frequency, allowing for an even larger volume reduction [17].

### 3.2.3.2 Comparison with switching losses

As shown by the eq. (3.1 to 3.9) and graphs above, MSC-DB can achieve significant reductions of inductor volumes, without increasing the switching frequency. This is achieved due to drastic reduction of voltage swing at the switching nodes of the differential-input buck converters. The reduced voltage swing not only allows for the use of smaller inductance value but also drastically reduces switching losses. As a consequence, further reduction of the inductance values, by operating at higher switching frequencies while still maintaining improved efficiency is possible. The following subsection takes the switching losses into account and demonstrates further volume reduction, through an analysis of the system of interest.

As shown in Fig. 3.4 when operating from a 6.6 V nominal input, the buck converters of MSC-DB have voltage swings of 2.2V at the switching nodes. This reduced voltage swings translates into, lower blocking voltages for the downstream buck switches, when compared to conventional
architecture. Since, the switching losses are proportional to the blocking voltages of the switches [19], the MSC-DB buck converters have smaller switching losses. This reduction allows a significant increase in the switching frequency, while maintaining equal or better efficiency, as demonstrated in Table II. The table shows normalized values of the switching node (v_x1-3) voltage swings v_{sw,norm}, inductances L_{norm}, as well as calculated values of semiconductors switching losses P_{sw,norm} for the implemented topology of Fig. 3.4, with respect to their equivalents in a conventional topology. The calculations of the losses are performed using well-known analysis, described in [5], under the previously described nominal operating conditions. The results of this analysis match the obtained experimental results, demonstrated later.

Table II shows that, for the same switching frequency, not only reductions in the inductor size by 50% and 27% but also that the reduction is accompanied with reductions in switching losses. The losses are reduced up to a 44% of the conventional value [19]. Furthermore, the table also shows that, if operating at twice the switching frequencies, the MSC based architecture can achieve inductor volume reductions that exceed 75% while maintaining lower switching losses than the conventional counterpart. The results of this analysis confirming significant improvements in power density, i.e. reduction of volume and simultaneous efficiency improvements are later confirmed with experimental results, shown in Section 3.5.
Table II: Inductor volume and switching loss reductions

<table>
<thead>
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<th>$V_{sw_norm}$</th>
<th>$L_{norm}$</th>
<th>$P_{sw_norm}$</th>
<th>$f_{sw_norm}$</th>
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<td>0.44</td>
<td>1</td>
</tr>
<tr>
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<td>0.73</td>
<td>0.44</td>
<td>1</td>
</tr>
<tr>
<td>Dual-input buck 3.3 V (incr. $f_{sw}$)</td>
<td>0.44</td>
<td>0.25</td>
<td>0.88</td>
<td>2</td>
</tr>
<tr>
<td>Dual-input buck 1 V (incr. $f_{sw}$)</td>
<td>0.44</td>
<td>0.27</td>
<td>0.88</td>
<td>2</td>
</tr>
</tbody>
</table>

Considering the advantages of MSC-DB architecture, it can be concluded that the topology results in significantly smaller volume requirement for the bulky inductors compared to the conventional topology and results in much lower switching losses, providing higher efficiency. This is the key to achieve a practical low volume implementation as reducing the volume without increasing the efficiency would result in higher heat density, requiring larger heat sinks and/or advanced cooling systems. As discussed already, this topology is able to achieve this by combining the best from both the worlds of switched-capacitor and inductor-based converter designs. The multi-output switched-capacitor stage (MSC), while consuming smaller volume and operating at the highest efficiency manner, provides multiple outputs for the downstream stages. These outputs result in significantly smaller filter volume and higher efficiency for the differentially connected buck (DB) converter stages.
3.3 Controllers

As described earlier, an advantage of MSC-DB compared to previous solutions, shown in Figs. 2.1 and 2.2, is that the control of the entire system is performed with a single centralized controller. This section describes control requirements for MSC-DB architecture, addresses output voltage regulation challenges, such as cross-regulation, and shows two control solutions for the same. Controllers based on digital voltage mode pulse-width modulation and mixed-signal current programmed mode (CPM) methods are presented. The two different implementations are shown to demonstrate that the introduced architecture can be implemented both for applications where the voltage mode control is preferable, due to the lower cost of implementation [17], and for the application where the CPM providing inherent current protection is almost exclusively used [24].

3.2.3 Digital voltage-mode pulse-width modulation controller

A block diagram of the voltage-mode pulse-width modulation controller is shown in Fig. 3.7. This controller architecture is similar to the well-known digital controller architectures discussed in numerous publications [25]-[29] and has been modified to extend it for three different output voltages. All three output voltages are referred to the same ground, and since the voltage levels are different, three different attenuators $H_{1-3}$ are utilized to provide appropriate voltage levels for a three-input analog-to-digital converter ($ADC_1$). In this case, an ADC with three separate conversion channels was utilized. Alternatively a single channel ADC can also be used with a
front-end analog multiplexer to time share the ADC [30] among the three output voltages. The digital equivalents of the PMA output voltages are then subtracted from their respective references and the corresponding errors, $e_i[n]$ are obtained. The PID compensator modules create control signals for a multi-input multi-output (MIMO) digital pulse-width modulator (DPWM), which provides the gating signals for the transistors of the downstream converter stages ($SW_{7-12}$). In this case the multi-input multi-output DPWM is a simplified version of the architecture described in [27]. This controller allows independent control of three different output voltages and, as shown in previous art [25]-[29], requires fairly simple hardware for implementation, much simpler than that of the conventional structures requiring multiple controllers.

The controller also provides signals to the front-end MSC circuit, such that fixed conversion ratios of a $2/3^{rd}$ and $1/3^{rd}$ are maintained across the intermediate capacitors, $C_{mid2}$ and $C_{mid1}$, respectively. Since the voltages across the intermediate nodes do not need to have a tight regulation, MSC stage operates in open loop with a 50% duty ratio, achieving peak efficiency [9].
Fig. 3.7 Digital voltage-mode controller implementation for output voltage regulations
3.3.2 Cross-regulation suppression

In conventional converter architectures, this voltage-mode controller is able to effectively compensate for load variation due to transients [17], [26], [27], and input voltage variation due to SOC of the battery, which is slow in nature [20]. However, in the MSC-DB architecture it cannot be used without modification. Any high frequency perturbation in the intermediate capacitors, i.e. outputs of the SC stage, would propagate to the output voltages. This is mainly because the voltage mode control is susceptible to high frequency input voltage perturbation [17], [24]. In the introduced architecture this drawback of the voltage mode control could potentially create undesired cross-coupling between the output voltages. It can be seen that this problem exists due to the stacked-up intermediate capacitor configuration of the front-end SC stage. Since the differential input buck stages are connected across the intermediate capacitors, load transients at the output of one of them, can create perturbation in the stacked capacitors, affecting the outputs of the other downstream stages.

To minimize this problem, the cross regulation suppression module of Fig. 3.8 is incorporated. Here, a feed-forward based approach [31], [32] is utilized, where ADC\textsubscript{2} is used to acquire information about the intermediate capacitor voltages. When there is a significant perturbation in the intermediate capacitors, due to load transients, the cross regulation suppression module adjusts the instantaneous duty ratio values, provided by the PID compensators, such that the cross regulation problem is minimized. The effectiveness of the cross regulation suppression module is shown in the experimental results section of this chapter.
Fig. 3.8 Digital controller implementation with cross regulation suppression module
3.3.3 Mixed-signal peak current programmed mode (CPM) control

Current programmed mode control (CPM) has better audio susceptibility [33] than the voltage mode systems and, thus, inherently provides a better suppression of intermediate voltage perturbation, without the need for an additional cross regulation suppression module and associated sensing of the intermediate voltages. For that reason, a mixed signal current programmed mode controller is also developed and implemented on a chip, as discussed in the integrated implementation of the introduced topology in Chapter 4. This, CPM control has additional advantages over voltage mode counterparts such as inherent over-current protection and on-line efficiency optimization [24].

A block diagram of MSC-DB with the developed mixed-signal CPM controller [24] is shown in Fig. 3.9. The controller has identical structure to the one shown in [24]. Digitally implemented voltage-loop compensators produce digital current references, $i_c[n]$, which are then passed through a digital-to-analog converter (DAC) and compared with outputs of senseFETs [24], to create triggering signals for SR latches. A SR latch and dead time generator block is then used to generate constant frequency pulse-width modulated gating signals for the switches.
Fig. 3.9 Mixed-signal CPM control implementation with integrated circuits
3.4 Cell Balancing and MSC Efficiency Improvements through Bi-Directional Energy Transfer

In a wide range of portable applications utilizing multiple battery cells - such as laptops, ultrabooks, tablet computers - cell balancing is a highly desirable feature. It extends battery runtime, as well as battery lifetime [34], by providing equal discharge of battery cells. However, such a feature is rarely implemented in the targeted applications, mainly due to the need for dedicated power converters [35], that could significantly increase the volume, price and weight of the portable devices.

In the introduced topology the cell balancing can easily be incorporated, by adding a single inductor, $L_{bat}$ and a simple control circuit, as shown in Fig. 3.10. Here, the balancing scheme based on maintaining the same voltage across battery cells is applied. Furthermore, the incorporated inductor improves power processing efficiency of the MSC stage, by improving balancing of the flying capacitor voltages under large differences in the output load conditions.

As discussed in the principle of operation section, the MSC stage is operated in the open loop, with phases $\Phi_1$ and $\Phi_2$ having equal durations over a switching period. As a result, during regular operation, the voltage across the right side of the cell balancing inductor of Fig. 3.10, $v_{xb}(t)$, i.e. its switching node, ideally switches between $2/3V_{batt}$ and $1/3V_{batt}$ with a 50 % phase duration. Therefore, in steady state, the resulting average voltage across the switching node and, consequently, across the left side of the inductor, i.e. the voltage across the bottom battery cell, will be $1/2V_{batt}$, where, again, $V_{batt}$ is the voltage of the 2-cell battery pack. This means that, ideally, during the normal operation of the MSC stage the battery cells are balanced.
However, due to mismatches in the battery cells, parasitic and losses in the system, 50% duty ratio might not result in an ideal balancing of the cells. To compensate these mismatches, an additional control loop is implemented around the switched capacitor circuit, as shown in Fig. 3.10. If a cell imbalance is observed, the duty ratio of switch capacitor phases is slightly varied from the regular 50%, without significantly affecting the intermediate capacitor voltages. This is possible as a tight regulation of the intermediate nodes is not required for proper system operation.

Fig. 3.10 Practical implementation of cell balancing and MSC efficiency improvement with $L_{bal}$
The controller for balancing is implemented as shown in Fig. 3.10. The $ADC_3$ provides information regarding the battery cell voltages (voltage of the battery pack and voltage of the bottom cell) and divide-by-2 block, which is essentially a 1-bit right shift operator, gives the average of the two battery cells voltages. This voltage is then compared with the $Cell_2$ voltage. The obtained error is then passed to the PI compensator, which creates control signal for the digital pulse width modulator (DPWM). Accordingly the DPWM adjusts the duration of the gating signal phases for $SW_{1,6}$ and provides battery cell balancing.

In addition to the cell balancing, the inductor $L_{bal}$ further improves power processing efficiency of the MSC stage under large differences in the output loads. For example, when the 1V output (Fig. 3.10) of the PMA provides much more power than the other two. The inductor provides a bi-directional energy transfer path between the battery cells and intermediate capacitors, through the operation of the flying capacitors. In the event of unbalanced loads, the intermediate capacitors, and hence the shuttling capacitors, might show charge imbalance resulting in voltages difference from the ideal $V_{batt}/3$ value and, therefore, a reduction in power processing efficiency [9]. In the presence of $L_{bal}$, this imbalance is minimized as the bidirectional energy transfer allows maintaining equal charge in the shuttling capacitors while balancing battery cells. Furthermore, in the absence of $L_{bal}$, the energy to the output of $buck_3$ is transferred to $C_{mid3}$ via $C_{s1}$ and $C_{s2}$, whereas $L_{bal}$ creates a direct path from the battery cell to $C_{mid3}$ through $C_{s2}$. This creates a lower resistance path for energy transfer between the battery cells and the bottom intermediate capacitor, $C_{mid3}$, further improving power processing efficiency of the front-end MSC stage.
It is important to note here that, this additional cell balancing inductor, $L_{bal}$ is quite small, due to three main reasons. First, it processes only differential power, which is a small portion of the overall converter power. Second, it’s switching node, $v_{xb}(t)$ has a relatively small voltage swing of only 50% of the battery voltage, $V_{batt}$. Third, unlike downstream buck converters providing output voltage regulation, $L_{bal}$ does not need to meet any specific ripple requirement, allowing its value to be further reduced.

### 3.5 Experimental Systems and Results

In order to practically verify proper functionality of the MSC-DB and its effectiveness to reduce the volume of bulky inductors and to increase efficiency, experimental prototypes were implemented and thoroughly tested. The power stage of the system shown in Fig. 3.10 was developed with discrete transistors, gate drivers, and passive components. The controller was implemented using an FPGA-based development board and off-shelf analog-to-digital converters. As shown in the figure, three stacked buck converters are connected differentially across the intermediate capacitor string. The MSC stage provides the intermediate node voltages of the capacitive string. For two 3.3 V Li-ion battery cells, these voltages are approximately 6.6V, 4.4V, and 2.2V. The MSC stage operates at a fixed switching frequency of 500 kHz while the downstream stages, providing 5V/ 3W, 3.3V/ 9W and 1V/ 3W, respectively, switch at 1 MHz. The cell balancing inductor, $L_{bal}$, provides equal discharge of both battery cells, while improving efficiency of the MSC stage.

As mentioned earlier, the compensator and the DPWM architectures are identical to those used in universal digital controller architecture, details of which are shown in [27].
Figs. 3.11 and 3.12 show comparisons of the inductor currents and switching node voltages of the conventional and MSC-based 2-input downstream buck stages when providing 3.3 V and 1 V at their outputs, respectively. As mentioned in Chapter 2, the conventional buck has a 5V input and the input of the differential buck is this case is 2.2V. For demonstration purposes the inductors of both configurations are selected to be the same. The results demonstrate lower switching node voltage swing, and consequently, about 50% lower inductor current ripple for the 3.3 V 2-input buck of the MSC-DB architecture (Fig. 3.11), allowing for the same percentage of inductor volume reduction, while maintaining the same current ripple. For the 1 V output, this reduction is about 30% as shown in Fig. 3.12.

Fig. 3.11 Inductor currents and switching node voltages of the conventional and MSC-DB 2-input downstream stage for 3.3 V output. Ch2: switching node, \( v_{x2} \) (5 V/div); Ch3: inductor current (250 mA/div)
Fig. 3.12 Inductor currents and switching node voltages of the conventional and MSC-DB 2-input downstream stage for 1 V output. Ch2: switching node, $v_{x3}$ (5 V/div); Ch3: inductor current (250 mA/div)

3.5.1 System efficiency

Fig. 3.13 shows measured efficiency comparison of the conventional and 2-input downstream buck converters providing 1 V output over a 250 mA to 3 A load variation. For the conventional case, the buck converter operates from a 5V bus voltage, whereas in the proposed topology it operates from the 2.2V intermediate capacitor voltage. The results confirm up to 53% reduction in total losses, improving the overall efficiency by 12% at lighter loads, where the switching losses are dominant, as well as a noticeable improvement throughout the entire operating range. For portable applications, this improvement is quite important and extends the battery life significantly, as portable devices spend a large portion of their on-time in sleep or idle mode [36].
Fig. 3.13 Efficiency comparisons of MSC-DB 2-input buck architecture and the conventional downstream converter.

Fig. 3.14 shows the measured efficiency of MSC front-stage alone and combined 2-stage MSC-DB for 1 V output. The MSC stage shows above 90% efficiency for 0.25 A to 3A output current. As shown in Fig. 3.14, a relatively flat efficiency curve of the MSC stage is the key for overall high system efficiency. Furthermore, having very high light load efficiency makes this solution attractive to portable applications, as it extends the battery life of the portable devices that spend a large portion of their on-time in sleep-mode [36].
The results from Figs. 3.11 to 3.14 confirm that the MSC-DB architecture results in large reductions of both the inductor volume and conversion losses and, therefore, has higher power density than the conventional solutions.

![Efficiency vs. Load Current](image)

Fig. 3.14 Measured efficiency of MSC front-stage alone and combined MSC-DB, from battery source to 1V output

### 3.5.2 Minimizing cross regulation between outputs

As discussed in the controller implementation section of this chapter, the stacked configuration of the intermediate capacitor network inherently imposes cross-regulation problem between different outputs when regulated by a voltage mode controller. This problem is demonstrated in Fig. 3.15, where load transients in any of the output stages negatively affects outputs of other
phases and results in sub-transient responses of their controllers. In Fig. 3.15, the actual load transients are marked with red circles, and sub-transients can be noticed in the other outputs during those times.

The digital controller with cross-regulation suppression module of Fig. 3.8, reduces the effects of the cross regulation by utilizing a feed-forward architecture. When the centralized controller detects a transient in one of the buck output voltages, it utilizes the feed-forward information to adjust the duty ratios of the other two buck stages, to minimize their sub-transients. The effectiveness of the cross regulation suppression control action during a light-to-heavy and heavy-to-light transients at 1V output are shown in Fig. 3.16 and 3.17, respectively. This solution reduces the voltage deviations of the other two phases by more than five times, limiting the sub-transient responses to 20 mV deviation.

![Fig. 3.15 Cross regulation between output voltages. Actual load steps are marked in red dotted circles (LS_1 to LS_3). Ch1: buck_3 output voltage, V_{out_3} (200 mV/div); Ch2: buck_2 output voltage, V_{out_2} (500 mV/div); Ch3: buck_1 output voltage, V_{out_1} (500 mV/div)](image-url)
Fig. 3.16 Significant suppression of cross regulation, during light-to-heavy load transient. Ch1: load step signal; Ch2: buck₁ output voltage, $V_{out1}$ (100 mV/div); Ch3: buck₂ output voltage, $V_{out2}$ (100 mV/div); Ch4: buck₃ output voltage, $V_{out3}$ (100 mV/div)

Fig. 3.17 Significant suppression of cross regulation, during heavy-to-light load transient. Ch1: load step signal; Ch2: buck₂ output voltage, $V_{out2}$ (100 mV/div); Ch3: buck₁ output voltage, $V_{out1}$ (100 mV/div); Ch4: buck₃ output voltage, $V_{out3}$ (100 mV/div)
3.5.3 Cell balancing using $L_{bal}$

Fig. 3.18 demonstrates how the battery-cell balancing, described in Section 3.4 is performing, while regulating the output voltages for the case when the top cell has a larger state-of-charge than the bottom one. To show the effect over a relatively short period, two 5F ultra capacitors, having much smaller capacity than conventional battery cells, are used. An initial large mismatch between the capacitors was created to demonstrate the effectiveness of the cell balancing feature. It can be seen that by slightly changing the SC duty ratio from its 50% nominal value, the initial imbalance between $V_{batt1}$ and $V_{batt2}$ is effectively eliminated. Fig. 3.18 also shows how the output voltage is perturbed during this operation. However, it is important to note here that, such a large mismatch ($\sim$1V) would not occur during the normal system operation and hence, the balancing would be performed without creating any disturbance at the outputs.

Fig. 3.18 Performing battery cell balancing while regulating the output voltage. Ch1: $buck_3$ output voltage, $V_{out 3}$ (200 mV/div); Ch2: bottom battery cell voltage (1 V/div); Ch3: top battery cell voltage (1 V/div); Ch4: current of the cell balancing inductor, $L_{bal}$ (1 A/div)
3.6 Summary

A novel high power density power management architecture (PMA) for battery-powered mobile applications combining multi-output switched capacitor (MSC) and differential buck (DB) buck is introduced. In comparison with the conventional PMA, the architecture that was named MSC-DB has drastically smaller (and lighter) output inductors, which, in the targeted applications, are the bulkiest parts of the power management systems and significant contributors to the overall device size and weight. Also, the new PMA has higher power processing efficiency and unlike conventional systems can be regulated with a single controller.

To achieve reduced inductor volume and improved efficiency, the front-end buck converter stage, existing in conventional systems, is replaced with an inductor-less MSC converter and the downstream stages are realized as 2-input DB converters. The MSC stage creates multiple voltage inputs for the downstream stages while operating with fixed conversion ratios, i.e. in open loop, at the peak power processing efficiency. The differential buck stages that are connected across the MSC taps provide tight output voltage regulation and, due to reduced voltage swings compared to conventional buck converters, have drastically reduced inductors and switching losses.

Furthermore, by adding a small inductor to the MSC-DB architecture, a battery cell balancing feature, not existing in conventional systems, is introduced allowing for significant extension of battery-operating time in mobile devices. This inductor also improves power processing efficiency of the MSC under unbalanced load conditions, by providing bidirectional energy transfer that improves voltage sharing across the flying capacitors.

Both voltage mode and current-programmed mode based controllers for the PMA are presented and a practical solution for suppressing cross-regulation issue, which is inherent in voltage mode
controlled stacked capacitor architecture, is presented. A practical implementation of the controller part for cell balancing feature is also incorporated.

The advantages of MSC-DB architecture are experimentally verified through both discrete and IC-based implementations. Experimental results obtained with the prototypes demonstrate that, compared to conventional buck downstream stages, the inductors of MSC-DB have up to 50% smaller inductors, and that the efficiency of the converters is improved by up to 12%, due to reduced switching losses. Both of these confirm drastic improvements in both power density and power processing efficiency.

### 3.7 References


Chapter 4

A CONFIGURABLE POWER MANAGEMENT IC FOR LOW-VOLUME DC-DC CONVERTERS

4.1 Introduction

In modern battery powered handheld portable applications, such as tablet computers, smartphones etc., power management systems provide multiple voltage levels using many
different dc-dc converters [1]. As already mentioned, one of the main challenges related to the implementation of the traditional power management module is their overall weight and size. In numerous portable devices they are by far the largest contributors to the overall size and weight [2], taking a significant portion of the overall volume [3]. Due to the strict limitation of available space, these modules are often implemented in integrated chip (IC) also known as power management ICs (PMICs), where the semiconductor switches, along with gate drivers, controller and sensing circuitries are packaged on the same silicon die. However, bulky reactive components, such as inductors and capacitors, often cannot be integrated in PMICs [4]-[5] and as a result, the overall volume of the existing power management solution is largely contributed by the output filter’s reactive components, where inductors are the most dominant [6].

The goal of this thesis is to introduce a compact and efficient power management solution for portable applications, reducing the volume of the output filters. In this solution, a Multi-Output Switched-Capacitor (MSC) stage provides an intermediate capacitor voltage divider, where the downstream stage converters, providing tightly regulated output voltages, are differentially connected. This arrangement allows for reducing the downstream stages’ inductors drastically, by reducing the voltage swings at switching nodes and furthermore improves their efficiencies significantly, by minimizing switching losses. As previously mentioned, these advantages potentially create opportunity for an increased level of on-chip integration of the power management modules compared to existing solutions.

In this chapter a practical integrated implementation of such power management solution is proposed (Fig. 4.1). The introduced PMIC-SCB (Power Management IC for Switched-Capacitor Buck) is highly configurable and can be utilized beyond the specific architectures, such as the
introduced MSC-DB. As shown in Fig 4.1, designed PMIC-SCB module consists of two separate power stages, which can be controlled independently with switching frequency up to 10 MHz. As a result of this very generic design approach of PMIC-SCB module, it can be utilized in a wide range of converters, including H-bridge based architectures. These include hybrid multilevel converter [7], multilevel voltage source inverter [8], modular multilevel converter for HVDC transmission [9], and differential power converter for photovoltaic [10] and server applications [11]. Depending on the application’s voltage and current specification, the introduced PMIC can be configured accordingly; allowing significantly smaller volume for implementation compared to conventional power management solutions. Furthermore, in numerous applications, such as battery powered portable applications, accurate current sensing or measurement in dc-dc converters is not only required for protection from overload conditions [12], but also often utilized for increasing converter efficiency through multi-mode operation [13], [14] and improving dynamic response [15]. As a result, a complete mixed-signal CPM [5] compatibility is also incorporated in the introduced PMIC, which consist of an on-chip DAC, programmable slope compensator, and senseFET based current sensing.

Fig. 4.1 System level diagram of the introduced power management module
4.2 Principle of Operation

The primary focus of the chapter is on the PMIC module and how it can be configured to implement the low volume power management architecture introduced in this thesis. However, as it will be shown in Chapter 5, the integrated power management module can also be utilized in a wide range of other applications. The custom designed PMIC-SCB implements a combined switched-capacitor (SC) and inductor based topology. Each of the two separate power stages in PMIC-SCB (Fig. 4.1) implements the power stage for switched-capacitor and differentially connected buck converter, respectively. SC converters have high power density, as they don’t need bulky inductors, but only demonstrate high efficiency at fixed conversion ratios. This makes them unsuitable for battery powered applications, where battery voltage is varied depending on the state-of-charge (SoC) [16]. However, as shown in Chapter 3, by combining them with inductor based topology brings certain advantages compared to conventional power management solutions. In such a topology, the SC power stage provides a fixed ratio voltage division across an off-chip capacitor network such that, the inductor-based power stage only works with a portion of the input voltage. This reduces voltage swings at the switching node and hence, a smaller inductor and reduced switching losses are achieved. The PMIC presented in this thesis can be configured in series or parallel manner, depending on the application requirement, and hence can be utilized in a wide range of applications.

4.2.1 Stacked-up/series configuration

Depending on the application, the input voltage of handheld portable electronics devices can be provided by a single Li-ion battery cell (i.e. smart phones) or by multiple cells (i.e. tablet
computers). In order to address this wide range of battery configuration variation, the introduced power management module is designed such that they can be stacked up together depending on application requirements. This allows not only withstanding higher input voltage rating, but also divides the input voltage in multiple voltage levels to be utilized by inductor based stages. For example Fig. 4.2 shows how two ICs can be stacked-up together, to create a switched capacitor stage providing half the input voltage across each of the downstream inductor stage. Similarly as shown in Fig. 4.3, three ICs can be stacked together for the SC stage to provide 1/3rd and 2/3rd of the input voltage across downstream stages. This topology then, becomes the architecture introduced in this thesis.

![Fig. 4.2 Two chips stacked-up configuration](image-url)
Fig. 4.3 Three chips stacked-up configuration
4.2.2 Parallel interleaved configuration

Where the motivation of stacked up configuration discussed above, is to support higher battery voltage ratings and to create more voltage levels in the capacitor network, the introduced power management module can also be configured in parallel manner to provide high current/power levels. Such a configuration is shown in Fig. 4.4, where each of the 2 stacked-up modules has 2 parallel modules, with the ability to deliver twice as much current to the load. This also allows the inductor based stages to be operated in interleaved manner [17]. Furthermore, parallel configuration of the introduced power management ICs can also provide multiple output voltages.

Fig. 4.4 Four chips parallel interleaved configuration
4.3 Practical Implementation

In addition to two separate power stages and their associated gate drivers, the introduced power management IC also integrates a Digital-to-Analog Converter (DAC), slope compensator and a senseFET based current measurement circuit for complete mixed signal CPM [5] compatibility (Fig. 4.1). Design details of each of these building blocks are briefly explained in the following subsections.

4.3.1 Segmented Power Stages

There are two separate, independently controlled, power stages implemented inside PMIC-SCB. Although the power stages have identical design, the one for the downstream buck, includes additional circuitry for current sensing, allowing CPM controllability (Fig. 4.1), as explained in the next subsection. Each power stage consists of a high side PMOS and a low side NMOS switches, divided into eight segments. The segmented power stage allows the trade-off between gate charge and on-resistance of the switches to dynamically optimize efficiency [5], depending on the operating conditions. Along with the power stage, the gate drivers are also implemented inside the chip. As shown in Fig. 4.5, the associated gate drivers are also segmented to have a uniform turn on/off time, regardless of the number of active segments. In addition, a programmable dead-time generator block, creating non-overlapping gating signals for PMOS and NMOS switches, is also implemented (Fig. 4.1).
4.3.2 SenseFET for current sensing

A senseFET based current sensing circuit [18] is implemented to acquire the information about high side switch current, $i_{sw}(t)$ (Fig. 4.6). When the high side switch turns on, the senseFET copies a small portion ($I/K$ when all segments are on) of the current, $i_{sense}(t)$ and passes it through the sense resistor $R_{sense}$. The voltage across this resistor, $v_{sense}$, thus contains the high side current information given by:

$$v_{sense}(t) = \frac{i_{sw}(t)}{K} \cdot R_{sense} \quad (4.1)$$
As the operating condition of the buck stage changes from higher to lower load current levels, smaller number of power stage segments become active, dynamically changing $K$ ratio. This allows copying a larger portion of the high side switch current during light load condition, limiting the range of voltage across $R_{\text{sense}}$ and thus improving the current sensor linearity [5].

![Diagram of SenseFET based high-side current sensing for PMIC-SCB modules](image)

**Fig. 4.6 SenseFET based high-side current sensing for PMIC-SCB modules**

### 4.3.3 Digital-to-analog converter

An 8-bit charge redistribution DAC, similar to the one shown in [19], is implemented. To reduce the total area for implementation, a series capacitor is added ($C_a = C$ in Fig. 4.7), allowing significant reduction of subsequent capacitors and thus, reducing total required area by 8 times. Although all the switches are sized proportional to the corresponding capacitor values, to achieve uniform settling time during charging/discharging phase, one of the practical challenges for such
DAC architecture is the monotonicity. However, in mixed-signal CPM control [5], since an output voltage feedback is utilized, it compensates for any non-monotonic offset in the DAC.

In addition, since the charge redistribution DAC operates with a charging and discharging phase and the system must comply with targeted high switching frequency operation, two identical DACs are designed with an analog MUX, allowing interleaved operation as shown in Fig. 4.8. This allows the output of the DAC to be always ready during the switching period, regardless of the charging phase of the individual DAC modules.
4.3.4 Slope Compensator

Finally a programmable slope compensator is also implemented in PMIC-SCB, since the CPM control is inherently unstable for duty ratio higher than 50% [20]. In the introduced topology the differentially connected downstream buck converters operate close to 50% duty ratio, and hence, slope compensation is necessary to provide a stable current loop. The charge redistribution DAC implementation allows easy incorporation of slope compensation. Four binary weighted current sinks (Fig. 4.9), utilizing equivalent output capacitor of the DAC, creates the necessary ramp at
the DAC output. This allows programmable slope compensation, depending on the operating condition of the converter.

![Diagram](image)

Fig. 4.9 Implementation of binary weighted programmable slope compensator

### 4.3.5 Capacitive coupling and Manchester encoding

As discussed in the principle of operation section of this chapter, the implementation of the introduced power management architecture requires the designed IC to be placed in stacked-up series configuration, resulting in different ground references among them. In order to send control signals from an off-chip controller module, additional level shifters are required. A simple low-cost, yet practical, solution is presented here in order to address this issue. As Fig. 4.10 shows, capacitive coupling based level shifting is utilized in this implementation, which has low component count and very simple design. However, the drawback of capacitive coupling is the variation of the common mode value being dependent on the pulse width of the input signal. In order to solve the problem, a Manchester encoding [21] technique is utilized, which solves this
problem by transmitting the signal and the clock through a 2-input XOR gate. This allows the
signal to have fixed common node voltage regardless of the input signal by creating a time
varying input signal at the clock frequency. In order to recover the data from the output, the IC
only needs to perform another XOR function, as shown in the waveforms of Fig. 4.10.

Fig. 4.10 Capacitive coupling and manchester encoding to transfer data between off-chip
controller module and on-chip sensing and controller circuitry
4.4 Experimental System and Results

The introduced PMIC solution, shown in Fig. 4.1, is fabricated in a standard 0.13µm CMOS technology. The chip micrograph is shown in Fig. 4.11 and Table III summarizes its main specifications. A digital controller is implemented on FPGA to verify the proper functionality of the PMIC. Figs.4.13-4.20 show experimental waveforms for a 2-chip stacked-up power management architecture, as shown in Fig. 4.12, where the switched-capacitor power stages are operating at 580 KHz and buck power stages at 9.3 MHz switching frequencies.

Table III: PMIC-SCB implementation specifications

<table>
<thead>
<tr>
<th>Specifications</th>
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<td>Total Area</td>
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<td>mm²</td>
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<td>SC Switching Freq.</td>
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<td>KHz</td>
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<td>Buck Switching Freq.</td>
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<td>MHz</td>
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<td>$V_{in}$</td>
<td>3</td>
<td>V</td>
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<tr>
<td>$V_{out1}, V_{out2}$</td>
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<td>V</td>
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<td>Buck L,C</td>
<td>100, 10</td>
<td>nH, µF</td>
</tr>
<tr>
<td>$R_{on}$ PMOS, NMOS</td>
<td>150, 125</td>
<td>mΩ</td>
</tr>
</tbody>
</table>
Fig. 4.11 Fabricated IC (PMIC-SCB) micrograph
Fig. 4.12 Experimental test bench schematic for the integrated implementation, utilizing two custom made PMIC-SCB in stacked-up configuration

Fig. 4.13 shows the operation of the MSC stage, consisting of two PMIC-SCBs providing half the input voltage at the intermediate node, $V_{mid}$. As the input voltage, $V_{in}$ is selected to be 3V in this case, $V_{mid}$ shows 1.5V steady output. Furthermore, voltage swings at the switching nodes for the bottom and top PMICs are 0 V to 1.5 V and 1.5 V to 3 V, respectively.
Fig. 4.13 Steady state operation of the MSC stage at 580 KHz. Ch1: switching node of top PMIC SC stage (2 V/div), Ch2: switching node of bottom PMIC SC stage (2 V/div), Ch3: input voltage (1V/div), Ch4: intermediate voltage (1V/div)

Fig. 4.14 shows steady state operation of the MSC stage and both downstream 2-input buck stages (Fig. 4.12). MSC stage operates with 580KHz switching frequency and buck stages operate at 9.3MHz. Both PMIC-SCBs operate with 1.5V voltage swing at the switching nodes, half of the input voltage $V_{in}$. As shown in this figure, although the power stage for MSC stage and 2-input buck stage operate with 2 different frequencies, both power stages for the top PMIC switches between 3V and 1.5V for and the bottom PMIC switches between 1.5V and 0V.
Fig. 4.14 Steady state operation of both MSC and 2-input buck stages; Ch1: SC switching node (top chip), $V_{x, sc2}$ (2 V/div); Ch2: Buck switching node (bottom chip), $V_{x, buck1}$ (1 V/div); Ch3: SC switching node (bottom chip), $V_{x, sc1}$ (2 V/div); Ch4: Buck switching node (top chip), $V_{x, buck2}$ (1 V/div)

Fig. 4.15 shows steady state operation of the MSC stage and the bottom downstream buck converter, providing output, $V_{out1}$, while operating from intermediate voltage $V_{mid}$ (Fig. 4.12). Inductor current of the bottom downstream buck converter, $i_{L1}$ is also shown, which is measured using current probe. MSC stage operates with 580KHz switching frequency and buck converter operates at 9.3 MHz with 1.5V voltage swing at the switching mode, $V_{x1}$. As shown in this
figure, a very small inductor of 100nH results in less than 100mA ripple current, due to the reduced voltage swing of 1.5V.

Fig. 4.15 Steady state operation of the MSC stage at 580 KHz and bottom buck stage at 9.3 MHz. Ch1: switching node of top PMIC SC stage (2 V/div), Ch2: switching node of bottom PMIC buck stage (1 V/div), Ch3: switching node of top PMIC SC stage (2 V/div), Ch4: inductor current of the bottom buck stage (100 mA/div)

Fig. 4.16 shows inductor current and switching node waveforms for both 2-input converters operating in steady state. Due to reduced voltage swings of 1.5V in both of these converters, only 100nH of small inductors are required to achieve less than 100mA of current ripples.
Fig. 4.16 Steady state operation showing both switching nodes and current waveforms for 2-input downstream converters; Ch1: Inductor current (top chip), $i_{L2}$ (100 mA/div); Ch2: Buck switching node (bottom chip), $V_{x_{buck1}}$ (1 V/div); Ch3: Inductor current (bottom chip), $i_{L1}$ (100 mA/div); Ch4: Buck switching node (top chip), $V_{x_{buck2}}$ (1 V/div)

Fig. 4.17 shows linearity test result of the designed DAC, implemented on PMIC-SCB. The red straight-line connecting all the test points shows satisfactory linearity of the designed DAC.
Fig. 4.17 DAC linearity test result

Figs. 4.18 and 19 show DAC output with two different slope compensation levels. Compared to Fig. 4.18, Fig. 4.19 shows a steeper slope at the DAC output due to higher level of slope compensation applied. These results show proper functionality of the programmable slope compensator, implemented on PMIC-SCB.
Fig. 4.18 DAC output with low slope compensation; Ch4: DAC output (350 mV/div)

Fig. 4.19 DAC output with high slope compensation; Ch4: DAC output (350 mV/div)
Finally, Fig. 4.20 shows experimental results for closed loop mixed signal CPM controller, where to allow flexibility in prototyping the digital parts of the controller, i.e. compensator and error generator are implemented on FPGA. As shown in [22] hardware-efficient implementation of those blocks has become straightforward and is quite feasible. The senseFET output resembles the inductor current during high side switch conduction. The DAC output with adequate slope compensation shows a stable steady state operation for duty ratio higher than 50%. As shown by the switching node, $V_{x,\text{buck1}}$ waveform in Fig. 4.20, when the senseFET output reaches DAC output, the SR latch (Fig. 4.1) resets properly.

Fig. 4.20 Closed-loop CPM controller waveforms; Ch1: Inductor current, $i_{L1}$ (50 mA/div); Ch2: switching node, $V_x$ (1 V/div); Ch3: DAC output with slope compensator (500 mV/div); Ch4: senseFET output (500 mV/div)
4.5 Co-packaging with Power Inductors

As previously mentioned MSC-DB architecture allows potential integration of power management ICs (PMICs) with on-chip inductors. Recent advance in on-chip inductors for power electronics has resulted in the inductors that can handle sufficient amounts of current needed for the targeted applications [23]. However, the achievable maximum inductance values and efficiency-related limitations when operating at switching frequencies beyond 10 MHz still prevent their wider use in the conventional power management architectures [23]. The PMA architecture introduced here reduces the inductance value requirement without the need for significant increase in switching frequency, potentially allowing full on-chip integration of the inductors with the other PMA modules. To demonstrate this possibility, PMIC-SCB modules were co-packaged with on-chip power inductors [23]. Two different packaging options were realized as shown in Fig. 4.21 and 4.23. They show 1-IC with 1 inductor and 2 ICs with 2 inductors packaging options, respectively, while Fig. 4.22 and 4.24 show zoomed-in versions of these packages, indentifying PMICs and inductors. These packages demonstrate that MSC-DB effectively increases level of on-chip implementation capability, creating a possibility for full on-chip integration in near future.
Fig. 4.21 IC layout of PMIC-SCB

Fig. 4.22 IC layout of PMIC-SCB
Chapter 4: A Configurable Power Management IC for Low-Volume Dc-Dc Converters

Fig. 4.23 IC layout of PMIC-SCB

Fig. 4.24 IC layout of PMIC-SCB
4.6 Summary

The power management IC introduced in this chapter combines switched-capacitor and inductor based dc-dc converters to drastically reduce inductor requirement, which is often the bulkiest component of existing power management solutions. This IC is targeted for portable applications where low volume implementation is the main priority. The introduced PMIC module is highly configurable for different voltage and power levels and hence, can easily be adopted in numerous applications. Apart from allowing a very small volume for implementation, it also allows for decreasing switching losses of the system. The integrated solution features mixed signal current program mode compatibility, allowing inherent protection, dynamic efficiency optimization and simpler control with superior dynamic response [5]. Experimental results obtained with prototype ICs show operation at 9.3 MHz allowing for a drastic reduction of the inductance values.
4.7 References


Chapter 5

IC Module for Distributed Power Supplies

5.1 Introduction

Distributed power supplies, also known as granular power supplies, are commonly used in high power applications such as multi-level converters [1], due to their attractive features such as modular design and scalability based on power processing requirement. In more recent
publications [2], [4], [5] distributed power supplies have also been proposed for a wide range of low to medium (up to several hundred watts) power management applications starting from harvesting energy from dc sources, i.e. photovoltaic (PV), battery, fuel cell stack etc [2], [3], to delivering power to series connected loads, i.e. server computers, stacked battery cells etc [4],

Fig. 5.1 Distributed energy harvesting using granular power supplies
In order to harvest energy from series connected dc sources, i.e. PV, battery or fuel cells stack, granular power supply based approach (Fig. 5.1), is commonly chosen as these low voltage cells do not interface well with higher power systems [2]. These power supplies, while connected across the energy cells, operate at low dc voltage, ranging from less than 1V (PV cell) to 3.3 V (Li-ion) cells, and provide dc-dc or dc-ac conversion using multi-level inverter topologies [2]. Each granular power supply can independently control and optimize the power flow to or from its source. For a PV string, this allows performing independent maximum power point tracking (MPPT) from individual panels [6]. In addition to energy harvesting applications, granular power supplies have also been proposed for power delivery in series connected computer servers [7] and for charging of stacked battery cells [8].

In these applications [4]-[7], a distributed power supply is commonly implemented using discrete components on multiple printed circuit boards, along with sensing and controller circuits (Fig. 5.2). In order to provide communication with a centralized controller, additional opto-coupler and/or transformer providing galvanic isolation is required. Although in high power application these additional components with associated cost are often acceptable, in low to medium power application the additional cost and complexity often prevents a wider adoption of distributed power supply architectures. Furthermore, in low power applications, the discrete implementation imposes limits on the maximum achievable switching frequency, due to parasitics, negatively influencing overall size of the converter. On the other hand, integrated chip (IC) solution in such applications can result in simpler implementation due to smaller footprint, higher speed, lower component count, and higher switching frequency operation. However, an IC implementation of granular power management architecture has several practical implementation challenges including stacked up configuration of ICs, controller complexity, communication between ICs.
These issues prevent a straightforward transfer of the PCB based architectures developed for high power to the IC level and their use in low to medium power applications.

The main goal of this chapter is to demonstrate how the introduced PMIC module, discussed in Chapter 4, can practically solve the existing implementation challenges and enable adoption of distributed architectures in low to medium power applications. As already shown in Chapter 4, the IC features a novel practical low cost interface for communication with off-chip controller modules, a segmented power stages, along with complete 10 MHz mixed-signal current-programmed mode [9] controller, providing inherent current protection, simpler control, and online efficiency optimization.

Fig. 5.2 Conventional implementation of granular power supplies on PCB
5.2 System Description and Principle of Operation

The system level diagram of the introduced IC targeted for wide range of applications was shown in Chapter 4 and is repeated here in Fig. 5.3. It consists of two separate power stages along with gate drivers and additional sensing circuitry for mixed signal CPM compatibility. The two power stages have separate input voltages \( v_{dd1}, v_{dd2} \) and reference grounds \( v_{ss1}, v_{ss2} \) and can be controlled independently with different switching frequencies. This very generic design approach is the key for high adoptability in numerous applications, as shown in the following subsections.

![Integrated Chip Diagram](image)

Fig. 5.3 Custom designed IC for the targeted applications
5.2.1 Multilevel inverter in PV applications

The simplified diagram of Fig. 5.4, showing only the power stages of the designed IC, demonstrates how the introduced IC module can be utilized in multilevel inverter applications, providing dc-ac conversion for grid-connected photovoltaic systems. This converter architecture allows output voltage synthesis with a large number of levels, which is an important feature of the multilevel converters [1]. In addition, the granular power supply based approach to implement the multilevel architecture, allows MPPT on individual PV cells, optimizing global efficiency for the energy harvesting system.

Fig. 5.4 Multilevel inverter in PV applications
5.2.2 Differential Power Processing Architectures

Fig. 5.5 shows how the introduced IC can be utilized in differential power processing (DPP) architectures [7]. In these applications the two power stages of the IC are connected between different nodes of the series connected capacitor network. This power management architecture allows independent regulation of the capacitor network node voltages while dealing with the difference of power in subsequent stages.
5.2.3 Isolated Dual-Active-Bridge (DAB) Topologies

Fig. 5.6 shows how the introduced IC can also be utilized in isolated converter topologies, such as DAB, implementing bi-directional power supply. For point-of-load (PoL) server applications, this architecture allows bi-directional energy transfer between series-connected server nodes and a virtual bus, while each granular power supply dealing with differential power processing [10]. Moreover, the introduced IC is suitable for implementing dual active bridge converter to be used in low-voltage charger application in a military uninterrupted power supply (UPS) systems, as shown in [5].

Fig. 5.6 Isolated DAB architecture for series-connected load applications
5.3 Simulation Results

In order to verify the proper functionality of the introduced power management module in a wide range of distributed power supply applications, detailed cadence simulations are performed and results are presented in this section.

Fig. 5.7 shows Cadence simulation results for the designed IC for multilevel ac-dc inverter application, as shown in Fig. 5.4. Four ICs are configured across 2.5V DC sources, modeling PV panels, to perform these simulations. Peak-to-peak output voltage of 20V consists of 9 different voltage levels, constructed by 4 ICs (8 power stages). Switching nodes of these power stages demonstrates 2.5V swings, verifying proper operation of the designed IC in the targeted multilevel inverter application.

Fig. 5.7 Cadence simulation results for multilevel inverter consisting of 4 ICs providing 9 level AC output voltages
Fig. 5.8 shows Cadence simulation results for the designed IC for differential power processing for series connected loads, as shown in Fig. 5.5. In this case 2 power stages of the same IC are connected across 3 series connected loads of consuming 2.5A, 2A and 1.5A respectively, from a 3V bus. In order to provide fixed 1V output across each of the loads, one differential converter operates with 1A of current, while the other one shown 0A differential current. The switching nodes for both of these converters operate with 2V swings, verifying proper operation of the designed IC in the targeted DPP application.

Fig. 5.8 Cadence simulation results for DPP converters consisting of 2 ICs providing 3 loads with 1V regulated outputs from 3V bus voltage
Fig. 5.9 shows simulation results for the designed IC for isolated dual-active-bridge (DAB) topology for series connected loads, as shown in Fig. 5.6. In this case 4 ICs are connected across 2 series connected loads from a 3V bus. As shown in this figure, in the case of unbalanced loads the bi-directional dual-active-bridges provide balanced 1.5V load voltages across each of the loads. This is accomplished by providing bi-directional energy transfer between the loads and a virtual bus, demonstrating proper operation of the IC in such applications.

Fig. 5.9 Cadence simulation results for isolated dual-active-bridge (DAB) topology consisting of 4 ICs providing 2 loads with 1.5V regulated outputs from 3V bus voltage
5.4 Summary

A practical integrated solution enabling distributed/granular power management in low to medium power levels is presented. The custom designed and fabricated IC solves the major implementation challenges in these applications, namely cost and speed related problems as well as communication challenges, providing a low cost practical interface for off-chip controller modules, to support a wide range of applications. In these applications, in addition to achieving smaller footprint and better thermal management, the introduced IC can also optimize overall system efficiency. Simulation results show proper operation of the introduced IC module.

5.5 References:


Chapter 6

Conclusions and Future Work

This thesis introduces a novel power management architecture and its integrated implementation, targeted for battery powered portable applications, where achieving low volume and high efficiency are the key priorities. The presented topology combines a fixed ratio multi-output switched capacitor converter stage with differential-input buck converters to achieve low volume and high power processing efficiency. The front-end switched capacitor stage provides high power density and high efficiency while the downstream two-input buck converters provide tight output voltage regulation. Introduced low volume implementation allows drastic reduction of
output filter volumes without the need for increasing switching frequency, hence limiting switching losses and improving the efficiency of the system. The implemented power management IC (PMIC) is highly configurable to support a wide range of input, output voltage and current levels, which can be adjusted based on specific application requirement. The PMIC also features mixed signal current program mode compatibility, allowing inherent protection, dynamic efficiency optimization and simpler control with superior dynamic regulation. The custom PMIC is fabricated in a standard 0.13µm CMOS process and results are obtained through operation at 9.3 MHz switching frequency, allowing for the use of very small filter components. Experimental comparisons with a two-cell battery input conventional 5V bus architecture, providing 15W of total power in three different voltage outputs, demonstrate up to 50% reduction in the inductances of the downstream converter stages and up to 53% reduction in losses, equivalent to the improvement of the power processing efficiency of 12%.

6.1 Thesis Contributions

The most significant contributions of this dissertation are provided in the following subsections.

6.1.1 Low-volume power management architecture

The presented topology is targeted for battery powered portable applications; where PMAs are of major concern due to their size and efficiency. Moving forward as more and more portable devices are going to be produced with power hungry features, such as larger screen, faster processing speed, power management units need to cope up with the ever increasing demand for
low volume and high efficiency. The introduced topology, combining a switched capacitor converter stage with two-input buck converters, achieves significant improvement compared to conventional solutions, both in terms of size and efficiency. The front-end switched capacitor stage provides high power density and high efficiency while the downstream two-input buck converters provide tight output voltage regulation. This configuration allows drastic reduction of output filter volumes without the need for increasing switching frequency, hence does not result in additional switching losses, limiting system efficiency.

### 6.1.2 Power management IC for combined SC and inductor based topology

In order to fully realize the advantages of the introduced topology and to practically demonstrate its feasibility in the targeted portable applications, a custom power management IC (PMIC) is designed and fabricated. The design of the PMIC is accomplished in a highly configurable fashion and thus, it can support a wide range of input, output voltage and current levels, based on specific application requirements. The PMIC also features mixed signal current program mode compatibility, allowing inherent protection, dynamic efficiency optimization and simpler control with superior transient response.

Furthermore, in order to demonstrate the effectiveness of the introduced PMIC as a solution to practically implement on-chip inductors, co-packaging of the PMIC with on-chip inductors is presented. This shows how the novel topology can not only reduce the size of the bulky inductors, but also creates the possibility to combine them in the same package. The thesis is ultimately aimed to create an increased level of on-chip integration of power management units, reducing their sizes and costs.
6.1.3 Distributed power supply applications

The novel integrated power management IC enables implementation of distributed power supply architectures in low to medium power applications, where such solutions are traditionally avoided due to several practical challenges related to speed, protection, and synchronization between modules. The custom designed IC in 0.13 µm process solves the major implementation challenges in these applications, as well as communication challenges, providing a low cost practical interface for off-chip controller modules, to support a wide range of applications. In these applications, in addition to achieving smaller footprint and better thermal management, the introduced IC can also optimize overall system efficiency. Simulation results show proper operation of the introduced IC module in these applications.

6.2 Future Work

This thesis clearly demonstrates the advantages of combining inductor and switched-capacitor based topologies to achieve superior performance (i.e. efficiency) and figure-of-merits (FoM) (i.e. energy density) compared to conventional topologies. As both of these topologies have their own limitation and advantages, significant improvement in terms of size and efficiency can be achieved by developing such hybrid topologies, bringing the bests of both worlds. As a result future work can be focused on additional topology design and implementation, with the goal of achieving performance and FoM beyond the physical limitation of conventional topologies, such as buck converter.
Future work could also include development of fully integrated power management modules, implementing inductors and capacitors on the same die as PMICs. Since the introduced power management module allows significantly smaller filter components, it creates the possibility to implement on-chip inductors. Such technology for on-chip inductors from Tyndall is compatible with standard CMOS process [1], allowing implementation of the introduced PMIC on the same die. Hence, the technology for complete integration of both inductors and PMICs is already present. Furthermore, recent progress in both academia and industry shows a significant improvement in capacitance density is achievable through trench technology [2]. This means the introduced topology can result in fully integrated power management modules for portable applications. Compared to the existing solutions, including co-packaging PMIC with inductors, this would result in smaller volume, reduced cost and improved efficiency and reliability.

6.3 References


Appendix A

An On-Chip Integrated Auto-Tuned Hybrid Current-Sensor for High-Frequency Low-Power Dc-Dc Converters

A.1 Introduction

In widely used dc-dc converters for battery powered portable applications, improving accuracy of current measurement circuits while reducing their power consumption can bring numerous
benefits. Improvements are not only important for over current protection [1], but will also enable utilization of advanced control method relying on the accurate measurement of instantaneous inductor current. Some of examples include on-line efficiency optimization methods [2], [3] and those for obtaining fast dynamic response [4]. Improvements in the performances of current sensors can also result in a wider adoption of current programmed mode control (CPM) in the targeted applications operating at switching frequencies exceeding 1 MHz, where, due to stringent power requirements, voltage mode controllers are still predominantly used.

In the targeted dc-dc converters, obtaining accurate current information has proven to be challenging [5]. The methods, where a current passing through a sense-resistor or a MOSFET is extracted from the voltage drop [6]-[9], are either avoided, due to extra losses across the resistor, or have a poor accuracy, due to the variations of the transistor on-resistance. SenseFET based approach [6], [10]-[12] provides a high accuracy of up to 4% [10]. However it requires a power hungry high gain bandwidth amplifier, due to the discontinuous current of the senseFET.

On the other hand observer based systems, such as those based on a time-constant matching RC filter across the power stage inductor [6], [13]-[14], estimate current without adding significant losses. However, a mismatch in time constants results in poor accuracy and dynamic regulation [14]. The mismatch is caused by large variations of the inductor time constant, i.e. inductance, $L$ and its parasitic resistance, $R_L$. Furthermore, even when the constants are matched a wrong estimation of the dc value of the current occurs if $R_L$ is not known. In [14] a calibration technique is proposed for RC filter time constant matching. That technique is intended for improving dynamic regulation, and does not address the dc mismatch problem.
An accurate calibration technique that combines two voltage drop methods, by utilizing an auxiliary switch and a sense resistor [15], requires 2 ADCs and is targeted for lower frequency and not so cost sensitive applications.

The main goal of this appendix is to introduce a novel on-chip implemented current sensor of Fig. A.1. The hybrid sensor combines senseFET and RC based techniques to enable accurate current measurements in converters operating at frequencies beyond 1 MHz while maintaining low power consumption. The sensor also utilizes two sample and hold circuits and a novel 2-point high under sampling rate based self-tuning technique to eliminate the need for costly ADCs and allows practical cost-effective implementation. The senseFET of Fig. A.1 is utilized to calibrate the RC filter based current measurement circuit, which then is able to provide accurate current information. As explained in this appendix, the senseFET is only operated when the calibration is needed and thus significantly reduces the power consumption of the overall sensing circuit.

The following section explains the principle of operation of the introduced auto-tuning technique for hybrid current sensor. Practical implementation is discussed in Section A.3, and Section A.4 presents experimental results verifying proper system operation.
A.2 Principle of Operation

The hybrid sensor of Fig. A.1 has two different current sensing circuits incorporated to combine the accuracy of senseFET and practically lossless nature of RC filter. The senseFET, which is frequently used sensing solution in on-chip implemented converters [5], [16], utilizes a high gain-bandwidth operational amplifier to copy a portion \( (1/K) \) of the primary switch, \( SW_1 \) current (Fig. A.1). This current is then passed through a sense resistor, \( R_{sense} \) and hence, the voltage across the resistor, \( v_{sense}(t) \) contains the information of the main switch current, \( i_{sw1}(t) \), and the ratio of the two values, i.e. the gain, is given by:
By changing the value of $R_{sense}$, the gain of the senseFET can be changed.

On the other hand, for observer based current measurement technique, a RC filter is placed across the inductor, $L$ and its series parasitic resistor, $R_L$ (Fig. A.1). The voltage across the filter capacitor $C_f$, $v_f(t)$ contains the information of the inductor current, given by the following equation:

$$v_f(s) = i_L(s) \cdot \frac{1}{R_L} \cdot \frac{s \cdot \tau_L}{1 + s \cdot \tau_f},$$

(A.2)

where $i_L$ is the inductor current, $\tau_L = L/R_L$ the inductor time constant, and $\tau_f = C_f R_f$ the time constant of the filter. By observing this equation it can be noticed that the dc components of the inductor current and the filter output, $I_L$ and $V_f$, do not depend on the time constant matching but only on the value of $R_L$, i.e. $V_f = R_L I_L$. On the other side, for a properly designed converter and roughly adjusted filter (with an order of magnitude) the relation between the components at the switching frequency and its multiples can be approximated with the following equation:

$$v_f(s) \approx i_L(s) R_L \frac{\tau_L}{\tau_f},$$

(A.3)

Since, at those frequencies, $||s \tau_L||>>1$ and $||s \tau_f||>>1$. The equation also indicates that, in a roughly adjusted filter the delay or the phase shift between the components at the switching frequency and higher is virtually negligible.
Appendix A

Equations (A.2) and (A.3) and previous analysis show that, under the given constrains, in RC filter based methods, only $R_L$ affects the measurement of the dc component of the inductor current, while both $R_L$ and the ratio of the time constants affect the measurement of its ripple component. For the same inductor current, these effects are demonstrated in Figs. A.2 and A.3, showing how the variations of $R_L$ and in the ratios of time constants change the output of the RC filter, respectively.

Fig. A.2 Effect of $R_L$ variations in steady state, due to temperature tolerances, aging and component variation
Fig. A.3 Effect of time constant mismatch in steady state

In the hybrid sensor introduced here, the accurate measurement of the inductor current at high frequencies is achieved through a two-step auto-tuning process, where in the first step the value of $R_L$ is determined and accurate measurements of the dc component of the inductor ensured. Then, in the second step a high accuracy of the ripple component is provided.

The two calibration steps are performed with senseFET, which is only operated once every thousands of switching cycle (at a high under sampling rate) and hence does not need continuous operation of the power hungry high gain-bandwidth amplifier. The details of both steps are described in the following subsections, with the help of diagrams of Fig A.4.
A.2.1 DC matching

The dc component of the sensed voltage across the filter capacitor, $C_f$, contains the information of the average inductor current. Mismatches in dc, due to variation of $R_L$, will result in wrong representation of average inductor current, as shown in Fig. A.2, making it unsuitable in applications such as equal current sharing, efficiency optimization etc. In order to calibrate the dc matching, the midpoints of the sensed voltages from senseFET and RC filter are used (point B in Fig. A.4), where the instantaneous inductor current value is equal to that of the dc current. Comparing these points the gain of the sense-FET is tuned by changing $R_{\text{sense}}$ (Eq.A.1), until the both average values match with each other.

A.2.2 Time constant matching

Mismatches in time constants result in wrong ripple measurement, as shown in Fig. A.3. After matching the gain of the senseFET, as explained in Section A.2, any mismatch between the peaks of sensed voltages of two current sensing circuits is due to the time constant mismatch. This results in suboptimal dynamic regulation [14]. As a result, point C in Fig. A.4, where the inductor current reaches its peak, is used to eliminate any time constant mismatch. The time constant of the hybrid current sensing circuit is tuned properly, by changing $R_f$, to eliminate any difference between the two peaks, thus, allowing accurate information of the inductor current ripple.
An IC is designed and fabricated to implement the introduced hybrid self-tuning current sensor. As explained in the previous section, two pieces of information are needed to accurately tune the sensing filter. The dc is calibrated by comparing the dc values of the sensed voltages and the time constant is calibrated by comparing the peaks. As shown in Fig. A.1, two sample-and-hold circuits are used to capture these values from the senseFET and sensing filter. These values are then compared with an analog comparator which is used to calibrate the gain and time-constants.
of the circuit. This is accomplished by changing the value of two digitally controlled potentiometer (DPOT) modules, implemented on the IC. As shown in Fig. A.5, the FPGA based calibration module adjusts the resistance values of the DPOTs, through the scan-chain, providing serial to parallel interface from the calibration module of the FPGA to the DPOTs implemented on the IC.

![Integrated Chip (IC)](image)

Fig. A.5 Digitally Programmable Potentiometer (DPOT) and calibration modules

As mentioned in previous section, in order to match the dc, the gain of the senseFET circuit is calibrated by changing $R_{\text{sense}}$, which is implemented using a DPOT. Any variation of dc, due to $R_L$ variation is captured in this value and hence, can be adjusted accordingly in the controller for equal current sharing and/or efficiency optimization schemes. Similarly, after matching the dc, in order to match the time constants of the RC filter a DPOT is implemented in series with a fixed valued capacitance, $C_f$ (Fig. A.1). The DPOT implementing $R_f$ is adjusted until the peaks of both current sensing waveforms match. The DPOT is implemented on the IC where as the filter
capacitance, \( C_f \) is kept off-chip. Since depending on the value \( R_L \) and \( i_L \), the sensed voltage, \( v_f(t) \) can be small, in order to have a better matching an amplifier is used across, \( C_f \). Due to the continuous triangular shape of \( v_f(t) \), this amplifier requires significantly smaller bandwidth, 3 to 5 times the switching frequency, compared to current matching opamp of the senseFET circuit, where at least 10 times higher bandwidth is required. Hence, even with 4 times higher the gain, \( v_f(t) \) amplifier will be consuming around twice as much power as the senseFET amplifier. As a result, if the calibration module is used once every 1000 cycles for maximum of 10 cycles, due to sequential calibration of dc and peak matching, the total power consumption, including comparator and digital logic, will be less than \( 5/100^{th} \) of senseFET based approach.

Fig. A.6 shows the output of sample and hold circuits and analog comparator, along with both sensed voltages during dc calibration. The calibration process is started by introducing sample-and-hold (S/H) clock, and as the initial dc value of the senseFET (\( v_{\text{sense}} \)) is much smaller than that of the filter (\( v_f \)), comparator shows low output. In the subsequent switching intervals the value of \( R_{\text{sense}} \) DPOT is increased, which in return increases \( v_{\text{sense}} \) value. This is continued until the comparator output changes from low to high, showing proper calibration of the dc gain.
Similarly, Fig. A.7 shows the output of sample and hold circuits and analog comparator, along with both sensed voltages during peak calibration. The calibration process is started by introducing sample-and-hold (S/H) clock. In this case the initial peak value of the senseFET ($v_{\text{sense}}$) is much larger than that of the filter ($v_f$), and hence, comparator shows high output. In the subsequent switching intervals the value of $R_f$ DPOT is decreased, which in return increases $v_f$ ripple. This is continued until the comparator output changes from one to zero, showing proper calibration of the time constant matching. In addition, the calibration time can be significantly
reduced by implementing binary weighted resistive network as DPOT and a binary search algorithm as shown in [17].

Fig. A.7 Simulated waveforms for peak calibration

Fig. A.8 shows how the dynamic regulation is significantly improved when time constants are matched, by comparing the converter response for the same PI controller with 25% smaller (top waveform) and larger (middle waveform) filter time constants, respectively. The bottom waveform of Fig. A.8 shows the peak of the sensed voltage across the filter, $v_f(t)$, representing the peak of inductor current waveform. It clearly demonstrates that a significantly improved response for $V_{f2.pk}$ is achieved, as the time constants, in that case, are properly matched.
Fig. A.8 Effect of time constant mismatch in closed loop transient simulations.
A.4 Experimental System and Results

The integrated solution of the introduced on-line calibration technique, along with a 4 MHz, 350 mW power stage, is fabricated in 0.13µm technology, as shown in Fig. A.1. The chip provides programmable output voltage (0.8-1.4 V), from input voltage up to 2.7 V. The chip micrograph is shown in Fig. A.9 and Table A.I summarizes its main specifications. Analog sensing circuitry such as sample-and-hold and comparator are integrated on chip, where a FPGA is used to implement the calibration module.

Fig. A.10 shows the senseFET output, $v_{\text{sense}}(t)$ along with switching node voltage, $v_x(t)$ and the inductor current, $i_L(t)$ measured with a current probe. As shown in this figure, when the switching node voltage goes to high, meaning the high side switch of the converter turning on, the output of the senseFET voltage waveform shows the shape of the inductor current. This verifies the proper functionality of the senseFET based current sensing integrated on the chip.

Table A.I: IC implementation specifications

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
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<td>µm</td>
</tr>
<tr>
<td>Total Area</td>
<td>1 x 2</td>
<td>mm²</td>
</tr>
<tr>
<td>Switching Freq.</td>
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<td>MHz</td>
</tr>
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<td>$R_{\text{on}}$ PMOS, NMOS</td>
<td>270, 220</td>
<td>mΩ</td>
</tr>
<tr>
<td>$V_{\text{in}}$</td>
<td>2.7</td>
<td>V</td>
</tr>
<tr>
<td>$V_{\text{out}}$</td>
<td>0.8-1.4</td>
<td>V</td>
</tr>
<tr>
<td>Buck $L,C$</td>
<td>2, 10</td>
<td>µH, µF</td>
</tr>
</tbody>
</table>
Fig. A.9 Die Photo of implemented IC
Fig. A.10 SenseFET output. Ch1: senseFET output, \( V_{\text{sense}} \) (200 mV/div); Ch2: inductor current, \( i_L \) (50 mA/div); Ch3: switching node, \( V_x \) (1 V/div).

Fig. A.11 shows how the gain of the senseFET can be calibrated by changing \( R_{\text{sense}} \) DPOT. The top waveform of Fig. A.11 is the inductor current which is measured using a current probe. Two different senseFET measurements (\( v_{\text{sense}} \)), for different DPOT values, are superimposed to demonstrate the difference in gain. The bottom waveform shows the switching node of the converter, demonstrating 4 MHz switching frequency.
Fig. A.11 SenseFET gain calibration. Ch1: *senseFET output*, $V_{\text{sense}}$ (100 mV/div); Ch2: *inductor current*, $i_L$ (50 mA/div); Ch3: *switching node*, $V_x$ (1 V/div)

Fig. A.12 shows how the time constant of the RC filter can be calibrated by changing $R_f$ DPOT. The top waveform is the inductor current which is measured using a current probe. Two different measurement of $v_f$ across the filter capacitor, $C_f$ is superimposed to demonstrate the effect of time constant variation. The bottom waveform shows the switching node of the converter, demonstrating 4 MHz switching frequency.
Fig. A.12 Time constant calibration. Ch2: inductor current, \(i_L\) (50 mA/div); Ch3: RC filter output, \(V_f\) (50 mV/div); Ch4: switching node, \(V_x\) (1 V/div)

Fig. A.13 shows both sensed voltage waveforms, from senseFET, \(v_{\text{sense}}(t)\) and RC filter, \(v_f(t)\), superimposed on each other. The actual inductor current waveform from the current probe is also shown. As shown in this figure, when the gain and time constants are matched, both sensed waveforms have identical shape and their average and peak value match, showing a proper calibration.
**Fig. A.13** Matched gain and time constants. Ch1: *senseFET output*, $V_{sense}$ (200 mV/div) Ch2: *inductor current*, $i_L$ (50 mA/div); Ch3: *switching node*, $V_x$ (1 V/div)

### A.5 Conclusions

A hybrid on-chip implemented current sensor, suitable for high frequency low-power dc-dc converter ICs is presented here. Combining a conventional senseFET with simple RC filter based sensorless technique, allows improving accuracy without paying penalty in power consumption. The introduced calibration technique targets both dc and ripple current matching, making the sensing suitable for efficiency optimization techniques and is able to achieve superior dynamic regulation. The effectiveness of the proposed calibration technique is verified on a custom IC
fabricated in 0.13µ process. Simulation and experimental results show proper functionality of the proposed calibration system.

### A.6 References


Appendix B

Power Management Architecture for Universal Input Ac-Dc Adapter Support in Battery Powered Applications

B.1 Introduction

Modern battery-powered portable electronic devices, such as cell phones, laptops, tablet PCs, portable DVD players, and the like, use ac-dc wall adapters to recharge their enclosed batteries. These electronic devices require a wide range of fixed input voltages for proper operation. Today, depending on the application, output voltages of power adapters range between 5 V and
20 V [1]. The wide variety of the device requirements creates a burden for the user who, alongside portable devices, needs to carry a number of device-specific power adapters, which are often bulky.

The requirement for the use of an application specific adapter is related to the power management system of a portable device, whose typical architecture is shown in Fig. B.1 [2]. The system consists of a battery charger, dc-dc bus voltage converter, and a set of point of load (PoL) dc-dc converters supplying functional blocks. Depending on the conversion ratio and power rating the PoL can be realized as switch mode power supply (SMPS) or low-dropout (LDO) linear regulators. A set of switches for reconfiguring the system depending on the mode of operation is also often included. Here, when the adapter is connected, switch $SW_1$ is turned on, switch $SW_2$ is turned off and the adapter is used for both providing the bus voltage ($V_{bus}$) and battery charging [3]. When the adapter is unplugged, $SW_1$ is turned off, $SW_2$ is turned on and the battery provides the bus voltage, through the dc-dc bus converter. In both of these modes, i.e. adapter-powered and battery-powered, the bus voltage is the same. Other voltages, required by various functional blocks of the device, are derived from the bus voltage, using downstream dc-dc SMPS and linear LDOs.
The presented conventional architecture has a significant drawback of imposing a fairly strict limit on the adapter output voltage. This limit comes from the fact that the bus and the adapter voltages need to be approximately the same, since the efficiency and dynamic performance of the downstream stages are strongly affected by the bus voltage variations [4]. The adapter voltage is further constrained by the limitations imposed by the internal battery charging converter and its required input voltages. As a consequence, dedicated device-based adapters are usually needed for laptop and tablet computers, mobile phones and all other devices we use.

The goal of this appendix is to introduce a simple universal-input power management system architecture that eliminates the need for application-specific adapters by allowing a wide range of dc input voltages to be connected to a battery-powered portable device. The new flyback-converter based architecture, shown in Fig. B.2, breaks the fairly strict three-way dependence between the bus ($V_{bus}$), battery ($V_{batt}$), and adapter ($V_{adapt}$) voltages existing in the conventional solutions. Also, the new architecture is well suited for incorporating emerging programmable bus voltage techniques, where the bus voltage is dynamically varied to optimize the overall system.
efficiency [5]. Furthermore, the power management architecture eliminates the need for application-specific battery packs, potentially allowing a wider range of battery packs to be used with a given portable device.

**B.2 System Description and Principle of Operation**

The core element of the power management system architecture of Fig. B.2 is a flyback-based converter. The following subsections explain its operation in three distinct modes of operation: i) adapter-powered bus regulation and battery charging, ii) adapter-powered bus regulation only, which is utilized when the battery is fully charged, and iii) battery-powered bus regulation.

Fig. B.2: Universal-input power management system
Appendix B

B.2.1 Adapter-powered bus regulation and battery charging

In this mode of operation, both the bus voltage regulation and battery charging are provided. The sequence of gating signals for proper converter operation is selected based on the adapter and battery voltages. The following subsections discuss the introduced converter operation for both higher and lower adapter voltages compared to the battery voltage.

B.2.1.1 Operation for $V_{adap} \geq V_{batt}$

Fig. B.3a shows the circuit configuration and the key converter waveforms for the case when the adapter voltage is higher than the battery voltage. Those include the gating signals of all three switches, the magnetizing inductance current and the battery charging current.

In this mode $SW_4$ is not used, hence it is always off, and the switching period $T_{sw}$ has three distinctive intervals. The switch $SW_1$ is turned on during the first two intervals, providing the input current from the adapter. During the first interval, labeled as $d_1 T_{sw}$, the magnetizing inductance is charged and, during the second and third intervals, the stored energy is distributed between the battery and the bus, respectively. This is achieved by operating $SW_2$ with a duty ratio $d_1$ and by gating $SW_3$ with duty ratio $d_2$ to charge the battery. In the third interval, when $SW_1$ is turned off, the magnetizing inductor current flows through the transformer, and hence transfers the energy to the bus through the diode $D_1$. As shown in Fig. B.3a, when $SW_2$ is on, the magnetizing inductor current has a slope of $V_{adap}/L_{m}$, where $V_{adap}$ is the adapter output voltage and $L_{m}$ is the magnetizing inductance. During the conduction of $SW_3$, the slope is changed to
\(\frac{(V_{\text{adapt}} - V_{\text{batt}})}{L_m}\), where \(V_{\text{batt}}\) is the battery voltage. Since in this case \(V_{\text{batt}}\) is smaller than \(V_{\text{adapt}}\), a positive slope of magnetizing inductance current occurs when \(SW_3\) conducts.

![Diagram](image)

Fig. B.3a: Adapter-powered mode of operation when \(V_{\text{adapt}} \geq V_{\text{batt}}\). Top: converter configuration; Bottom: key converter waveforms
It can be found that the relation between the three voltages in this mode is described with the following equation:

\[
V_{bus} = n \cdot V_{adap} \cdot \frac{d_1 + d_2}{1 - d_1 - d_2} - n \cdot V_{batt} \cdot \frac{d_2}{1 - d_1 - d_2}
\] (B.1)

where \( d_1 \) and \( d_2 \) are the duty ratio values of switches \( SW_2 \) and \( SW_3 \), respectively. This equation shows that, by adjusting \( d_1 \) and \( d_2 \), both the bus voltage regulation and the charging of the battery can be achieved independent of the adapter voltage value. It also shows that the rigid correlation between the battery, adapter, and bus voltages existing in the conventional architecture is eliminated. As described in Section B.3, the digital controller of Fig. B.1 sets the two duty ratio values, such that the desired bus voltage regulation and battery charging profile are achieved. The controller also provides seamless mode transitions.

### B.2.1.2 Operation for \( V_{adap} < V_{batt} \)

Fig. B.3b shows the circuit configuration and the key converter waveforms, for the case when the adapter voltage is lower than the battery voltage.

The gating sequence in this mode of operation is similar to those for \( V_{adap} \geq V_{batt} \) situation. However, in this case, there is a major difference affecting the transformer design. When \( SW_3 \) is turned on, during the second interval, a negative voltage is applied across the magnetizing inductor (in Fig. B.3b indicated by, the negative slope of its current). This means that on the secondary side of the flyback transformer the reflected voltage is also opposite, possibly causing
conduction of the diode, $D_1$. To prevent this, the turns ratio of the flyback transformer $n$ can be selected such that it satisfies the following equation:

$$n \cdot (V_{batt} - V_{adap}) < V_{bus} \quad (B.2)$$

![Diagram of Flyback Transformer](image)

Fig. B.3b: Adapter-powered mode of operation when $V_{adap} < V_{batt}$. Top: converter configuration; Bottom: key converter waveforms
B.2.1.3 Adapter-powered bus regulation only

The adapter-powered bus regulation only mode is activated when the battery is fully charged, and hence, there is no need for further charging. In this mode, the converter operates as a conventional flyback. Here, the previously described interval 2 of Figs.B.3a and B.3b is eliminated by turning off both $SW_1$ and $SW_2$ at the end of the first interval. Throughout this mode, $SW_3$ and $SW_4$ are kept off and the conversion ratio is:

$$V_{bus} = n \cdot V_{adap} \cdot \frac{d_1}{1-d_1}$$  (B.3)

where, $d_1$ is the duty ratio for $SW_1$ and $SW_2$. The adapter-to-bus steady-state conversion ratio for this mode can also be found from equation (1), by setting $d_2$ to zero.

B.2.2 Battery-powered bus regulation

Fig. B.4 demonstrates the operation of the power management module when an adapter is not connected and the battery powers the device. In this case $SW_1$ and $SW_3$ are always turned off, $SW_2$ is kept on and $SW_4$ operates at a switching frequency $f_{sw}=1/T_{sw}$, with duty ratio $d$. When $SW_4$ is turned on, $V_{batt}$ is seen across the transformer primary side. When $SW_4$ is turned off, the diode $D_1$ conducts. This operating mode is similar to that of the conventional flyback converter. Hence, the ideal battery-to-bus voltage conversion ratio is:

$$V_{bus} = n \cdot V_{batt} \cdot \frac{d}{1-d}$$  (B.4)
The equation shows that the bus voltage can be regulated without imposing a strict limitation on the battery pack voltage. Therefore, a large flexibility in selecting battery packs for a given device is provided. It is important to note that the direction of the magnetizing inductor current is the same in all three modes of operation, allowing smooth mode transitions.

Fig. B.4: Battery-powered mode of operation Top: converter configuration; Bottom: key converter waveforms
B.3 Practical Implementation

A practical implementation of the introduced power management system, including switch realization, is shown in Fig. B.5. The figure also shows a block diagram of the digital controller.

B.3.1 Power stage

The four switches on the primary side of the flyback transformer in Fig. B.5 (labeled $SW_{1-4}$) enable the desired multi-mode operation. In this case the transistor $SW_5$ replaces diode $D_1$ of Fig. B.2, to minimize the conduction loss. $SW_4$ is realized with back-to-back transistors providing bi-directional voltage blocking and thus, allowing battery voltage $V_{batt}$ to be higher or lower than $V_{adap}$. The back-to-back connection also prevents the magnetizing inductance current from flowing through $SW_3$ and $SW_4$ when $SW_2$ is turned off in adapter-powered mode of operation. Also, as mentioned earlier, during battery powered mode (Fig. B.4), $SW_4$ is turned off rather than $SW_2$, to prevent the primary side current circulating through $SW_4$ and the body diode of $SW_3$. An RCD snubber [6] is incorporated to provide over-voltage protection from the flyback-transformer’s leakage inductance current.
B.3.2 Digital Controller

The multi-mode digital controller of Fig. B.5 regulates both the bus voltage and the battery charging process. The Mode Control module generates various gating sequences for $SW_{1-5}$, depending on the state-of-charge of the battery, and detects the presence of the adapter. The presence of adapter and battery voltage level are detected through $Mux$ and the analog-to-digital converter $ADC_1$. This module periodically samples both $V_{adap}$ and $V_{batt}$ to detect the adapter input and to monitor the battery voltage, preventing overcharging of the battery.

Fig. B.5: Practical implementation of the introduced architecture
B.3.2.1 Bus voltage regulation in Battery-powered or adapter-powered mode

When simultaneous battery charging and bus regulation is not required, the converter operates as a conventional digital voltage-mode pulse-width modulated system [7], [8]. An analog-to-digital converter, $ADC_2$ senses the bus voltage and, after a comparison with the desired reference $V_{ref}$, an error signal $e[n]$ is created. This signal is fed to a PID compensator. The digital duty ratio command generated by the PID, $d[n]$, is then passed to a multi-input multi-output DPWM module through the Mode Control module, creating the signals as previously described in Section B.2.

B.3.2.2 Combined battery charging with bus voltage regulation, mode transitions and soft start

When the battery voltage drops, indicating that charging is needed, gating pulses are sent to $SW_3$ immediately after $SW_2$ turns off, providing pulsating currents to the battery cells, as described in Section B.2. This dual pulse injection can create a sub-transient response in the output voltage, requiring the PID to update the duty command for this new steady-state operation. In order to reduce the perturbation of the output voltage from the battery cell charging, the width of the $SW_3$ gate pulses is slowly incremented from zero. This soft-starting mechanism allows the controller to gradually adjust the duty ratio, providing a seamless transition.

A duty ratio predicting method is implemented in order to achieve a smooth transition after connection or disconnection of the adapter. In this method, a new initial duty command $d_{new}[n]$ is determined based on the new operating mode and the corresponding past and present input
voltages. This duty information is then sent to the PID module to set up the initial duty ratio for the gating signals in the new operating mode.

**B.4 Experimental System and Results**

To verify the operation of the universal-input power management system, a 20 W, 100 kHz experimental prototype was developed. The results obtained with the experimental setup are shown in Figs.B.6 to B.13.

Fig. B.6 shows the steady-state operation of the converter in the presence of a 9 V adapter and a 3 V battery, where both the bus voltage regulation at 5 V and battery charging are simultaneously performed. The results confirm that, for the newly introduced topology, a dedicated adapter with a voltage close to the bus value is not needed. It can be seen that the bus voltage is well regulated, even though relatively large differences between the adapter, bus, and battery voltage values exist. Fig. B.7 shows a magnified version of the steady state current waveforms with the slopes indicated.
Appendix B

Fig. B.6: Steady-state operation in battery charging mode, when $V_{adap}=9\,\text{V}, V_{batt}=3\,\text{V}, V_{bus}=5\,\text{V}$

Fig. B.7: Magnified steady-state operation in battery charging mode, when $V_{adap}=9\,\text{V}, V_{batt}=3\,\text{V}, V_{bus}=5\,\text{V}$
Fig. B.8 shows simultaneous system operation of 5 V bus regulation and battery charging when adapter voltage is 9 V and battery voltage is 7.5 V. The result verifies that the introduced architecture is able to regulate the bus when both adapter and battery voltages are higher than the bus voltage. Fig. B.9 shows the waveforms for the case when the adapter voltage is lower (4V) and battery voltage is higher (6V) than the bus voltage (5V). This verifies the proper system operation for $V_{adap} < V_{batt}$.

![Waveforms](image)

Fig. B.8: Steady-state operation in battery charging mode, when $V_{adap} = 9V, V_{batt} = 7.5V, V_{bus} = 5V$
Fig. B.9: Magnified steady-state operation in battery charging mode, when $V_{\text{adap}}=4\text{V}, V_{\text{batt}}=6\text{V}, V_{\text{bus}}=5\text{V}$

Figs.B.10 and B.11 show the system operation from the battery when the battery voltage is 7.5V and 3V, respectively. These waveforms demonstrate tight bus voltage regulation irrespective of the battery voltage.
Fig. B.10: Steady-state operation from battery input, when $V_{\text{batt}}=7.5\,\text{V}, V_{\text{bus}}=5\,\text{V}$

Fig. B.11: Steady-state operation from battery input, when $V_{\text{batt}}=3\,\text{V}, V_{\text{bus}}=5\,\text{V}$
Figs. B.12 and B.13 show transitions between the adapter-powered and the battery-powered modes of operation during the adapter connections/disconnection process. Fairly smooth transitions causing no larger than 200 mV variation of the bus voltage are achieved, which is comparable to those of state of the art solutions [2].

Fig. B.12: Transition from adapter-powered mode to battery-powered mode
Fig. B.13: Transition from battery-powered mode to adapter-powered mode

B.5 CONCLUSIONS

A universal-input flyback-based power management architecture is introduced. It allows a wide range of dc voltages to be connected to the inputs of portable devices, eliminating the need for device-specific ac-dc adapters. The architecture also potentially allows a wider range of battery packs to be used with a given battery powered portable device. The new topology and its complementary digital controller allow smooth transitions between the adapter and battery supplied modes of operation. Experimental verification with a 20W prototype fully confirms functionality of the new universal-input power management system.
B.6 References


