A Gate Sinking Threshold Voltage Adjustment Technique for High Voltage GaN HEMT

by

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A thesis submitted in conformity with the requirements for the degree of Master of Applied Science
Graduate Department of Electrical and Computer Engineering
University of Toronto

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Abstract

GaN-based power electronics receive many interests because of its wider bandgap, higher electron mobility and higher critical electrical field than silicon. However, the intrinsic AlGaN/GaN-based HEMT is a “normally-on” device. This thesis proposes a gate sinking method during the metal gate deposition to adjust the $V_T$ towards enhancement mode operation. This recessed gate process relies on the chemical reaction between Ta and AlGaN using a simple RTA procedure rather than the more complicated RIE method. This eliminates the need for etching with nanometer precision. During the Ta sputtering process, both Ar and N$_2$ carrier gases are used to form TaN with work function in the range of 4.15 to 4.7 eV. The fabricated HV GaN HEMTs exhibit $V_T$ shift from $-5$ to $-2$ V. Moreover, the proposed device is compatible with silicon-CMOS technology to ensure cost-effective implementation of future high performance smart power ICs.
Acknowledgments

Foremost, heartfelt gratitude to my supervisor Dr. Wai Tung Ng for his continues guidance, inspiration, and encouragement throughout my master program at University of Toronto. Professor Ng has been an excellent advisor and a great mentor in life. His knowledge and vision in power electronics have helped me to explore my research interest. His scientific attitude and technical excellence deeply impress me. I always admire him having both successful career and lovely family. I am very proud to work with him in my MASc study.

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<th>Acronym</th>
<th>Definition</th>
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<tbody>
<tr>
<td>SCCM</td>
<td>Standard Cubic Centimeters per Minute (a flow measurement)</td>
</tr>
<tr>
<td>MESFET</td>
<td>Metal Semiconductor Field Effect Transistor</td>
</tr>
<tr>
<td>HEMT</td>
<td>High Electron Mobility Transistor</td>
</tr>
<tr>
<td>SOA</td>
<td>Safe Operation Area</td>
</tr>
<tr>
<td>BV</td>
<td>Breakdown Voltage</td>
</tr>
<tr>
<td>$R_{on,sp}$</td>
<td>Specific On Resistance</td>
</tr>
<tr>
<td>RTA</td>
<td>Rapid Thermal Annealing</td>
</tr>
<tr>
<td>ALD</td>
<td>Atomic Layer Deposition</td>
</tr>
<tr>
<td>D-mode</td>
<td>Depletion Mode (normally-on)</td>
</tr>
<tr>
<td>E-mode</td>
<td>Enhancement Mode (normally-off)</td>
</tr>
<tr>
<td>RIE</td>
<td>Reactive Ion Etching</td>
</tr>
<tr>
<td>CVD</td>
<td>Chemical Vapor Deposition</td>
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Chapter 1  Recent Development in Power Electronics

Power electronic devices used in switched mode power supply (SMPS) require high voltage and high current handling capabilities to efficiently process electrical energy [1]. Examples of power device applications include energy conversions [2], amplifications, and electric drives [3]. Three common categories of power devices are transistors, diodes, and thyristors. Modern power transistors include bipolar junction transistor (BJT), MOS field effect transistor (MOSFET), merged MOS-bipolar hybrid device such as insulated-gate bipolar transistor (IGBT), and wide bandgap (WBG) power transistors [1]. Power BJTs, MOSFETs and IGBTs are mainly fabricated on traditional silicon substrate, while WGB power transistors are built with new type of substrates such as silicon carbide (SiC), gallium nitride (GaN) and diamonds [4].

The performance of silicon-based power electronics are limited by their on-resistance, switching speed, and junction temperature [4]. WBG based power electronics have received a lot of interest due to their wider bandgap, higher electron mobility and higher breakdown electrical field than silicon. These properties result in higher temperature tolerance, lower conducting resistance and higher breakdown voltage for WBG based devices when compared with silicon-based devices. These characteristics provide WBG devices with added advantages in power electronics [5].

In Section 1.1, the trends in power transistors will be reviewed. A comparison between silicon and WBG material properties will be discussed in Section 1.2. The GaN featured power devices are introduced in Section 1.3. Finally, the thesis objectives and organization will be outlined in Section 1.4.

1.1 Trends in Power Transistors

The first popular power transistor was the silicon bipolar junction transistor (BJT) developed in the 1960s. However, as large base currents are required to control these devices, control circuits for power BJTs are highly complex. BJTs have low on-resistance because of its two-carriers conduction, as opposed to the unipolar conduction in MOSFET. However, the turn-off mechanism in BJTs relies on charge recombination that is too slow for modern high-speed
switching power electronic circuits. As a result, power MOSFETs were introduced in 1970s as a better candidate. MOSFETs are voltage-controlled and majority carrier devices. They offer advantages such as simpler design of gate drive circuit, higher switching speed, higher input-impedance and wider safe-operating area (SOA). Power MOSFETs quickly dominated power electronic applications. In 1980s, the IGBT structure that offered the high output current capability of BJT with voltage-controlled gate of a MOSFET was introduced. Today, IGBTs fill the gap between bipolar devices and MOSFETS (see Figure 1.1) and becomes one of the mainstream devices in power electronic industry [1, 4, 6, 7].

![Diagram showing power capacity and operation frequency of different types of devices and their respected applications](image.png)

Figure 1.1 Power capacity and operation frequency of different types of devices and their respected applications [7].

In the past four decades, silicon-based power devices dominated the SMPS market. However, silicon devices are limited by their operating temperatures, breakdown strength and switching
frequencies due to their narrow bandgap, low critical electrical field strength and saturation velocity. WBG power devices, in contrast, offer improved characteristics. These devices will be introduced in the next Section.

1.2 Comparisons of Silicon and WBG Materials

Both SiC and GaN materials offer superior characteristics to overcome the limitations of silicon as suggested by the physical properties in Table 1.1. GaAs has high electron mobility which is good for the current conduction, but its low critical electrical field limits the improvement in breakdown voltage. Diamond is an ideal material for power device but it is difficult to be processed. By comparison, GaN has higher electron mobility due to an availability of the two-dimensional electron gas (2-DEG). As a result, the channel resistance in GaN devices is lower. However, the lack of good quality GaN single crystal substrates prevented the practicality of vertical GaN power devices. As an alternative to single crystal GaN, high quality GaN layers can be grown on sapphire, SiC, or silicon substrates. In particular, lateral GaN on silicon devices are good candidates to support the integration of CMOS technology.

Table 1.1 Physical Properties of Various Materials at 300 K [4, 8]

<table>
<thead>
<tr>
<th>Semiconductor Materials</th>
<th>Bandgap $E_g$ (eV)</th>
<th>Electron Mobility $\mu_n$ (cm$^2$/Vs)</th>
<th>Saturation Velocity $V_{sat}$ ($10^7$ cm/s)</th>
<th>Critical Field $E_c$ (MV/cm)</th>
<th>Thermal Conductivity $\sigma_T$ (W/cm·K)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>1.12</td>
<td>1400</td>
<td>1.0</td>
<td>0.3</td>
<td>1.3</td>
</tr>
<tr>
<td>GaAs</td>
<td>1.43</td>
<td>8500</td>
<td>1.0</td>
<td>0.4</td>
<td>0.55</td>
</tr>
<tr>
<td>SiC</td>
<td>3.25</td>
<td>700</td>
<td>2.5</td>
<td>2.2</td>
<td>3.8</td>
</tr>
<tr>
<td>GaN</td>
<td>3.44</td>
<td>1800 (2-DEG)</td>
<td>2.5</td>
<td>3.3</td>
<td>1.3</td>
</tr>
<tr>
<td>Diamond</td>
<td>5.46</td>
<td>2200</td>
<td>3</td>
<td>5.7</td>
<td>20</td>
</tr>
</tbody>
</table>
As a result, GaN HEMTs have received significant attention with its potential for a better trade-off between specific ON resistance ($R_{on,sp}$) and breakdown voltage (BV) over its silicon counterparts. A typical trade-off between $R_{on,sp}$ and BV can be expressed as [8]:

$$R_{on,sp} = \frac{4 \cdot V_{BR}^2}{\varepsilon_0 \cdot \varepsilon_r \cdot E_{crit}^2}$$  \hspace{1cm} (1.1)

where $\varepsilon_0$ and $\varepsilon_r$ refer to the permittivity of free space and relative permittivity, respectively. The trade-offs between Si, SiC and GaN materials are as plotted in Figure 1.2.

![Figure 1.2](image_url)  

Figure 1.2 The specific on-resistance versus breakdown voltage limits for Si, SiC and GaN [8].

The GaN HEMT limit is promising because it has the lowest ON-state resistance for a given breakdown voltage when compared to silicon devices and SiC power devices. This characteristic allows GaN HEMTs to exhibit lower on-state resistance and higher forwarding blocking voltage in the off-state. The ability to fabricate the GaN power devices alongside with modern VLSI process is promising for the next generation smart power ICs. The compatibility with silicon
fabrication technology, allows GaN on silicon power devices to be more cost effective than GaN on SiC devices built on exotic substrates. The competition between SiC and GaN as candidates of power electronics is still on going. Both SiC and GaN power devices are expected to fill their respective applications.

1.3 Emergence of GaN MESFET

As mentioned, traditional power MOSFETs are fabricated on silicon, one of the most common semiconductor materials. Nevertheless, wide bandgap (WBG) materials, including GaN, have their advantages over silicon. As opposed to MOSFET, GaN power devices are mainly Metal semiconductor FET (MESFET). Cross-sectional views of the two structures are illustrated in Figure 1.3. Traditional silicon MOSFETs are fabricated on $p$-doped silicon, whereas MESFET is fabricated on a semi-insulating substrate. The channel can be grown on silicon, sapphire or SiC substrates. The source and drain contacts of both structures consist of heavily doped $n^+$ regions to reduce the parasitic resistances [9].

![Cross-sectional structure of basic MOSFET and MESFET](image)

Figure 1.3 Left (a) cross-sectional structure of basic MOSFET and right (b) cross-sectional structure of basic MESFET [9].

When a positive drain to source voltage $V_{DS}$ is applied to a MOSFET, the current $I_{DS}$ is blocked by the reverse biased $n^+$ drain / $p$ body diode. When a positive gate voltage is applied, electrons are attracted to the oxide layer and form a channel to allow $I_{DS}$ to flow. The metal gates in
MESFETs are in direct contact with the semiconductor, forming a Schottky-barrier diode. When a positive $V_{DS}$ is applied to a MESFET, electrons can flow from the source to the drain even without a gate bias voltage. When a negative gate voltage is applied, the channel becomes depleted, and the MESFET is turned off. As a result, The MESFET is called a depletion-mode (D-mode) device that is “normally-on”. To fabricated a D-mode MESFET, both Schottky and ohmic contacts are required.

D-mode transistors are not desirable due to the safety concern in the event of gate driver circuits failure. Enhancement-mode MESFETs with positive threshold voltage are much more appropriate. A normally-off MESFET can be obtained by modifying the depletion region under the gate region when $V_{GS} = 0$. Parameters that can adjust the threshold voltage include choices of gate material, channel depth, channel material, and placement of additional materials under the gate [9].

Techniques of adjusting threshold voltage will be reviewed based on a GaN high electron mobility transistor (HEMT) structure, as shown in Figure 1.4. The current conduction of HEMT utilizes the two dimensional gas (2-DEG) that exists at the AlGaN/GaN interface [10]. This will be explained in the next chapter. This thesis focuses on effective ways to adjust the threshold voltage of GaN power HEMT with fabrication techniques compatible with current silicon CMOS processes.

![Cross-sectional view of a HEMT with the 2-DEG channel](image)

Figure 1.4 Cross-sectional view of a HEMT with the 2-DEG channel [9, 10].
1.4 Thesis Objectives and Organization

Threshold voltage adjustment is the first step to form E-mode GaN HEMTs. With GaN power device fabricated on silicon, modern power IC can enjoy superior trade-offs of both GaN power HEMT and the mature fabrication technology of VLSI.

This chapter has provided the necessary background for GaN HEMs. However, there is lack of discussion on the fabrication techniques that can effectively adjust the threshold voltage. The objectives of this thesis are to examine CMOS compatible fabrication techniques, which can adjust the threshold voltage of GaN power HEMTs.

There are five chapters in this thesis. Chapter 1 provides an overview of the development of power electronics and background information on the GaN HEMTs.

Chapter 2 explains the working mechanism of HEMTs and reviews different techniques that can be used to adjust the threshold voltage. These include oxidization insulation, fluorine implantation, and gate recession.

Chapter 3 proposes a gate recessed HEMT structure. Different experimental device structures are presented. The final device dimensions and photo-mask design will be described in detail.

Chapter 4 presents the fabrication processes and experimental results. Experimental results are analyzed and the effectiveness of each threshold voltage adjustment technique discussed.

Chapter 5 summarizes the characteristics of the proposed device and its fabrication process. Finally, suggestions for future work are discussed.
Chapter 2  A Review of GaN HEMTs

This chapter describes the conventional techniques to adjust the threshold voltage of GaN HEMTs. The contents are organized as follows: Section 2.1 introduces the power GaN MESFET, including power GaN HEMT. Section 2.2 analyzes various methods for adjusting the threshold voltage of GaN HEMTs. Section 2.3 evaluates the practical fabrication techniques for GaN material and their compatibility with silicon-based CMOS technology. Section 2.4 proposes a gate sinking method for the adjustment of threshold voltage. Finally, Section 2.5 provides a summary of the chapter.

2.1 The GaN MESFET Structure

This section will provide a background of GaN HEMTs through the discussion of Schottky contacts and metal semiconductor FETs (MESFETs) and high electron mobility transistors (HEMTs). This is followed by a discussion on the GaN HEMT structures, including GaN substrate, GaN/AlGaN interface, two-dimensional electron gas (2-DEG), and GaN HEMT operating mechanism.

2.1.1 Metal-Semiconductor Contact and MESFETS

When a metal with work function $\Phi_M$ and Fermi level $E_{FM}$ is brought into contact with a semiconductor with electron affinity $\chi_S$, bandgap $E_g$, and Fermi level $E_{FS}/E_{FM}$, a metal/semiconductor junction with a Schottky barrier is formed [11]. For the case $\Phi_M > \Phi_S$ (the work function of semiconductor), the energy-band diagrams are as shown in Figure 2.1, where W stands for the depletion width of the junction. Figure 2.1 (a) and (b) show the band diagrams before and after physical contact, respectively. Figure 2.1 (c) and (d) show the energy-band diagram under forward bias and reverse bias conditions, respectively.

The ideal Schottky barrier height $\Phi_B$ is determined by $\Phi_M$, $\Phi_S$, and $\chi_S$ as well as the applied bias voltage $V_a$ on the metal contact [10]. This barrier allows current to pass through when the metal contact is forward biased but block the current when the metal contact is reverse biased [11].
By increasing the doping concentration of the semiconductor, $W$ becomes thinner. When the depletion width is less than 5 nm, the tunneling probability of carriers increases [11]. At this time, the electrons can pass through the barrier with forward or reverse bias, such contact cannot block current from either direction, forming an ohmic contact [10].

Some metal with a certain work function $\Phi_M$, can form both ohmic and Schottky contact with on the same type of semiconductor but with different doping concentrations. This is due to the different amounts of energy-band bending. The higher the $n$-type doping concentration, the steeper the energy-band bending and the thinner the barrier. Typically, a doping concentration of as high as $10^{20}$ cm$^{-3}$ is required to form ohmic contact [10]. MESFETs use ohmic contacts for the source and drain electrodes and Schottky contact for the gate electrode.

![Energy-band diagrams](image)

Figure 2.1 Energy-band diagrams showing a metal/semiconductor junction. (a) energy-band diagram of metal and semiconductor before contact, (b) energy-band diagram of metal in contact with semiconductor forming a Schottky contact, (c) Schottky contact with positive biased metal layer, (d) Schottky contact with negative biased metal [10].
Figure 2.2 (a) shows a cross-sectional view of a MESFET and its energy-band diagram with $V_{GS} = 0 \text{ V}$ and $V_{DS}$ is positive. The buffer/substrate is a non-conducting material. Both the source (S) and drain (D) ohmic contacts are metal on highly doped $n^+$ semiconductor. The gate (G) electrode is formed by metal on lightly doped $n$ region, the metal and the $n$-doped semiconductor forms a Shottcky barrier as shown in Figure 2.2 (b).

![Figure 2.2](image)

Figure 2.2 (a) Cross-sectional view of a MESFET and (b) energy-band diagram along the AA' cutline [10].

When $V_{GS} = 0 \text{ V}$, the depletion width is thinner than the thickness of the semiconductor layer. Therefore, the electrons form the $n^+$ source region are able to drift to the $n^+$ drain region with a positive $V_{DS}$. When a negative voltage is applied to the gate, the depletion width increases. When the $V_{GS}$ value is large enough such that the depletion edge reaches the semiconductor/buffer interface, the channel is “cut off”. The $V_{GS}$ is equal to the threshold voltage $V_T$. This is a “normally-on” device because when no gate voltage is applied, drain/source current ($I_{DS}$) can pass through the devices. A negative gate voltage $V_T$ at the gate can turn off the devices. The turn-off mechanism relies on the depletion under the gate region; hence the name depletion-mode, or D-mode MESFET [12].
There are techniques available to reshape the depletion region, including engineering the energy-band diagrams and decreasing the thickness of the channel region, such that even at $V_{GS} = 0$ the depletion edge can reach the semiconductor/buffer interface. The change in the energy-band diagram leads to a change in the threshold voltage. When a device is not conducting without gate bias voltage, this device is called “normally-off”. This type of MESFET is commonly referred as an enhancement mode device or E-mode MESFET.

A special case of MESFET is the high electron mobility transistor (HEMT). Similar to the MESFET, the gate of the HEMT is a Schottky contact. In contrast to the MESFET with an n-doped region as the channel, the current conduction in a HEMT utilizes a two dimensional electron gas (2-DEG). The 2-DEG lies underneath the gate at the interface between two materials, such as AlGaN/GaN interface.

2.1.2 GaN HEMT Fundamentals

The lattice constant for the Al$_x$Ga$_{1-x}$N alloy is [10]:

$$a = (0.3189 - 0.0077x) \text{ nm}$$  \hspace{1cm} (2.1)

The lattice constant for Al$_{0.28}$Ga$_{0.72}$N and GaN are 0.3167 and 0.3189 nm, respectively. In Figure 2.3, when the AlGaN is grown pseudo-morphically on GaN, the lattice difference creates tensile and compressive strain on AlGaN. The piezoelectric property of the materials introduces a sheet of polarization charge at the interface [13].

![Figure 2.3 The schematic atomic arrangement of AlGaN/GaN heterojunction][14].
Figure 2.4 Basic GaN HEMT structure and its energy band-diagram [15].

Figure 2.4 shows the energy-band diagram for the device under the gate region along the y-direction. Because the AlGaN and GaN regions have different electron affinities, there is a discontinuity in the energy-band at the interface as indicated by the red circle in Figure 2.4 (c). This discontinuity and the sharp conduction band bending forms a valley, which can confines electrons in a potential well. The confinement is only in the y-direction. Therefore, the electrons are free to move along the x- and z-directions (in and out of the page). This sheet of charge is a two-dimensional electron gas (2-DEG).

Applying a negative gate voltage reduces the amount of electrons at the interface. When the concentration of the electrons at the interface reaches zero, the channel is interrupted, and the HEMT is in OFF state. Applying positive gate voltage increases the electron concentration at the
interface, the amount of $I_{DS}$ is enhanced. When the threshold voltage is greater than zero, the HEMT becomes a ‘normally-off’ or E-mode device.

2.1.3 Power GaN HEMT Optimization Considerations

As explained in the last section, the surface of AlGaN layer has a sheet of polarization charge. Therefore, the device surface needs to be passivated with insulation layers such as SiN$_x$ and SiO$_2$. The electric field distribution causes the breakdown location to be at the gate edge. This location is undesired because the damage to the electrode during breakdown is irreversible and the device could be destroyed.

A gate field plate (FP) structure can be implemented to re-shape the electric field distribution and move the maximum electric field away from the gate edge. The breakdown voltage is increased and the breakdown location is away from the gate electrode. Parameters to be considered when designing a FP for GaN HEMT include the FP length, the FP distance from the AlGaN surface, and the choice of dielectric under FP [16].

Another issue with GaN HEMTs is drain current collapse at high current level. This is due to the excessive charge trapping inside AlGaN barrier. This trapping causes reliability issue for GaN HEMT working under high voltage high current conditions. Techniques such as multi-level field-plates, $n$-doped GaN cap layer or recessed gate structure can mitigate this phenomenon [17].

An important consideration of power HEMT design is to reduce the ON-resistance. Switched mode power electronic circuits utilize the HEMT as an on/off switch for large amount of current conduction current. A small increase in the ON-resistance can increase the conduction loss of switched mode power electronic circuits and decreases their efficiency. An increase in the sheet charge in the 2-DEG can decrease the ON-resistance.

E-mode HEMTs with high threshold voltage are more desirable for switched mode power applications. However, E-mode HEMTs are more difficult to fabricate than D-mode HEMTs [18]. The fabrication technology of HEMTs is also required to be compatible with silicon-based CMOS technology in order to incorporate E-mode HEMTs in modern VLSI. E-mode HEMTs can be designed with proper threshold voltage adjustment. The fundamental of threshold voltage
adjustment is to reshape the energy-band diagram under the gate electrode. The techniques include modifying the material properties of gate electrode and AlGaN barrier layer, changing the dimensions of the layers, inserting insulators under gate electrode, and implanting certain ions under gate electrode. The next section will provide a review of effective techniques that perform threshold voltage adjustment.

2.2 Techniques for Threshold Voltage Adjustment

This section reviews effective methods that can be used to adjust the threshold voltage of GaN HEMTs during fabrication. These include metal insulator semiconductor (MIS-HEMT) structure, fluoride-based plasma treatment, and recessed gate.

2.2.1 MIS-HEMT with Insulated Layer

Compare to traditional D-mode HEMT, the MIS-HEMT structure has an additional insulator layer underneath the gate. Some of the commonly used insulator materials are silicon dioxide (SiO₂), silicon, silicon nitride (SiN), Titanium dioxide (TiO₂) and aluminum oxide (Al₂O₃) [19-21].

The cross-sectional view of a basic MIS-HEMT is as shown in Figure 2.5. The major fabrication steps for the HEMT include mesa etching, source and drain ohmic contacts deposition, insulator disposition and gate formation. The typical metal systems for ohmic contact formation are Ti/Al or Ti/Al/Ni/Au [19, 20] where the traditional gate metal stack consists of Ni/Au. The insulating layer requires an extra step of photolithography when compared to conventional D-mode HEMT. This insulating layer can be deposited using electron beam evaporation (E-beam), chemical vapor deposition (CVD), or atomic layer deposition (ALD). ALD Al₂O₃ layer is well studied because of its high dielectric constant and discontinuity. The ALD method exhibits the best thickness control compared to other deposition methods [20, 21].
Gate insulating method is effective in controlling threshold voltage thanks to the high dielectric constant. However, the drawbacks of the MIS-HEMT structure are the thickness tolerance of the deposited insulator, the low saturation current ($I_{max}$) when compared to D-mode devices, and an extra photolithography step required by the insulator deposition [21]. The extra ALD step also increases the cost and the fabrication throughput.

### 2.2.2 Fluoride-Based Plasma Treatment

The fluoride ions can be introduced under the gate without decreasing the AlGaN thickness. The cross-sectional view of a fluoride-based (CF$_4$ plasma) treated HEMT is as shown in Figure 2.6. Negative charged ions can shift the threshold voltage positively because of the increase in barrier height of the AlGaN layer. With a deep fluoride implantation, the fluoride atoms can deplete the 2-DEG effectively for threshold voltage adjustment, see Figure 2.7 [22, 23].
Figure 2.7 Conduction-band diagram of (a) conventional D-mode HEMT (b) novel HEMT with CF₄ plasma treatment [22].

The fabrication steps are similar to those for the MIS-HEMT except that there is no insulator deposition but a CF₄ plasma treatment instead. The plasma treatment process and Ni/Au gate electrode formation can be achieved by the same photolithography step. The gate electrode and plasma treated region can be self-aligned [23].

The fluoride-based plasma treatment method can adjust the threshold voltage positively without degrading the saturation current nor requiring an extra photolithography step. However, plasma treatment does damage the AlGaN layer and cause reliability issues. It has been reported that an undesired negative threshold voltage shift appears after 288 hours of electrical stress. To maintain stable threshold voltage, a relatively complicated ‘dual gate’ configuration needs to be employed [24].

2.2.3 Recessed Gate

The mole fraction and thickness of AlₓGa₁₋ₓN barrier layer can affect the 2-DEG sheet charge density [14]. As a result, these two parameters can adjust threshold voltage. A gate recessed structure, as shown in Figure 2.8, is capable of adjusting the threshold voltage of GaN HEMTs positively. A decrease in the AlGaN layer thickness can reduce the carrier mobility and electron density, and increase sheet resistance as shown in Figure 2.9. The recessed gate HEMT has a
thinner AlGaN layer under the gate region to reduce the 2-DEG concentration. The disturbance of the 2-DEG can shift the threshold voltage of the HEMT in the positive direction.

![Gate recess](image)

Figure 2.8 Cross-sectional view of a recessed gate HEMT [25].

![Figure 2.9](image)

Figure 2.9 (a) Electron mobility and sheet carrier density measured at 300 K, and (b) Sheet resistance of AlGaN/GaN layer, as functions of remaining AlGaN layer thickness [26].

The first documented E-mode AlGaN/GaN HMET was fabricated on a thin AlGaN layer with Ti/Al/Ni/Au source and drain contacts and Ni/Au gate contacts [27]. This E-mode HEMT proves that the reduction in the AlGaN thickness can effectively adjust the threshold voltage. The fabrication process of the recessed gate requires one extra gate etching comparing to
conventional D-mode device. However, the lack of highly selective chemical wet-etching recipes in GaN leads to the requirement of an accurate reactive ion etching (RIE) recipe to fabricate the recessed GaN HEMT [25, 28, 29].

Similar to MIS-HEMT, the recessed gate structure requires an extra gate etching photolithography. This recessed gate structure can adjust the threshold voltage in the positive direction and suppress current collapse without any current degradation [10, 21]. However, RIE induces damages to the AlGaN layer that can increase the drain to source leakage current. Although RTA can repair this damage at 700 °C, such high temperature is not compatible with the traditional Ni/Au gate metal stack [22]. Moreover, the threshold voltage is sensitive to the etching depth at the gate, and there is no effective way to prevent etching though the entire AlGaN layer. The RIE must be carefully controlled to nanometer scale with endpoint detection or a method of ‘self-stopping’.

2.2.4 A Summary of Threshold Voltage Adjustment Methods

MIS-HEMT, F-implant HEMT, and gate recess HEMT are potential structures to achieve E-mode HEMT. There are also hybrid-structures, which combine two or more techniques that can further improve the device performance, see Figure 2.10 and Figure 2.11.

Figure 2.10 Cross-sectional view of a F-plasma treated MIS-HEMT [30].

Figure 2.11 Cross-sectional view of a recessed MIS-HEMT [31].
These structures exhibit superior electrical characteristic, but the complexity of the fabrication process is a major concern. Moreover, the increased cost of manufacturing limits the practicality and feasibility of these devices.

Table 2.1 A Summary of Aforementioned $V_T$ Adjustment Techniques [21]

<table>
<thead>
<tr>
<th>Method</th>
<th>MIS structure</th>
<th>F-plasma treatment</th>
<th>Recessed gate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Advantages</td>
<td>Low leaking current</td>
<td>High Current density</td>
<td>Suppress current collapse, no extra material involved</td>
</tr>
<tr>
<td>Disadvantages</td>
<td>Current degradation, controllability</td>
<td>Controllability, reliability, AlGaN damage</td>
<td>AlGaN damage, controllability, gate leakage</td>
</tr>
<tr>
<td>Fabrication difficulties</td>
<td>ALD</td>
<td>F-ion implant depth</td>
<td>RIE self-stop, recess depth control</td>
</tr>
</tbody>
</table>

Table 2.1 summarizes the advantages, disadvantages and difficulties of each threshold voltage ($V_T$) adjustment techniques. Combinations of these techniques seem to improve device performance and eliminate potential issues, but the cost aspect and fabrication difficulties need to be taken into consideration. Moreover, the compatibility issues of these reported techniques with silicon-based process are yet to be solved. For example, most reported processes chose to use gold for the ohmic and Schottky contact metal stack. This is clearly not compatible with silicon CMOS.

2.3 Process GaN with Silicon Compatible Technology

To integrate GaN HEMT with silicon-based circuits, the fabrication techniques and materials are analyzed. Based on the fabrication procedures discussed in Section 2.2, gold is a commonly used material in GaN fabrication because of its high work function and good current conductivity, resulting in low reverse leakage and low parasitic resistance, respectively. However, modern
CMOS technology avoids gold metal because it kills the carrier lifetimes in silicon [32]. In this section, gold-free ohmic and Schottky contacts of GaN HEMTs are reviewed.

### 2.3.1 Gold Free Ohmic Contact on GaN

The formation of ohmic contacts on GaN usually required high annealing temperatures, typically around 900 °C. The most popular metal stack for ohmic contacts is Ti/Al/Ni/Au as reviewed in previous section. The two mechanisms to form ohmic contacts are either a low Schottky barrier height or tunneling. Electrons are able to transit through the reduced Schottky barrier formed by metals with low work functions, such as aluminum (Al) and titanium (Ti). Another possibility is for electrons to tunnel through a thin Schottky barrier formed on highly doped $n$-region or on a thin AlGaN region [32-35].

A popular metal stack that can form low Schottky barrier height is titanium nitride (TiN) which can be formed by chemical reaction between Ti and GaN. The work function of TiN is smaller to that of Ti. When Ti reacts with GaN, the Ti-atoms penetrate into AlGaN layer and form a low work function barrier link with the 2-DEG through AlGaN layer. With the link of TiN between metal and 2-DEG, electrons can flow in both directions, forming an ohmic contact [36]. In order to be compatible with silicon-based fabrication technology, the use of gold in the metal stack must be eliminated. The study of new gold-free metal stacks consist of TiN/Ti/Al/Ti/TiN has attracted much attention [32].

![Figure 2.12](image.png)

Figure 2.12 A schematic representation of tunneling based ohmic contact in AlGaN/GaN heterostructures [37].
Figure 2.12 shows a schematic representation of the tunneling ohmic contact mechanism. When the distance between the metal and the 2-DEG are close enough, the probability of tunneling increases and hence the tunneling current increases [37]. A novel method of enhancing the tunneling current has been reported in 2002 by Qiao et al. [38]. The reaction between Ta and AlGaN layer under rapid thermal annealing (RTA) after metallization results in the Ta metal ‘consuming’ the AlGaN layer. Qiao et al. also mentioned that Al and Ti can form a stable phase Al₃Ti at 500 °C that does not react with AlGaN layer. The technique utilizes the ‘sinking’ phenomenon of tantalum to reduce the AlGaN barrier thickness and the stability of Al₃Ti to control the remaining AlGaN thickness. Grego et al. recently reported a self-stopping mechanism for the fabrication of a Ta/Al metal stack. In contrast to Ta/Ti/Al system, the Ta/Al system forms Al₃Ta alloy at 700 °C. The resistivity of the Ta/Al/Ta metal stack is more than 10 times larger than that for the Ta/Ti/Al system [39].

![Ohmic contacts](image)

Figure 2.13 Decreases in remaining AlGaN layer lead to decreases in contact resistivity [38].
As shown in Figure 2.13, the contacts in Qiao et al.’s experiments consist of 71 nm thick Al, 25 nm thick Ti, different layer thicknesses of tantalum: (a) 5 nm, (b) 10 nm, and (c) 50 nm. After RTA at 950 °C, the metals start to sink into the 28 nm thick AlGaN layer. The remaining AlGaN layers are 25 nm thick, 20 nm thick and all consumed for wafer (a), (b), and (c), respectively. The reduction in the AlGaN layer thickness enhances the tunneling probability. This results in an increase in conduction current and decrease in contact resistance [38].

The self-stopping Ta layer introduces the possibility of forming a new gate recessing without the need for accurate dry etching. AlTi₃ can stop the alloying of the AlGaN layer with Ta. The alloying relies on the reaction between Ta and GaN to form TaN [38]. The presence of Ga out diffuse towards the surface [40]. The possibility of using TaN as gate electrode is the focus of this thesis.

### 2.3.2 Gate Fabrication Procedures

The work functions for tantalum and aluminum are 4.25 eV and 4.28 eV, respectively [41]. They are very similar. However, these values are a bit low for forming a gate contact for GaN HEMT. Tantalum nitride (TaN) can be formed during sputtering in argon (Ar) and nitrogen (N₂) mixing gases environment. The work function of TaN varies from 4.13 eV (similar to n⁺ poly silicon) [42] to 5.05 eV (similar to p⁺ poly silicon) [43].

Different work function can be obtained with different ratio of nitrogen in the TaN film. This nitrogen ratio can be controlled by the nitrogen flow rate measure in standard cubic centimeters per minute (SCCM) during the sputtering process. Therefore, the work function of TaN can be adjusted by different nitrogen flow rate during sputtering. The work function of CVD TaN film is measured to be 5 eV and is stable up to 800 °C [43], where the sputtered TaN with flow rate of 8 to 10 sccm N₂ results in work function of 4.5 to 4.7 eV after post metal annealing (PMA) at 950 °C[44]. Therefore, TaN is a suitable gate material for GaN HEMT, but its work function and thermal stability need to be experimentally verified.
2.4 Gate Sinking Method

The gate sinking effect has been observed in GaAs and InP based HEMT at elevated temperature, this has not yet been reported in AlGaN/GaN HEMT below 400 °C for Au based contacts. There is no detectable metal inter-diffusion into AlGaN layers [45-47].

In InAlN MISHEMT structures, the gate metal Iridium (Ir)/Au can be sunk or inter-diffused into the InAlN layer during annealing at 700°C in oxygen gas environment. This annealing-induced gate sinking can increase the gate capacitance by a factor of two and therefore increasing the threshold (positive increase) [47].

Figure 2.14 Speculative Cross-sectional views of a Ta based gate electrode (a) before annealing and (b) after annealing.

It is possible to utilize the inter-diffusion of Ta metal during annealing to decrease the remaining AlGaN thickness and to adjust the threshold voltage. This process relies on the chemical reaction between metal Ta and AlGaN [38] layer using RTA in nitrogen gas rather than the more
complicated RIE method. This proposed method reduces the difficulty of forming a recessed gate and can avoid plasma damaging AlGaN layer during RIE process. Moreover, Ta and its nitride are compatible with modern silicon process and there are researches on using TaN as a substitute for poly silicon [43, 44]. Figure 2.14 (a) and (b) show speculative cross-sectional views of a proposed Ta based gate HEMT before and after annealing. After RTA, the gate Ta is expected to react with GaN and form TaN [48].

However, tantalum gate electrode has a work function of around 4.2 eV that needs to be adjusted for a more reliable Schottky barrier at the gate. During the sputtering process, both Ar and N$_2$ carrier gases are used to form TaN [44]. Its work function can vary from ~4.15 eV to ~4.7 eV. The control of the recessing depth is still need to be determined.

### 2.5 Summary

This chapter provides the background information for GaN HEMTs and their working principles. GaN on Si can form promising power devices if GaN HEMTs can be fabricated using silicon compatible techniques. At the same time, the availability of E-mode devices will also simplify the power electronic circuit designs. The first step to achieve E-mode devices is to adjust the threshold voltage of a traditional D-mode HEMT [22].

Three common ways of adjusting the threshold voltage of GaN HEMTs are analyzed in terms of their performance and fabrication difficulties. Recessed gate process is a relatively easy method except that the gate recession is typically achieved by reactive ion etching. This RIE process not only damages the AlGaN surface but also lacks a self-stopping mechanism. It is also difficult to control the etching depth in the nano-meter scale [21].

Common ways of fabricating both ohmic and Schottky contacts involve the use of gold metal. However, gold is well known to be avoided non-desirable contaminate in silicon technology. Therefore, research on gold-free GaN process is necessary. Ta and its nitride are reported to be suitable in forming both ohmic and Schottky contacts. Moreover, TaN has a similar work function to poly silicon, which is desirable in combining GaN with silicon technology [44].
Ta and its reaction with AlGaN [38] are suitable for forming recessed gate HEMTs instead of RIE. There are currently metal sinking articles in InAlN and GaAs materials [47], but none on the gate sinking of Ta/TaN on AlGaN/GaN HEMT. Therefore, it is necessary to investigate the proposed recessed gate techniques using Ta or TaN with the assistance of thermal treatment.
Chapter 3  Device Design and Experimental Set-up

In the previous chapter, several effective ways to adjust the threshold voltage of D-mode HEMTs are discussed and a gate-sinking method for GaN HEMT is proposed. There are multiple factors that can affect the threshold voltage in this device. This chapter will provide a systematic approach to optimize the design of the proposed HEMT.

Section 3.1 discusses the proposed device structure. Section 3.2 reviews a paper on ohmic contact metal systems. This forms the basis for a series of experiments to repeat the published work. Section 3.3 focuses on the design of the Schottky gate contact and the parameters that can adjust the threshold voltage. Section 3.4 provides the choice of device dimension and photomask layout.

3.1 Device Structure Design

We obtained some GaN wafer samples from The Hong Kong University of Science and Technology (HKUST) and Taiwan Semiconductor Manufacturing Company (TSMC) with sapphire substrate and silicon substrate, respectively. There are differences in layer structure between each wafer. The buffer layer, GaN layer, GaN quantum layer, AlGaN layer, and GaN cap layer are all pre-fabricated on top of the substrate. The substrate details are not provided to us, but the AlGaN and 2-DEG properties provided by TSMC and HKUST are listed in Table 3.1.

<table>
<thead>
<tr>
<th>Sample description</th>
<th>Al% of AlGaN</th>
<th>AlGaN thickness(nm)</th>
<th>Mobility (cm²/V·s)</th>
<th>N_s (10^{13} cm^{-2})</th>
<th>Substrate</th>
<th>Sample size</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSMC</td>
<td>28</td>
<td>25</td>
<td>&gt;1800</td>
<td>&gt;1</td>
<td>Silicon</td>
<td>½ of 2 inch</td>
</tr>
<tr>
<td>HKUST 1</td>
<td>28</td>
<td>18</td>
<td>1000~1150</td>
<td>1.19~1.33</td>
<td>Sapphire</td>
<td>½ of 2 inch</td>
</tr>
<tr>
<td>HKUST 2</td>
<td>27</td>
<td>21</td>
<td>1570~1850</td>
<td>1.15~1.23</td>
<td>Sapphire</td>
<td>¼ of 2 inch</td>
</tr>
</tbody>
</table>
The differences in the wafer parameters affect the electrical properties of the HEMTs. The composition of the Al in AlGaN affects the thickness of the AlGaN layer, the energy-band diagram as well as the 2-DEG concentration. These changes can affect the current density, breakdown voltage, and threshold voltage. Therefore, each wafer should only be used for the investigation of one fabrication parameter at a time such that the experimental results can be compared with each other.

Figure 3.1 Definition of the device dimensions for the proposed HEMT structure.
Figure 3.1 provides a basic structure of the proposed HEMT. The geometries of this HEMT are as labeled on the device. This device is simulated by a tool called NovaTCAD\(^1\). The HEMT is built using a GaN on silicon substrate. The thin AlN nucleation layer is first deposited on the silicon substrate to improve the material qualities [49]. A GaN buffer layer is then deposited on top of the AlN. An Al\(_{0.28}\)Ga\(_{0.72}\)N layer is then grown on top of the GaN quantum well layer. The source and drain ohmic contacts are made of Au\(^2\), and are very close to the AlGaN/GaN interface.

A group of simulation is used to investigate how the material properties of the AlGaN/GaN layer affects the electrical properties of the HEMT. The device parameters are as listed in Table 3.2. The work function for the TaN varies from 4.13 eV to 5.05 eV [44]. The work function of the gate is defined to be 4.5 eV, the average value for TaN.

<table>
<thead>
<tr>
<th>Wafer Name</th>
<th>(t_{\text{AlGaN}})</th>
<th>(\text{Al % of AlGaN})</th>
<th>(L_{\text{SG}})</th>
<th>(L_{\text{gate}})</th>
<th>(L_{\text{drift}})</th>
<th>(S/D) length</th>
<th>(t_{\text{sink}})</th>
<th>(\Phi_{\text{Gate}})</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSMC</td>
<td>25nm</td>
<td>28</td>
<td>0.7 (\mu)m</td>
<td>0.8 (\mu)m</td>
<td>5.5 (\mu)m</td>
<td>1.5 (\mu)m</td>
<td>0nm</td>
<td>4.5eV</td>
</tr>
<tr>
<td>HKUST1</td>
<td>18nm</td>
<td>28</td>
<td>0.8 (\mu)m</td>
<td>5.5 (\mu)m</td>
<td>1.5 (\mu)m</td>
<td>0nm</td>
<td>4.5eV</td>
<td></td>
</tr>
<tr>
<td>HKUST2</td>
<td>21nm</td>
<td>27</td>
<td>0.8 (\mu)m</td>
<td>5.5 (\mu)m</td>
<td>1.5 (\mu)m</td>
<td>0nm</td>
<td>4.5eV</td>
<td></td>
</tr>
</tbody>
</table>

Figure 3.2 plots the simulation results of the threshold voltages for the same structure but with different wafer parameters. The TSMC wafer has the most negative threshold voltage because it has the thickest AlGaN layer. The thick AlGaN layer leads to a higher 2-DEG concentration. Therefore, to turn off HEMTs fabricated on the TSMC wafer requires a more negative gate voltage when compared to those on the HKUST wafers. However, the TSMC device has the highest transconductance and current density as shown in Figure 3.3 and Figure 3.4. The simulation results of the breakdown voltage are compared in Figure 3.5. The forward voltage

\(^1\) A semiconductor device and technology simulation tool from Crosslight Inc. (www.crosslight.com).

\(^2\) Gold is the default ohmic contact material for GaN HEMT simulation in NovaTCAD.
blocking capabilities are different for each wafer. The TSMC wafer with the highest conductivity has the lowest breakdown voltage and the largest off-state current.

Figure 3.2 Comparisons of the threshold voltage of different wafers.

Figure 3.3 Simulated transconductance for different wafers.

Figure 3.4 Simulated IV characteristics for different wafers.

Figure 3.5 Simulated blocking characteristics for different wafers.
The breakdown location is at the edge of the gate electrodes as shown in Figure 3.6. The simulation results suggest that the electrical properties of the HEMTS are different when the wafer parameters change. Therefore, the experiments need to be designed with consideration of the differences in wafers. Due to the difference in wafer conditions, the results from the devices fabricated on each wafer are only suitable for comparison with the same wafers.

Figure 3.6 (a) Cross-sectional view of the simulated HEMT, (b) zoom-in cross-sectional view near the surface, (c) electrical field distribution at the surface with one dimensional cut (1D cut).
3.2 Ohmic Contact Metal System

A published work describes that tantalum (Ta) metal can react with AlGaN layer under rapid thermal annealing. The depth of the AlGaN consumption is proportional to the thickness of Ta layer. Qiao et al. has mentioned the AlGaN layer used in their experiment is 28 nm. The thicknesses of Ta are 5, 10 and 50 nm. The results of the ohmic contacts from 10 and 50 nm thick Ta are similar, and are better than the ohmic contacts from the 5 nm group [38].

The AlGaN thicknesses on the wafers from TSMC and HKUST are 25, 21, and 18 nm. To form ohmic contact, the thickness of the Ta should be 10 nm as reported in [38]. The choice of metal stack is as listed in Table 3.3. In this experiment, the Ta thickness is varied. The smallest value is 10 nm to increase the chance of forming ohmic contact. The 20 and 30 nm thick Ta layers are used to test the sensitivity of forming good ohmic contact. If the results from TSMC -1 to 3 are similar, then the choices of Ta thickness for different wafers are only required to be thicker than 10 nm. The TSMC -4 sample is fabricated with a Ta/Al/Ta metal system consisting of 10 nm thick Ta metal as the first layer. The comparison between the TSMC-1 and TSMC-4 samples is used to compare contact resistivity for two different metal systems.

<table>
<thead>
<tr>
<th>Wafer</th>
<th>First layer</th>
<th>Second layer</th>
<th>Third layer</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSMC -1</td>
<td>Ta 10 nm</td>
<td>Ti 25 nm</td>
<td>Al 71 nm</td>
</tr>
<tr>
<td>TSMC -2</td>
<td>Ta 20 nm</td>
<td>Ti 25 nm</td>
<td>Al 71 nm</td>
</tr>
<tr>
<td>TSMC -3</td>
<td>Ta 30nm</td>
<td>Ti 25 nm</td>
<td>Al 71 nm</td>
</tr>
<tr>
<td>TSMC -4</td>
<td>Ta 10nm</td>
<td>Al 71 nm</td>
<td>Ta 25 nm</td>
</tr>
</tbody>
</table>

The rapid thermal annealing (RTA) conditions are as listed in Table 3.4. The RTA temperatures start from a relatively low value (350 °C) which is a bit higher than the passivation temperature
at 300 °C. The temperature increment is chosen to be 100 °C from 350 to 550 °C and is then changed to 50 °C above 550 °C. Measurements of the IV curves between the metal pads are recorded after each RTA step. The purpose is to observe the gradual ‘metal sinking’ process. This will be useful for controlling the sinking depth of the gate later on. These measurements can also be used to calibrate the recipes and set-ups of facilities at Toronto Nano Fabrication Centre (TNFC). The increase in RTA temperature will be stopped once the metal pads behave like ohmic contacts.

Table 3.4 Rapid Thermal Annealing Conditions

<table>
<thead>
<tr>
<th>RTA Temperature (°C)</th>
<th>350</th>
<th>450</th>
<th>550</th>
<th>600</th>
<th>…</th>
<th>900</th>
</tr>
</thead>
<tbody>
<tr>
<td>RTA Time (s)</td>
<td>60</td>
<td>60</td>
<td>60</td>
<td>60</td>
<td>…</td>
<td>60</td>
</tr>
</tbody>
</table>

3.3 Schottky Contact Metal System

The tantalum (Ta) metal is the key for the formation of recessed gate. The work functions of tantalum and its nitride are important in determining the Schottky barrier height. During the Ta metal sputtering process, adding nitrogen into the argon gas can form TaN film. The flow rate of the nitrogen gas can affect the TaN work function [44]. Therefore, the two parameters for gate formation are nitrogen flow rate during sputtering and annealing thermal budget during metal sinking.

3.3.1 Metal Work Function Choice

The work function of Ta is around 4.25 eV [41] and the work function of TaN varies from 4.13 eV to 4.7 eV [43, 44]. Table 3.5 lists the gate electrode fabrication conditions. The experiments are designed for the HKUST1 wafers. HKUST1-1 wafer uses Ta as gate material for reference, and the HKUST1 -2 and HKUST1- 3 wafers use TaN as gate material. The gate metal thickness is set to be 200 nm. A group of simulations have been done to investigate the energy-band

---

3 The recipe for PECVD SiN needs 300 °C. Refer to Appendix C.5 Passivation with PECVD.
diagram, threshold voltage, transconductance and IV characteristics as the work function changes.

Table 3.5 Choices of Gate Electrode Fabrication

<table>
<thead>
<tr>
<th>Wafer</th>
<th>S/D metal</th>
<th>Ar flow rate (sccm)</th>
<th>N\textsubscript{2} flow rate (sccm)</th>
<th>Gate metal</th>
<th>Expected $\Phi_M$ (eV)</th>
<th>Gate thickness (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>HKUST1 -1</td>
<td>Ta/Al/Ta</td>
<td>20</td>
<td>0</td>
<td>Ta</td>
<td>4.25</td>
<td>200</td>
</tr>
<tr>
<td>HKUST1 -2</td>
<td>Ta/Al/Ta</td>
<td>20</td>
<td>2</td>
<td>TaN</td>
<td>4.5~4.7</td>
<td>200</td>
</tr>
<tr>
<td>HKUST1 -3</td>
<td>Ta/Al/Ta</td>
<td>20</td>
<td>2</td>
<td>TaN</td>
<td>4.5~4.7</td>
<td>200</td>
</tr>
</tbody>
</table>

Figure 3.7 demonstrates the energy-band diagrams for different gate metal work functions ($\Phi_M$), varying from 4.25 eV, 4.5e V to 4.7 eV. The Schottky barriers increase as the work function increases. However, the AlGaN/GaN heterostructures remains unchanged, and hence the 2-DEG concentration stays the same when $\Phi_M$ changes between 4.25 eV and 4.7 eV.

Figure 3.7 Energy-band diagram as a function of varying gate work function.
Figure 3.8 Threshold voltages stay the same as the gate work function changes between 4.25 eV and 4.7 eV.

Figure 3.9 Threshold voltage plotted in log scale.

Figure 3.8 shows that the threshold voltages remain unchanged as the metal work function change between 4.25 eV and 4.7 eV. However, changing the drain current to log scale, as shown in Figure 3.9, indicate that the off-state current level decreases as Φ_M increases. Therefore, the gate metal with higher work function is more desirable in suppressing the reverse leakage current.

3.3.2 RTA Conditions and Sinking Depths

The reaction between the Ta metal and AlGaN layer allows the gate electrodes of the HEMTs to sink into the AlGaN layer. This forms the recessed gate HEMTs with adjusted threshold voltages. However, the relationships between the gate sinking depths and the RTA conditions are difficult to simulate. Instead, simulations with the gate sinking depth using ideal RIE (no plasma induced damage to AlGaN surface) can predict the performance of the HEMTs with varying recessing depth. The following simulations are to investigate how the gate recess depth (t_sink) affects the electrical properties including energy band, 2-DEG, threshold voltage, off-state leakage current, and I_DS-V_DS characteristics. Table 3.6 lists the simulation parameters for the HEMT structure described in Figure 3.1.
Table 3.6 Simulation Parameters for Investigating RTA Conditions

<table>
<thead>
<tr>
<th>Wafer Name</th>
<th>$t_{\text{AlGaN}}$</th>
<th>Al % of AlGaN</th>
<th>$L_{SG}$</th>
<th>$L_{\text{gate}}$</th>
<th>$L_{\text{drift}}$</th>
<th>S/D length</th>
<th>$t_{\text{sink}}$</th>
<th>$\Phi_{\text{Gate}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSMC</td>
<td>25nm</td>
<td>28</td>
<td>0.7 $\mu$m</td>
<td>0.8 $\mu$m</td>
<td>5.5 $\mu$m</td>
<td>1.5 $\mu$m</td>
<td>variable</td>
<td>4.7eV$^4$</td>
</tr>
</tbody>
</table>

Figure 3.10 Cross-sectional view of the device structure (left) and its zoom-in view (right).

Figure 3.10 provides a cross-sectional view of the simulated HEMT on silicon substrate. As shown in the zoom-in surface view, the 1-D cut to examine energy-band diagram is at the gate region, and the results are as shown in Figure 3.11. The metal gate electrodes have the same work function (4.7 eV), thus the Schottky barrier heights are the same for all structures. The increase in recess depth reduces the AlGaN layer thickness under the gate region and modifies the conduction band between the AlGaN/GaN interfaces. The potential well formed due to AlGaN/GaN the heterostructures is shallower with a thinner AlGaN layer. As a result, the threshold voltages of HEMTs are changed.

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$^4$ The work function of TaN.
Figure 3.11 Energy-band diagram changes with different recessed gate depths.
The simulated threshold voltages are as plotted in linear and log scale in Figure 3.12 and Figure 3.13, respectively. As the Ta gate metal sinks into the AlGaN layer, the threshold voltages shift towards positive direction from $-5$ V to $-1.2$ V.

![Graph](image)

$V_{DS} = 5$ V TSMC wafer

Figure 3.12 Threshold voltages are shifted in the positive direction as the recessed gate depths increase.

Figure 3.13 plots the same curves in Figure 3.12 but with the drain current in log scale. The HEMT structure without any gate recess has the smallest off-state leakage current. As the AlGaN thickness decreases, the distance between the gate metal and the 2-DEG at the AlGaN/GaN interface becomes smaller. As a result, the probability for electrons to tunnel through the AlGaN layer increases and the off-state leakage current increases.
Figure 3.13 Drain currents plotted in log scale. The leakage current increases as the recess depth.

Figure 3.14 Transconductance versus gate voltage with different recessed depth.

Figure 3.14 plots the transconductance of HEMTs with different recessed gate depths. The peaks of the transconductance are shifted in the positive voltage direction with the reduction in recessed gate depth. Figure 3.15 is the $I_{DS}-V_{DS}$ curve when gate is shorted to the source. The current density seems not to be affected by the variations of recessed gate depth. The $I_{DS}-V_{DS}$ curve for the HEMT with 12 nm recessed depth has a slightly lower drain current at $V_{DS} = 5$ V because its threshold voltage is adjusted to be $-1.2$ V, the drain current has not saturated.
Figure 3.15 I-V characteristics for different recessed gate depths.

Table 3.7 lists the RTA conditions for the gate formations. The Ta group is used as the reference. The TaN groups are the experimental groups. Qiao et al. has chosen the starting RTA temperature to be 600 °C [38]. To leave some margin for experiment, the starting temperature for the gate electrode is designed to be 500 °C. The annealing condition for the third wafer HKUST1-3 is to be determined based on the measurements of HKUST1-2. After gaining a better understanding with experiments on HKUST1 wafers, suitable gate metal stacks are selected for the fabrication using the TSMC wafers to verify any experimental speculation.

Table 3.7 RTA Conditions for Gate Electrode

<table>
<thead>
<tr>
<th>Wafer</th>
<th>Gate metal</th>
<th>N\textsubscript{2} flowrate (sccm)</th>
<th>RTA 500 °C</th>
<th>RTA 600 °C</th>
<th>RTA 700 °C</th>
</tr>
</thead>
<tbody>
<tr>
<td>HKUST1-1</td>
<td>Ta</td>
<td>0</td>
<td>60s</td>
<td>60s</td>
<td>60s</td>
</tr>
<tr>
<td>HKUST1-2</td>
<td>TaN</td>
<td>2</td>
<td>60s</td>
<td>60s</td>
<td>60s</td>
</tr>
<tr>
<td>HKUST1-3</td>
<td>TaN</td>
<td>TBD</td>
<td>To be determined based on the results from HKUST1-2 (TBD)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TSMC 1-4</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
<td>TBD</td>
</tr>
</tbody>
</table>
3.4 Device Dimensions and Mask Layout Design

The dimensions of the HEMT can affect their electrical properties, including threshold voltage, saturation current and breakdown voltage. This section explains the design of HEMT dimensions followed by discussions on two parameters, the drift length and the gate length.

3.4.1 Design of Device Dimension

The photolithography facilities at TNFC are limited to 2 μm. Therefore, most dimensions are defined to be at least twice as large (5μm) to reduce any difficulty with photolithography. Figure 3.16 illustrates the HEMT structure, identifying the gate length ($L_G$), source and drain length, source and gate space ($L_{SG}$), and drift length ($L_{drift}$). Table 3.8 lists the values of the dimensions listed in Figure 3.16. The metal pad areas for all HEMTs are designed to be 100 μm × 100 μm. The source and gate spacing is 5 μm for all HEMTs. The drift length increases from 5 to 20 μm. The gate lengths are designed to be 5, 10, or 15 μm. These dimensions are selected because of the photolithography limitation. The full mask description is shown in Appendix A and B.

Figure 3.16 Cross-sectional view of a HEMT with all the important dimensions labeled.
Table 3.8 Dimensions for the HEMT Design

<table>
<thead>
<tr>
<th>Parameters</th>
<th>L$_{SG}$</th>
<th>L$_{gate}$</th>
<th>L$_{drift}$</th>
<th>S/D width</th>
<th>Source/drain length</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sizes</td>
<td>5 μm</td>
<td>2 μm (test)</td>
<td>5 μm</td>
<td>100 μm $\times$ 100 μm</td>
<td>30 μm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5 μm</td>
<td>10 μm</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>10 μm</td>
<td>15 μm</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>15 μm</td>
<td>20 μm</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

3.4.2 Electrical Property Variations as a Function of L$_{drift}$

Table 3.9 lists the dimensions defined in Figure 3.16 for the simulation experiment. The wafer for this simulation uses the parameters from TSMC wafer samples. The only variable in this group of simulations is the drift length. Increasing the drift region lengths of HEMTs can increase the breakdown voltage but at the cost of larger on-resistance. All dimensions are designed to match the mask design. The sinking depth is arbitrarily set to be 4 nm. The gate work function is 4.7 eV, same as TaN.

Table 3.9 Simulation Parameters for Varying Drift Region Length

<table>
<thead>
<tr>
<th>Wafer Name</th>
<th>t$_{AlGaN}$</th>
<th>Al % of AlGaN</th>
<th>L$_{SG}$</th>
<th>L$_{gate}$</th>
<th>L$_{drift}$</th>
<th>S/D width</th>
<th>t$_{sink}$</th>
<th>$\Phi_{Gate}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSMC</td>
<td>25nm</td>
<td>28</td>
<td>5 μm</td>
<td>15 μm</td>
<td>variable</td>
<td>100 μm</td>
<td>4 nm</td>
<td>4.7 eV</td>
</tr>
</tbody>
</table>

Figure 3.17 plots the gate voltage versus drain current curves with different drift region lengths. The threshold voltage remains unchanged as the drift region length increases. However, a longer drift region length increases the length of current path, leading to an increase in the on-resistance. The current density of a HEMT with a shorter drift region length is higher when compared to the current density of a HEMT with a longer drift region length. As shown in Figure 3.18, the
saturation current of HEMTs with different drift region length are at similar level. However, the current for a HEMT with 5 \( \mu \)m drift region length increases faster than the current of other HEMTs. This implies that the on-set of saturation is affected by the drift region length.

Figure 3.17 The threshold voltages remain the same even with different drift region length.

Equation 3.1 defines the specific on-resistance calculation method for this thesis:

\[
R_{on,sp} = \frac{V_{DS}}{I_{DS}}, V_{DS} = 1 \text{ V}, V_{GS} = 1 \text{ V}, \text{width} = 100 \ \mu \text{m} \tag{3.1}
\]

The simulated \( I_{DS} \) is in mA/mm. the calculated \( R_{on,sp} \) for HEMTs with different drift region lengths are plotted in Figure 3.19. \( R_{on,sp} \) is found to be proportional to drift region length. \( R_{on,sp} \) and breakdown voltage form an important trade-off for power transistors. The breakdown voltages of different drift length are as plotted in Figure 3.20. The gate voltage is set at −7 V to turn off the HEMT. For the HEMTs with drift lengths 5 and 10 \( \mu \)m, the simulations stop converging when drain voltage reaches 30 V. The HEMTs with \( L_{\text{drift}} \) of 15 and 20 \( \mu \)m first experience abrupt current increase at around 40 and 60 V, respectively, and then the drain current gradually increases as drain voltages reach 500 V. This indicates a leakage current path. This surface leakage path can be suppressed by the implementation of a field plate and proper passivation. However, the design of field plates is not the focus of this thesis. Future
optimization work on field plate is important to enhance the forward blocking characteristics of the HEMTs.

Figure 3.18 Drain current versus drain voltage with different drift lengths.

Figure 3.19 Specific on-resistances of HEMTs increase with the drift lengths.

Figure 3.20 Simulated breakdown voltages of HEMTs with different drift region lengths.
3.4.3 Electrical Property Changes as a Function of $L_{\text{gate}}$

Table 3.10 lists the parameters used in simulations designed to investigate the effect of varying the gate lengths. The wafer used in the simulation is based on parameters for the TSMC wafer samples. The dimensions used in this simulation are chosen from devices that will be fabricated later at TNFC. The gate sinking depth in this section is chosen to be 0 nm to estimate the threshold voltages of HEMTs without gate recessing.

Table 3.10 Parameters for Investigating the Effect of Varying the Gate Length

<table>
<thead>
<tr>
<th>Wafer Name</th>
<th>$t_{\text{AlGaN}}$</th>
<th>Al % of AlGaN</th>
<th>$L_{\text{SG}}$</th>
<th>$L_{\text{gate}}$</th>
<th>$L_{\text{drift}}$</th>
<th>S/D width</th>
<th>$t_{\text{sink}}$</th>
<th>$\Phi_{\text{Gate}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSMC</td>
<td>25nm</td>
<td>28</td>
<td>5 $\mu$m</td>
<td>variable</td>
<td>20 $\mu$m</td>
<td>100 $\mu$m</td>
<td>0 nm</td>
<td>4.7 eV</td>
</tr>
</tbody>
</table>

Figure 3.21 shows that the threshold voltage is unaffected by the change in gate length between 5 $\mu$m and 15 $\mu$m. The current density is affected by the gate length. The HEMT with a gate length of 5 $\mu$m has the highest current density. This HEMT also has the steepest slope for the drain current versus the drain voltage curves as shown in Figure 3.22. As a result, the HEMTs with shorter gate lengths (greater than 5 $\mu$m) are expected to have lower on-resistances.

![Figure 3.21](image1)

Figure 3.21 The threshold voltages are different for HEMTs with different gate length.

![Figure 3.22](image2)

Figure 3.22 The IV characteristics of HEMTs with different gate lengths.
Figure 3.23 show that the gate length does not affect the breakdown voltage of a HEMT structure without field plate. Since the increase in gate length does not enhance the forward blocking for HEMTs but contribute to on-resistance, the gate length of HEMTs should be designed to be as short as possible. As a result, a device with 2 \( \mu m \) gate length is added to the mask design to obtain a better performance. However, the 2 \( \mu m \) gate length may not be fabricated properly with the lift-off photolithography technology in TNFC.

![Figure 3.23 Simulated breakdown voltages for HEMTs with different gate lengths.](image)

### 3.5 Summary

This chapter proposes a recessed gate HEMT structure and its fabrication sequence. The experiments are designed for the wafer samples received from TSMC and HKUST. The critical parameters for ohmic contacts are the thickness of the tantalum metal and the annealing condition. The critical parameters for Schottky contacts are nitrogen flow rate and annealing condition. Finally, the device dimensions including \( L_{\text{gate}} \) and \( L_{\text{drift}} \) are discussed.
Chapter 4  Device Fabrication and Experimental Results

This chapter presents the fabrication process for the proposed HEMT devices with adjusted threshold voltage. The detailed fabrication steps with critical processing parameters are discussed in the following sections. In addition, the measured electrical properties of ohmic contacts, the Schottky contacts and the proposed HEMT will be discussed in Section 4.2, 4.3 and 4.4. The advantages and limitations of the proposed HEMT structure over the conventional recessed gate HEMT will be discussed along with the experimental results.

4.1 Fabrication Flow

The proposed device is to investigate the application of a gate sinking phenomenon to provide threshold voltage adjustment. In addition, this device is designed to be compatible with standard CMOS flow. Materials incompatible with standard CMOS are avoided in this fabrication.

Figure 4.1 is a flow chart for the proposed HEMT process. The cross-sectional views are not drawn to scale to better distinguish some of the small features. Compared to the conventional recessed gate HEMT, the proposed fabrication process requires one less gate etching step. The entire fabrication process is performed using the facilities at the Toronto Nanofabrication Centre (TNFC) with five customized photo-masks.

The wafers are diced into samples with a size of 1.2 × 1.2 cm. Each wafer provides a group of 3 to 4 samples. After dicing, the wafer samples are cleaned with piranha solution, and SC- I and II solutions\(^5\). The mesa reactive ion etching defines the active device areas as shown in Figure 4.1 (a). The ohmic contacts are either consisted of a Ta/Al/Ta or a Ta/Al/Ti metal system [38] as seen in Figure 4.1 (b). After rapid thermal annealing (RTA), the ohmic contacts consume part of the AlGaN layer as shown in Figure 4.1 (c). Gate metal is then sputtered to form Schottky contacts. This are followed by the passivation and metallization steps. Figure 4.2 shows a micrograph of the fabricated device. Figure 4.3 shows the wafer splits for the fabrication. Figure 4.4 is a photograph of a fabricated die.

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\(^5\) Refer to standard cleaning procedure in Appendix C.1.
Figure 4.1 Process steps for the proposed HEMT device.
Figure 4.2 Micrograph of the fabricated device and its cross-sectional structure.
Figure 4.3 Description of the wafer samples. Group 3 is used for the fabrication process experiments.

Figure 4.4 Photograph of one fabricated wafer sample. The mask layout is as described in Appendix A.
4.2 Ohmic Contact Experiments

The ohmic contact experiments are carried out according to the designs presented in Section 3.2. A group of TSMC wafer samples are fabricated under the same condition and annealed at the same time. The metal systems are as listed in Table 4.1. The thickness of the initial tantalum layer is different for the ohmic contacts. Wafer sample T-3 is the first to receive 10 nm layer of Ta. After this, wafer sample T-2 is loaded to the chamber and another 10 nm layer of Ta is deposited onto both wafer samples T-2 and T-3. Wafer sample T-1 is then loaded to the chamber and a final 10 nm layer of Ta is deposited onto all three wafer samples. Lastly, all three wafer samples are deposited with the rest of the metal stack consisting of Ti (25 nm thick) and Al (71 nm thick). All Ohmic contacts are sputtered in pure argon gas environment.

Table 4.1 Group 1 (TSMC wafer) Metal System for the Ohmic Contacts

<table>
<thead>
<tr>
<th>Metal system</th>
<th>T-1 (nm)</th>
<th>T-2 (nm)</th>
<th>T-3 (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ta</td>
<td>10</td>
<td>20</td>
<td>30</td>
</tr>
<tr>
<td>Ti</td>
<td>25</td>
<td>25</td>
<td>25</td>
</tr>
<tr>
<td>Al</td>
<td>71</td>
<td>71</td>
<td>71</td>
</tr>
</tbody>
</table>

The source and drain ohmic contact resistances of Ta/Al/Ti metal stack system are measured using the transmission line model (TLM) shown in Figure 4.5. All the I-V curves shown in Figure 4.6 are measured between the third and the fourth contacts. On each wafer sample, there are four identical TLM patterns as shown in Figure 4.4. The IV curves between each separation are measured once on each TLM pattern. The presented IV curves in Figure 4.6 are the average of these four measurements.
Figure 4.5 TLM mask layout for extracting the contact resistance.

Figure 4.6 (a) Resistance between ohmic contacts.

Figure 4.6 (b) Ohmic contact characteristics after annealing at 350 °C for 40 seconds.

Figure 4.6 (c) Ohmic contact characteristics after annealing at 400 °C for 40 seconds.

Figure 4.6 (d) Ohmic contact characteristics after annealing at 600 °C for 40 seconds.
In Figure 4.6 (a), the resistivity of the ohmic contacts on wafer samples T-2 and T-3 is lower than that for wafer sample T-1. This implies that the metal sinking has already taken place during the metal sputtering process. Figure 4.6 (b) shows the IV curves after annealing at 350 °C for 40 seconds in N$_2$ gas environment. The contact resistance reduces and the probability of tunneling increases for wafer samples T-2 and T-3. However, the contact resistance increases on wafer sample T-1. Figure 4.6 (c) shows the IV curves after annealing at 450 °C for 40 seconds. The contact resistances on all three wafer samples decrease and the IV curves are similar to those measured before annealing. Figure 4.6 (d) shows that the IV curves are linear after annealing at 600 °C for 40 seconds. The contacts on all three wafers are ohmic.

The above observation indicates that annealing could help the metal stack to sink into the AlGaN layer. This also increases the probability for carrier tunneling. Annealing at 450°C seems to decrease the probability of tunneling and the contacts exhibit Schottky contact behavior. Annealing at 600 °C for 40 seconds can improve the ohmic contacts. However, wafer sample T-2 has a slightly higher resistivity than wafer samples T-1 and T-3. More experiments need to be conducted in the future in order to explain this difference in resistances. Figure 4.7 shows the calculated contact resistance of wafer 1. There are eight 200 × 100 μm metal pads with incremental spacing. The calculated contact resistance is 1.08 mΩ·cm$^2$.

![Graph](image)

Figure 4.7 Contact resistance of Ta/Al/Ti system calculated to be 1.08 mΩ·cm$^2$ by using TLM method.
The IV characteristics for TSMC wafer sample 1: Ta (10 nm)/Al (71 nm)/Ti (25 nm) and TSMC wafer sample 4: Ta (10 nm)/Al (71 nm)/Ta (25 nm) system are as plotted in Figure 4.8. This verifies that the Ta/Al/Ta metal stack exhibit higher contact resistance than the Ta/Al/Ti system [39]. However, the Ta/Al/Ta system avoids the use of Ti in the fabrication.

![IV Characteristics Graph](image)

**Figure 4.8** Comparisons of ohmic contacts between Ta/Al/Ti and Ta/Al/Ta systems on TSMC wafer samples.

To sum up, the process of metal sinking into AlGaN layer starts when metal is sputtered and continues with annealing. The metal stacks used in this thesis are Ta/Al/Ta and Ta/Al/Ti. The temperature for forming ohmic contact is greater than 600 °C. Ohmic contacts need to be sputtered and annealed before Schottky gates that need lower annealing temperature.
4.3 Schottky Gate Experimental Results

This section presents the experiments for Schottky contact formation following the design in Section 3.3. Three processing parameters that can affect the threshold voltage are nitrogen flow rate during sputtering, Schottky contact metal stack choices and annealing conditions, which are discussed in order in the following sections.

4.3.1 Nitrogen Flow Rate during Sputtering

Work function of the sputtered TaN varies from 4.13 to 5.05 eV [44]. The difference in nitrogen flow rate during gate metal sputtering affects the work function for TaN, and hence the threshold voltage. This section compares two gate materials: pure Ta gate and pure TaN (N₂ flow rate = 2 sccm). A group of HKUST1 wafer samples is fabricated with the same etching and ohmic contact recipes. Table 4.2 lists the nitrogen flow rate for the sputtered 200 nm gate stacks.

<table>
<thead>
<tr>
<th>Gate stack</th>
<th>H1-1</th>
<th>H1-2</th>
<th>H1-3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Argon gas flow rate</td>
<td>20 sccm</td>
<td>20 sccm</td>
<td>20 sccm</td>
</tr>
<tr>
<td>Nitrogen gas flow rate</td>
<td>0 sccm</td>
<td>2 sccm</td>
<td>2 sccm</td>
</tr>
<tr>
<td>Annealing temperature</td>
<td>500 °C 60 s</td>
<td>500 °C 60 s</td>
<td>600 and 700 °C 60 s</td>
</tr>
<tr>
<td>Ohmic contact stacks</td>
<td>Ta/Al/Ta</td>
<td>Ta/Al/Ta</td>
<td>Ta/Al/Ta</td>
</tr>
</tbody>
</table>

Figure 4.9 shows the IV characteristics for device 15 on each wafer sample. Wafer samples H1-1 and H1-2 are annealed at 500 °C with different gate materials and therefore the threshold voltage differs from each other. The threshold voltages for wafer samples H1-1 and H1-2 are −2.5 V and −3.2 V, respectively. The leakage currents for devices on wafer samples H1-1 and H1-2 are 1
mA and 0.3 mA, respectively. The undesired leakage current at the TaN gate is three times less than the leakage current of the Ta gate after annealing at 500 °C for 60 seconds.

Figure 4.9 Comparison of different metal stacks with the same annealing temperature. Device 47: \( I_{DS} \) vs \( V_{GS} \) at \( V_{DS} = 5 \) V.

Figure 4.10 Comparison of different annealing temperatures with the same gate metal stack. Device 47: \( I_{DS} \) versus \( V_{GS} \) at \( V_{DS} = 5 \) V.
Wafer samples H1-2 and H1-3 are fabricated with the same gate metal stack, but annealed differently. Figure 4.10 shows that annealing wafer sample H1-3 at 600 °C exhibits a higher saturation current than those in wafer sample H1-2. However, the gate leakage current increases significantly. Annealing wafer sample H1-3 at 700 °C rapidly increases the undesired gate leakage current. The differences in sinking speed for Ta and TaN can be used to control the sinking process. The gate metal stack can be consisted of two layers: Ta at the bottom and TaN on top. The first layer of Ta can consume the AlGaN layer to adjust the threshold voltage and the second TaN cap layer can slow down the sinking process and migrate the leakage current.

4.3.2 Schottky Contact Metal Stacks

As discussed in previous sections, tantalum is the key metal that allows gate sinking to take place. The thicknesses of the first Ta layer are designed to be 5 nm, 10 nm and 15 nm (see Table 4.3). Using the same method mentioned in Section 4.2, the three TSMC wafer samples (fabricated with ohmic contacts) are sputtered at the same time.

<table>
<thead>
<tr>
<th>Wafer</th>
<th>Ta</th>
<th>N₂ flowrate</th>
<th>TaN</th>
<th>RTA 350 °C</th>
<th>RTA 450 °C</th>
<th>RTA 550 °C</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSMC -1</td>
<td>5 nm</td>
<td>8 sccm</td>
<td>190 nm</td>
<td>60 s</td>
<td>60 s</td>
<td>60 s</td>
</tr>
<tr>
<td>TSMC -2</td>
<td>10 nm</td>
<td>8 sccm</td>
<td>190 nm</td>
<td>60 s</td>
<td>60 s</td>
<td>60 s</td>
</tr>
<tr>
<td>TSMC -3</td>
<td>15 nm</td>
<td>8 sccm</td>
<td>190 nm</td>
<td>60 s</td>
<td>60 s</td>
<td>60 s</td>
</tr>
</tbody>
</table>

After the initial Ta sputtering in argon gas environment with a flow rate of 30 sccm, the chamber is filled with argon and nitrogen gases with flow rates of 20 and 8 sccm, respectively during the deposition of the 190 nm TaN cap layer.
Figure 4.11 Threshold voltages measured right after the gate stacks are sputtered.

Figure 4.11 shows the range of the threshold voltages on three wafer samples. The measurements are done right after sputtering without annealing. The devices under test are selected to have identical dimensions on the three wafer samples. The devices have different gate lengths and drift lengths. Figure 4.12 provides the statistical information on the threshold voltages for three Ta layer thicknesses. Some test devices are found to be physically defective after fabrication. Therefore, the numbers of devices measured are different for each wafer. The three plots illustrate that the threshold voltage distributions vary on each wafer sample. The increase in Ta thickness tends to adjust the threshold voltage in the positive direction. The median for wafer samples TSMC-1 (T-1), 2 (T-2), and 3 (T-3) are $-4.7 \, \text{V}$, $-3.6 \, \text{V}$ and $-3.2 \, \text{V}$, respectively.
This threshold voltage adjustment without annealing proves that Ta starts to sink into AlGaN layer during sputtering. The sinking depth is proportional to the thickness of the Ta layer. The second TaN (N₂ flow rate = 8 sccm) layer is capable of stopping or slowing down the sinking process. Figure 4.13 shows the IV curves of several randomly selected devices. Devices with same number have the same gate lengths and drift lengths. Devices with 5 nm thick Ta have more negative threshold voltages than the devices with 10 and 15 nm thick Ta. The sinking
process is already taking places during sputtering. The sinking depth affects the threshold voltage.

Figure 4.13 $I_{DS}$-$V_{GS}$ characteristics at $V_{DS} = 5$ V for different device gate lengths and drift lengths.
4.3.3 Anneal-Assisted Gate Sinking

After measuring electrical properties, wafer samples T-1, T-2, T-3 and another wafer sample T-4 (the one with Ta/Al/Ta ohmic contact), fabricated separately with 200 nm pure Ta gate, are passivated using PECVD to grow 300 nm thick silicon nitride at 300 °C for 30 minutes. The device characteristics before and after passivation are similar.

![Threshold voltage comparison before and after passivation](image)

**Figure 4.14** Threshold voltage comparison before and after passivation.

Figure 4.14 shows that after passivation, the variance of the threshold voltages decreases while the mean and median stay the same. For wafer sample T-2 (10 nm thick Ta), there is an approximately $+0.5$ V of $V_T$ shift. After passivation, some devices on the T-3 wafer sample exhibit a large leakage current in mA range. Figure 4.15(a) and (b) shows the $I_{DS}$ versus $V_{GS}$ characteristics of devices with 10 and 15 nm layer of Ta at the gate, respectively. The device with 15 nm of Ta exhibits a large reverse leakage current. Devices with leakage currents in the mA range are excluded from the comparisons.
Figure 4.15 An increase in gate leakage after passivation. $I_{DS}$ versus $V_{GS}$ at $V_{DS} = 5$ V.

The main reason for the elimination is the leakage current of 15 nm group increases from μA range to mA range. Such undesired gate leakage is caused by over sinking the gate. If Ta consumes too much AlGaN, the remaining AlGaN will be thin. Hence, the barrier width is small, and the gate tunneling probability increases. This large gate leaking current makes the device unable to turn off. When the gate leakage current increases, the threshold voltage is difficult to be determined.

It is expected when the Ta layer consumes too much of AlGaN layer, the gate will start to conduct current. Hence, a precise control of the sinking depth is crucial for the proposed device and this can be achieved by controlling the Ta layer thickness and annealing temperature. The conventional RIE technique is relatively difficult to etch precisely in nanometer scale. Because the leakage current is in mA range and the ON/OFF ratio for these leaky devices is less than 5, devices with leakage in mA range are excluded from Figure 4.14 and future comparisons.

After passivation and metallization, the wafer samples are annealed sequentially at 350, 450, and 550 °C for 60 seconds. Figure 4.16 shows the range of threshold voltages for all four wafer samples. The four plots show that the threshold voltage shifts in the positive direction as annealing temperature goes up. Some test devices are found to be either physically defective or
have large leakage. More than 50% of leaky devices are found on wafer samples T-2 and T-3. As shown in Figure 4.17, the turn-off current is 50% of the turn-on current at $V_{DS} = 5$ V. The leakage current of a normal device, as shown in Figure 4.18, is in μA range.

![Figure 4.16 Threshold voltage comparisons between different annealing temperatures.](image-url)
Figure 4.17 Wafer samples T-3, device 65 has large leakage current when annealed at 450° C.

Figure 4.18 $I_D$ versus $V_G$ at $V_{DS} = 5$ V for device 59.
4.4 Additional Electrical Properties

Figure 4.19 to Figure 4.21 show the output characteristics of the fabricated HEMT on TSMC wafer sample T-2 device 28 annealed 350°C for 60 seconds comparing to a simulated device with the same dimension and similar threshold voltage on the TSMC wafer sample. The parameters for the measured device are listed Table 4.4 and the parameters for simulated devices are listed in Table 4.5. The comparison between the measured data and simulated data is summarized in Table 4.6.

Table 4.4 Dimensions for Device 28 on Wafer Sample TSMC-2

<table>
<thead>
<tr>
<th>Wafer Name</th>
<th>( t_{\text{AlGaN}} )</th>
<th>Al % of AlGaN</th>
<th>L_SG</th>
<th>L_gate</th>
<th>L_drift</th>
<th>S/D width</th>
<th>Gate</th>
<th>RTA</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSMC-2 device 28</td>
<td>25 nm</td>
<td>28</td>
<td>5 μm</td>
<td>15 μm</td>
<td>20 μm</td>
<td>100 μm</td>
<td>Ta(10nm) TaN(190nm)</td>
<td>350°C 60 s</td>
</tr>
</tbody>
</table>

Table 4.4 list the dimensions for device 28 fabricated on wafer sample TSMC-2. The gate metal stacks for this device include 10 nm thick Ta layer and 190 nm thick TaN layer. The results are measured after annealing at 350 °C for 60 seconds. Because the measured threshold voltage is around −3 V, the metal gate sinking depth for simulation is chosen to be 4 nm, and the simulated \( V_T \) is also around −3 V. Other simulation parameters (listed in Table 4.5) are the same with those in the measured device. The work function for gate metal is 4.7 eV in the simulation, assuming that it is the same as the TaN gate.

Table 4.5 Dimensions for Simulated Device as a Comparison to TSMC-2 Device 28

<table>
<thead>
<tr>
<th>Wafer Name</th>
<th>( t_{\text{AlGaN}} )</th>
<th>Al % of AlGaN</th>
<th>L_SG</th>
<th>L_gate</th>
<th>L_drift</th>
<th>S/D width</th>
<th>( t_{\text{sink}} )</th>
<th>( \Phi_{\text{Gate}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSMC</td>
<td>25 nm</td>
<td>28</td>
<td>5 μm</td>
<td>15 μm</td>
<td>20 μm</td>
<td>100 μm</td>
<td>6 nm</td>
<td>4.7 eV</td>
</tr>
</tbody>
</table>
Figure 4.19 compares the simulated threshold voltage with the measured data. The simulation result shows a slightly more positive threshold voltage, $-3.2 \text{ V}$ comparing to the measured threshold voltage $-3.4 \text{ V}$. The drain currents at $V_{GS} = 0 \text{ V}$ are different between simulation and measurement. Figure 4.20 compares the $I_{DS} - V_{DS}$ characteristics between simulations and measurements. Due to the difference in threshold voltage, the saturation currents of measurements are larger than of the simulated values. The simulation results also exhibit a large gate leakage current when the gate voltage becomes positive. This is also observed in measurement, but the absolute value of the leakage current is smaller in the measurement. This could be due to the difference in tunneling probabilities between the actual device and the CAD simulation.

![Figure 4.19 $I_{DS}$ vs $V_{GS}$ at $V_{DS} = 5 \text{ V}$.](image1)

(a) Simulation  
(b) Measurement

Figure 4.20 Simulated and measured $I_{DS}$ vs $V_{DS}$ characteristics.
Figure 4.21 illustrates the breakdown voltages. The simulated breakdown voltage is 490 V while the measured breakdown voltage is only 62 V. However, zooming into the 0 to 140 V range, an abrupt drain current increase is observed at around 60 V as shown in Figure 4.21 (b). The power dissipation at 60 V is around 200 mW. Because of the lack of field plate and other breakdown voltage enhancement techniques, this power is located at a spot near the edge of gate electrode. This leads to the damage of the gate electrode, and the drain current increases abruptly with the lost gate control.

(a) Simulated breakdown voltage  
(b) Zoom in to 0 to 140 V range  
(c) Measured breakdown voltage

Figure 4.21 Breakdown voltages measured at $V_{GS} = -7$ V. (a) and (b) are simulated breakdown voltages (c) is the measured result.
Table 4.6 Comparison between Simulation and Experimental Results

<table>
<thead>
<tr>
<th></th>
<th>$V_T$ (V)</th>
<th>BV (V)</th>
<th>Recessed depth</th>
<th>Annealing temp</th>
<th>$R_{on,sp}$ (Ω·mm)$^6$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simulation</td>
<td>-3.2</td>
<td>52</td>
<td>6 nm</td>
<td>NA</td>
<td>41</td>
</tr>
<tr>
<td>Experiment</td>
<td>-3.4</td>
<td>62</td>
<td>NA</td>
<td>350 °C</td>
<td>36</td>
</tr>
</tbody>
</table>

Table 4.6 summarizes comparisons between simulated and experimental electrical properties for two HEMTs with similar parameters. The experimentally obtained breakdown voltage is lower than simulation results because the fabricated device breakdown location is at gate edge without any breakdown voltage optimization. Therefore, the gate electrode is damaged while blocking a high voltage. The measured $R_{on,sp}$ is larger than simulation results because the wires and probes used contribute to parasitic resistances. The simulation HEMT has electrical properties close to measurements of device 28 on TSMC-2 wafer except for breakdown voltage. Therefore, the sinking depth for this device is speculated to be approximately 6 nm after RTA at 350 °C for 60 seconds.

4.4.1 Electrical Characteristics as a Function of Drift Length

Table 4.7 lists dimensions of devices under test. The only variable is the drift region length as defined in Section 3.1. The electrical properties to be investigated are the threshold voltage, transconductance, drain current, and breakdown voltage.

Table 4.7 A Summary of Dimensions of Device under Test to Investigate Drift Length

<table>
<thead>
<tr>
<th>Wafer Name</th>
<th>$t_{AlGaN}$</th>
<th>Al % of AlGaN</th>
<th>L$_{SG}$</th>
<th>Gate stack</th>
<th>L$_{gate}$</th>
<th>L$_{drift}$</th>
<th>S/D width</th>
<th>RTA</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSMC-2</td>
<td>25 nm</td>
<td>28</td>
<td>5 μm</td>
<td>Ta(10 nm) /TaN</td>
<td>15 μm</td>
<td>variable</td>
<td>100 μm</td>
<td>350° C 60 s</td>
</tr>
</tbody>
</table>

$^6$ Refer to equation 3.1
As the drift region length increases, the specific on-resistance is also expected to increase. Figure 4.22 shows that the threshold voltage remains the same for different drift region lengths. At the same time, the saturation current and transconductance decrease as drift length increases.

![Figure 4.22 Threshold voltage and transconductance at $V_{DS} = 5\, \text{V}$, as a function of $L_{\text{drift}}$.](image1)

The green triangle dashed line ($L_{\text{drift}} = 10\, \mu\text{m}$) does not follow the predication and it also exhibits a large off leakage current compared to other plots. The speculation is that the gate metal sinks too deep such that the gate tunneling current significantly affects the electrical properties. It can be foreseen that the saturation current for the case with $L_{\text{drift}} = 10\, \mu\text{m}$ will be larger than other groups because of the gate tunneling current flowing to the drain.

The $I_{DS}$ vs $V_{DS}$ characteristics at $V_{GS} = 1\, \text{V}$ is as shown in Figure 4.23. As the drift region length increases, the saturation current decreases because of the increased parasitic resistances. However, the current of the device with $10\, \mu\text{m} L_{\text{drift}}$ (the green triangle dashed line) is greater than that of the device of $5\, \mu\text{m} L_{\text{drift}}$ (the red cross solid line). This is caused by the large gate leakage current as mentioned before. This gate leakage should also affect the breakdown behavior of the HEMTs.
Figure 4.23 Drain current versus drain voltage when gate voltage is 1 V as a function of $L_{\text{drift}}$.

Figure 4.24 Breakdown voltage as a function of drift length.
Figure 4.24 shows that the breakdown voltage increases with increasing drift length. As explained before, the device with 10 µm $L_{\text{drift}}$ is affected by its large gate leakage current and therefore does not follow the trend of the other three devices. The breakdown voltages for all devices are relatively low because these devices are not yet optimized to achieve high breakdown voltage. Moreover, the breakdown locations of these devices are found to be at the edge of the gate electrode. Once the device breakdown, the gate is defected and the device does not behave like a HEMT.

### 4.4.2 Electrical Characteristics as a Function of Gate Length

Table 4.8 lists the dimensions of the devices under test. The only variable is the gate length as defined in Section 3.1. The electrical properties to be investigated are the threshold voltage, transconductance, and drain current.

<table>
<thead>
<tr>
<th>Wafer Name</th>
<th>$t_{\text{AlGaN}}$</th>
<th>Al % of AlGaN</th>
<th>$L_{\text{SG}}$</th>
<th>$L_{\text{gate}}$</th>
<th>$L_{\text{drift}}$</th>
<th>S/D width</th>
<th>RTA</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSMC-1</td>
<td>25 nm</td>
<td>28</td>
<td>5 µm</td>
<td>variable</td>
<td>15 µm</td>
<td>100 µm</td>
<td>No annealing</td>
</tr>
</tbody>
</table>

Figure 4.25 shows the threshold voltages of GaN HEMT as a function of the gate length. There is no obvious change in threshold voltage with different gate lengths. The saturation current and transconductance are larger when the gate length is smaller. These gate lengths are designed in micrometer range due to the limitation of the fabrication facilities. The relatively long gate length increases the channel length of the HEMT, and therefore increases the total resistance of the current path. The long channel length has a negative impact on saturation current as shown in Figure 4.26.
Figure 4.25 Threshold voltage and transconductance at $V_{DS} = 5$ V, as a function of $L_{gate}$.

Figure 4.26 Drain current versus drain voltage when gate voltage is 1 V as a function of $L_{gate}$. 
4.5 Summary

This chapter provides the fabrication process flow of the proposed recessed gate HEMT and the justification of each step. The process uses silicon compatible techniques and allows this proposed device to be incorporated in modern CMOS integrated circuit. The techniques of threshold voltage adjustment are also experimented.

Since the design aims for threshold voltage adjustment, other techniques such as breakdown location adjustment and $R_{on,sp}$ improvement are not optimized. The turn-off leakage current is also significant due to the limitation of the design. However, the threshold voltage adjustment is experimentally verified. The measured threshold voltage adjustments are in good agreement with the simulation results.
Chapter 5   Conclusions and Future Work

In this thesis, the threshold adjustment for AlGaN/GaN based HEMT is investigated, and an effective way to shift threshold voltage is introduced and verified experimentally. This chapter provides a summary for this thesis and some suggestions for future work.

5.1 Thesis Contributions

GaN on silicon creates the possibility to replace silicon power MOSFET in power circuit. Therefore, the fabrication techniques of GaN HEMT need to be compatible with silicon technology. Compared to conventional D-mode GaN HEMT, the E-Mode GaN HEMT is more suitable for IC design. Threshold voltage adjustment is the first step to develop E-mode HEMT. There are three common methods to adjust threshold voltage: MIS-HEMT structure, fluoride-based plasma treatment, and recessed gate structure. Each method has its drawbacks and requires optimizations.

The traditional RIE method to form recessed gate structure suffers the uncontrollability of the etching depth. This work focuses on the use of a ‘gate-sinking’ method to achieve positive threshold voltage shift. This proposed method reduces the difficulty of forming a recessed gate using precise nanometer scale etching techniques. The process comparisons between RIE method and ‘gate sinking method’ are listed in Table 5.1 below. The proposed method not only eliminates the gate RIE step but also provides a self-stopping mechanism based on different inter-diffusion conditions between for Ta and TaN.

The effectiveness of the proposed threshold adjustment technique is verified experimentally. The fabricated HV GaN HEMTs exhibit a threshold voltage shift from −5 V (with no gate sinking) to −2 V (after gate sinking). The device dimensions that affect the electrical properties such as saturation current, transconductance and breakdown voltage have been discussed and confirmed by measurements.
Table 5.1 Fabrication Procedures for Recessed Gate HEMT

<table>
<thead>
<tr>
<th>Step</th>
<th>RIE method</th>
<th>Proposed method</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Mesa etching</td>
<td>Mesa etching</td>
<td>Device isolation</td>
</tr>
<tr>
<td>2</td>
<td>Ohmic contact (Au based)</td>
<td>Ohmic contact (Ta based)</td>
<td>Form source and drain</td>
</tr>
<tr>
<td>3</td>
<td>Etch recessed gate</td>
<td>N/A</td>
<td>Form recessed gate structure</td>
</tr>
<tr>
<td></td>
<td>Deposit gate (Au based)</td>
<td>Deposit gate (Ta/TaN)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>RTA</td>
<td>RTA (inter-diffusion)</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Passivation and metallization</td>
<td>Passivation and metallization</td>
<td>Passivation and field plate</td>
</tr>
</tbody>
</table>

5.2 Suggestions for Future Work

This proposed recessed gate HEMT will need further optimization of the device dimensions and field plate structures to further improve the trade-offs between BV and $R_{on,sp}$.

Another focus may be to combine this ‘gate sinking’ method with MIS-HEMT structure to mitigate gate leakage current. A more complicated gate metal stack with RTA in oxygen gas may be used to form an oxide layer at the gate. A potential Ta/Metal/Ta stack can be used to form a gate electrode with an in-situ dielectric layer. The first Ta layer is sputtered in pure argon gas to perform the gate sinking process. The second Metal (possibly Al) can be sputtered in oxygen rich environment to form a layer of insulator within gate. The last Ta metal is sputtered in nitrogen rich environment to form the self-stopping TaN layer. Other deposition techniques such as CVD, ALD, and E-beam can also be considered.
References


Appendices

The appendices have the following documents: full mask layout plan, device design split, and detailed fabrication recipes.

Appendix A: Mask Layout

Appendix A includes the detailed photo mask layout.

Figure A1. Mask 1 for RIE.
Figure A2. Mask 2 for ohmic contact formation.
Figure A3. Mask 3 for Schottky contact formation.
Figure A4. Mask 4 for contact hole opening.
Figure A5. Mask 5 for metallization.
Appendix B: Full Device Description

Appendix B includes the detailed device design split. All units are in μm. The number indicates the device number.

Table B1. TLM and Diode Dimension

<table>
<thead>
<tr>
<th>TLM device number</th>
<th>Metal pad width</th>
<th>Metal pad length</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>200</td>
<td>100</td>
</tr>
<tr>
<td>2</td>
<td>100</td>
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</tr>
<tr>
<td>3</td>
<td>200</td>
<td>100</td>
</tr>
<tr>
<td>4</td>
<td>100</td>
<td>100</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Diode device number</th>
<th>Junction length</th>
<th>Length</th>
<th>Width</th>
</tr>
</thead>
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<tr>
<td>5</td>
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<td>200</td>
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<td>12</td>
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<td>100</td>
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Figure B1. Definitions of TLM metal pad length and width.

Figure B2. Definitions of diode length, width and junction length.
Table B2. Single HEEMT Dimension 1

<table>
<thead>
<tr>
<th>Single HEMT device number</th>
<th>Gate length</th>
<th>S to G space</th>
<th>Drift Length</th>
<th>Gate/mesa overlap</th>
<th>Pad size</th>
<th>S/D length</th>
</tr>
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<td>13</td>
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Figure B3. Single HEMT dimension definition 1.
Figure B4. Single HEMT dimension definition 2.

Table B4. Circular HEMT Dimensions

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Figure B5. Dimensions of the circular HEMT.

Table B5. Circular Diode Dimensions

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Figure B6. Dimensions of circular diode.
Appendix C Fabrication Details

Appendix C presents the detailed fabrication recipes. These recipes were initially provided by Dr. Edward Hua Ping Xu from the Toronto Nanofabrication Centre (TNFC). They are modified during the device fabrications.

Appendix C.1 Standard Cleaning

The standard cleaning procedure requires Piranha clean, SC-I and SC-II recipes. Piranha clean recipe consists of Sulfuric acid which can get rid of organics, as shown in Figure C1. SC-I and SC-II clean procedures are used to wash off any oxide or metal.

Figure C1. Flowchart for Standard cleaning procedure used in this thesis.
Wafers are first placed in freshly made Piranha cleaning solution, consisting of \( \text{H}_2\text{SO}_4 \) (98%): \( \text{H}_2\text{O}_2 \) = 3 : 1 for 10 minutes. Piranha clean must be made right before use, otherwise its temperature will decrease to room temperature. The solution needs to be placed in the special beaker labeled “PIRANHA”. After 10 minutes, the wafers (in a holder) is removed from the PIRANHA beaker and rinsed in DI water for 10 minutes.

The second solution used for cleaning is SC-I: \( \text{NH}_4\text{OH} \) (29%): \( \text{H}_2\text{O}_2 \): DI water = 1: 1: 5. A hotplate is used to raise the temperature of the SC-I solution to 65 °C. The wafers are placed in the heated solution for 10 minutes followed by rinsing in DI water for 10 minutes.

The third solution is SC-II: \( \text{HCl} \) \( \text{H}_2\text{O}_2 \) : DI water = 1 : 1 : 6. The cleaning procedures are similar to SC-I: 10 minutes of cleaning in 65 °C followed by 10 minutes of rinsing in DI water. The wafers will then be dipped in Acetone, isopropanol in succession. This is followed by rinsing in DI water for 5 minutes and then air dry using a Nitrogen gas gun. Every wafer sample has gone through the above standard cleaning right after they have been diced.

Appendix C.2 Photolithography

The clean water samples are first baked at 100 °C on a hot plate for 2 minutes to dehydrate before the photoresist deposition. During the photoresist spin-on process, a primer (HMDS) is first dropped onto the wafer followed by a spin at 5000 rpm for 1 minute. Positive photoresist S1818 is then dropped onto the wafer and spinned in the same manner. The wafer is then baked at 100 °C for 2 minute to harden the photoresist. The exposure time in MA4, pre-heated at 350W, is tested to be between 40 to 42 seconds for the best resolution. The exposed wafer is developed slowly in a developer solution consists of MF312: DI water = 1: 1 for 60 seconds followed by an optical inspection and post-bake at 90 °C for 1 minute.

If the exposure lines on the wafer are found to be too wide or too narrow during the inspection, the photoresist on this wafer shall be removed with acetone and the photolithography steps are repeated with adjustment to exposure time and develop time. For a light mask, if the lines are too wide then the exposure time should be longer, and narrower lines imply an over-exposure.
Appendix C.3 MESA Etching

MESA etching is used to define the separate regions for each device designed on a wafer. Deep Reactive Ion Etching (DRIE) method is chosen to remove the top AlGaN/GaN layer, and hence isolating device from the other. This is the most important step in the whole process and cannot be undone. The process is carried on with an RIE machine called “miniloc” which is reserved for non-silicon wafer etching only. Only one wafer can be etched at a time due to the reflective power minimization during etching. An example of mask layout and a targeted cross-section for a single device are as follow.

![Mask layout and cross-section](image)

Figure C2. Mask layout and the expected cross-section after MESA etching.

Before etching, the entire chamber needs to be manually cleaned with isopropanol. This is because of the fact that the previous user would have likely used a different wafer and recipe which can contaminate our wafer. After the manual cleaning, a “CLEAN RECIEPE” consists of H₂ and O₂ needs to be run before the actual etching. After the cleaning process, a test-run will be performed with the real etching recipe for plasma checking and pre-heating purpose. The recipe used to etch GaN is 20 sccm Cl₂, 10 sccm BCl, 200W ICP and 50 W RIE for 10 minutes in total. The etching schedule is as following: turned on for 100 seconds then cool down for 100 seconds then repeat till the total time reaches 600 seconds. There must be frequent cool down during the entire etching period to prevent overheating of the wafer and the photoresist.
When RIE completes, the photoresist on top of the wafer needs to be removed with acetone. The method of removal involves placing the wafer in acetone for 10 minutes and ultrasound for 1 minute. The surface should be very clean after the ultrasound step. The wafer will then go through its final standard cleaning procedures as mentioned in Appendix C.1, before contact sputtering.

**Appendix C.4 Ohmic Contact and Schottky Contact Sputtering**

Prior to the photoresist deposition, each wafer must go through standard cleaning one last time. The cleaned device will then be deposited with photoresist and exposed with Ohmic mask or Schottky mask.

For the formation of Ohmic contacts, the patterned wafer will be deposited with the following metal stack: Ta/Al/Ta or Ta/Al/Ti. The first Ta layer is to react with AlGaN surface layer to form ohmic contact. The top Ta or Ti layer is to form alloy with Al to stop the metal sinking. The metal layers are deposited at a rate of about 1.3 Å/s, 200 W DC, 25 ± 1°C and 20 sccm Ar gas. During lift-off, the wafer will be slowly washed in Acetone for 10 minutes and then be put in another beaker containing clean acetone in ultrasound for 1 minute. This whole process repeats until the wafer has only the desired metal pattern left on it. The disadvantage of this lift-off method is that some small patterns might be washed away before the entire wafer gets lift-off.

Figure C3. Mask layout and the expected cross-section for ohmic contacts.
For the formation of Schottky contacts, the patterned wafer will be deposited with Ta layer under 20 sccm Ar, followed by TaN sputtered in 20 sccm Ar and a certain amount of N\textsubscript{2} with flow rate varies from 0 to 8 sccm. Putting more nitrogen into the system raises the difficulty of plasma forming. Plasma failure happens often. Restarting the process with calculated remaining time is necessary. The wafer will then go through aforementioned lift-off process. The last metallization step follows the same procedure as the ohmic contact formation using tantalum.

![Mask layout and the expected cross-section for a Schottky contact.](image)

**Appendix C.5 Passivation with PECVD**

The SiN passivation layer is carried out using Plasma Enhanced Chemical Vapour Deposition (PECVD). The temperature for growing SiN is 300 °C with a rate of 10 nm/min. The duration is 30 minutes to achieve an expected thickness of 300 nm. The actual SiN thickness measured using a ‘profilometer’ is around 360 nm. The pattern definition of the passivation layer carried out using DRIE. The photoresist is deposited after the SiN deposition. The structure is then etched with a ‘phantom etcher’ which is reserved for the etching of silicon relater material only. Similar to the ‘Miniloc’, the etching process requires physical cleaning and the standard cleaning procedures. After a test run, the wafer can be etched with following recipe: 46 sccm SF\textsubscript{6}, 5 sccm O\textsubscript{2}, 150 mTorr pressure, 2 Torr HE backside cooling, 200 W ICP and 25 W RIE for 2 minutes in
total. The etch rate is about 200 nm/min. The simplified mask and the expected cross-sectional view are as shown in Figure C5.

Figure C5. Mask layout and the expected cross-section after passivation and metalization.

Appendix C.6 Rapid Thermal Annealing

The cleaned wafer will be annealed using Rapid Thermal Annealing (RTA) at a certain temperature for a curtain amount of time. The tested combinations are listed in Table C1.

Table C1. Rapid Thermal Annealing Recipes.

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