A Transformerless Dual Active Bridge DC-DC Converter for Point-of-Load Power Supplies

by

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A thesis submitted in conformity with the requirements for the degree of Master of Applied Science
Graduate Department of Electrical and Computer Engineering
University of Toronto

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2015

Abstract

Point-of-load (POL) power supplies contribute significantly to the overall volume, weight, and cost of many electronic devices. This comes as no surprise given the major power density limitations of the buck converter commonly used in these applications. The goal of this thesis is to present a solution which addresses these limitations. This is achieved through the proposal of a novel converter topology, referred to as a transformerless dual active bridge (DAB) dc-dc converter. The proposed converter uses an ac-link to transfer power, instead of the more conventional dc-link, since it offers a significant reduction in the volume of the bulky inductor, as well as soft switching and 50% duty cycle operation of all active devices.

The advantages of the proposed converter have been verified with a 12-3.3 V, 10 A, 0.3-1 MHz experimental prototype. The results demonstrate a reduction of approximately 50% in the volume of reactive components, while maintaining high power processing efficiency.
Acknowledgments

I would like to thank the following people for helping me reach this stage:

- My parents, Mr. Amin and Dr. Omayma, and my brothers, Tarek and Khaled, for their unconditional love and support
- My supervisor, Prof. Aleksandar Prodić, for his support, guidance, and insight
- My colleagues at the lab, Nenad, Adrian, Mahmoud, Justin, Maryam, Tim, Parth, Ahsan, Behzad, Shadi, Giacomo, Marzieh, Jordan, Samuel, Tanveer, Rafael, Tassio, Joshua, Lina, Abrar, Tom, Mia, Ivan, Caniggia, and Celso, for their friendship and support
- My colleagues at Alpha Technologies Ltd., Victor, Lucas, Wilson, Luccas, Rahul, Frank, and Brian, for their friendship and support
- Nathan Ozog and Prof. Juri Jatskevich from UBC for their inspiration and support
- Prof. Genov, Prof. Tate, and Prof. Iravani from UofT for their feedback
- UofT and Texas Instruments for their financial support
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Chapter 1

1 Introduction

Point-of-load (POL) power supplies are used in numerous electronic devices ranging from small handheld devices such as cell phones, to large warehouse sized systems such as servers. Their function is to reduce a relatively high dc bus voltage to the different levels required by various digital and analog loads, such as memories, microprocessors, and power amplifiers. POL power supplies don’t require isolation since it is achieved by the front-end converter which connects the ac power to the device. Figure 1.1 shows a block diagram of a simplified POL architecture for a typical high-end server. In general, the voltage range for POL applications can vary between 2.4-60 V for the dc bus, and 0.6-18 V for the dc loads.

![Block diagram of simplified point-of-load (POL) architecture for typical high-end server](image)

Figure 1.1: Block diagram of simplified point-of-load (POL) architecture for typical high-end server

The most commonly used converter topology in POL power supplies is the buck converter, due to its relatively low component count, simple design and control, and high efficiency for low switching frequencies. Its drawbacks, however, include a bulky output filter inductor, high switching losses due to its hard switching nature, and low duty cycle operation for high step-down conversion ratios. These factors pose a major limitation on the power density of the buck
converter, and as a consequence, the contribution of POL power supplies to the overall volume, weight, and cost of many electronic devices, is quite significant. For example, up to 30% of the overall real estate of a typical server motherboard is occupied by these power supplies [1]. The majority of that area can be accounted for by the reactive components, where the bulky output filter inductors of the buck converters are by far the largest, as shown in the example POL module of Figure 1.2.

![Synchronous buck point-of-load (POL) module](image)

Figure 1.2: Synchronous buck point-of-load (POL) module [2]

1.1 Thesis Objectives

The main objective of this thesis is to present a solution which addresses the power density limitations of the buck converter commonly used in POL power supplies. This is achieved through the proposal of a novel POL converter topology, referred to as a transformerless dual active bridge (DAB) dc-dc converter. In comparison with the buck converter, the proposed converter offers improved power density by:

a) Significantly reducing the volume of the bulky inductor

b) Operating all active devices with soft switching

c) Operating all active devices with 50% duty cycle

The second objective is to compare the proposed converter to the conventional DAB dc-dc converter [3], [4], which is commonly used in high power applications requiring galvanic isolation and bi-directional power flow. Similar to the conventional DAB converter, the proposed
converter uses two active bridges interfaced by an ac inductor. The active bridges generate square wave voltages at both ends of the ac-link, and the inductor is used as an impedance to limit power transfer. However, unlike the conventional converter, the proposed converter uses a dc-blocking capacitor instead of a transformer, and a single-phase configuration consists of two half-bridges rather than full-bridges, with the ground used as the ac-link return path. Since POL power supplies don’t require transformer isolation, this configuration is used as it offers an improvement in power density and introduces the possibility of replacing the discrete magnetic components with PCB air core components.

The final objective is to verify the advantages of the proposed converter with an experimental prototype designed for an input voltage of 12 V, an output voltage of 3.3 V, a maximum load current of 10 A, and a switching frequency of 0.3-1 MHz. The results demonstrate a significant reduction in the volume of reactive components, while maintaining high power processing efficiency.

1.2 Thesis Overview

The main content of this thesis discusses the operation and design of the transformerless DAB dc-dc converter. Chapter 2 reviews the conventional and state-of-the-art POL solutions, and explains the research motivation behind the proposed solution. Chapter 3 analyzes the proposed converter and explains its benefits. Chapter 4 describes the experimental setup and presents important results. Finally, Chapter 5 provides concluding remarks and suggests possible areas of future work.
Chapter 2

2 Previous Art and Research Motivation

Point-of-load (POL) power supplies contribute significantly to the overall volume, weight and cost of electronic devices, such as cell phones, laptops and servers. As these devices continue to improve in performance, their power demands and thus power supply requirements increase. This is resulting in larger, heavier, and more expensive power supplies, which calls for an improvement in the power density of future POL converters.

2.1 Buck Converter

The most commonly used converter topology in POL power supplies is the buck converter of Figure 2.1. It consists of a half-bridge, and a low-pass filter formed by an inductor and capacitor. The half-bridge generates a rectangular wave voltage at the switching node, \( v_x \), which is filtered by the low-pass filter to produce a dc output voltage. Figure 2.2 shows the conduction path of the buck converter during its two subintervals, and Figure 2.3 shows its main steady-state waveforms.

![Figure 2.1: Circuit schematic of buck converter](image-url)
In the targeted applications, the benefits of the buck converter include a low component count, a simple design and control procedure, and a high efficiency for low switching frequencies. Its drawbacks include a bulky output filter dc inductor (due to its large energy storage requirement), relatively high switching losses (due to its hard switching nature), and low duty cycle operation for high step-down conversion ratios, all of which pose a major limitation on its power density.
The majority of the buck converter’s volume can be accounted for by its reactive components, where the bulky output filter dc inductor is by far the largest, as shown in Figure 1.2. The reason the inductor is much larger than the capacitor is due to the fact that the energy density of capacitors can be up to a thousand times larger than that of inductors, in the targeted applications [5]. Furthermore, the reason the energy storage requirement of the inductor is large is due to the high inductance value that is required. The value of the output filter inductance of the buck converter is usually selected to limit the inductor current ripple under all operating conditions, and is equal to [6]

\[
L = \frac{1}{2\Delta i_L} V \left(1 - \frac{V}{V_g}\right) \frac{1}{f_s},
\]  

(2.1)

where \(\Delta i_L\) is the inductor current ripple, \(V\) is the output dc voltage, \(V_g\) is the input dc voltage, and \(f_s\) is the switching frequency.

In addition to requiring a large inductor, the power density of the buck converter is also limited by its high switching losses due to the hard switching of its active devices. Although the converter offers a relatively high efficiency for low switching frequencies, increasing the switching frequency in order to reduce the volume of its reactive components causes a reduction in the overall system efficiency and may lead to an unreasonable heat sink size.

Finally, since the buck converter uses duty cycle control to obtain different output voltages, high step-down conversion ratios present the practical challenges of low duty cycle control [7], and impose an additional limit on power density by limiting the practical operating frequency due to the \(t_{on}\) and \(t_{off}\) limitations of the active devices.

To summarize, the power density of the buck converter is limited by three major factors:

a) The large volume of its output filter dc inductor

b) High switching losses due to hard switching

c) Low duty cycle operation for high step-down conversion ratios
2.2 Switched-Capacitor Converters

In order to improve the power density of POL power supplies, the limitations posed by the buck converter should be addressed. Several solutions have been proposed in the past which mainly focus on reducing the volume of its reactive components. The solutions presented in [8]-[11] eliminate the bulky inductive components with switched-capacitor (SC) converters. These converters demonstrate improved power density and efficiency for a fixed conversion ratio. However, in applications that require variable conversion ratios, the SC converters experience voltage regulation issues and reduced efficiency [8]. The solutions of [11]-[13] eliminate these issues by cascading the SC and buck converters to obtain a much smaller inductor compared to the conventional buck. These benefits come at the expense of increased conduction losses and capacitive volume. Finally, the topologies of [14]-[16] eliminate the drawbacks of the cascaded converters by combining the SC and buck converters into a single hybrid structure. In order to extend on this work, the buck converters used in these architectures could potentially be replaced with the soft-switching converters described in the following section to offer further improvements in power density.

2.3 Soft-Switching Converters

Addressing the three major limitations to power density improvement of the buck converter requires a solution that offers a reduced inductor volume, soft switching, and ideally, 50% duty cycle operation. These attributes are commonly found in soft-switching dc-dc converters, such as resonant and dual active bridge (DAB) converters. Although the advantages of these converters have been recognized, they have not been widely adopted in low-to-medium power applications due to a relatively large component count, a slow dynamic response, a complex design and control procedure, and the difficulty of achieving high efficiency over a wide range of load currents and input voltages [6]. Having said that, the recent solution presented in [17] introduces an active clamp LLC resonant converter intended for POL applications. Its output voltage is regulated against load variations using a simple on/off control, and it is proposed that the converter is a good candidate for the multiple-parallel-module approach discussed in [18], in which the converter efficiency remains constant over a wide load range. Furthermore, the active clamp is used to address the voltage oscillation across its rectifier devices caused by transformer secondary-side leakage inductances and MOSFET output capacitances.
This thesis extends on this work by focusing on DAB converters since they are known to have smaller inductors compared to resonant converters [19]. In particular, a novel POL converter topology is proposed which replaces the transformer of the conventional DAB converter with a dc blocking capacitor. This allows an improvement in its power density and introduces the possibility of replacing the discrete magnetic components with PCB air core components. In comparison with the buck converter, the proposed converter is able to achieve:

a) A significant reduction in the volume of the bulky inductor

b) Soft switching of all active devices

c) 50% duty cycle operation of all active devices
Chapter 3

3 Transformerless Dual Active Bridge (DAB) DC-DC Converter

The conventional dual active bridge (DAB) dc-dc converter [3], [4], shown in Figure 3.1, is commonly used in high power applications requiring galvanic isolation and bidirectional power flow. Examples include hybrid electric vehicles (HEV) and uninterruptable power supplies (UPS). When compared to the galvanically isolated versions of the buck converter, such as the full-bridge and half-bridge isolated buck converters, the DAB converter offers several benefits. These include utilization of the isolation transformer’s leakage inductance as the main energy transfer element, smaller filter components, reduced device and component stresses, reduced switching losses due to soft switching, reduced sensitivity to system parasitics, and ultimately improved power density and efficiency [4].

Since POL converters don’t require isolation, the use of the conventional DAB converter is not practical due to the presence of a transformer which limits its power density. Therefore, the transformerless DAB dc-dc converter of Figure 3.2 is proposed. It essentially replaces the transformer of the conventional DAB converter with a dc-blocking capacitor, and uses the ground as the ac-link return path instead of the full-bridge circuit.
Although the inductor is no longer a built-in component (since it is usually built into the transformer of the conventional DAB converter), this configuration offers improved power density due to the high power density of capacitors in these applications [5]. Furthermore, the proposed configuration introduces the possibility of eliminating the heavy and expensive magnetics since it is feasible to replace a magnetic core inductor with an air core PCB inductor similar to those in [20], [21], but it is not feasible to do the same with a transformer.

The proposed converter can also be extended to a multi-phase configuration, as shown in Figure 3.3, allowing an increased power capacity, the distribution of component stresses and losses, and a reduction in the energy storage requirements of the input and output filter elements if the phases are phase-shifted from each other. In fact, the dual-phase configuration of Figure 3.4 can be controlled to operate very similar to the conventional DAB converter if the two phases are 180 degrees phase shifted from each other, such that no current flows through the ground path connecting the input and output bridges (ac-link ground).
Figure 3.4: (a) Circuit schematic of dual-phase configuration of proposed converter (b) Circuit schematic of dual-phase configuration of proposed converter represented similar to conventional DAB converter
3.1 Principle of Operation

The principle of operation of the proposed converter is quite simple. The two half-bridges generate square wave voltages at the switching nodes, \( v_x \) and \( v_y \), shown in Figure 3.5. The series capacitor blocks the dc component of these voltages, effectively creating an ac-link between the two half-bridges that only allows the flow of ac current. Finally, the ac inductor acts as an impedance and limits the power transfer through the ac-link. The converter can be seen as an inverter formed by the input half-bridge, followed by an ac-link which transfers power, followed by a rectifier formed by the output half-bridge.

The principle of operation of the conventional DAB converter is described in Appendix A for reference and comparison. Similar to the conventional DAB converter, the proposed converter uses an ac inductor. Unlike the conventional converter, it uses a dc-blocking capacitor instead of a transformer, and a single phase consists of half-bridges rather than full-bridges, with the ground used as the ac-link return path. As previously mentioned, if two phases are operated in parallel with a 180 degree phase shift between them, as shown in Figure 3.6, the converter operates more like the conventional DAB converter and ideally, no current flows through the ac-link ground. In this case, the ac square wave voltages at the differential switching nodes, \( v_p \) and \( v_s \), as well as the input and output currents, \( i_g \) and \( i \), look similar to those in the conventional DAB converter.
It is noteworthy to mention that the proposed converter is capable of providing bidirectional power flow, similar to the conventional DAB converter. This is evident in the symmetry of its configuration. However, this feature is not required for POL power supplies.

Compared to the buck converter, the proposed configuration exploits the concept of ac power transfer to achieve a significant reduction in the energy storage requirement of the inductor, reduced switching losses due to soft switching, and 50% duty cycle operation of all active devices, which eliminates the drawbacks of low duty cycle control. This comes at the expense of an increased component count, increased design and control complexity, a larger inductor peak and rms current, increased switching stress, and increased capacitive energy storage requirements.

Although the proposed converter looks similar to the series resonant dc-dc converter [6], its operation is different. The proposed converter is designed such that the ac-link impedance is dominated by the inductor at the operating frequency, while the series resonant converter is designed such that it operates near the resonant frequency of the ac-link. In general, resonant converters are known to have larger inductors compared to DAB converters [19].
3.2 AC-Link Power Transfer

The principle of ac power transfer for the proposed converter requires two ac systems which are operated at the same frequency, phase shifted from each other, and interfaced by an inductor. In this case, the two ac systems are the ac components of the square wave voltages generated by the half-bridges, and the input half-bridge leads the output half-bridge such that power is delivered to the load. There are four variables that can be used to control the amount of power flow in the proposed converter:

a) The duty cycle of the input half-bridge to control the magnitude of the input ac system

b) The duty cycle of the output half-bridge to control the magnitude of the output ac system

c) The switching frequency to control the frequency of the ac systems

d) The phase shift between the input and output half-bridges to control the relative phase shift between the ac systems

Similar to the most common operating mode of the conventional DAB converter, and for the sake of simplicity, the analysis of the proposed converter will assume a fixed 50% duty cycle for all switches, and will adjust the switching frequency and phase shift between the half-bridges to control the amount of power flow between the input and output. There are four different circuit topologies under this mode of operation. Figure 3.7 shows the conduction path of the proposed converter during all four subintervals, and shows the corresponding steady-state voltages and currents. The output of the converter has been replaced with a dc voltage source for simplification, and the following assumptions have been made:

- All components are ideal
- The converter operates as a step-down converter
- The converter operates with uni-directional power flow
- The capacitor voltage $v_{c1}(t)$ is well approximated by its dc component $V_{c1}$
Figure 3.7: Circuit schematic of proposed converter showing conduction path during all four subintervals
Table 3.1: Steady-state currents and voltages of proposed converter during all four subintervals

<table>
<thead>
<tr>
<th>Subinterval:</th>
<th>I</th>
<th>II</th>
<th>III</th>
<th>IV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time:</td>
<td>(0 &lt; t \leq D \phi T_s / 2)</td>
<td>(D \phi T_s / 2 &lt; t \leq T_s / 2)</td>
<td>(T_s / 2 &lt; t \leq (1 + D \phi)T_s / 2)</td>
<td>((1 + D \phi)T_s / 2 &lt; t \leq T_s)</td>
</tr>
<tr>
<td>Conducting switches:</td>
<td>(S_1, S_4)</td>
<td>(S_1, S_3)</td>
<td>(S_2, S_3)</td>
<td>(S_2, S_4)</td>
</tr>
<tr>
<td>(v_x(t)):</td>
<td>(V_g)</td>
<td>(V_g)</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>(v_y(t)):</td>
<td>0</td>
<td>(V)</td>
<td>(V)</td>
<td>0</td>
</tr>
<tr>
<td>(v_L(t)):</td>
<td>(V_g - V_C)</td>
<td>(V_g - V_C - V)</td>
<td>(-V_C - V)</td>
<td>(-V_C)</td>
</tr>
<tr>
<td>(i_x(t)):</td>
<td>(i_L(t))</td>
<td>(i_L(t))</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>(i_C(t)):</td>
<td>(i_L(t))</td>
<td>(i_L(t))</td>
<td>(i_L(t))</td>
<td>(i_L(t))</td>
</tr>
<tr>
<td>(i(t)):</td>
<td>0</td>
<td>(i_L(t))</td>
<td>(i_L(t))</td>
<td>0</td>
</tr>
</tbody>
</table>

The capacitor in the ac-link blocks the dc component of the square wave voltages, \(v_x\) and \(v_y\), generated by the half-bridges, such that the current flowing through the inductor is purely ac. Since the half-bridges are operated with 50% duty cycle, the dc components of \(v_x\) and \(v_y\), are \(V_g/2\) and \(V/2\), respectively, and the voltage across the blocking capacitor is

\[
V_C = \frac{1}{2}(V_g - V) \tag{3.1}
\]

The main steady-state waveforms of the single-phase and dual-phase configurations of the proposed converter under this mode of operation are shown in Figure 3.8, and the power transfer equation for the general multi-phase configuration, which is derived in Appendix B.1, is equal to:
\[ P_{out} = \frac{nV_g V}{8f_s L} D_\phi D_\phi', \quad (3.2) \]

where \( n \) is the number of phases, \( V_g \) is the input dc voltage, \( V \) is the output dc voltage, \( f_s \) is the switching frequency, \( L \) is the inductance per phase (assuming each phase has the same inductance), and \( D_\phi \) is the phase shift ratio between the input and output half-bridges defined as follows:

\[ D_\phi = \frac{T_\phi}{T_s / 2} = \frac{\phi}{\pi}, \quad (3.3) \]

and

\[ 0 \leq D_\phi \leq 1, \quad (3.4) \]

and

\[ D_\phi' = 1 - D_\phi, \quad (3.5) \]

where \( T_\phi \) is the phase shift in seconds, \( T_s \) is the switching period in seconds, and \( \phi \) is the phase shift in radians.

Compared to the buck converter, which controls the duty cycle to control the conversion ratio, all active devices of the proposed converter can be operated with 50% duty cycle for any conversion ratio. Since the power density of the buck converter for high step-down conversion ratios is limited by small duty cycle values which limits the practical operating frequency of the converter, the proposed converter offers improved power density capability by allowing higher frequency operation.
Figure 3.8: (a) Steady-state waveforms of single-phase configuration of proposed converter (b) Steady-state waveforms of dual-phase configuration of proposed converter
3.3 Soft-Switching Characteristics

The inductor current of the proposed converter is purely ac, which introduces the possibility of soft switching. Compared to the buck converter, which has an inductor current dominated by a dc component and experiences hard switching, the proposed converter allows a significant reduction in switching losses. Since switching losses limit power density improvement by limiting the practical operating frequency of the converter, the proposed converter offers improved power density capability by allowing higher frequency operation.

There are two possible methods for achieving soft switching in the proposed converter, if the switches have been realized using power MOSFETs with built-in body diodes, as shown in Figure 3.9 (a). The first method, known as zero-voltage switching (ZVS), uses a small snubber capacitance across the MOSFETs in a half-bridge, as shown in Figure 3.9 (b), and dead-time operation of the half-bridge (i.e. both MOSFETs are simultaneously off for a short period of time). The snubber capacitor ensures there is little change in the voltage across the MOSFET during its turn-off (low $dv/dt$), and the dead-time ensures the snubber capacitor is discharged to zero voltage before the MOSFET is turned on. The second method, known as zero-current switching (ZCS), does not require a snubber capacitance or dead-time operation, but is limited to the output active devices since their switching transition occurs near the zero crossing of the inductor current. Both methods depend on the inductor current value at the switching transition of the device, therefore, the operating range for soft switching of the active devices using ZVS and ZCS must be evaluated.
3.3.1 Zero-Voltage Switching (ZVS)

Figure 3.10 shows the steady-state waveforms of the inductor current and MOSFET control signals with falling edge dead-time adjustment. Both snubber capacitors and dead-time adjustment are required for ZVS operation. During the dead-time, the MOSFETs in a half-bridge are both off, but the inductor current cannot be interrupted and will therefore continue to flow through one of their body diodes. Since the inductor current is ac, it may either flow through the body diode of the MOSFET that has just switched off, or it may charge/discharge the snubber capacitors in a resonant manner until it can flow through the body diode of the MOSFET that is about to turn on. ZVS operation requires the latter. For example, consider the ZVS equivalent circuit in Figure 3.11 of the converter during the dead-time between $t_2^-$ and $t_2$. If the inductor current is positive, the snubber capacitors $C_{sn1}$ and $C_{sn2}$ are charged and discharged, respectively, in a resonant manner. Choosing an appropriate snubber capacitance ensures that there is a small
change in the voltage across switch $S_1$ during its turn-off (low $dv/dt$), thus reducing turn-off losses. Choosing an appropriate dead-time will ensure the voltage of switch $S_2$ has reached zero before it is turned on, thus enabling turn-on with ZVS. The choice of snubber capacitance affects the ZVS operating range since the energy stored in the inductor must be sufficient to charge/discharge the snubber capacitors to their required final value. The operating range for ZVS switching of the active devices, which is derived in Appendix B.2, is defined as follows:

ZVS of the input-side switches occurs when

$$D_\phi > \frac{V - V_g + 8 f_s LI_{L,\text{min}}}{2V}, \quad (3.6)$$

and ZVS of the output-side switches occurs when

$$D_\phi > \frac{V_g - V + 8 f_s LI_{L,\text{min}}}{2V_g} \quad (3.7)$$

![Figure 3.10: Steady-state waveforms of inductor current and MOSFET control signals for ZVS](image)
3.3.2 Zero-Current Switching (ZCS)

ZCS does not require snubber capacitors as shown in Figure 3.9 (a) or dead-time operation of the half-bridges as shown in Figure 3.12 because it occurs if the MOSFET is turned on when the inductor current reaches the zero crossing. For example, for switch $S_3$ to turn on with ZCS, the inductor current must be zero at time, $t_1$. The operating range for ZCS switching of the active devices is derived in Appendix B.2. ZCS switching of the input-side switches is not possible since the converter is operated as a step-down converter, and ZCS of the output-side switches occurs when

$$D_p = \frac{V_g - V}{2V_g}$$

(3.8)
3.4 Converter Mode of Operation

It is evident that ZVS of the input-side active devices is possible for most operating conditions, whereas ZCS of these devices is not possible. As for the output-side active devices, both ZVS and ZCS are possible but their range of operation depends on the phase shift between the input and output half-bridges, where the minimum phase shift for soft switching is limited as follows:

\[ D_\phi \geq \frac{V_g - V}{2V_g} \]  \hspace{1cm} (3.9)

Since ZVS of the output-side active devices requires snubber capacitors and a larger phase shift compared to ZCS (which also means higher inductor peak and rms currents), the converter will be operated with ZVS of the input-side active devices and ZCS of the output-side active devices. Therefore, the proposed converter will use snubber capacitors for the input half-bridge as shown in Figure 3.13, and dead-time operation of these switches as shown in Figure 3.14. This mode of operation requires dead-time adjustment to achieve ZVS of the input-side active devices, a fixed
phase shift to achieve ZCS of the output-side active devices, and modulation of the switching frequency to control the amount of power flow between the input and output. Finally, the power transfer equation for the general multi-phase configuration under this mode of operation can be expressed as follows:

\[ P_{\text{out}} = \frac{nV_x V}{8f_s L} D_s D_s', \]  

where the phase shift ratio is fixed as follows:

\[ D_s = \frac{V-g - V}{2V_g} \]  

![Circuit schematic of proposed converter with input half-bridge snubber capacitors for proposed mode of operation](image)

Figure 3.13: Circuit schematic of proposed converter with input half-bridge snubber capacitors for proposed mode of operation
3.4.1 Inductor Selection

Since the phase shift is fixed to achieve ZCS of the output-side active devices, the selection of the inductance value is based on the output power of the converter and the desired switching frequency range (assuming fixed input and output voltages). The inductance value must be selected for the maximum output power and minimum switching frequency since it acts as an impedance and limits power transfer. Rearranging (3.10) yields

$$L = \frac{n V_s V}{8 f_s P_{out} D_p D_q}$$  \hspace{1cm} (3.12)$$

This allows the proposed converter to have a much smaller inductance compared to the buck converter, where the inductor is used for low-pass filtering and its inductance value (2.1) is usually selected to limit the inductor current ripple under all operating conditions.
3.4.2 DC-Blocking Capacitor Selection

The selection of the dc-blocking capacitance value is based on the resonant frequency of the ac-link since the principle of operation of the proposed converter requires the impedance of the ac-link to be dominated by the inductor at the operating frequencies. Therefore, the capacitance is selected such that the resonant frequency is a decade below the minimum switching frequency of the converter, as follows:

$$f_0 = \frac{f_s}{10} = \frac{1}{2\pi \sqrt{LC}}$$  \hspace{1cm} (3.13)

Rearranging (3.13) yields

$$C = \left(\frac{10}{2\pi f_s}\right)^2 \frac{1}{L}$$  \hspace{1cm} (3.14)

3.4.3 Snubber Capacitor and Dead-Time Selection

The selection of the snubber capacitors for the input half-bridge is based on the required range for soft switching of the input-side active devices, which is derived in Appendix B.2, and results in the following equation:

$$C_{sn} = \frac{L I_{\text{min}}^2}{2 V_g V},$$  \hspace{1cm} (3.15)

where $I_{L,\text{min}}$ is the minimum inductor current required to achieve ZVS turn-on of the input-side active devices

There is a trade-off between turn-off losses and the ZVS range when it comes to selecting the snubber capacitance. A larger snubber capacitance reduces turn-off losses but it also reduces the ZVS range since the energy stored in the inductor has to be large enough to charge/discharge the snubber capacitors to their required final values.

The dead-time requirement for the input half-bridge can be approximated by assuming that the inductor current value does not change during the dead-time, and is equal to [22]
\[ t_d \approx 2C_{\text{sn}} \frac{V_g}{i_L(t_2)}, \] 

(3.16)

### 3.4.4 Output Capacitor Selection

To select the output capacitor for a required steady state voltage ripple, the capacitor ripple current of Figure 3.15 (a) is considered. The output capacitance expression is derived in Appendix B.3, and results in the following equation:

\[ C_{\text{out}} = \frac{T_s}{8\Delta v} i_L(t_2) \left( \frac{i_L(t_2) - I}{i_L(t_2)} \right)^2 \]  

(3.17)

For the same output power, the output capacitor requirement can be reduced by operating phases in parallel with a phase shift between them. For example, if two phases are operated in parallel with a 180 degree phase shift between them as shown in Figure 3.15 (b), the peak ripple current is reduced by a half which results in a significant reduction in the capacitance value. This configuration also allows the component stresses to be distributed among the components.
3.5 Converter Dynamics

In order to provide a well regulated output voltage in the presence of disturbances in the input voltage and load current, and variations in component values, a closed-loop controller needs to be designed. This requires a small-signal average model of the proposed converter. There are two commonly used methods for obtaining the small-signal model of a dc-dc converter, the averaged switched circuit method of [23] and the state-space averaging method of [24]. Both methods usually use average values calculated over one switching period and assume negligible current...
and voltage ripples. For many dc-dc converters these two methods can be used to obtain an accurate small-signal and continuous-time transfer function approximation for frequencies well below the switching frequency. However, in the case of DAB converters, the assumption of negligible current ripple is not valid because the inductor current is purely ac, and thus these methods would compute inaccurate transfer functions.

To overcome this issue, the generalized averaging technique of [25] can be used. Compared to the conventional state-space averaging method which only considers the dc term in the Fourier series, and therefore assumes negligible ripple in state variables, the generalized averaging technique includes more terms in the Fourier series to obtain a more accurate model. This is required because the inductor current is purely ac so its dc term is zero and its ripple is large. The continuous-time small-signal model of [26] shows that an accurate model of the conventional DAB converter can be obtained by using the dc term and first order terms of the inductor current and output capacitor voltage as state variables.

### 3.5.1 Generalized Average Model

Similar to the approach of [26], a third-order continuous-time state-space average model of the proposed converter shown in Figure 3.16 can be obtained using the dc and first order terms of the inductor current and output capacitor voltage as state variables. The parasitic resistance $R_p$ models the resistance of the switches, inductor, capacitor and PCB traces, referred to the ac-link. The generalized average model is derived in Appendix B.4 and results in the following equation:

$$
\frac{d}{dt} \begin{bmatrix} v_{0} \\ \frac{i_{L1R}}{i_{L1I}} \end{bmatrix} = \begin{bmatrix} \frac{1}{RC_{out}} & \frac{-2\sin(\pi d_{p})}{\pi C_{out}} & \frac{-2\cos(\pi d_{p})}{\pi C_{out}} \\ \frac{\pi L}{\cos(\pi d_{p})} & \frac{-R_p}{L} & \frac{-\omega_s}{\cos(\pi d_{p})} \\ \frac{-\omega_s}{\sin(\pi d_{p})} & \frac{\pi L}{\cos(\pi d_{p})} & \frac{-R_p}{L} \end{bmatrix} \begin{bmatrix} v_{0} \\ i_{L1R} \\ i_{L1I} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ \frac{1}{\pi L} \end{bmatrix} \begin{bmatrix} v_{g} \\ 0 \\ 0 \end{bmatrix}
$$

(3.18)
3.5.2 Small-Signal Average Model

The small-signal model average model is then obtained by considering a small perturbation in the control signal (the converter switching frequency) and the resulting deviation of state variables from their steady state values. The resulting small-signal average model is derived in Appendix B.4 and results in the following equation:

\[
\begin{bmatrix}
\frac{\Delta v_0}{\Delta i_{L1}} \\
\frac{\Delta i_{L1}}{\Delta i_{L1L}}
\end{bmatrix} = 
\begin{bmatrix}
\frac{1}{RC_{out}} - \frac{2\sin(\pi D_\phi)}{\pi C_{out}} - \frac{2\cos(\pi D_\phi)}{\pi C_{out}} \\
\frac{\sin(\pi D_\phi)}{\pi L} - \frac{R_p}{L} W_s - \frac{\cos(\pi D_\phi)}{\pi L} - \frac{R_p}{L}
\end{bmatrix}
\begin{bmatrix}
\Delta v_0 \\
\Delta i_{L1R} \\
\Delta i_{L1L}
\end{bmatrix} + 
\begin{bmatrix}
0 \\
I_{0i} \\
-I_{0R}
\end{bmatrix} \Delta \omega_s \tag{3.19}
\]

3.5.3 Control-to-Output Transfer Function

Stability analysis and controller design of power converters requires the derivation of the small-signal control-to-output transfer function. Using the small signal-model of (3.19), the control-to-output transfer function of the proposed converter is derived as follows:

\[
G_{vo}(s) = C(sI - A)^{-1}B, \tag{3.20}
\]

where
\[ A = \begin{bmatrix} \frac{1}{RC_{\text{out}}} & \frac{2\sin(\pi D_\phi)}{\pi C_{\text{out}}} & \frac{2\cos(\pi D_\phi)}{\pi C_{\text{out}}} \\ \frac{\sin(\pi D_\phi)}{\pi L} & R_p & W_s \\ \frac{\cos(\pi D_\phi)}{\pi L} & -W_s & -\frac{R_p}{L} \end{bmatrix}, \] (3.21)

\[ B = \begin{bmatrix} 0 \\ I_{0l} \\ -I_{0R} \end{bmatrix}, \] (3.22)

and

\[ C = \begin{bmatrix} 1 & 0 & 0 \end{bmatrix} \] (3.23)
Chapter 4

4 Experimental Results

In order to verify the advantages of the proposed transformerless dual active bridge (DAB) converter over the buck converter, an experimental prototype was designed, built, and tested using the setup shown in Figure 4.1. The prototype consists of a power and control board connected to an Altera DE2 board which provides digital control signals.

![Experimental setup](image)

Figure 4.1: Experimental setup

4.1 Design

Table 4.1 shows a comparison of system data for a buck converter, the proposed single-phase converter, and the proposed dual-phase converter, designed for an input voltage of 12 V, an output voltage of 3.3 V, a maximum load current of 10 A, and a switching frequency of 0.3-1 MHz. The output capacitances of all converters were selected to obtain a 1% peak-peak output voltage steady-state ripple, and the inductance of the buck converter was selected to obtain a 30% peak-peak inductor current steady-state ripple.
Table 4.1: System data for buck converter, proposed single-phase converter, and proposed dual-phase converter

<table>
<thead>
<tr>
<th></th>
<th>Buck converter</th>
<th>Proposed single-phase converter</th>
<th>Proposed dual-phase converter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage ($V_g$)</td>
<td>12 V</td>
<td>12 V</td>
<td>12 V</td>
</tr>
<tr>
<td>Output voltage ($V$)</td>
<td>3.3 V</td>
<td>3.3 V</td>
<td>3.3 V</td>
</tr>
<tr>
<td>Maximum output current ($I_{max}$)</td>
<td>10 A</td>
<td>10 A</td>
<td>10 A</td>
</tr>
<tr>
<td>Switching frequency ($f_s$)</td>
<td>0.3 MHz</td>
<td>0.3-1 MHz</td>
<td>0.3-1 MHz</td>
</tr>
<tr>
<td>Inductance ($L$)</td>
<td>2658 nH</td>
<td>116 nH</td>
<td>2x231 nH</td>
</tr>
<tr>
<td>Maximum inductor peak current ($I_{L, pk, max}$)</td>
<td>11.5 A</td>
<td>40 A</td>
<td>20 A</td>
</tr>
<tr>
<td>Maximum inductor rms current ($I_{L, rms, max}$)</td>
<td>10.04 A</td>
<td>23.1 A</td>
<td>11.55 A</td>
</tr>
<tr>
<td>Dc-blocking capacitance ($C$)</td>
<td>n/a</td>
<td>244 µF</td>
<td>2x122 µF</td>
</tr>
<tr>
<td>Dc-blocking capacitor voltage ($V_C$)</td>
<td>n/a</td>
<td>4.35 V</td>
<td>4.35 V</td>
</tr>
<tr>
<td>Output capacitance ($C_{out}$)</td>
<td>37.9 µF</td>
<td>568 µF</td>
<td>126 µF</td>
</tr>
<tr>
<td>Snubber capacitance ($C_{sn}$)</td>
<td>n/a</td>
<td>2x45.3 nF</td>
<td>4x22.7 nF</td>
</tr>
<tr>
<td>Energy storage requirement of inductors ($E_L$)</td>
<td>176 µJ</td>
<td>92.4 µJ</td>
<td>92.4 µJ</td>
</tr>
<tr>
<td>Energy storage requirement of capacitors ($E_C$)</td>
<td>0.206 mJ</td>
<td>3.1 mJ</td>
<td>3 mJ</td>
</tr>
<tr>
<td>Weighted energy storage requirement ($E_W$)</td>
<td>176 mJ</td>
<td>97.8 mJ</td>
<td>95.4 mJ</td>
</tr>
<tr>
<td>Switch stress ($S$)</td>
<td>165.7 VA</td>
<td>499.7 VA</td>
<td>499.7 VA</td>
</tr>
</tbody>
</table>
It is evident from Table 4.1, that in comparison with the buck converter, the proposed single-phase and dual-phase converters both achieve a 47.5% reduction in the energy storage requirement of the inductor. Although, the maximum peak inductor currents are 3.48 and 1.74 times larger, the required inductances are 22.9 and 11.5 times smaller, respectively. As previously mentioned, this benefit is achieved by using an ac-link to transfer power since the ac inductors in the proposed converters are used as impedances, whereas the buck converter uses a dc inductor for low-pass filtering which requires a much larger inductance value. This comes at the expense of increased capacitive energy storage requirements, but it is a tradeoff that is well justified since the energy density of capacitors can be up to 1000 times larger than that of inductors, in the targeted applications [5]. In fact, by applying this factor to calculate the weighted energy storage requirement of reactive components, it is evident that the proposed single-phase and dual-phase converters achieve a 44.4% and 45.8% reduction, respectively. Since the volume of reactive components is proportional to their energy storage requirement, this translates to a significant reduction in the volume, weight, and cost of the bulky and expensive reactive components. Another tradeoff is that the switch stress in the proposed converters is 3 times larger than that of the buck converter. Although the area occupied by the active components is proportional to switch stress, their relative volume and weight compared to reactive components are considerably small.

It is also evident that increasing the number of phases for the proposed converter leads to smaller inductor peak and rms currents, and smaller input and output filter requirements. However, this comes at the expense of an increased component count, and increased gate drive and control requirements. Given the proposed design requirements, a dual-phase solution is selected since it offers a good balance in that regard when designing a discrete prototype which requires the selection of off-the-shelf surface-mount device (SMD) components.

The power board of the prototype shown in Figure 4.2 was built using a 4-layer, FR-4, 0.062” 1 oz. cu plate printed circuit board (PCB) and the main SMD components listed in Table 4.2. The top layer of the board contains the power components, the second layer contains the power ground and is placed here for shielding, the third layer contains the control and sensing traces, and the bottom layer contains the gate drive components. The size of the power board is 5.5 cm by 9.5 cm.
Figure 4.2: (a) PCB power layer (b) Layout of PCB power layer (c) Block diagram of PCB power layer (d) PCB gate drive layer

Table 4.2: List of main components used in power board of experimental prototype

<table>
<thead>
<tr>
<th>Main components</th>
<th>Part number</th>
</tr>
</thead>
<tbody>
<tr>
<td>6 x Dual N-Channel 20 V MOSFETs</td>
<td>Vishay - Si4204DY</td>
</tr>
<tr>
<td>4 x High-side &amp; low-side 4 A gate drivers</td>
<td>TI - UCC27211</td>
</tr>
<tr>
<td>2 x MnZn shielded 250 nH inductors (efficiency results)</td>
<td>Wurth - 744309025</td>
</tr>
<tr>
<td>2 x MnZn shielded 150 nH inductors (steady-state results)</td>
<td>Wurth - 744302015</td>
</tr>
<tr>
<td>16 x Ceramic 22 µF Capacitors</td>
<td>Murata - GRM219R61A226MEA0D</td>
</tr>
</tbody>
</table>
The power switches used in the prototype are n-channel MOSFETs rated for 20 V where two MOSFETs are packaged together in a single chip. These switches were selected to simplify the design by connecting the two MOSFETs in a half-bridge configuration and to minimize parasitic stray inductances. Since the on-resistance of a MOSFET is proportional to the square of its rated voltage, and the output-side switches only need to be rated for a small voltage, two MOSFETs were connected in parallel for these switches in order to reduce their effective on-resistance. Although connecting MOSFETs in parallel leads to increased switching losses, these losses are insignificant on the secondary side due to its ZCS operation.

Ceramic capacitors were used for the dc-blocking capacitors since they offer several advantages such as low cost, low effective series resistance (ESR), low effective series inductance (ESL), and high rms current rating.

Although the inductance value required in the proposed converter is much smaller than that of the buck converter and introduces the possibility of using air core discrete or PCB inductors, magnetic core inductors were selected to allow a fair comparison.

4.2 Steady-State Results

Figure 4.3 shows the oscilloscope waveforms of the ac voltages at the differential switching nodes, $v_p$ and $v_s$, and the ac inductor currents, $i_{L1}$ and $i_{L2}$, during steady-state operation for a switching frequency of 1 MHz. It is evident that the slew rate on the primary side voltage, $v_p$, is lower than that of the secondary side, $v_s$, due to the inclusion of snubber capacitors and dead-time operation for ZVS of the input-side switches. Furthermore, the secondary side voltage is phase shifted from the primary side voltage to achieve ZCS of the output-side switches. Finally, the two phases are 180 degrees phase-shifted from each other to minimize input and output filter requirements.
Figure 4.3: Oscilloscope waveforms showing steady-state operation for a switching frequency of 1 MHz. 
f2: differential switching node voltage $v_p(t)$ 15 V/div; m1: differential switching node voltage $v_s(t)$ 10 V/div; Ch4: inductor current $i_{L1}(t)$ 10 A/div; m2: inductor current $i_{L2}(t)$ 10 A/div; Time scale is 200ns/div.

Figure 4.4 shows the oscilloscope waveforms of the gate-to-source voltages of the input and output half-bridges of a single phase. Due to ZVS operation of the input half-bridge, a significant dead-time is applied to its gating signals, and due to ZCS operation of the output half-bridge, a negligible dead-time is applied to its gating signals.

Figure 4.4: Oscilloscope waveforms showing steady-state operation for a switching frequency of 1 MHz.
m2: gate-to-source voltage $v_{gs1}(t)$ 5 V/div; Ch1: gate-to-source voltage $v_{gs2}(t)$ 5 V/div; Ch3: gate-to-source voltage $v_{gs3}(t)$ 5 V/div; Ch2: gate-to-source voltage $v_{gs4}(t)$ 5 V/div; Time scale is 200ns/div.
Figure 4.5 shows the oscilloscope waveforms of the input half-bridge switching node voltage for a single phase, \( v_{x1} \), the gate-to-source voltage of its low-side MOSFET, \( v_{gs2} \), and the inductor current of the same phase, \( i_{L1} \). ZVS of the primary side MOSFETs is achieved by adding snubber capacitances to reduce the change in their voltage during turn-off, and adjusting the dead-time such that they are switched on when their voltage reaches zero.

![Oscilloscope waveforms showing steady-state operation for a switching frequency of 1 MHz.](image)

Figure 4.5: Oscilloscope waveforms showing steady-state operation for a switching frequency of 1 MHz. Ch1: switching node voltage \( v_{x1}(t) \) 5 V/div; Ch2: gate-to-source voltage \( v_{gs2}(t) \) 5 V/div; Ch4: inductor current \( i_{L1}(t) \) 10 A/div; Time scale is 200ns/div.

Figure 4.6 shows the oscilloscope waveforms of the output half-bridge switching node voltage for a single phase, \( v_{y1} \), and the inductor current of the same phase, \( i_{L1} \). ZCS of the secondary side MOSFETs is achieved by adjusting the relative phase shift of the input and output half-bridges such that the switching transitions of the output half-bridge occur at the zero crossings of the ac inductor current.
Figure 4.6: Oscilloscope waveforms showing steady-state operation for a switching frequency of 1 MHz. Ch1: switching node voltage $v_{y1}(t)$ 2 V/div; Ch4: inductor current $i_{L1}(t)$ 5 A/div; Time scale is 200ns/div.

4.3 Efficiency Results

Figure 4.7 shows the experimental and theoretical efficiency results for the existing converter prototype, and the theoretical results for an optimized prototype design. During light loads, an improvement in the efficiency of the proposed converter is achieved by using phase-shedding techniques, such that it operates as a single-phase converter. The theoretical results for an optimized design assume moderate improvements in the experimental prototype.

Since the proposed converter offers soft switching of all active devices, increasing the switching frequency to further reduce the volume of reactive components becomes a feasible option. To reduce the conduction losses, and input and output filter requirements, increasing the number of phases is also an option. In fact, input and output current ripple cancellation may be achieved by increasing the number of phases and operating them with a relative phase shift to each other.

Figure 4.8 shows the breakdown of the converter losses for the existing prototype. The two most significant sources of losses are the conduction losses of elements in the inductor current path and the turn-off switching losses of the input-side switches. Other losses have been grouped as miscellaneous losses.
Figure 4.7: Graph showing experimental and theoretical efficiency results for the existing converter prototype, and theoretical results for an optimized prototype design

Figure 4.8: Graph showing breakdown of converter losses for experimental prototype
The elements considered for conduction losses include the on-resistances of the primary and secondary side MOSFETs, $R_{DS(on)_pri}$ and $R_{DS(on)_sec}$, the resistances of the inductors, $R_L$, the resistances of the dc-blocking capacitors, $R_C$, and the PCB trace resistances, $R_{PCB}$. The total conduction loss is then calculated as the sum of the $I^2R$ losses of these elements, as follows:

$$P_{\text{cond}} = I_{L,\text{rms}}^2(nR_{PCB} + nR_{DS(on)_pri} + nR_{DS(on)_sec} + nR_C + nR_L)$$  \hspace{1cm} (4.1)

The main switching losses occur at the turn-off of the input-side switches and are equal to [22]

$$P_{\text{sw}} = 2n\left(\frac{t_f I_{L,\text{pk}}}{12C_{sn}}\right)^2 f_s$$ \hspace{1cm} (4.2)

where $t_f$ is the fall time of the MOSFET.

The miscellaneous losses include the conduction losses due to the ESR of the input and output capacitors, the switching losses due to non-ideal ZVS and ZCS, the inductor core losses, the body diode conduction and reverse recovery losses, and the power lost in charging the secondary side MOSFET output capacitances.
Chapter 5

5 Conclusions and Future Work

This thesis presented an overview of the major limitations associated with the buck converter commonly used in point-of-load (POL) power supplies, and provides a solution which addresses these limitations. The main content of the thesis introduces a transformerless dual active bridge (DAB) dc-dc converter and outlines its principle of operation, analysis, design, and practical implementation.

5.1 Major Accomplishments

A novel POL converter topology which addresses the power density limitations of the buck converter was presented. In comparison with the buck converter, the proposed converter offers the following benefits:

a) A significant reduction in the volume of the bulky inductor

b) Soft switching of all active devices

c) 50% duty cycle operation of all active devices

In comparison with the conventional DAB dc-dc converter, the proposed converter achieves an improved power density by replacing the transformer with a dc-blocking capacitor as POL power supplies don’t require transformer isolation. This also introduces the possibility of eliminating the heavy and expensive magnetics since it is feasible to replace a magnetic core inductor with an air core PCB inductor, but it is not feasible to do the same with a transformer.

Finally, the advantages of the proposed converter were verified with an experimental prototype designed for an input voltage of 12 V, an output voltage of 3.3 V, a maximum load current of 10 A, and a switching frequency of 0.3-1 MHz. The results demonstrate a reduction of approximately 50% in the volume of reactive components, while maintaining high power processing efficiency.
5.2 Future work

Extensive research has been carried out to improve the performance of the conventional DAB converter using various modulation schemes [27]-[29]. This analysis for the proposed converter is beyond the scope of the thesis and is regarded as future work. Additional future work also includes:

- The implementation of a closed loop controller which regulates the output voltage using pulse-frequency modulation (PFM) and controls the dead-time to ensure zero-voltage switching (ZVS) of the primary side switches, and the phase shift to ensure zero-current switching (ZCS) of the secondary side switches
- Eliminating the discrete magnetic core inductor and using an air core PCB inductor
- IC implementation of the power stage and controller
References


Appendices

A Conventional DAB DC-DC Converter

A.1 Principle of Operation

The conventional dual active bridge (DAB) dc-dc converter proposed in [3], [4] is shown in Figure A.1. It consists of two active bridges which are interfaced through a transformer. Not only does the transformer provide galvanic isolation and a conversion ratio, but its leakage inductance is also used as the main energy transfer element. The most common operating mode of the DAB converter uses 50% duty cycle for all switches, and adjusts the switching frequency and phase shift between the active bridges to control the amount of power flow between the input and output. The main steady-state waveforms of the converter under this mode of operation are shown in Figure A.2, and its ideal output power is equal to [4]

\[
P_{\text{out}} = \frac{V_g V}{n \omega_s L_{lk}} \phi (1 - \left| \phi \right|) / \pi
\]

(A.1)

where \( V_g \) is the input dc voltage, \( V \) is the output dc voltage, \( n \) is the transformer turns ratio, \( \omega_s \) is the switching frequency in radians per second, \( L_{lk} \) is the transformer leakage inductance referred to the primary side, and \( \phi \) is the phase shift in radians between the input and output active bridges.

![Circuit schematic of conventional dual active bridge (DAB) dc-dc converter with main voltages and currents labeled](image-url)
Figure A.2: Steady-state waveforms of conventional DAB dc-dc converter
B Transformerless DAB DC-DC Converter

B.1 Steady-State Analysis

The assumptions for the steady-state analysis of the proposed converter of Figure B.1 are as follows:

- All components are ideal
- All switches operate with 50% duty cycle
- The converter operates as a step-down converter
- The converter operates with uni-directional power flow
- The capacitor voltage \( v_{c1}(t) \) is well approximated by its dc component \( V_{c1} \)

![Circuit schematic of proposed converter with main voltages and currents labeled](image)

Figure B.1: Circuit schematic of proposed converter with main voltages and currents labeled

The phase shift between the two half-bridges will be represented using a phase shift ratio \( D_\phi \) defined as follows:

\[
D_\phi = \frac{T_\phi}{T_s/2} = \frac{\phi}{\pi} \quad \text{(B.1)}
\]

and

\[
0 \leq D_\phi \leq 1 \quad \text{(B.2)}
\]
and

\[ D_\varphi' = 1 - D_\varphi \quad (B.3) \]

where \( T_\varphi \) is the phase shift in seconds, \( T_s \) is the switching period in seconds, and \( \varphi \) is the phase shift in radians.

The converter contains four switches, and the switches in a half-bridge (e.g. \( S_1 \) and \( S_2 \)) must not be turned on simultaneously to avoid short-circuiting the dc voltage sources. This results in a maximum of four switching combinations and thus four possible circuit topologies. All four topologies can be analyzed by operating the converter with an arbitrary phase shift ratio \( 0 < D_\varphi < 1 \).

Figure B.2 shows the conduction path of the proposed converter during all four subintervals, and Table B.1 shows the corresponding steady-state voltages and currents. The output of the converter has been replaced with a dc voltage source for simplification.

Figure B.2: Circuit schematic of proposed converter showing conduction path during all four subintervals
Table B.1: Steady-state currents and voltages of proposed converter during all four subintervals

<table>
<thead>
<tr>
<th>Subinterval:</th>
<th>I</th>
<th>II</th>
<th>III</th>
<th>IV</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time:</td>
<td>$0 &lt; t \leq D_f T_s / 2$</td>
<td>$D_f T_s / 2 &lt; t \leq T_s / 2$</td>
<td>$T_s / 2 &lt; t \leq (1 + D_f)T_s / 2$</td>
<td>$(1 + D_f)T_s / 2 &lt; t \leq T_s$</td>
</tr>
<tr>
<td>Conducting switches:</td>
<td>$S_1, S_4$</td>
<td>$S_1, S_3$</td>
<td>$S_2, S_3$</td>
<td>$S_2, S_4$</td>
</tr>
<tr>
<td>$v_x(t)$:</td>
<td>$V_g$</td>
<td>$V_g$</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$v_y(t)$:</td>
<td>0</td>
<td>$V$</td>
<td>$V$</td>
<td>0</td>
</tr>
<tr>
<td>$v_L(t)$:</td>
<td>$V_g - V_C$</td>
<td>$V_g - V_C - V$</td>
<td>$-V_C - V$</td>
<td>$-V_C$</td>
</tr>
<tr>
<td>$i_x(t)$:</td>
<td>$i_L(t)$</td>
<td>$i_L(t)$</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$i_C(t)$:</td>
<td>$i_L(t)$</td>
<td>$i_L(t)$</td>
<td>$i_L(t)$</td>
<td>$i_L(t)$</td>
</tr>
<tr>
<td>$i(t)$:</td>
<td>0</td>
<td>$i_L(t)$</td>
<td>$i_L(t)$</td>
<td>0</td>
</tr>
</tbody>
</table>

To obtain the dc component of the capacitor voltage, the principle of inductor volt-second balance is applied

$$
\langle v_L \rangle_{T_s} = \frac{1}{T_s} \int_0^{T_s} v_L(t) dt = \frac{D_f}{2} (V_g - 2V_C - V) + \frac{D_f}{2} (V_g - 2V_C - V) = 0
$$

which yields

$$
V_C = \frac{1}{2} (V_g - V)
$$

The capacitor in the ac-link blocks the dc component of the square wave voltages, $v_x$ and $v_y$, generated by the half-bridges. Since the half-bridges are operated with 50% duty cycle, the dc components of $v_x$ and $v_y$, are $V_g/2$ and $V/2$, respectively.
To obtain the dc component of the inductor current, the principle of capacitor charge balance is applied

\[
\langle i_c \rangle_{T_i} = \frac{1}{T_s} \int_0^{T_s} i_c(t) dt = D_o I_L + D_o' I_L = 0
\]

which yields

\[
I_L = 0
\]

As expected, the dc component of the inductor current is zero, hence the term “ac-link.”

Having derived the dc components of the capacitor voltage and inductor current, the converter waveforms can now be constructed as shown in Figure B.3.
Conducting switches:

\[ S_1 \quad S_4 \quad S_1 \quad S_3 \quad S_2 \quad S_4 \]

\[ v_x(t) \quad V_g \quad 0 \]

\[ v_y(t) \quad 0 \quad V \quad 0 \]

\[ v_C(t) \quad V_c = (V_g - V)/2 \]

\[ v_L(t) \quad (V_g + V)/2 \quad (V_g - V)/2 \quad -(V_g - V)/2 \quad -(V_g + V)/2 \]

\[ i_L(t) \quad i_L(t_1) \quad i_L(t_2) \]

\[ i_g(t) \quad i_L(t_0) \quad i_L(t_3) \]

\[ i(t) \quad i_L(t) \quad 0 \]

\[ t_0: \quad t_1: \quad t_2: \quad t_3: \quad t_4: \]

\[ 0 \quad D_V T/2 \quad T_f/2 \quad (1+D_V)T_f/2 \quad T_f \]

Figure B.3: Steady-state waveforms of proposed converter
Since the inductor current repeats every half-cycle with a reversed sign, its half-wave symmetry will be exploited to derive its expressions at the switching transitions. The inductor current at time, \( t_1 \), can be expressed as the inductor current at time, \( t_0 \), plus the increase in current during subinterval \( I \). The increase in current can be expressed as the slope of the inductor current multiplied by the time during subinterval \( I \).

\[
i_L(t_1) = i_L(t_0) + \frac{V_g + V}{2L} D_v \frac{T_s}{2}
\]  
(B.8)

Similarly, the inductor current at time, \( t_2 \), can be expressed as follows:

\[
i_L(t_2) = i_L(t_1) + \frac{V_g - V}{2L} D_v \frac{T_s}{2}
\]  
(B.9)

Due to the half-wave symmetry of the inductor current, its value at time, \( t_2 \), is simply the negative of its value at time, \( t_0 \).

\[
i_L(t_2) = -i_L(t_0)
\]  
(B.10)

Using this relationship, and substituting (B.9) and (B.10) into (B.8), yields

\[
i_L(t_1) = -i_L(t_1) - \frac{V_g - V}{2L} D_v \frac{T_s}{2} + \frac{V_g + V}{2L} D_v \frac{T_s}{2}
\]  
(B.11)

\[
i_L(t_1) = \frac{T_s}{8L} [V_g (2D_v - 1) + V]
\]  
(B.12)

Substituting (B.12) into (B.9), yields

\[
i_L(t_2) = \frac{T_s}{8L} [V_g + V (2D_v - 1)]
\]  
(B.13)

Again, due to the half-wave symmetry, the inductor current at time, \( t_3 \), can be derived as follows:

\[
i_L(t_3) = -i_L(t_1) = \frac{T_s}{8L} [V_g (1 - 2D_v) - V]
\]  
(B.14)
Finally, the inductor current at time, \( t_4 \), is equal to its value at time, \( t_0 \).

\[
i_L(t_4) = i_L(t_0) = \frac{T_s}{8L} \left[ -V_g + V \left( 1 - 2D_\varphi \right) \right]
\]  
(B.15)

Having derived the inductor current expressions at the different switching transitions, the inductor rms, the average input, and the average output currents can be determined.

Due to the half-wave symmetry, the inductor rms current can be calculated over half a switching cycle. The waveform during half a switching cycle can be broken down into two trapezoidal piecewise segments, and the rms current can be expressed as

\[
I_{L,\text{rms}} = \frac{D_\varphi}{3} \left( i_L^2(t_0) + i_L(t_0)i_L(t_1) + i_L^2(t_1) \right) + \frac{D_\varphi'}{3} \left( i_L^2(t_1) + i_L(t_1)i_L(t_2) + i_L^2(t_2) \right)
\]  
(B.16)

The average input current can be derived by integrating the inductor current during subintervals \( I \) and \( II \), and dividing by the switching period. Again, the inductor current waveform can be broken down into two piecewise segments.

\[
\left\langle i_s \right\rangle_{T_s} = \frac{1}{T_s} \int_0^{T_s} i_L(t) dt = \frac{1}{T_s} \left[ \int_0^{t_1} i_L(t \rightarrow t_1) dt + \int_{t_1}^{t_2} i_L(t_1 \rightarrow t_2) dt \right]
\]  
(B.17)

Where the inductor current during subinterval \( I \) and \( II \) can be represented using the general equation of a straight line

\[
i_{L,t_0 \rightarrow t_1}(t) = \frac{T_s}{8L} \left[ -V_g + V \left( 1 - 2D_\varphi \right) \right] + \frac{V_g + V}{2L} t
\]  
(B.18)

\[
i_{L,t_1 \rightarrow t_2}(t) = \frac{T_s}{8L} \left[ V_g \left( 2D_\varphi - 1 \right) + V \right] + \frac{V_g - V}{2L} t
\]  
(B.19)

which yields

\[
I_s = \left\langle i_s \right\rangle_{T_s} = \frac{T_s}{8L} VD_\varphi D_\varphi' \]

(B.20)

Similarly, the average output current can be derived by integrating the inductor current during subintervals \( II \) and \( III \), and dividing by the switching period.
\[ \langle i \rangle_{T_s} = \frac{1}{T_s} \int_{t_1}^{t_2} i_L(t) \, dt = \frac{1}{T_s} \left[ \int_{t_1}^{t_2} i_{L, t_1 \rightarrow t_2} (t) \, dt + \int_{t_2}^{t_3} i_{L, t_2 \rightarrow t_3} (t) \, dt \right] \]  

(B.21)

Where the inductor current equation during subinterval \( II \) is given in (B.19) and the equation during subinterval \( III \) is the negative of (B.18) due to its half-wave symmetry.

\[ i_{L, t_2 \rightarrow t_1} (t) = -i_{L, t_2 \rightarrow t_1} (t) \]  

(B.22)

which yields

\[ I = \langle i \rangle_{T_s} = \frac{V}{R} = \frac{T_s}{8L} V \theta \, D_{\theta} \, D_{\theta}' \]  

(B.23)

The dc conversion ratio can be derived using (B.23) as follows:

\[ M = \frac{V}{V_{\theta}} = \frac{R T_s}{8L} \theta D_{\theta} D_{\theta}' \]  

(B.24)

The output power can also be derived using (B.23) as follows:

\[ P_{\text{out}} = IV \]  

(B.25)

\[ P_{\text{out}} = \frac{V V}{8L f_s} D_{\theta} D_{\theta}' = \frac{V V}{4 \omega L} \theta (1 - \frac{|\theta|}{\pi}) \]  

(B.26)
B.1.1 Multi-Phase Configuration

The analysis of the proposed converter can be extended to the multi-phase configuration of Figure B.4 which can allow increased power delivery and a reduction in the energy storage requirements of the input and output filter elements if the phases are phase shifted from each other. In addition to the assumptions used for the steady-state analysis of the single-phase configuration of the proposed converter, the assumptions for the multi-phase configuration are as follows:

- The capacitance value, $C$, is equal for all phases
- The inductance value, $L$, is equal for all phases

\[
I_g = nI_{g1}
\]  \hspace{1cm} (B.27)

Recalling the expression for the average input current of a single phase

\[
I_{g1} = \frac{T}{8L} V D_\phi D_{\phi'}
\]  \hspace{1cm} (B.28)

which yields

\[
I_g = \frac{nT}{8L} V D_\phi D_{\phi'}
\]  \hspace{1cm} (B.29)
Similarly, the average output current of the multi-phase configuration is simply the multiplication of the average output current of a single phase by the number of phases, \( n \).

\[
I = nI_i
\]  
(B.30)

Recalling the expression for the average output current of a single phase

\[
I_i = \frac{T_{\phi}}{8L} V_g D_{\phi} D_{\phi'}
\]  
(B.31)

which yields

\[
I = \frac{V}{R} = \frac{nT_{\phi}}{8L} V_g D_{\phi} D_{\phi'}
\]  
(B.32)

The dc conversion ratio can be derived using (B.32) as follows:

\[
M = \frac{V}{V_g} = \frac{nT_{\phi}}{8L} D_{\phi} D_{\phi'}
\]  
(B.33)

The output power can also be derived using (B.32) as follows:

\[
P_{out} = IV
\]  
(B.34)

\[
P_{out} = \frac{nV_g V}{8f_s L} D_{\phi} D_{\phi'} = \frac{nV_g V}{4\omega_s L} \phi (1 - \frac{|\phi|}{\pi})
\]  
(B.35)

To minimize the energy storage requirements of the input and output filter elements when using a multi-phase configuration, the phases should be phase shifted from each other by \( 360/n \) degrees.
B.1.2 Dual-Phase Example

As an example of a multi-phase configuration, the dual-phase configuration of Figure B.5 will be considered. The dual-phase configuration can be controlled to operate very similar to the DAB converter if the two phases are phase shifted from each other by 180 degrees.

![Diagram of dual-phase configuration](image)

Figure B.5: (a) Circuit schematic of dual-phase configuration of proposed converter with input and output currents labeled (b) Circuit schematic of dual-phase configuration of proposed converter represented similar to DAB converter with main voltages and currents labeled
The average input current of the proposed dual-phase configuration is simply the addition of the average input currents of the two separate phases

\[ I_g = I_{g1} + I_{g2} \]  \hspace{1cm} (B.36)

Recalling the expression for the average input current of a single phase

\[ I_{g1} = \frac{T_s}{8L_1} V D_{\varphi} D'_{\varphi} \]  \hspace{1cm} (B.37)

\[ I_{g2} = \frac{T_s}{8L_2} V D_{\varphi} D'_{\varphi} \]  \hspace{1cm} (B.38)

which yields

\[ I_g = \frac{T_s (L_1 + L_2)}{8L_1 L_2} V D_{\varphi} D'_{\varphi} \]  \hspace{1cm} (B.39)

Similarly, the average output current of the proposed dual-phase configuration is simply the addition of the average output currents of the two separate phases

\[ I = I_1 + I_2 \]  \hspace{1cm} (B.40)

Recalling the expression for the average output current of a single phase

\[ I_1 = \frac{T_s}{8L_1} V g D_{\varphi} D'_{\varphi} \]  \hspace{1cm} (B.41)

\[ I_2 = \frac{T_s}{8L_2} V g D_{\varphi} D'_{\varphi} \]  \hspace{1cm} (B.42)

Which yields

\[ I = \frac{V}{R} = \frac{T_s (L_1 + L_2)}{8L_1 L_2} V g D_{\varphi} D'_{\varphi} \]  \hspace{1cm} (B.43)
The dc conversion ratio can be derived using (B.43) as follows:

\[
M = \frac{V}{V_g} = \frac{RT_s(L_1 + L_2)}{8L_4L_2} D_\phi D_\phi'.
\]  

(B.44)

The output power can be derived using (B.43) as follows:

\[
P_{\text{out}} = IV
\]  

(B.45)

\[
P_{\text{out}} = \frac{V_g V(L_1 + L_2)}{8L_4L_2 f_s} D_\phi D_\phi' = \frac{V_g V(L_1 + L_2)}{4\omega_s L_4 L_2} \varphi (1 - |\varphi|) \frac{\pi}{\pi}
\]  

(B.46)

The steady-state converter waveforms for the proposed dual-phase configuration are shown in Figure B.6. It is evident that using two phases in parallel which are 180 degrees phase shifted from each other can allow increased power delivery and a reduction in the energy storage requirements of the input and output filter elements. The ripple of the input and output currents is now twice the switching frequency. Furthermore, the operation of the proposed dual-phase configuration is very similar to the DAB converter and no current flows through the ground path connecting the input and output bridges.
Conducting switches:

$\begin{array}{cccc}
S_1 & S_2 \\
S_3 & S_4 \\
S_5 & S_6 \\
S_7 & S_8 \\
\end{array}$

Figure B.6: Steady-state waveforms of dual-phase configuration of proposed converter
B.2 Soft-Switching Range

B.2.1 Zero-Voltage Switching (ZVS)

The choice of snubber capacitance affects the ZVS operating range since the energy stored in the inductor must be sufficient to charge/discharge the snubber capacitors to their required final value. An expression for the minimum inductor current required to achieve ZVS can be derived as follows.

Assuming ideal components, and equal snubber capacitances, the inductor current during the deadtime between $t_2^-$ and $t_2$, shown in Figure 3.10, can be expressed in terms of the capacitor voltages as

$$i_{L_{t_2^-}} (t) = 2C_{sn} \frac{d}{dt} v_{Cm} (t)$$  \hspace{1cm}  \text{(B.47)}

The minimum inductor energy required to achieve ZVS can be expressed as

$$E_{min} = \frac{1}{2} L I_{min}^2$$  \hspace{1cm}  \text{(B.48)}

and

$$E_{min} = \int_{t_2^-}^{t_2} \frac{1}{2} V_i L_{t_2^-} (t) dt$$  \hspace{1cm}  \text{(B.49)}

Substituting (B.47) into (B.49) yields

$$E_{min} = V C_{sn} \int_{t_2^-}^{t_2} d v_{Cm} (t)$$  \hspace{1cm}  \text{(B.50)}

where

$$\int_{t_2^-}^{t_2} d v_{Cm} (t) = V_g$$  \hspace{1cm}  \text{(B.51)}

Equating (B.48) and (B.50) yields
\[ \frac{1}{2} L I_{\min}^2 = C_m V_s V \quad (B.52) \]

Therefore, the minimum inductor current required to achieve ZVS can be expressed as

\[ I_{L,\text{min}} = \sqrt{\frac{2 C_m}{L} V_s V} \quad (B.53) \]

For an ideal converter, the ZVS conditions can be expressed as follows

Input-side switches:

\[ S_1 : i_L(t_0) < -I_{L,\text{min}} \quad (B.54) \]

\[ S_2 : i_L(t_2) > I_{L,\text{min}} \quad (B.55) \]

Output-side switches:

\[ S_3 : i_L(t_1) > I_{L,\text{min}} \quad (B.56) \]

\[ S_4 : i_L(t_3) < -I_{L,\text{min}} \quad (B.57) \]

Due to the half-wave symmetry of the inductor current, the ZVS conditions can be simplified as follows:

Input-side switches:

\[ S_1, S_2 : i_L(t_0) < -I_{L,\text{min}} \quad (B.58) \]

Output-side switches:

\[ S_3, S_4 : i_L(t_1) > I_{L,\text{min}} \quad (B.59) \]

Substituting the inductor current expression for the input-side switches, yields

\[ i_L(t_0) = \frac{T_s}{8L} \left[ V_s + V(1 - 2D) \right] < -I_{L,\text{min}} \quad (B.60) \]
Therefore, ZVS of the input-side switches occurs when

\[
D_\varphi > \frac{V - V_g + 8f_s LI_{L,\text{min}}}{2V}
\]  

(B.61)

Similarly, substituting the inductor current expression for the output-side switches, yields

\[
i_L(t_i) = \frac{T}{8L} \left[ V_g (2D_\varphi - 1) + V \right] > I_{L,\text{min}}
\]  

(B.62)

Therefore, ZVS of the output-side switches occurs when

\[
D_\varphi > \frac{V_g - V + 8f_s LI_{L,\text{min}}}{2V_g}
\]  

(B.63)

B.2.2 Zero-Current Switching (ZCS)

For an ideal converter, the ZCS conditions can be expressed as follows:

Input-side switches:

\[
S_1 : i_L(t_0) = 0
\]  

(B.64)

\[
S_2 : i_L(t_2) = 0
\]  

(B.65)

Output-side switches:

\[
S_3 : i_L(t_1) = 0
\]  

(B.66)

\[
S_4 : i_L(t_3) = 0
\]  

(B.67)

Due to the half-wave symmetry of the inductor current, the ZCS conditions can be simplified as follows:

Input-side switches:

\[
S_1, S_2 : i_L(t_0) = 0
\]  

(B.68)
Output-side switches:

\[ S_3, S_4 : i_L(t_i) = 0 \] (B.69)

Substituting the inductor current expression for the input-side switches, yields

\[ i_L(t_0) = \frac{T_s}{8L} \left[ -V_g + V \left( 1 - 2D_\varphi \right) \right] = 0 \] (B.70)

which can be simplified to

\[ -V_g + V \left( 1 - 2D_\varphi \right) = 0 \] (B.71)

and since

\[ 0 \leq D_\varphi \leq 1 \] (B.72)

\[ V_g > V \] (B.73)

The condition is never true since the converter is operated as a step-down converter, which means that ZCS of the input-side switches is not possible.

Similarly, substituting the inductor current expression for the output-side switches, yields

\[ i_L(t_i) = \frac{T_s}{8L} \left[ V_g \left( 2D_\varphi - 1 \right) + V \right] = 0 \] (B.74)

which can be simplified to

\[ V_g \left( 2D_\varphi - 1 \right) + V = 0 \] (B.75)

Therefore, ZCS of the output-side switches occurs when:

\[ D_\varphi = \frac{V_g - V}{2V_g} \] (B.76)
B.3 Output Capacitor Selection

To select the output capacitor for a required steady state voltage ripple, the capacitor ripple current of Figure B.7 is considered. The input capacitance is selected based on the allowable change in steady state voltage due to a change in capacitor charge

\[ C_{out} = \frac{\Delta Q}{\Delta V} \]  \hspace{1cm} (B.77)

Using the relationship for the ratio of the heights and areas of two similar triangles, the change in charge can be calculated as follows:

\[ \Delta Q = A_3 = A_4 \left( \frac{h_3}{h_4} \right)^2 \]  \hspace{1cm} (B.78)

which yields

\[ \Delta Q = \frac{1}{2} \frac{T_s}{2} i_L(t_2) \left( \frac{i_L(t_2) - I}{i_L(t_2)} \right)^2 \]  \hspace{1cm} (B.79)

and the change in voltage is the steady state peak-to-peak output voltage ripple

\[ \Delta V = 2\Delta v \]  \hspace{1cm} (B.80)

Finally, the output capacitance can be derived as follows:

\[ C_{out} = \frac{T_s}{8\Delta v} i_L(t_2) \left( \frac{i_L(t_2) - I}{i_L(t_2)} \right)^2 \]  \hspace{1cm} (B.81)
Figure B.7: Steady-state waveforms of output capacitor current and voltage ripple of single-phase configuration of proposed converter

B.4 Dynamic Model Derivation

This section uses the approach of [26]. Figure B.8 shows the proposed converter with its parasitic resistance and a load variation. The parasitic resistance models the resistance of the switches, inductor, capacitor and PCB traces, referred to the ac-link.
B.4.1 Generalized Average Model

The switching node voltages can be represented by switching functions as follows:

\[ v_s(\tau) = f_s(\tau)v_g(\tau) \]  \hspace{1cm} (B.82)

\[ f_s(\tau) = \begin{cases} 1, & 0 \leq \tau < T_s / 2 \\ 0, & T_s / 2 \leq \tau < T_s \end{cases} \] \hspace{1cm} (B.83)

\[ v_y(\tau) = f_y(\tau)v(\tau) \]  \hspace{1cm} (B.84)

\[ f_y(\tau) = \begin{cases} 1, & D_0 T_s / 2 \leq \tau < (1 + D_0)T_s / 2 \\ 0, & 0 \leq \tau < D_0 T_s / 2 \text{ or } (1 + D_0)T_s / 2 \leq \tau < T_s \end{cases} \] \hspace{1cm} (B.85)

The inductor current, capacitor voltage, and output voltage are selected as state variables, and the state equations are derived as follows:

\[ \frac{di_L(\tau)}{d\tau} = \frac{1}{L} \left[ f_s(\tau)v_g(\tau) - R_p i_L(\tau) - v_c(\tau) - f_y(\tau)v(\tau) \right] \] \hspace{1cm} (B.86)

\[ \frac{dv_c(\tau)}{d\tau} = \frac{1}{C} i_L(\tau) \] \hspace{1cm} (B.87)

\[ \frac{dv(\tau)}{d\tau} = \frac{1}{C_{out}} \left[ f_y(\tau)i_L(\tau) - \frac{v(\tau)}{R} - I_{out} \right] \] \hspace{1cm} (B.88)
To derive a linear time-invariant model, averaging will be applied by representing the state variables using their Fourier series as follows:

\[
x(\tau) = \sum_{k=-\infty}^{\infty} \langle x \rangle_k(t) e^{jk\omega \tau}
\]  

(B.89)

where

\[
\langle x \rangle_k(t) = \frac{1}{T} \int_{-T}^{T} x(\tau)e^{-jk\omega \tau} d\tau
\]  

(B.90)

\[
\langle x \rangle_k(t) = \frac{1}{T} \int_{-T}^{T} x(\tau) \cos(k\omega \tau) d\tau - j \frac{1}{T} \int_{-T}^{T} x(\tau) \sin(k\omega \tau) d\tau
\]  

(B.91)

To simplify the analysis the following relationships will be used:

\[
\frac{d}{dt} \langle x \rangle_k(t) = \left\{ \frac{d}{dt} x \right\}_k(t) - jk\omega \langle x \rangle_k(t)
\]  

(B.92)

\[
\langle xy \rangle_k = \sum_{i=-\infty}^{\infty} \langle x \rangle_{k-i} \langle y \rangle_i
\]  

(B.93)

\[
\langle xy \rangle_0 = \langle x \rangle_0 \langle y \rangle_0 + 2(\langle x \rangle_{1R} \langle y \rangle_{1R} + \langle x \rangle_{1I} \langle y \rangle_{1I})
\]  

(B.94)

\[
\langle xy \rangle_{1R} = \langle x \rangle_0 \langle y \rangle_{1R} + \langle x \rangle_{1R} \langle y \rangle_0
\]  

(B.95)

\[
\langle xy \rangle_{1I} = \langle x \rangle_0 \langle y \rangle_{1I} + \langle x \rangle_{1I} \langle y \rangle_0
\]  

(B.96)

Using (B.92) and (B.94) to (B.96) in the state-space equations (B.86) to (B.88) allows the derivation of the zeroth and 1st coefficients of the state variables as follows:

\[
\frac{d\langle i \rangle_0}{dt} = \frac{1}{L} \left[ \langle f_x \rangle_0 \langle v_g \rangle_0 + 2(\langle f_x \rangle_{1R} \langle v_g \rangle_{1R} + \langle f_x \rangle_{1I} \langle v_g \rangle_{1I}) - R_p \langle i \rangle_0 - \langle v_C \rangle_0 - \langle f_y \rangle_0 \langle v \rangle_0 - 2(\langle f_y \rangle_{1R} \langle v \rangle_{1R} + \langle f_y \rangle_{1I} \langle v \rangle_{1I}) \right]
\]  

(B.97)
\[
\frac{d\langle i_L \rangle_{1R}}{dt} = \frac{1}{L} \left[ \langle f_x \rangle_0 \langle v_g \rangle_{1R} + \langle f_x \rangle_{1R} \langle v_g \rangle_0 - R_p \langle i_L \rangle_{1R} - \langle f_y \rangle_{1R} - \langle i_L \rangle_{1R} - \langle f_y \rangle_{1R} \langle v_{1R} \rangle_0 \right] + \omega_s \langle i_L \rangle_{1I}
\]  
(B.98)

\[
\frac{d\langle i_L \rangle_{1I}}{dt} = \frac{1}{L} \left[ \langle f_x \rangle_0 \langle v_g \rangle_{1I} + \langle f_x \rangle_{1I} \langle v_g \rangle_0 - R_p \langle i_L \rangle_{1I} - \langle f_y \rangle_{1I} - \langle i_L \rangle_{1I} - \langle f_y \rangle_{1I} \langle v_{1I} \rangle_0 \right] - \omega_s \langle i_L \rangle_{1R}
\]  
(B.99)

\[
\frac{d\langle v_C \rangle_0}{dt} = \frac{1}{C} \langle i_L \rangle_0
\]  
(B.100)

\[
\frac{d\langle v_C \rangle_{1R}}{dt} = \frac{1}{C} \langle i_L \rangle_{1R} + \omega_s \langle v_C \rangle_{1I}
\]  
(B.101)

\[
\frac{d\langle v_C \rangle_{1I}}{dt} = \frac{1}{C} \langle i_L \rangle_{1I} - \omega_s \langle v_C \rangle_{1R}
\]  
(B.102)

\[
\frac{d\langle v \rangle_0}{dt} = \frac{1}{C_{out}} \left[ \langle f_y \rangle_0 \langle i_L \rangle_0 + 2 \left( \langle f_y \rangle_{1R} \langle i_L \rangle_{1R} + \langle f_y \rangle_{1I} \langle i_L \rangle_{1I} \right) - \langle v \rangle_0 - \langle i_{out} \rangle_0 \right]
\]  
(B.103)

\[
\frac{d\langle v \rangle_{1R}}{dt} = \frac{1}{C_{out}} \left[ \langle f_y \rangle_0 \langle i_L \rangle_{1R} + \langle f_y \rangle_{1R} \langle i_L \rangle_0 - \langle v \rangle_{1R} - \langle i_{out} \rangle_{1R} \right] + \omega_s \langle v \rangle_{1I}
\]  
(B.104)

\[
\frac{d\langle v \rangle_{1I}}{dt} = \frac{1}{C_{out}} \left[ \langle f_y \rangle_0 \langle i_L \rangle_{1I} + \langle f_y \rangle_{1I} \langle i_L \rangle_0 - \langle v \rangle_{1I} - \langle i_{out} \rangle_{1I} \right] - \omega_s \langle v \rangle_{1R}
\]  
(B.105)

Assuming the dynamics of the input voltage and load are much slower than those of the converter yields

\[
\langle v_g \rangle_0 = V_g
\]  
(B.106)

\[
\langle v_g \rangle_{1R} = \langle v_g \rangle_{1I} = 0
\]  
(B.107)

\[
\langle i_{out} \rangle_0 = i_{out}
\]  
(B.108)

\[
\langle i_{out} \rangle_{1R} = \langle i_{out} \rangle_{1I} = 0
\]  
(B.109)
The coefficients of the switching functions are then derived as follows:

\[ \langle f_x \rangle_0 = \langle f_y \rangle_0 = \frac{1}{2} \]  
\[ (B.110) \]

\[ \langle f_x \rangle_{LR} = 0 \]  
\[ (B.111) \]

\[ \langle f_x \rangle_{IL} = -\frac{1}{\pi} \]  
\[ (B.112) \]

\[ \langle f_y \rangle_{LR} = -\frac{\sin(\pi d_\phi)}{\pi} \]  
\[ (B.113) \]

\[ \langle f_y \rangle_{IL} = -\frac{\cos(\pi d_\phi)}{\pi} \]  
\[ (B.114) \]

Substituting (B.110) to (B.114) into (B.97) to (B.105) and decoupling the dynamics of \( v_0 \), \( i_{LIR} \), and \( i_{ILI} \) from the rest of the system yields

\[ \frac{d}{dt}\begin{bmatrix} \langle v \rangle_0 \\ \langle i_{LIR} \rangle \\ \langle i_{ILI} \rangle \end{bmatrix} = \begin{bmatrix} -\frac{1}{RC_{out}} \langle v \rangle_0 - \frac{2\sin(\pi d_\phi)}{\pi C_{out}} \langle i_{LIR} \rangle - \frac{2\cos(\pi d_\phi)}{\pi C_{out}} \langle i_{ILI} \rangle - \frac{1}{C_{out}} i_{out} \\ \frac{\sin(\pi d_\phi)}{\pi L} \langle v \rangle_0 - \frac{R_p}{L} \langle i_{LIR} \rangle + \omega_s \langle i_{ILI} \rangle \\ \frac{\cos(\pi d_\phi)}{\pi L} \langle v \rangle_0 - \omega_s \langle i_{LIR} \rangle - \frac{R_p}{L} \langle i_{ILI} \rangle - \frac{1}{\pi L} V_g \end{bmatrix} \]  
\[ (B.115) \]

Finally, organizing (B.115) to (B.117) into matrix form yields the following state equation:

\[ \frac{d}{dt} \begin{bmatrix} v_0 \\ i_{LIR} \\ i_{ILI} \end{bmatrix} = \begin{bmatrix} -\frac{1}{RC_{out}} & -\frac{2\sin(\pi d_\phi)}{\pi C_{out}} & -\frac{2\cos(\pi d_\phi)}{\pi C_{out}} \\ \frac{\sin(\pi d_\phi)}{\pi L} & -\frac{R_p}{L} & \omega_s \\ \frac{\cos(\pi d_\phi)}{\pi L} & -\omega_s & -\frac{R_p}{L} \end{bmatrix} \begin{bmatrix} v_0 \\ i_{LIR} \\ i_{ILI} \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0 \end{bmatrix} \begin{bmatrix} C_{out} \\ -\frac{1}{\pi L} \end{bmatrix} \begin{bmatrix} v_g \\ i_{out} \end{bmatrix} \]  
\[ (B.118) \]
B.4.2 Small-Signal Average Model

Considering a small perturbation in the control signal (the converter switching frequency) and the resulting deviation of state variables from their steady state values yields

\[ \Delta \omega_s = \omega_s - W_s \]  
(B.119)

\[ \Delta v_0 = v_0 - V_0 \]  
(B.120)

\[ \Delta i_{L1R} = i_{L1R} - I_{L1R} \]  
(B.121)

\[ \Delta i_{L1I} = i_{L1I} - I_{L1I} \]  
(B.122)

The small-signal average model is then derived as follows:

\[
\frac{d}{dt} \begin{bmatrix} \Delta V_0 \\ \Delta i_{L1R} \\ \Delta i_{L1I} \end{bmatrix} =
\begin{bmatrix}
- \frac{1}{R C_{out} \sin(\pi D_\phi)} \\
\frac{2 \sin(\pi D_\phi)}{\pi L} \\
- \frac{2 \cos(\pi D_\phi)}{\pi L}
\end{bmatrix}
\begin{bmatrix}
- \frac{R_p}{L} \\
W_s \\
- \frac{R_p}{L}
\end{bmatrix}
\begin{bmatrix} \Delta V_0 \\ \Delta i_{L1R} \\ \Delta i_{L1I} \end{bmatrix} + \begin{bmatrix} 0 \\ I_{0I} \\ -I_{0R} \end{bmatrix} \Delta \omega_s
\]  
(B.123)

B.4.3 Control-to-Output Transfer Function

The small-signal control-to-output transfer function is derived as follows:

\[
\frac{d}{dt} x = A x + B \Delta \omega_s
\]  
(B.124)

\[ y = C x \]  
(B.125)

\[ x = \begin{bmatrix} \Delta V_0 \\ \Delta i_{L1R} \\ \Delta i_{L1I} \end{bmatrix} \]  
(B.126)

\[ y = \Delta V_0 \]  
(B.127)
\[
A = \begin{bmatrix}
\frac{1}{RC_{\text{out}}} & -\frac{2\sin(\pi D_\phi)}{\pi C_{\text{out}}} & -\frac{2\cos(\pi D_\phi)}{\pi C_{\text{out}}} \\
\frac{\sin(\pi D_\phi)}{\pi L} & -\frac{R_p}{L} & W_s \\
\frac{\cos(\pi D_\phi)}{\pi L} & -W_s & -\frac{R_p}{L}
\end{bmatrix}
\]  

(B.128)

\[
B = \begin{bmatrix} 0 \\ I_{0I} \\ -I_{0R} \end{bmatrix}
\]  

(B.129)

\[
C = \begin{bmatrix} 1 & 0 & 0 \end{bmatrix}
\]  

(B.130)

\[
G_{\text{sys}}(s) = C(sI - A)^{-1}B
\]  

(B.131)