HYBRID PASSIVE COMPONENT FOR HIGH FREQUENCY AND HIGH EFFICIENCY POWER CONVERSION

by

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A thesis submitted in conformity with the requirements for the degree of Doctor of Philosophy
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Abstract

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This thesis proposes a hybrid passive power component that provides dielectric isolation and load-source matching capability, and is a viable alternative to the classical magnetic transformer at high operating frequencies. The hybrid passive power component is comprised of a multi-layer dielectric device denoted as the Multi-Layer Ceramic Isolation Device, which is used for isolated power transfer, and a high frequency air core coupled inductor topology denoted as the Mutual Branch Topology, which provides load-source matching. The Multi-Layer Ceramic Isolation Device is realized based on a four terminal multi-layer ceramic structure with barium strontium titanate and alumina layers. Some key advantages of this device are a reduction in losses over conventional decoupling techniques, high power density and ease of manufacturing due to the planar design. The Mutual Branch Topology is an air-core inductor network which can achieve improved efficiencies over an equivalent two winding classical transformer.

The multi-layer ceramic device and air core coupled inductor topology were tested separately and together within a resonant converter topology. A design procedure for each component is presented, along with simulation results that have been experimentally verified. The hybrid passive power component has been shown to have a higher efficiency compared to a classical transformer design in the MHz operating range.
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Glossary of terms

- **Litz wire** - Braided cable (made up of several interwound insulated conductors) used in electronics to carry alternating current, and reduce the skin effect and proximity effect losses
- **MLCID** - Multi Layer Ceramic Isolation Device
- **MBT** - Mutual Branch Topology
- **ESR** - Equivalent Series Resistance
- **$R_{MLT}$** - Mean length turn resistance
- **PT** - Piezoelectric Transformer
- **MATLAB** - High-level language and interactive environment for numerical computation, visualization and programming, developed by Mathworks Inc.
- **Simulink** - MATLAB tool used for real-time simulations of systems
- **SimPowerSystem Library** - Simulink library used for real-time power systems simulations
- **COMSOL Multiphysics** - Physics based finite-Element software, developed by COMSOL Inc.
- **SIMetrix** - Analog and mixed-signal circuit simulation tool, developed by SIMetrix Technologies Ltd.
- **GUI** - Graphical User Interface
- **BST** - Barium Strontium Titanate
- **Alum** - Alumina
- **Stack** - Basic structural unit of the MLCID made up of 3 dielectric layers and 4 interleaved plates
- **$M_n$** - Impedance matrix for an n-’stack’ configuration
- **4275A Multi-Frequency LCR meter** - Measurement tool used for measuring the impedance of two-port devices
- **TF** - Transfer Function
- **4395A Network Analyzer** - Measurement tool used for obtaining the transfer function, spectrum analysis or impedance measurement of a two or four port device
- **Altera DE2 Board** - FPGA development board, developed by Altera Inc.
• ZVS - Zero Voltage Switching
• ZCS - Zero Current Switching
• T-Model - Equivalent electrical model of a two port magnetic transformer
• $K_c$ - Inverse reluctance of the magnetic medium
• $L_{tor}$ - Inductance of a toroidal structure
• $L_{corr}$ - Correction term for analytical computation of inductance for a toroidal structure
• $r_{via}^{(in)}$ - Radius of inner vias for PCB built toroidal structure
• $r_{via}^{(out)}$ - Radius of outer vias for PCB built toroidal structure
• $R_{via}^{(in)}$ - Resistance of one inner via
• $R_{via}^{(out)}$ - Resistance of one outer via
• $r_{in}$ - Inner radius of toroidal structure
• $r_{out}$ - Outer radius of toroidal structure
• $h_{tr}$ - Height of vias/PCB
Chapter 1

Introduction

1.1 Towards High Frequency Power Converters

The trend of increasing the operating frequency for power converters is driven by the reduction in the converter footprint and mass [1]. An unwanted consequence of this trend is larger switching losses associated with semiconductor devices in conventional, hard-switched converters. The heat created by switching losses must be transferred to a lower temperature body which is usually achieved with the help of a heat sink or an equivalent cooling device. The temperature rise created by heat generation is usually mitigated by increasing the surface area of the heat sink to which the device is attached. However, this increases the converter mass and footprint. As the converter footprint is reduced for higher switching frequencies, the efficiency must also be increased in order to avoid overheating and increased thermal stress [2]-[3].

Soft switched converters have been employed at high switching frequencies (100kHz - 10MHz) in order to reduce semiconductor switching losses [4]-[5]. Resonant converters are the most widely used type of soft switched converters. Their structure can be divided into two main blocks: the switching network, made up of semiconductor devices, and the resonant tank, shown in Figure 1.1.1. The operating principles and design of resonant converters is well understood and has been covered extensively in the literature. A brief summary of the most
Chapter 1. Introduction

Salient issues for resonant converters are summarized in Appendix A.

![Basic components of a resonant converter](image)

**Figure 1.1.1: Basic components of a resonant converter**

In many cases, converters require galvanic isolation between the input source and the load, and/or a component that serves the purpose of matching the source to the load. Isolation and/or load matching can be realized in one of the following three ways: magnetic coupling, piezoelectric coupling and dielectric coupling.

### 1.2 Magnetic Coupling

Magnetic coupling based on the classical magnetic transformer is the most common method used for galvanic isolation and/or for source to load matching. Magnetic transformers operate based on Faraday’s Law of magnetic induction: the magnetic field from two or more windings share a common magnetic path, usually provided by a material exhibiting large permeability values, such as iron or ferrites. The main advantage of magnetic transformers is that they can provide source-load matching by adjusting the turns-ratio between the primary and secondary windings. However, magnetic based transformers cannot have an average voltage placed across the secondary or primary winding, otherwise DC core saturation takes place. Saturation can be prevented by either active means (current control) or by passive means (inserting a DC blocking capacitor in series with the winding subjected to an average voltage). The main disadvantages of high frequency magnetic transformers are the existence of losses arising from core losses and winding losses.
A reduction in the size of magnetic transformers at increasing switching frequencies is difficult to achieve because of increasing winding loss (skin and proximity effects) and core loss (Eddy currents and hysteresis), which leads to lower efficiencies and larger heat sink requirements to dissipate the additional heat generated [6]-[9]. The winding loss can be reduced with the help of Litz wire or copper foil, but results in an increased manufacturing cost. The increased core loss experienced at MHz frequencies by most ferromagnetic materials decreases transformer efficiency. Beyond a certain frequency, dependent on the ferromagnetic material, the transformer dimensions must be scaled up in order to prevent thermal runaway [10], [11]. Furthermore, at higher operating frequencies, the impact of inter-capacitance and intra-capacitance effects changes the nature of the transformer characteristics, with increased common mode noise, unless Faraday shielding between windings is introduced [12]. Because of increased core loss and heat generation, air-core inductors are sometimes preferred over ferrite cores at MHz frequencies and beyond.

Different design topologies, such as integrated on-chip magnetics [13] or flat core high frequency transformers [14], and different ferromagnetic materials [15] have been developed to reduce the magnetic transformer losses and footprint. However, the issue of magnetic transformer performance at high frequencies still remains a limitation which translates into reduced efficiencies (when compared to low frequency transformers) and more expensive devices.

### 1.3 Piezoelectric Coupling

Piezoelectric Transformers (PTs) can be used to provide isolation and source to load matching [16]. PTs are electromechanical devices that operate based on a two step process: converting electrical to mechanical energy with the help of a piezoelectric actuator on the primary side, and converting it back to electrical energy on the secondary side with a piezoelectric transducer. The effective turns ratio of PTs can be adjusted through changes in geometry to allow designers to match the source to the load characteristics, similar to magnetic transformers. PTs also
offer several advantages over magnetic transformers such as high voltage isolation between the primary and secondary sides, as well as no EM noise. The disadvantages presented by PTs are their load dependent input-output transfer function because of the resonant type of operation, a rather low upper bound on power handling capability due to the internal heat generated by the mechanical hysteresis, and lower efficiency when compared to magnetic transformers (90% to 98% max) [17], [18].

1.4 Dielectric Coupling

Individual decoupling capacitors connected between the active and return current paths are usually used to achieve dielectric isolation. The advantages of using capacitive coupling over magnetic coupling is a reduction in cost and a possible reduction in losses at high operating frequencies. Due to the advantages provided by dielectric isolation, galvanically isolated systems based on capacitive coupling have been developed and tested for power and data transfer in integrated circuits [19], or for galvanic isolation between source and load [20]. Capacitive isolation systems have also been used for contactless charging [21], for biosignal instrumentation isolation [22] or for isolated LED drivers [23]-[24].

The main disadvantages of the individual capacitors isolation technique are the lack of source/load matching and the use of discrete individual capacitors. Employing discrete capacitors introduces two concerns: one of size and parasitics, and one of capacitance mismatching. The mismatch in capacitance values of the discrete capacitors (typical tolerances of 10-20% for nF range capacitors) will create an unbalanced circuit which results in larger common mode currents, and leads to more electromagnetic interference. More electromagnetic interference results in the need for larger common mode filters or better shielding requirements to ensure that the electromagnetic interference standards can be complied with [25].
The focus of the thesis is the design and operation of a new hybrid device which can provide high efficiency galvanic isolation and load-source matching, at high operating frequencies. The hybrid device can be broken down into two separate components: a four port dielectric device for galvanic isolation, and an air-core inductor network. The proposed device uses components that exploit advantages of both dielectric and magnetic coupling and hence the new device is a hybrid device. The main advantages of the four port dielectric device is that it provides high efficiency, high power density and high common mode rejection which provides a close to balanced active and return path. The magnetics topology is built using air-core inductors due to ease of manufacturing/customization, and due to the high operating frequency range, where magnetic core losses are significantly larger than at lower frequencies.

1.5 Proposed Galvanic Isolation Device Based on Dielectric Coupling

A four port integrated dielectric isolation device denoted as a Multi-Layer Ceramic Isolation Device (MLCID), that can be used for high-frequency applications is proposed in this thesis [26]. The advantages offered by the proposed device over the above presented isolation methods (magnetic, piezoelectric) are lower manufacturing costs due to the planar design and low material costs, no skin and proximity effects design issues, no DC saturation, and higher efficiencies at MHz frequencies.

The MLCID exploits the intrinsic electric and displacement field profiles in order to obtain the required power coupling between input and output. A ceramic multi-layer implementation is chosen over other types of capacitor technologies such as electrolytic, alumina or thin-foil polymer implementations because of the wide relative permittivity range ceramics have and because ceramics can be easily integrated into a multi-layer structure, thus achieving higher power densities and improved control over manufacturing tolerances. A summary describing the different types of capacitor technologies available on the market is presented in Appendix
B.

The MLCID provides better performance (higher efficiency, better matching between active and return path and reduced footprint) over conventional dielectric isolation techniques but it cannot provide load-source matching like a classical transformer. While there are applications where source-load matching is not required, the range of applications for which the MLCID can be used is limited. However, the source-load matching limitation of the MLCID can be addressed by concatenating this device with an integrated air core magnetics topology.

1.6 Proposed Integrated Air Core Magnetics Topology

Two approaches for designing an inductor are with a magnetic core or an air core. The vast majority of inductors have magnetic cores, because they provide a significant increase in the energy storage capabilities of the inductor in a smaller volume, but introduce additional loss. Almost all inductors which are operated below the MHz region are magnetic core inductors, because of the significant increase in energy storage capabilities with relatively low additional losses (relative permeability in the 1000’s for iron/steel cores below the MHz range).

However, classical magnetic transformers have to contend with increased winding and core losses at high operating frequencies. Two main paths have been taken to improve the efficiency of the transformer at high frequencies: changing the transformer layout, or changing the magnetic materials used. The standard layouts of high-frequency transformers are the flat core or racetrack topologies which have the advantage of a lower footprint, while providing similar loss to a regularly wound transformer. Unfortunately, the disadvantages mentioned previously such as winding loss and core loss remain a limiting issue. The other avenue taken for improving transformer efficiency has been the search for better engineered magnetic materials.

While several research groups have reported improvements on different manufactured materials [15, 27], their relative permittivity has not been significantly altered. Furthermore, the magnetic material needs to be manufactured and shaped such that the field lines relative to the
magnetic axes are aligned in order to reduce hysteresis loss. This leads to issues of manufac-
turability and reproducibility of the manufacturing process. In the MHz range of operation, magnetic transformers do not offer a significant increase in power density over air-core transformers [28], while air core transformers can provide reduced power loss density and a higher quality factor.

One of the more popular magnetic cores for MHz frequency operation are powdered iron cores. The relative permeability values for most powdered iron cores (Carbonyl J, SF, TH, W) in the MHz frequency range are between 1 and 10 [29], which is a significant decrease from the relative permeability of low frequency operated cores (100-10000 range). The MHz region is where air-core inductors become a viable alternative since they eliminate the frequency dependent core losses at the expense of a reduced permeability [30], [31]. Fortunately, the reduction in permeability is small when compared to magnetic materials usable in the MHz range. Because of the reasons outlined above (low relative permeability gain, additional core losses), an air-core inductor design was adopted.

The Mutual Branch Topology (MBT) proposed in this thesis is an integrated toroidal two winding coupled air-core magnetic structure which can be used to replace the classical two winding magnetic transformer when used in conjunction with the Multi-Layer Ceramic Isolation Device [32].

1.7 Thesis Objectives and Outline

The thesis objectives are as follows:

- Design, manufacture and test a new dielectric isolation device (known as the Multi-Layer Ceramic Isolation Device) that can provide better performance in terms of efficiency and energy density over conventional capacitive isolation techniques.

- Design, manufacture and test a new air-core winding topology (henceforth known as the Mutual Branch Topology) which can be used to match the source to the load.
• Test the combination of the MLCID and MBT within a resonant converter configuration, and compare the efficiency results to an equivalent classical two-winding transformer.

The outline of the thesis is as follows: Chapter 2 presents the concept of capacitive coupling used and the preliminary tests performed for an interleaved capacitor constructed from a multilayer printed circuit board (to ensure simulation results agree with experimental data before manufacturing the multi layer ceramic structure); Chapter 3 details the model of the multi layer ceramic device, along with simulations, and experimental characterization, followed by experimental operation of the device within a resonant converter. Chapter 4 introduces the magnetic modeling used for the classical transformer, and the derivation of the MBT model, together with simulation results. Chapter 5 provides the analysis of the air-core inductor model used, together with simulation results. Finally, Chapter 6 presents the results of the MBT and MLCID used in conjunction with a resonant converter structure and the results are compared with those of an identical resonant converter with a classical magnetic transformer.
Chapter 2

Interleaved Plate Structure Modeling and Behavior

A circuit based model for a four plate interleaved structure including experimental validation for a four port dielectric structure constructed using a multi-layer printed circuit board is presented in this chapter. The purpose of this validation is to assess the viability of a 4-port interleaved structure for dielectric coupling.

2.1 Interleaved Plate Structure Geometry

Two approaches for implementing dielectric coupling using a pair of input plates and a pair of output plates are shown in Figure 2.1.1. The perpendicular plate arrangement presented in Figure 2.1.1 (a) requires a uniaxial dielectric polarization vector (the polarization vector of the dielectric has to form a non-zero angle with the applied electric field). While such a structure can be created in practice, it will not be able to provide good coupling between the input and output terminals. Further details on the modeling of a uniaxial dielectric structure modeling are presented in Appendix C.1.

The second type of dielectric coupling structure involves a set of four interleaved parallel plates as shown in Figure 2.1.1 (b). Consider such a four parallel plate configuration, with
Figure 2.1.1: Four port dielectric isolation structure with (a) perpendicular dielectric coupling and (b) parallel dielectric coupling all the plates having the same width 'w' (cross-section shown in Figure 2.1.2, width 'w' is perpendicular to the plane of the figure). The following constraints are placed on the geometry of the problem:

\[
\begin{align*}
I_A &= I_A^{(1)} + I_A^{(2)} & I_B &= I_B^{(1)} + I_B^{(2)} \\
d_A &= d_A^{(1)} + d_A^{(2)} & d_B &= d_B^{(1)} + d_B^{(2)}
\end{align*}
\]  

(2.1.1)

Assuming ideal dielectric media and ignoring fringing effects at the edges of the plates, the four plate arrangement can be represented using the equivalent circuit presented in Figure 2.1.3. The formulae used to compute the capacitance values of the capacitors displayed in Figure 2.1.3 are presented in Table 2.1.1.
2.2 Circuit Analysis

A Δ – Y impedance transformation for capacitances $C_{12}$, $C_{13}$ and $C_{23}$ shown in Figure 2.1.3 is performed. The new Y-connected capacitances denoted as $C_{1n}$, $C_{2n}$ and $C_{3n}$ are equal to:

$$
C_{1n} = \frac{\sum C_{123}}{C_23}
$$

$$
C_{2n} = \frac{\sum C_{123}}{C_{13}}
$$

$$
C_{3n} = \frac{\sum C_{123}}{C_{12}}
$$

(2.2.1)

where $\sum C_{123} = C_{12}C_{13} + C_{12}C_{23} + C_{13}C_{23}$. This Δ – Y transformation is used to simplify the circuit analysis results obtained. The equivalent Y-impedance circuit is shown in Figure 2.2.1.

The circuit shown in Figure 2.1.3 can be represented by its Norton equivalent, which consists of a current source and an impedance in parallel with it. The Norton equivalent current
CHAPTER 2. INTERLEAVED PLATE STRUCTURE MODELING AND BEHAVIOR

Figure 2.2.1: Changing from a Delta to a Y load configuration

source is equal to:

\[ I_N = \frac{C_D}{C_{3n} + C_D} \cdot I_S \] (2.2.2)

where \( C_D = \frac{C_{2n}C_{34}}{C_{2n} + C_{34}} \). The open circuit voltage of the Norton circuit is equal to:

\[ V_{OC} = \frac{1}{j\omega C_{23}} \cdot \frac{C_E}{C_E + C_{3n}} I_S \] (2.2.3)

where \( C_E = \frac{C_{2n}C_{34}C_{34}}{C_{24}C_{34} + C_{2n}C_{24} + C_{2n}C_{34}} \). With the help of the short circuit current and open circuit voltage, the equivalent impedance can be computed as follows:

\[ C_N = \frac{V_{OC}}{I_{SC}} = \frac{C_{12}C_{13} + C_{12}C_{23} + C_{13}C_{23} + C_{13}C_{24} + C_{12}C_{24}}{C_{12} + C_{13}} \] (2.2.4)

The equivalent impedance of the interleaved capacitor structure can be used to compute the output voltage magnitude based on the input load. A derivation of the state space model of the four terminal system is presented in Appendix C.2.

2.3 PCB Implementation of the Capacitive Coupling Device

The implementation of the capacitive coupling device is attempted as a proof of concept using a multi-layered PCB board. The metallic plates are made out of copper foil while the dielectric is glass reinforced epoxy laminate sheets (FR-4), which has a dielectric constant of 4.8 and a breakdown strength of 50kV/mm. The dielectric strength decreases to 4.35kV/mm
near and above 100MHz and the dissipation factor is 0.017 in the MHz range. The PCB design parameters are displayed in Table 2.3.1.

<table>
<thead>
<tr>
<th>Parameters of PCB design</th>
<th>ε (F/m)</th>
<th>$4.25 \cdot 10^{-10}$</th>
<th>$I_{in}$ (A)</th>
<th>1.0</th>
<th>$\omega$ (MHz)</th>
<th>10</th>
</tr>
</thead>
<tbody>
<tr>
<td>$l_A$ (m)</td>
<td>0.2</td>
<td>$l_A^{(1)}$ (m)</td>
<td>0.1</td>
<td>$l_A^{(2)}$ (m)</td>
<td>0.1</td>
<td></td>
</tr>
<tr>
<td>$l_B$ (m)</td>
<td>0.2</td>
<td>$l_B^{(1)}$ (m)</td>
<td>0.1</td>
<td>w (m)</td>
<td>0.15</td>
<td></td>
</tr>
<tr>
<td>$d_A$ (m)</td>
<td>1.2 $\cdot 10^{-3}$</td>
<td>$d_A^{(1)}$ (m)</td>
<td>6 $\cdot 10^{-4}$</td>
<td>$d_A^{(2)}$ (m)</td>
<td>6 $\cdot 10^{-4}$</td>
<td></td>
</tr>
<tr>
<td>$d_B$ (m)</td>
<td>1.2 $\cdot 10^{-3}$</td>
<td>$d_B^{(2)}$ (m)</td>
<td>6 $\cdot 10^{-4}$</td>
<td>$R_{load}$ (Ω)</td>
<td>10</td>
<td></td>
</tr>
</tbody>
</table>

Table 2.3.1: PCB multi-layer design parameters

A 4395A Network/Spectrum/Impedance Analyzer from Agilent is used to obtain the input-to-output transfer function of the manufactured PCB board. The transfer function obtained is presented in Figure 2.3.1. The frequency sweep performed was from 10kHz to 100MHz and the RF source had a power rating of 0dBm (1mW). The voltage transfer function can be seen in Figure 2.3.1. Note that the transfer function obtained has a 20dB/decade rise from 10kHz to 200kHz after which the transfer function levels off at approximately -7.4dB, until it reaches 1MHz. The resonance displayed at 2MHz is due to the parasitic inductance of the system.

The initial +20dB slope appears because the input source "sees" an equivalent capacitor in series with the output load. Beyond 200kHz, the transfer function levels off at about -7.4dB, until 1MHz. We would like to achieve a voltage transfer function as close to 0dB as possible in the final design and implementation of the dielectric isolation device, for the operating frequency range of interest, because that is equivalent to having good coupling between input and output. The -20dB slope which appears beyond 2MHz is due to the parasitic inductor which becomes the dominant impedance of the system.

2.4 Simulation Results of a Four Plate Dielectric Device

To observe how different geometrical or material parameters affect the behavior of the four plate system, we designed and created a Graphical User Interface in MATLAB. The MATLAB
GUI window is presented in Figure 2.4.1, and the GUI documentation and operation details are provided in Appendix D.1.

In order to obtain good capacitive coupling between the input and output terminals, the...
capacitance ratio in equation 2.2.2 should be as close as possible to 1. Consequently, it is
desirable to have $C_D \gg C_3n$ which results in $C_{12} \gg C_{13}$ and $C_{34} \gg C_{23}$. The difference
in capacitance magnitudes can be achieved by using dielectric layers with different relative
permittivity values.

This relationship between the relative permittivity of different dielectric layers and volt-
age transfer function will be exploited and shown in the following chapter, which presents
the design specifications and the experimental results for the manufactured dielectric isolation
devices named Multi-Layer Ceramic Isolation Devices (MLCIDs).
Chapter 3

Multi-Layer Ceramic Isolation Device

As previously stated in the introduction, a ceramic planar structure implementation was chosen over other capacitor technologies because it is easier to create a large difference in permittivity between different dielectric layers and it is easier to maintain tighter tolerances on geometrical and material parameters.

3.1 Modeling of the Dielectric Coupling Device

A cross-section of the structural unit of the integrated dielectric device is presented in Figure 3.1.1 (a). The basic design makes use of a set of electrode plates and two dielectric materials with different relative permittivity values. The behavior of a passive four port device can be specified by four parameters: the input/output voltages and currents. Assuming no fringing fields, perfect conducting electrodes and isotropic dielectrics, the relationship between the voltages/currents and the electric/displacement fields presented in Figure 3.1.1(b) can be specified with the help of equations 3.1.1-3.1.4, where $\vec{D}_{ij}$ and $\vec{E}_{ij}$ represent the displacement...
Figure 3.1.1: (a) Basic structural unit of capacitive coupling device structure and (b) picture showing the electric fields and currents injected into the four plates and electric fields between electrodes i and j respectively.

\[
V_{in} = -\int_{1}^{2} \vec{E}_{12} d\vec{l} - \int_{2}^{3} \vec{E}_{23} d\vec{l} \\
V_{out} = -\int_{2}^{3} \vec{E}_{23} d\vec{l} - \int_{3}^{4} \vec{E}_{34} d\vec{l} \\
I_{out} = \int \int_{S} \frac{\partial \vec{D}_{12}}{\partial t} d\vec{S} \\
I_{in} = \int \int_{S} \frac{\partial \vec{D}_{12}}{\partial t} d\vec{S} + \int \int_{S} \frac{\partial \vec{D}_{23}}{\partial t} d\vec{S} + \int \int_{S} \frac{\partial \vec{D}_{13}}{\partial t} d\vec{S}
\]

The difference in relative permittivity between the two dielectric materials presented in Figure 3.1.1(a) has to be large \((\varepsilon_{r}^{(1)}/\varepsilon_{r}^{(2)} \geq 100)\) in order to provide good power coupling between the input and output terminals.

A series of Finite Element Analysis simulations were performed with the help of COMSOL.
Multiphysics 4.3 for the following reasons: to observe the electric/displacement field distribution, to confirm that the predicted dielectric coupling is achieved, and to observe the fringing fields generated. Figures 3.1.2 and 3.1.3 show the results of a simulation for the basic structural unit with $\varepsilon_r^{(1)} = 1300$ and $\varepsilon_r^{(2)} = 9$. The displayed results are divided into two sections: (a) electric field and (b) displacement field. The electric field profile shown in Figure 3.1.2(a) is highest in the region of low permittivity ($|\vec{E}_{12}| \ll |\vec{E}_{23}|$ and $|\vec{E}_{34}| \ll |\vec{E}_{23}|$). This suggests that $V_{in} \approx V_{out} \approx -\int_{S}^{3} \vec{E}_{23} d\vec{l}$, based on equations 3.1.1-3.1.2. The $\vec{D}$ field is concentrated across the high permittivity regions as seen in Figure 3.1.3(a). For a high permittivity ratio, $|\vec{D}_{13}| \ll |\vec{D}_{12}|$ and $|\vec{D}_{23}| \ll |\vec{D}_{12}|$. A consequence of these two inequalities is that most of the current flows between the top two and bottom two plates. Based on equations 3.1.3-3.1.4, it can be concluded that $I_{in} \approx I_{out} = \int_{S}^{3} \frac{\partial \vec{D}_{12}}{\partial t} d\vec{S}$. Since $V_{in} \approx V_{out}$ and $I_{in} \approx I_{out}$, the MLCID structural unit behaves analogously to a magnetic based isolation transformer with an equivalent turns ratio of unity.

![Figure 3.1.2: COMSOL simulation for the distribution of (a) electric field with (b) close-up of the fringing fields for a basic MLCID stack](image)

Figures 3.1.2(b) and 3.1.3(b) also highlight the fringing fields that need to be taken into account when designing such a device. The largest fringing electric fields appear at the edge of the electrode plates 2 and 3, and are approximately twice as large as the electric field magnitude at the center of the two electrodes. The displacement field magnitude is largest at the edge of
the electrode plates and the high permittivity dielectric (high displacement field is less of a problem since breakdown is dependent on the electric field magnitude). The magnitude of the fringing displacement fields is approximately 2.5 times as large as the fields developed at the center of the plates. The fringing fields developed at the edge of the plates and at the interface between the different dielectrics do not have a noticeable effect on the electrical behavior of the MLCID, which suggests that ignoring the fringing fields is a reasonable assumption in deriving a circuit model for the four port device. However, the electric fringing fields will place a bound on the maximum allowable input/output voltage (electric field breakdown).

Assuming ideal dielectric media and ignoring fringing field effects at the edges of the plates, the four plate arrangement can be represented using the equivalent circuit shown on the left hand side of Figure 3.1.4. The right hand side of the figure shows the impedance network required to model an eight plate system or two “stack” configuration. For a one “stack” input current source \((I_S)\) configuration, the equations describing the behavior of the system in matrix form are:

\[
\mathbf{M}_1 \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} I_S \\ 0 \\ 0 \end{bmatrix}
\]  

(3.1.5)
where $M_1$ is a $3 \times 3$ matrix equal to:

$$M_1 = \begin{bmatrix} Z_{1g}^{-1} + Z_{12}^{-1} & -Z_{12}^{-1} & 0 \\ -Z_{12}^{-1} & Z_{12}^{-1} + Z_{2g}^{-1} + Z_{23}^{-1} + Z_L^{-1} & -Z_{23}^{-1} - Z_L^{-1} \\ 0 & -Z_{23}^{-1} - Z_L^{-1} & Z_{12}^{-1} + Z_{23}^{-1} + Z_L^{-1} \end{bmatrix}$$ (3.1.6)

and the impedances $Z_{ij}$ are equal to:

$$Z_{ij} = \frac{1}{j\omega C_{ij}} + ESL_{ij} + ESR_{ij}$$ (3.1.7)

where $ESL_{ij}$ is the parasitic inductance associated with element $ij$ and $ESR_{ij}$ is the resistance associated with element $ij$.

Increasing the number of stacks for a Multi-Layer Capacitive Isolation Device (MLCID) increases the total capacitance values associated with every matrix element, and as a result,
it decreases the total reactive impedance of the system. The input-output network for an n-
"stack" device is presented in Figure 3.1.5. Note that the second black terminal is chosen as a
reference terminal, similar to Figure 3.1.4.

\[ M_n = \begin{bmatrix}
(2n-1)Z_1^{-1} + nZ_2^{-1} + (n-1)Z_3^{-1} & -nZ_2^{-1} & -(n-1)Z_3^{-1} \\
-nZ_2^{-1} & nZ_2^{-1} + (n-1)Z_3^{-1} & -(2n-1)Z_3^{-1} \\
-(n-1)Z_3^{-1} & -(2n-1)Z_3^{-1} & (n-1)Z_2^{-1} + nZ_3^{-1} + (2n-1)Z_3^{-1}
\end{bmatrix} \quad (3.1.8) \]

Solving for the input/output voltages can be achieved with the following matrix inversion mul-
triplication:

\[
\begin{bmatrix}
V_1 \\
V_2 \\
V_3
\end{bmatrix} = M_n^{-1} \begin{bmatrix}
I_S \\
0 \\
0
\end{bmatrix}
\quad (3.1.9)
\]

This multi-"stack" circuit network model is implemented in the MATLAB GUI introduced in
section 2.4 (see Appendix D.1 for more details) and is used to simulate the behavior of the
MLCID in order to choose appropriate geometrical design parameters (surface area, number of
stacks, thickness, overlap of plates) and dielectric material properties (relative permittivity, loss
tangent) for the manufacturing of the prototypes. The MLCID manufactured specifications are
the focus of the next subsection.
3.2 MLCID Prototype Design Parameters

Two MLCIDs comprised of five multi-layer ceramic "stacks" were manufactured by TRS Technologies Inc. 150$\mu$m Barium Strontium Titanate (BST) and 500$\mu$m Alumina layers were used as the two different dielectric layers. The individual BST layers had a measured relative permittivity of approximately 1300 and a loss tangent of 0.68% at 25°C, with a 15% permittivity variation from 0-70°C. The individual alumina layers had $\varepsilon_r = 9$, a loss tangent of 0.15% and negligible permittivity temperature variation. The dielectric layers were sintered individually and bonded together with epoxy resin. Cr/Au (500A/2000A) layers were used for the electrode plates. The devices have a rated voltage of 300V and a rated current of 2A. The manufactured MLCID parameters are displayed in Table 3.2.1. The dielectric loss of the BST decreases as a function of frequency in the kHz range, but there is a slight increase once it enters the MHz range [33]. For the performed simulations, it was assumed that the loss tangent remained constant.

![Table 3.2.1: MLCID parameters](image)

For the current MLCID design, the DC and AC maximum voltage ratings are different. The AC electric rating is based on the dielectric breakdown strength of the alumina layer due to the fact that the voltage drop will be much larger across the alumina layer. The breakdown field for alumina layers is approximately 25kV/mm [34].

Since the dielectric thickness of the alumina layers is 500 $\mu$m, the breakdown voltage across it will be equal to approximately 12.5kV. When applying a DC voltage to the MLCID, the voltage drop will occur mostly across the BST layers. The breakdown strength of the BST layers
is dependent on the sintering temperature. Reference [35] reports that the lowest breakdown strength of BST is 20kV/mm, which will be used in the breakdown voltage approximations. For a parallel plate configuration, the electric field towards the center of the plates can be assumed constant and computed using the following formula:

\[ E_{\text{break}} = \frac{V_{\text{break}}}{d_t} \]  

(7)

where \( d_t \) is the dielectric thickness. Thus, the breakdown voltage is equal to approximately 3kV, when considering no fringing field effects. Accounting for fringing fields results in a DC voltage breakdown strength of 1.2kV for the MLCIDs which is much lower than the 12.5kV breakdown across the alumina layer. Therefore, the voltage breakdown \( V_{\text{break}} \) of the MLCID is set to 1.2kV. The voltage breakdown strength can be customized for future MLCID designs by varying the thickness of the dielectric layers. The constructed devices are presented in Figure 3.2.1; one terminal of the device has two connecting red leads, while the other terminal has two connecting black leads.

The rated current is relatively low for the constructed devices (2A) due to the connection between the plates and the leads; higher current ratings can be achieved with better lead connections to the electrodes. The current limitation is imposed in order to limit temperature gradients and localized heating across the ceramic dielectric layers. Breakdown due to local thermal stresses is one of the most common failures of ceramic devices, as presented in Appendix B. The tests performed on the manufactured MLCIDs are presented and compared with the simulation results in the following two sections.

### 3.3 MLCID Impedance Measurements

To theoretically compute the capacitance between any two terminals of the MLCID, a fictitious current source is connected between the two selected terminals. This equates to selecting a specific current vector that can be used to compute the voltage vector with equation 3.1.9.
The impedance "seen" between the two terminals should be equal to the voltage drop between the two terminals, divided by the current of the test source:

$$Z_{ij} = \frac{V_i - V_j}{I_S}$$  \hspace{1cm} (3.3.1)

The capacitance measurement can then be extracted with the following formula:

$$C_{ij} = \frac{1}{\text{imag}(Z_{ij})\omega}$$  \hspace{1cm} (3.3.2)

For example, if we wish to measure the capacitance between the two black leads of Figure 3.1.5, then the configuration presented in Figure 3.3.1, in conjunction with equation 3.3.3 will be used.

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = M_5^{-1} \begin{bmatrix} I_S \\ 0 \\ 0 \end{bmatrix}$$  \hspace{1cm} (3.3.3)

If we wish to measure the capacitance between the top black and red leads as shown in Figure 3.3.2, then equation 3.3.4 will be used.
Based on the design parameters presented in Table 3.2.1, the theoretical capacitances of an individual alumina and barium titanate (BT) layer are:

\[
C_{Al} = \varepsilon_0 \varepsilon_{low} \frac{Area}{t_{Al}} = 16pF
\]  
(3.3.5)

\[
C_{BT} = \varepsilon_0 \varepsilon_{high} \frac{Area}{t_{BT}} = 7.67nF
\]  
(3.3.6)
CHAPTER 3. MULTI-LAYER CERAMIC ISOLATION DEVICE

The theoretical capacitance values for a one and five 'stack' MLCID configuration are given in Table 3.3.1. The capacitances obtained for the 5 stack configuration will be compared to the experimentally obtained measurements.

<table>
<thead>
<tr>
<th>MLCID theoretical capacitances</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{ij}$</td>
</tr>
<tr>
<td>$C_{1g}$</td>
</tr>
<tr>
<td>$C_{12}$</td>
</tr>
<tr>
<td>$C_{13}$</td>
</tr>
<tr>
<td>$C_{2g}$</td>
</tr>
<tr>
<td>$C_{23}$</td>
</tr>
<tr>
<td>$C_{3g}$</td>
</tr>
</tbody>
</table>

Table 3.3.1: MLCID theoretical capacitances

The capacitance and Equivalent Series Resistance of the MLCID prototype was measured with a 4275A Multi-Frequency LCR meter from Agilent. The measurements were recorded for 10 discrete frequency values in the 10kHz - 10MHz range. Two known capacitors were initially tested in order to assess the behavior of the device: a 1nF polypropylene capacitor and a 100nF ceramic capacitor. The measurements obtained are presented in Table 3.3.2. For the 1nF capacitor, the measurements obtained are close to 1nF, with a slight dip as the frequency is increased. For the ceramic 100nF capacitor, the nominal value is off by approximately 10nF from the measured one - most probably because the actual capacitance of the device is slightly

<table>
<thead>
<tr>
<th>Test capacitor measurements</th>
</tr>
</thead>
<tbody>
<tr>
<td>freq</td>
</tr>
<tr>
<td>10kHz</td>
</tr>
<tr>
<td>20kHz</td>
</tr>
<tr>
<td>40kHz</td>
</tr>
<tr>
<td>100kHz</td>
</tr>
<tr>
<td>200kHz</td>
</tr>
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</tr>
<tr>
<td>4MHz</td>
</tr>
<tr>
<td>10MHz</td>
</tr>
</tbody>
</table>

Table 3.3.2: Test capacitor measurements
off from the rated value. Similar to the 1nF test case, the measured capacitance drops initially; after 200kHz however, it starts increasing. The 4MHz and 10MHz measurements displayed an overflow error, because the measured capacitance increased past the measurement range of the device. The increase in measured capacitance is due to the parasitic inductance of the system. The effect of parasitics is more evident for the 100nF test case because the resonant frequency is 10 times lower than the 1nF test case, assuming a comparable parasitic inductance.

Capacitor losses can be grouped in two main categories: conduction and dielectric losses. If a circuit representation that accounts for the different physical loss mechanisms is used, then conduction losses (leads and connections to electrodes) are represented by a series resistance, while dielectric losses are represented by a resistance in parallel with an ideal capacitor. However, with the LCR meter, the extracted measurements were a capacitive term and a series resistive term (Equivalent Series Resistance or ESR). The ESR values decrease with increasing frequency because the dielectric loss of the capacitor (parallel resistance in an equivalent physically correct circuit representation) remains relatively constant over the tested frequency range. Thus, since loss measurements are lumped into an equivalent series resistance term, the ESR value would have to decrease as the frequency increases since the capacitor reactance decreases as a function of frequency (1/\( \omega \) dependence).

Capacitance measurements were performed between all two lead pairs of the MLCIDs. The two red leads were labeled as R1/R2 and the two black leads were labeled as B1/B2. The capacitance values obtained are displayed in Table 3.3.3. Similar to the test case results presented in Table 3.3.2, the capacitances in the 100’s pF range stay fairly constant, while the measurements of the capacitances in the 10’s of nF range increase significantly in the MHz range. The parasitic inductance introduced by the MLCID should also be larger than the two test cases because of the long leads connected to the MLCID (\( \approx 10cm \)).

The measured capacitances between R1-B1 and R2-B2 are approximately 47.5nF; the measured capacitances between terminals R1-R2, R1-B2, R2-B1, B1-B2 are all approximately equal to 162pF. These values are higher than the theoretical results presented in Table 3.3.1
Table 3.3.3: MLCID capacitor measurements

<table>
<thead>
<tr>
<th>freq</th>
<th>(R1-R2)</th>
<th>(R1-B1)</th>
<th>(R1-B2)</th>
<th>(R2-B1)</th>
<th>(R2-B2)</th>
<th>(B1-B2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10kHz</td>
<td>161.7pF</td>
<td>47.75nF</td>
<td>163pF</td>
<td>162.8pF</td>
<td>47.8nF</td>
<td>162.6pF</td>
</tr>
<tr>
<td>20kHz</td>
<td>161.7pF</td>
<td>47.53nF</td>
<td>163pF</td>
<td>162.7pF</td>
<td>47.6nF</td>
<td>162.5pF</td>
</tr>
<tr>
<td>40kHz</td>
<td>161.6pF</td>
<td>47.32nF</td>
<td>163pF</td>
<td>162.7pF</td>
<td>47.4nF</td>
<td>162.2pF</td>
</tr>
<tr>
<td>100kHz</td>
<td>161.7pF</td>
<td>47.19nF</td>
<td>163pF</td>
<td>162.6pF</td>
<td>47.3nF</td>
<td>162.3pF</td>
</tr>
<tr>
<td>200kHz</td>
<td>161.7pF</td>
<td>47.89nF</td>
<td>163pF</td>
<td>162.5pF</td>
<td>47.9nF</td>
<td>163.3pF</td>
</tr>
<tr>
<td>400kHz</td>
<td>161.7pF</td>
<td>52.40nF</td>
<td>163pF</td>
<td>162.6pF</td>
<td>51.9nF</td>
<td>162.1pF</td>
</tr>
<tr>
<td>1MHz</td>
<td>162pF</td>
<td>192nF</td>
<td>163pF</td>
<td>162.7pF</td>
<td>153nF</td>
<td>162.4pF</td>
</tr>
<tr>
<td>2MHz</td>
<td>163pF</td>
<td>N/A</td>
<td>164pF</td>
<td>163.7pF</td>
<td>N/A</td>
<td>163.6pF</td>
</tr>
<tr>
<td>4MHz</td>
<td>168pF</td>
<td>N/A</td>
<td>169pF</td>
<td>168.2pF</td>
<td>N/A</td>
<td>167.9pF</td>
</tr>
<tr>
<td>10MHz</td>
<td>214pF</td>
<td>N/A</td>
<td>211pF</td>
<td>205.6pF</td>
<td>N/A</td>
<td>204.9pF</td>
</tr>
</tbody>
</table>

(38.4nF and 143pF). This discrepancy appears because of the difference between the calculated and measured capacitance of a single Alumina and BST layer. This is confirmed by the single layer measurements offered by TRS Technologies:

\[ C_{Al} = 17.7 \text{pF} \quad \tan\delta = 0.0015 \quad (3.3.7) \]
\[ C_{BT} = 9.66 \text{nF} \quad \tan\delta = 0.0068 \quad (3.3.8) \]

When compared to the values computed in equations 3.3.5-3.3.6 (16pF and 7.67nF), the measurements offered by TRS are larger than the theoretical values. This discrepancy is most likely related to a slightly larger electrode area than given by the design parameters. If the TRS single stack capacitance values are used in conjunction with the circuit model, then the theoretical capacitance values obtained between different MLCID terminals are very close to the measured ones, as can be seen in Table 3.3.4. The ESR values associated with each capacitance measurement in Table 3.3.3 are shown in Table 3.3.5.

Since the reactance and ESR values of a capacitor change with frequency, a better indicator of device efficiency is the loss tangent \( \tan\delta \):

\[ \tan\delta = \frac{ESR}{X_c} = ESR \cdot \omega C \quad (3.3.9) \]
Table 3.3.4: MLCID adjusted capacitances

<table>
<thead>
<tr>
<th>Leads</th>
<th>Theoretical</th>
<th>Measured</th>
<th>% Difference</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_1 - R_2$</td>
<td>159 pF</td>
<td>161.7 pF</td>
<td>1.7%</td>
</tr>
<tr>
<td>$R_1 - B_1$</td>
<td>48.34 nF</td>
<td>47.75 nF</td>
<td>1.2%</td>
</tr>
<tr>
<td>$R_1 - B_2$</td>
<td>159 pF</td>
<td>163 pF</td>
<td>2.5%</td>
</tr>
<tr>
<td>$R_2 - B_1$</td>
<td>159 pF</td>
<td>162.8 pF</td>
<td>2.3%</td>
</tr>
<tr>
<td>$R_2 - B_2$</td>
<td>48.34 nF</td>
<td>47.8 nF</td>
<td>1.1%</td>
</tr>
<tr>
<td>$B_1 - B_2$</td>
<td>159 pF</td>
<td>163 pF</td>
<td>2.5%</td>
</tr>
</tbody>
</table>

Table 3.3.5: MLCID ESR measurements

<table>
<thead>
<tr>
<th>freq</th>
<th>(R1-R2)</th>
<th>(R1-B1)</th>
<th>(R1-B2)</th>
<th>(R2-B1)</th>
<th>(R2-B2)</th>
<th>(B1-B2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10kHz</td>
<td>90Ω</td>
<td>3.45Ω</td>
<td>75Ω</td>
<td>80Ω</td>
<td>3.4 Ω</td>
<td>80Ω</td>
</tr>
<tr>
<td>20kHz</td>
<td>50Ω</td>
<td>2.25Ω</td>
<td>40Ω</td>
<td>40Ω</td>
<td>2.2 Ω</td>
<td>42 Ω</td>
</tr>
<tr>
<td>40kHz</td>
<td>26Ω</td>
<td>1.49Ω</td>
<td>55Ω</td>
<td>26Ω</td>
<td>1.4 Ω</td>
<td>55Ω</td>
</tr>
<tr>
<td>100kHz</td>
<td>12Ω</td>
<td>0.88Ω</td>
<td>11Ω</td>
<td>9Ω</td>
<td>0.85Ω</td>
<td>12Ω</td>
</tr>
<tr>
<td>200kHz</td>
<td>5 Ω</td>
<td>0.62Ω</td>
<td>4.3Ω</td>
<td>5Ω</td>
<td>0.6 Ω</td>
<td>5.4 Ω</td>
</tr>
<tr>
<td>400kHz</td>
<td>3 Ω</td>
<td>0.46Ω</td>
<td>4.4Ω</td>
<td>2.8 Ω</td>
<td>0.44 Ω</td>
<td>5.4 Ω</td>
</tr>
<tr>
<td>1MHz</td>
<td>1.4Ω</td>
<td>0.34Ω</td>
<td>1.2Ω</td>
<td>1.0 Ω</td>
<td>0.33Ω</td>
<td>0.93Ω</td>
</tr>
<tr>
<td>2MHz</td>
<td>0.6Ω</td>
<td>N/A</td>
<td>0.6Ω</td>
<td>0.4Ω</td>
<td>N/A</td>
<td>0.18Ω</td>
</tr>
<tr>
<td>4MHz</td>
<td>0.65Ω</td>
<td>N/A</td>
<td>0.4 Ω</td>
<td>0.5Ω</td>
<td>N/A</td>
<td>0.32 Ω</td>
</tr>
<tr>
<td>10MHz</td>
<td>0.35Ω</td>
<td>N/A</td>
<td>0.46Ω</td>
<td>0.4Ω</td>
<td>N/A</td>
<td>0.22 Ω</td>
</tr>
</tbody>
</table>

where $X_c$ is the capacitor reactance in Ohms. Similar to the capacitance or inductance of a device, the loss tangent changes very little, and is dependent on the dielectric/electrode materials, as well as the manufacturing process. The ESR values in Table 3.3.5 result in low loss tangent terms. The loss tangent associated with the ESR is $\approx 0.01$ for the R1-B1/R2-B2 terminals and $\approx 0.00087$ for the R1-R2/R1-B2/R2-B1/B1-B2 terminals.

The experimentally measured capacitances are in agreement with the theoretically computed values, which confirms that the simulation models used were correct. The experimentally obtained voltage transfer function of the MLCID presented in the next section will also confirm that the device operates as predicted by the theoretical model.
3.4 Voltage Transfer Function of MLCID

The theoretical voltage Transfer Function (TF) for the MLCID is presented in Figure 3.4.1. The Bode plot frequency range is from 1kHz to 500MHz with a 50 Ω output impedance. Below 100kHz, the Transfer Function rises by 20dB/decade, and it encounters a simple pole at a frequency of approximately 130kHz, after which it asymptotically approaches 0dB.

![Simulation Bode Plot of Input-Output Voltage TF of MLCC](image1)

Figure 3.4.1: Simulation of MLCID transfer function

The experimental transfer function of the MLCID prototype was obtained with the Agilent 4395A Network/Spectrum/Impedance Analyzer. The setup used for the TF measurement is shown in Figure 3.4.2. The RF signal source input was passed through a 11667A power

![Figure 3.4.2: Agilent 4395A network analyzer setup](image2)
splitter. One of the power splitter outputs was connected to an output terminal (R) while the second power splitter output was connected to the MLCID, and its output was sent to a second terminal (A). The 4395A Network Analyzer uses the signals seen at its two output terminals (A and R) to generate the transfer function of the MLCID.

The MLCID transfer function obtained with the calibrated 4395A Network Analyzer is shown in Figure 3.4.3. The frequency sweep performed was from 1kHz to 500MHz with an IF Bandwidth of 1kHz. Note that Figure 3.4.3 displays a simple pole at \( \approx 32.5 \) kHz, which is four times lower than the simulation pole frequency. This discrepancy can be explained with the help of Figure 3.4.4.

The power splitter introduces a 50Ω input resistance in series with the MLCID. Thus, the equivalent resistance of the measurement setup is actually 100Ω, not 50Ω. Since the equivalent Thevenin impedance of the MLCID is a series capacitance, the location of the pole is given by the following expression:

\[
 f_{pole} = \frac{1}{2\pi R_{series}C_{th}} \tag{3.4.1} 
\]

Thus, if the total series resistance of the system is doubled, then the pole frequency will be
halved. This explains why the frequency is lower by a factor of two in our experiments, which leaves another factor of two that needs to be accounted for.

The remaining factor of two discrepancy can also be explained with the help of 3.4.4. The main thing to note is that the input and output ports of the 4395A Network analyzer are grounded. As seen in Table 3.3.3 a capacitance of $\approx 48\text{nF}$ was measured between leads R1-B1 and R2-B2. Thus, both the active and return path for the MLCID have an equivalent series capacitance with values twice as large as the equivalent Thevenin capacitance. If the output port is not grounded, then the active and return equivalent capacitances can be added together, resulting in an equivalent capacitance of $\approx 24\text{nF}$. However, since both the input and output ports are grounded, the equivalent capacitance of the return path is shorted out, leaving an equivalent series capacitance twice as large as $C_{th}$. Based on equation 3.4.1, doubling the capacitance causes the pole frequency to be two times smaller.

In summary, the simple pole present in the experimental TF is at a factor of four lower frequency when compared to the simulation results due to: (a) a 50$\Omega$ series resistance in the measurement setup introduced by the power splitter and (b) the fact that the input and output ports of the 4395A are both grounded. The higher frequency ($>20\text{MHz}$) roll-off and multi-resonance phenomenon is expected to appear in the experimental results due to parasitic inductance present in the measurement system and transmission line effects respectively.
The MLCID ability to provide capacitive coupling between the input and output terminals was tested with the help of an oscilloscope and function generator. The measurement circuit is laid out in Figure 3.4.5.

![Circuit diagram for function generator setup](image)

Figure 3.4.5: Circuit diagram for function generator setup

The input and output voltages are displayed in the following oscilloscope captures (Figures 3.4.6 and 3.4.7), for 36kHz and 1MHz. For 36kHz the output voltage is approximately half of the input, and it leads the input by approximately 45°. The 45° phase shift was expected at 132kHz (four times larger than 36kHz) based on the theoretical computations. The factor of four discrepancy between the theoretical and measured results can be again explained with the help of a circuit diagram of the measurement setup, presented in Figure 3.4.5. The function generator has a 50Ω input resistance which doubles the total resistance in the measured system, and the oscilloscope and function generator ports are grounded, similar to the Agilent 4395A Network Analyzer, which creates a similar setup.

At 1MHz, the input and output voltage waveforms are in phase and almost equal in magnitude. Both the oscilloscope captures shown in Figures 3.4.6 and 3.4.7 are in agreement with the Voltage TF measurements obtained with the 4395A Network Analyzer and confirm that the MLCID prototype operates properly. The next section presents the simulation and experimental results obtained with a 1MHz resonant DC-AC converter. The purpose of this resonant converter implementation is to test the MLCID performance which was used as part of the
Chapter 3. Multi-Layer Ceramic Isolation Device

3.5 Resonant Converter Design with MLCID

The 1MHz resonant converter operation was simulated with the help of SIMetrix. The simulations presented in this section were obtained with a series L-C resonant tank. Figure 3.5.1 presents the overall circuit schematic of the resonant converter. The full bridge inverter was connected to a 12V DC power supply.

The transistor chosen for the resonant converter full bridge is the IRF7501 MOSFET from International Rectifier. The IRF7501 has a \( V_{DS} \) rating of 20V and a maximum channel current...
of 2.4A with a maximum peak current of 19A. The maximum $V_{GS}$ value is ±12V and the peak gate voltage should not exceed 16V.

If the full bridge inverter is gated at 1MHz, with a square wave input of 45-50% duty cycle, then the rise and fall time of the output voltage is around 70ns, which represents the ramp $V_{DS}$ experiences, or the Miller Plateau duration.

The series resonant tank has a resonant frequency slightly below 1MHz, which allows us to operate at 1MHz with ZVS. The operating frequency was chosen around 1MHz and not higher (5-10MHz range) due to increasing difficulties in obtaining appropriate switching on/off times with off-the-shelf switching components. Figure 3.5.2 presents the simulated converter voltage output, together with the inverter current and load current. Note that the obtained currents are sinusoidal with a fundamental frequency of 1MHz.

Figure 3.5.3 presents the effects of Zero-Voltage Switching on power losses; the figure displays the current through $Q_1$ along with the voltage across it and the power delivered to $Q_1$. Note that there is a power spike whenever the transistor turns off, but there is no equivalent turn-on spike. This is because Zero Voltage Switching ensures soft turn-on but has no influence on the turn-off characteristics.

The choice of gate driver for the full bridge MOSFETs was based on two main parameters:
The gate charge $Q_G$ required to turn the MOSFET on/off comes into play for the selection of an appropriate Gate Driver. If the driver can provide 500mA of current to the gate of the MOSFET, then the turn-on delay and rise time should be around 16ns, which is acceptable.

The TPS28XX MOSFET gate driver family from Texas Instruments provides a suitable gate driver for the resonant converter. It can supply a current output of up to 2A peak, with a gate voltage rise and fall time of approximately 14ns. The TPS28XX class was designed for high frequency, power MOSFET applications, and is suitable for the resonant converter design.
3.5.1 Resonant Converter Tests

The half bridge gate driver chosen (LM5100B) is an 8-pin IC with two inputs (low side input and high side input) and two outputs (low and high side gate output). A bootstrap capacitor is connected to two of the LM5100B terminals, and is used to generate and maintain the high side voltage of the high side driver. The gate drive inputs (LI and HI) were generated with an Altera DE2 board. These signals are shown in Figure 3.5.4 for a 100kHz and a 1MHz gating signal. Two half bridge tests are shown in Figure 3.5.5, with and without an output load.

The MLCID prototype together with a series 200nH surface mount inductor (labeled as \( L_R \) in Figure 3.5.1) constituted the resonant tank of the converter. The MLCID isolated the input and output terminals of the device and introduced the capacitive element required for a series L-C resonant tank. Figure 3.5.6 shows the (a) MOSFET gate voltages, and the sinusoidal output voltage from the resonant converter for an output load of (b) 50Ω and, (c) 10Ω. Note that the output voltage obtained has little distortion, which is as expected. A summary of the MLCID performance metrics, together with an experimental efficiency plot for the MLCID is presented next.
3.6 Summary of MLCID Performance

Table 3.6.1 presents relevant parameters of several X1 capacitors that have been designed for line-to-line isolation applications, the same application as for the stand-alone MLCID prototypes. These safety capacitors have to be able to operate at a rated voltage of 250VAC and withstand voltages as high as 1500VAC and impulse voltages in the 2500-4000V range. As mentioned in section 3.2 the MLCID can theoretically withstand 1.2kV; the two devices have not been stress tested due to their high manufacturing cost and time, but we will assume for the sake of comparison that the MLCIDs will hold at 1200VAC. Since the capacitors presented in Table 3.6.1 are close in value to the capacitances of the MLCID associated with the active and return current path (nF range), we are able to compare the MLCID parameters with these isolation capacitors. The dimensions are provided in terms of the total volume of the device.

<table>
<thead>
<tr>
<th>Capacitor</th>
<th>V(mm³)</th>
<th>C</th>
<th>Tol(%)</th>
<th>f₀</th>
<th>tanδ</th>
</tr>
</thead>
<tbody>
<tr>
<td>KHB103KP87</td>
<td>1089</td>
<td>10nF</td>
<td>±10</td>
<td>1kHz</td>
<td>≤ 2.5%</td>
</tr>
<tr>
<td>W1X223S</td>
<td>942</td>
<td>22nF</td>
<td>±20</td>
<td>1kHz</td>
<td>≤ 2.5%</td>
</tr>
<tr>
<td>PMR210</td>
<td>4800</td>
<td>100nF</td>
<td>±20</td>
<td>1kHz</td>
<td>15.6%</td>
</tr>
<tr>
<td>AC103M140</td>
<td>883</td>
<td>10nF</td>
<td>±20</td>
<td>1kHz</td>
<td>≤ 5.0%</td>
</tr>
<tr>
<td>440LD55-R</td>
<td>2125</td>
<td>10nF</td>
<td>±20</td>
<td>1kHz</td>
<td>≤ 2%</td>
</tr>
</tbody>
</table>

Table 3.6.1: Commercial X1 capacitors
For isolation purposes, two such devices are required for use, which would double the volume occupied by the decoupling network (disregarding the separation distance which would add to the total space requirements). Note that the MLCID volume ($\approx 650\text{mm}^3$) is already less than one individual capacitor.

The tolerance level of individual capacitors can be as low as $\pm 1-5\%$, but this is usually
offered for capacitors in the pF range. For X1 capacitors in the nF range, the standard tolerances are ±10% and ±20%. This suggests that there might be a difference in capacitance as high as 10-20% if two individual capacitors are used for decoupling. On the other hand, the MLCID impedance measurements show that the relative capacitance difference between the active and return path is around 1%, which means that using the MLCID instead of the decoupling capacitors will result in a more balanced circuit (reduced common mode signal). The last column of Table 3.6.1 presents the loss tangent obtained for the given capacitor. Most reported tests were performed at 1kHz with a 1V RMS input voltage. A quick comparison with the loss tangents of the MLCID (max 1%) reveals that the loss tangents provided by the MLCIDs are much lower than the maximum values quoted for the different decoupling capacitors. These lower loss tangents will result in higher efficiency for the MLCID.

![Figure 3.6.1: Power ratio transfer function for a frequency and output load sweep](image)

The circuit model developed in this section is used to obtain the efficiency of the MLCID prototype with the help of the MLCID GUI, for a range of input signal frequencies and output resistances. The dielectric loss of each layer and the resistance associated with each electrode is included in the MATLAB GUI model and shown in Figure 3.6.1, with the assumption that the
loss tangent does not increase as a function of frequency. At 1MHz, the efficiency is above 99% for load resistances in the 10Ω-10kΩ range. The efficiency drops for low or high output loads, similar to the behavior of magnetic transformers or other transformerless isolation devices such as coupling capacitors. The efficiency results presented in Figure 3.6.1 have been experimentally validated at 1MHz for several different output loads, as presented in Figure 3.6.2. The efficiency results were extracted by comparing the converter-MLCID output efficiency with that of the converter plus a stand-alone 25nF capacitor. As can be seen, the efficiency obtained from the experimental results is slightly lower than the computed efficiency values. This small discrepancy appears mainly because of the loss associated with the connection between the leads and the stack electrodes. The AC resistance of an individual lead was measured to be approximately 20mΩ at 1MHz, which explains why there is a larger difference between the simulated and experimental efficiency for higher output loads. Note that this additional loss introduced by the leads will be significantly reduced if the MLCID is surface mounted.

![Figure 3.6.2: Efficiency of MLCID at 1MHz](image-url)
Chapter 4

Magnetic Model of Air Core Coupled Inductors

The following section presents the modeling and simulation results of an air-core inductor network, denoted as the Mutual Branch Topology (MBT). The purpose of the MBT is to provide load-source matching, similar to the classical magnetic transformer. A comparison between the classical two-winding transformer, an equivalent T-model implementation, and the MBT is performed through the use of simulations, in order to highlight the advantages of the MBT topology. Finally, a method of obtaining the "optimal" inductance values for an MBT implementation is presented.

4.1 Equivalent Electrical Model of the Two-Winding Transformer

Figure 4.1.1 displays the electric circuit model of the classical two-winding transformer with all non-idealities included, where $L_{L1}$ and $L_{L2}$ represent the leakage inductances of the two windings, $R_1$ and $R_2$ the copper loss associated with the two windings, $L_c$ the magnetizing reactance branch and $R_c$ the core loss. For the remainder of this section, the core loss will be
neglected \((R_c = \infty)\) because the magnetics design which will be presented later in the thesis is air-core.

Consider the coupled transformer model presented Figure 4.1.2(a); this model assumes perfect coupling between the two windings \((L_{L1} = L_{L2} = 0)\) and ignores losses \((R_1 = R_2 = 0)\). The same current-voltage characteristics of the two winding transformer can be obtained with the help of three separate reactive components, as shown in Figure 4.1.2(b). This three component system displayed in Figure 4.1.2(b) is known as a T-model implementation.

Note that inductors \(L_A\) and \(L_B\) are not the leakage inductances \(L_{L1}\) and \(L_{L2}\) from Figure 4.1.1; they represent stand-alone components, and as such, the T-model implementation should not be confused with the electrical model representation referred to the primary or secondary side. In order to obtain the same transfer function as the two winding transformer with the

![Figure 4.1.1: Electrical circuit representation of a two winding transformer](image)

![Figure 4.1.2: (a) Coupled model of a two-winding transformer and (b) T-model equivalent representation](image)

T-model implementation, the three discrete components of the T-model need to have the fol-
lowing inductance values:

\[
L_A = L_1 - M \\
L_B = L_2 - M \\
L_M = M
\]  

(4.1.1) 
(4.1.2) 
(4.1.3)

Note that if good coupling is assumed \((M \approx \sqrt{L_1 \cdot L_2})\), then \(L_B\) will have a negative value for a step-down configuration, and \(L_A\) will have a negative value for a step-up configuration. For a practical implementation, the negative inductance component will have to be implemented using a capacitive element. There is a small range of values for turns ratios near or equal to one where both \(L_A\) and \(L_B\) are greater than zero, but the focus of the upcoming analysis will not be on isolation transformers.

The proof that the circuits presented in Figures 4.1.2(a) and 4.1.2(b) provide the same input-output transfer function is provided in Appendix E. The T-model implementation is used as an analysis tool of the actual transformer, but there are no practical load-source matching topologies implemented by using three discrete physical components for the following reasons: (a) no galvanic isolation is provided, (b) the T-model implementation will only be able to provide the appropriate step-up/step-down ratio only for a certain frequency range, and (c) the overall power losses of an equivalent T-model implementation will be larger than for the two-winding transformer, as will be shown in the next section.

### 4.2 T-Model and Transformer Efficiency Analysis

The analysis of the performance of a two-winding magnetic transformer and a T-model implementation presented in this section will take into account only the losses due to the inductor windings, while ignoring core losses since the eventual implementation is air core. The purpose of this analysis is to observe how a practical T-model implementation will behave in terms
of losses when compared to the traditional two-winding transformer, and serve as a stepping stone to the Mutual Branch Topology design.

Figure 4.2.1: (a) Two winding transformer with winding loss and (b) practical T-model implementation represented by individual inductors

Figure 4.2.1(b) displays the circuit diagram of the physical T-model implementation with three separate components (the shaded boxes represent individual physical components) while Figure 4.2.1(a) shows the two winding transformer with winding loss, assuming perfect coupling between the two windings. It is important to note that for the T-model implementation, one of the series components will have a negative reactance (negative inductor value). For a step-down input-output voltage transfer function, inductor $L_B$ of the T-model implementation will have a negative value, which suggests the need for a capacitor. Similarly, for a step-up implementation, inductor $L_A$ will have to be replaced by a capacitive element in a practical implementation. The following analysis will treat both $L_A$ and $L_B$ as series inductors in terms of computed losses, to obtain a "fair" comparison between the T-model implementation and the two-winding transformer (otherwise, the capacitor dielectric loss will be dependent on the selected capacitor, and as a consequence, the overall efficiency will depend on the quality of the capacitor selected).

The equations used to describe the behavior of the two-winding transformer are presented below in phasor form:

$$ V_1 = j\omega L_1 I_1 + j\omega M I_2 $$

(4.2.1)
\[ V_2 = j\omega MI_1 + j\omega L_2 I_2 \]  
\[ V_1 = V_{in} - I_1 R_1 \]  
\[ V_2 = (R_2 + R_{out}) I_2 \]

The resistance values \( R_1 \) and \( R_2 \) are determined based on the following equations:

\[ L_1 = N_1^2 \cdot K_c \]  
\[ L_2 = N_2^2 \cdot K_c \]  
\[ R_1 = N_1 \cdot R_{MLT} \]  
\[ R_2 = N_2 \cdot R_{MLT} \]

The parameter \( K_c \) represents the inverse reluctance (permeance) of the magnetic medium and it is equal to \( K_c = \frac{\mu_r}{\mu_0} \) while \( R_{MLT} \) represents the per-turn resistance of the windings, which is assumed to be the same for both windings of the two-winding transformer. The T-model implementation presented in Figure 4.2.1 can be described with the following equation:

\[
\begin{bmatrix}
V_{in} \\
0 \\
0 \\
0
\end{bmatrix} =
\begin{bmatrix}
R_A & R_B & 1 & 1 \\
j\omega L_A & 0 & -1 & 0 \\
0 & j\omega L_M & 0 & -1 \\
j\omega L_B + R_B + R_{out} & - (j\omega L_B + R_B + R_M + R_{out}) & 0 & -1
\end{bmatrix} 
\begin{bmatrix}
I_A \\
I_M \\
V_A \\
V_M
\end{bmatrix}
\]

The inductance values of the three discrete components \( (L_A, L_M, L_B) \) are given by equations 4.1.1-4.1.3. The resistances of the three components are obtained with the help of the following equations:

\[ R_A = \frac{\sqrt{L_A}}{K_c} \cdot R_{MLT} \]  
\[ R_B = \frac{\sqrt{L_B}}{K_c} \cdot R_{MLT} \]
\[ R_M = \sqrt{\frac{L_M}{K_c}} \cdot R_{MLT} \]  

(4.2.12)

These three equations ensure that the resistance associated with each component of the T-model implementation is proportional to the equivalent number of turns with the same \( R_{MLT} \) as for the two winding transformer. The total losses of the two winding transformer (\( P^{(1)}_{\text{loss}} \)) and the practical T-model implementation (\( P^{(2)}_{\text{loss}} \)) are described by the following two equations:

\[ P^{(1)}_{\text{loss}} = R_1 \cdot |I_1|^2 + R_2 \cdot |I_2|^2 \]  

(4.2.13)

\[ P^{(2)}_{\text{loss}} = R_A \cdot |I_A|^2 + R_B \cdot |I_B|^2 + R_M \cdot |I_M|^2 \]  

(4.2.14)

Table 4.2.1 presents simulation parameters for a 4:1 step-down transformer, and for the equivalent T-model implementation. Figure 4.2.2 presents (a) the total losses and (b) the efficiency of the two-winding transformer (solid blue line) and of the T-model implementation (dashed green line), as a function of output load. The losses obtained for the equivalent T-model are consistently larger across the load spectrum, when compared to the two-winding transformer. This is because the total resistance of the three inductors is larger than the total resistance of the two-winding transformer and because of the large current in the parallel inductor branch (\( I_M \)). The current magnitudes for the two-winding transformer and T-model implementation are shown in Figure 4.2.3. This figure highlights the main issue with the T-model implementation - the parallel branch current \( I_M \) has a loss associated with it due to the
Figure 4.2.2: (a) Power Loss and (b) Efficiency as a function of output load for the two-winding transformer and the T-model implementation

Figure 4.2.3: Magnitude of currents as a function of output load for (a) the two-winding transformer and (b) the T-model implementation

copper loss in inductor $L_M$, and there is no equivalent loss mechanism in the two winding model.
4.3 Mutual Branch Topology

An implementation of the T-model transformer using discrete components has larger losses than the actual two-winding transformer, as shown in Section 4.2. However, the T-model implementation can be modified to include mutual coupling between the two inductors \((L_A\) and \(L_M\) for step-down configuration or \(L_M\) and \(L_B\) for a step-up configuration) in order to reduce losses and increase system efficiency. By selecting an appropriate value of the inductor magnitudes and mutual coupling coefficient, the appropriate voltage step-up or step-down ratio can be obtained. The circuit representation of this new proposed model, referred to as the Mutual Branch Topology (MBT), is displayed in Figure 4.3.1. Similar to the T-model implementation, one of the series inductances will have a negative value and will have to be replaced by a capacitive element in a physical implementation (\(L_x\) for a step-up configuration, \(L_z\) for a step-down configuration). The set of equations used to describe the behavior of the system shown in Figure 4.3.1 are provided below:

\[
\begin{bmatrix}
V_{in} \\
0 \\
0 \\
0
\end{bmatrix}
= 
\begin{bmatrix}
R_x & R_y & 1 & 1 \\
-j\omega L_x & j\omega M_{xy} & -1 & 0 \\
j\omega M_{xy} & j\omega L_y & 0 & -1 \\
-j\omega L_z + R_z + R_{out} & -(j\omega L_z + R_z + R_y + R_{out}) & 0 & -1
\end{bmatrix}
\begin{bmatrix}
I_x \\
I_y \\
V_x \\
V_y
\end{bmatrix}
\]

Figure 4.3.1: The Mutual Branch Topology circuit representation for a step-down configuration
Note that the impedance matrix of equation 4.3.1 is similar to the one shown in equation 4.2.9 that is used to describe the T-model operation. The main difference are the $j\omega M_{xy}$ mutual coupling terms which appear in the impedance matrix.

The equation used to compute the power loss of the MBT is provided below:

$$P_{loss}^{(3)} = R_x \cdot |I_x|^2 + R_y \cdot |I_y|^2 + R_z \cdot |I_z|^2$$  \hspace{1cm} (4.3.2)  

The equivalent winding resistance of the three inductors is computed in a similar fashion to the equivalent resistances of the T-model (see equations 4.2.10-4.2.12). The practical representation of the MBT for a step-down or step-up configuration is shown in Figure 4.3.2.

Figure 4.3.2: Circuit diagram for the practical implementation of a (a) step-down MBT and (b) step-up MBT

The MBT parameters displayed in Table 4.3.1 are for a 4:1 step-down implementation at 100kHz and $R_{MLT}$ is set to be the same as for the other two topologies, whose parameters are
shown in Table 4.2.1.

<table>
<thead>
<tr>
<th>Simulation parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L_x$</td>
</tr>
<tr>
<td>$L_y$</td>
</tr>
<tr>
<td>$k_{xy}$</td>
</tr>
<tr>
<td>$L_z$</td>
</tr>
</tbody>
</table>

Table 4.3.1: Simulation parameters of the MBT for a 4:1 step-down configuration at 100kHz

With the parameters displayed in Tables 4.2.1 and 4.3.1, a load sweep and several real time simulations were performed in order to compare the efficiency of the two-winding transformer, T-model practical implementation, and MBT. Note that the same inverse reluctance $K_c$ and resistance per mean length turn $R_{MLT}$ is used for all three implementations, to ensure a fair comparison.

Figure 4.3.3, which displays the efficiency of the three topologies as a function of load, highlights the fact that the MBT provides better efficiency over the two-winding transformer and T-model for the given set of parameters. As seen from Tables 4.2.1 and 4.3.1, the resistances associated with elements $L_x$, $L_y$ and $L_z$ are not lower in magnitude than for the two-winding transformer. The main reason for the increased efficiency and decreased total losses of the MBT is the lower input current magnitudes, when compared to the other two models.

![Figure 4.3.3: Simulated efficiencies of the three models as a function of output load: the two-winding model ($\eta^{(1)}$), the T-model ($\eta^{(2)}$) and the MBT ($\eta^{(3)}$)](image-url)
Figure 4.3.4 highlights this important advantage of the MBT implementation: the magnitude of the currents flowing through the inductor network is lower for the Mutual Branch Topology when compared to the T-model implementation. This advantage is observed in a plot of the efficiencies of the three models: the two-winding model ($\eta^{(1)}$), the T-model ($\eta^{(2)}$) and the MBT ($\eta^{(3)}$). While efficiencies for large loads are similar for the given parameters, there is a clear advantage of the MBT in terms of losses for light loads.

Time domain simulations were performed with the help of MATLAB Simulink and the SimPowerSystems Library. Figure 4.3.5 displays the plot of the currents for the three discussed models as a function of time. An output load of 2.5Ω and a sinusoidal voltage source were used. Note that as previously mentioned, the magnitude of the input current ($I_x$) is reduced for the MBT case, when compared to the input current of the two-winding transformer ($I_1$) and T-model implementations ($I_A$).

Table 4.3.2 displays a new set of parameters for the three different models (two-winding transformer, T-model implementation and MBT) used for a set of simulations at 5MHz. Figures 4.3.6 and 4.3.7 display the current magnitudes and the efficiency as a function of load for the
three models operated at 5MHz. Note that the MBT implementation has higher efficiencies than the two-winding transformer and T-model implementation.

![Figure 4.3.5: Time domain simulation of the model currents for a 2.5Ω load](image)

A MBT step-up configuration can be obtained by switching the input and output terminals of the step-down configuration with some slight modifications to the inductor values. The

<table>
<thead>
<tr>
<th>Simulation parameters</th>
<th>$V_{in}$</th>
<th>40V RMS</th>
<th>$f_0$</th>
<th>5MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>$N_1$</td>
<td>40</td>
<td>$N_2$</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>$K_c$</td>
<td>0.25nH/turn</td>
<td>$R_{MLT}$</td>
<td>5mΩ/turn</td>
<td></td>
</tr>
<tr>
<td>$L_1$</td>
<td>400nH</td>
<td>$R_1$</td>
<td>200mΩ</td>
<td></td>
</tr>
<tr>
<td>$L_2$</td>
<td>25nH</td>
<td>$R_2$</td>
<td>50mΩ</td>
<td></td>
</tr>
<tr>
<td>$L_A$</td>
<td>300nH</td>
<td>$R_A$</td>
<td>173mΩ</td>
<td></td>
</tr>
<tr>
<td>$L_B$</td>
<td>-75nH</td>
<td>$R_B$</td>
<td>87mΩ</td>
<td></td>
</tr>
<tr>
<td>$L_M$</td>
<td>100nH</td>
<td>$R_M$</td>
<td>100mΩ</td>
<td></td>
</tr>
<tr>
<td>$L_x$</td>
<td>300nH</td>
<td>$R_x$</td>
<td>173mΩ</td>
<td></td>
</tr>
<tr>
<td>$L_y$</td>
<td>50nH</td>
<td>$R_y$</td>
<td>63mΩ</td>
<td></td>
</tr>
<tr>
<td>$k_{xy}$</td>
<td>0.7</td>
<td>$M_{xy}$</td>
<td>98.6nH</td>
<td></td>
</tr>
<tr>
<td>$L_c$</td>
<td>-100nH</td>
<td>$R_c$</td>
<td>100mΩ</td>
<td></td>
</tr>
</tbody>
</table>

Table 4.3.2: Simulation parameters for a 4:1 transformer at 5MHz
results of a 1:4 step-up configuration simulation are presented in Figures 4.3.8-4.3.9, for the same design parameters presented in Table 4.3.2. The set of equations which need to be solved to determine the behavior of the system are different when compared to the MBT step-down,
as exemplified by equation 4.3.3:

\[
\begin{bmatrix}
V_{in} \\
0 \\
0 \\
0
\end{bmatrix} =
\begin{bmatrix}
\frac{j \omega L_x + R_x + R_y}{j \omega L_y} & \frac{j \omega L_x + R_x}{j \omega M_{yz}} & 1 & 0 \\
\frac{j \omega L_y}{j \omega M_{yz}} & \frac{j \omega L_y}{j \omega M_{yz}} & -1 & 0 \\
\frac{j \omega M_{yz}}{j \omega L_z} & \frac{j \omega L_z}{j \omega L_z} & 0 & -1 \\
\frac{-R_y}{R_y} & \frac{R_z + R_{out}}{R_y} & -1 & 1
\end{bmatrix}
\begin{bmatrix}
I_y \\
I_z \\
V_y \\
V_z
\end{bmatrix}
\] (4.3.3)

Figure 4.3.8: Magnitude of (a) input, (b) output currents and (c) output voltages as a function of output load for the 1:4 step-up configurations at 5MHz

Figure 4.3.9: Efficiency of 1:4 step-up models at 5MHz as a function of output load

In summary, the MBT is able to provide higher efficiency for the entire simulated load range
(1-100Ω) when compared to the two winding transformer, for both the step-up and step-down configurations.

4.4 Optimization of Mutual Branch Topology

A Graphical User Interface (GUI) developed in MATLAB (denoted as the MBT GUI) is used to assess the impact that the mutually coupled inductors have on the transfer function of the system. Figure 4.4.1 displays the GUI window. The MBT GUI is able to display (a) the magnitude of the output voltage, (b) the magnitude of the series inductor current and (c) the magnitude of the parallel inductor current. The simulated voltages and currents are displayed as a function of both load and frequency, and details on the MBT GUI are provided in Appendix D.2. The effects of the mutual inductance on the efficiency of the system cannot be easily assessed with the GUI. In order to obtain “the best” set of inductor values, an optimization algorithm was developed. The code used to perform the inductor design optimization is presented in Appendix D.3. For the rest of the discussion presented, we will assume that we
are dealing with a step-down configuration \((L_x, L_y \text{ and } M_{xy})\); however, the same discussion also applies for a step-up configuration.

The objective of the MBT optimization code is to obtain the \(L_x, L_y \text{ and } M_{xy}\) values which minimize the total loss of the MBT. This is achieved by setting an upper limit on the value of the series element \(L_x\), and sweeping through the possible values of \(L_x, L_y \text{ and } M_{xy}\). The total inductor loss is given by the following equation:

\[
W_{\text{loss}} = R_x \cdot I_x^2 + R_y \cdot I_y^2
\]  

(4.4.1)

where \(R_x \text{ and } R_y\) are the associated loss of the mutually coupled inductors \(L_x \text{ and } L_y\) respectively, and \(I_x \text{ and } I_y\) are the RMS fundamental currents flowing through them. The smallest loss value obtained will be considered the optimal design. If mutual inductance plays no beneficial role in loss reduction, then we expect that \(M_{xy} = 0\), the series inductor \(L_x\) will take the largest possible value (the upper limit of the values swept), and the parallel inductor \(L_y\) will have the same value as in a T-model implementation, for the upper limit \(L_x\) value and established turns ratio. This is what would be expected intuitively if the mutual inductance terms plays no role in loss reduction, since a larger \(L_y\) inductance will translate into a higher impedance, and consequently lower current magnitude in the parallel branch, for the same voltage drop.

Consider as an example a 4:1 step-down configuration design, with a maximum series \((L_x)\) inductance set to 300nH. If no mutual coupling is considered, then the inductor values for the optimal design will be: \(L_x = 300nH\) and \(L_y = 100nH\). If mutual coupling is considered, then the optimization process must be initiated and the steps to be taken are outlined below:

- The inductor values \((L_x, L_y)\) and mutual inductance are swept through a range of values (for example, from 40nH to 300nH with 5nH resolution, with \(M_{xy}\) from -100% to 100% with 1% resolution). For each iteration, the inductor currents \(I_x\) and \(I_y\) are computed.

- The equivalent number of turns for each inductor is obtained based on equation 4.4.2
(assuming a toroid shape for the inductor):

\[ N_{\text{equiv}} = \sqrt{\frac{L \cdot 2\pi}{\mu \cdot h_{\text{via}} \ln \left( \frac{r_{\text{in}}}{r_{\text{out}}} \right)}} \] (4.4.2)

where \( r_{\text{in}} \) and \( r_{\text{out}} \) are the inner and outer radii of a toroid.

- The equivalent number of turns \( N_{\text{equiv}} \) is used to compute the resistance associated with both windings.

- If the voltage transfer function is within reasonable limits of the desired step-up/step-down ratio, then the total loss in the inductors is computed based on equation 4.4.1. If this loss is smaller than the best case recorded up to this point, then the current case becomes the best case and the iteration of the inductor values continues until all inductor value combinations within the given range have been considered.

As an example, the optimization algorithm is applied for an input voltage source of 40V RMS, at 5MHz and a 10Ω output load. The results for the lowest power loss obtained are as follows: \( L_x = 300nH, L_y = 50nH, M_{xy} = 70\% \). The magnitude of the currents obtained for this optimal case were equal to: \( I_x = 2.44A \) and \( I_y = 2.68A \). The maximum loss in the inductors was equal to \( W_{\text{loss}} = 0.32W \).

If no mutual inductance is considered, then for the same input parameters, the following best case scenario results: \( L_x = 300nH, L_y = 100nH \), with \( I_x = 3.23A \) and \( I_y = 3.26A \). The power loss in the inductors is equal to \( W_{\text{loss}} = 0.59W \) which is almost twice as large as the best case when mutual inductance is considered.

The output voltage and inductor currents obtained with the MBT GUI are presented in figure 4.4.2, for 5MHz, a 10Ω output load, and a maximum series inductance \( (L_x) \) of 300nH. Note that there is a drop in voltage for high loads (see Figure 4.4.2(a)), but this is only for output impedances of 1-2Ω. The currents through windings \( L_x \) and \( L_y \) are fairly constant for most of the selected load range (see Figure 4.4.2 (b)-(c)). This optimization process can be applied for
Figure 4.4.2: (a) Voltage output, (b) input current, and (c) parallel branch current as a function of output load and frequency for optimized inductor values.
different frequencies, different geometries, and different upper limits on the inductance values of the elements.
Chapter 5

Mutual Branch Topology Specifications

The Mutual Branch Topology consists of a pair of coupled air core inductors. The first choice in the design of the air-core inductors is the geometrical configuration chosen, which can be, axial, spiral or toroidal. The axial design is used extensively, but in the case of an air-core inductor, it will have a large leakage field since the magnetic field lines are not shaped by any magnetic core with large permeability (such as ferrite E-core or pot core inductors); a similar argument can be made for spiral inductors. While the use of axial and spiral air core inductors is practiced in the signal processing industry (where the power levels, and consequently leakage fields, are smaller), having an axial or spiral power air-core inductor can create EMC issues which will limit the power level at which the converter can operate [25]. The issue of leakage magnetic field is the main reason why a toroidal geometry was chosen, since leakage fields are minimized with such a design.

5.1 Geometry of Toroidal Air-Core Inductor

In order to facilitate and customize the design of the MBT windings, a PCB implementation is chosen. The toroidal inductor has an inner radius ($r_{in}$) and an outer radius ($r_{out}$). The inner circle (with the center at coordinates $x=y=0$) has a series of $N$ vias displaced equidistantly around its circumference, where $N$ is the number of turns of the inductor. The coordinates of
CHAPTER 5. MUTUAL BRANCH TOPOLOGY SPECIFICATIONS

via ‘i’ (with respect to the center of the inner circle) are given by the following equations:

\[ x_i = r_{in} \cdot \sin[(i - 1)\theta] \]  \hspace{1cm} (5.1.1)  
\[ y_i = r_{in} \cdot \cos[(i - 1)\theta] \]  \hspace{1cm} (5.1.2)

in which \( \theta \) is an angle equal to:

\[ \theta = \frac{2\pi}{N} \text{rad} \]  \hspace{1cm} (5.1.3)

The outer set of vias is displaced around a secondary concentric circle of radius \( r_{out} \). The coordinates of outer via ‘i’ is given by the following equations:

\[ x_i = r_{out} \cdot \sin\left[\frac{(2i - 1)\theta}{2}\right] \]  \hspace{1cm} (5.1.4)  
\[ y_i = r_{out} \cdot \cos\left[\frac{(2i - 1)\theta}{2}\right] \]  \hspace{1cm} (5.1.5)

The trace length between the inner and outer vias is equal to:

\[ D = r_{in}^2 + r_{out}^2 - 2r_{in}r_{out}\cos(\theta/2) \]  \hspace{1cm} (5.1.6)

with the position of the corner of upper trace ‘i’ situated at coordinates:

\[ x_{i}^{(u)} = r_{in} \cdot \sin[(i - 1)\theta] + r_{via} \cdot \cos[\pi - \phi - (i - 1)\theta] \]  \hspace{1cm} (5.1.7)  
\[ y_{i}^{(u)} = r_{in} \cdot \cos[(i - 1)\theta] + r_{via} \cdot \sin[\pi - \phi - (i - 1)\theta] \]  \hspace{1cm} (5.1.8)  
\[ z_{i}^{(u)} = -h_{via} \]  \hspace{1cm} (5.1.9)

where \( h_{via} \) is the height of the vias and angle \( \phi \) is equal to:

\[ \phi = \tan^{-1}\left[\frac{r_{out} \cdot \sin(\theta/2)}{r_{out} \cdot \cos(\theta/2) - r_{in}}\right] \]  \hspace{1cm} (5.1.10)
The coordinates for the corner of the lower trace 'i' are:

\[
\begin{align*}
  x_i^{(l)} &= r_{in} \cdot \sin[i\theta] + r_{via} \cdot \cos[\pi - \beta - (i-1)\theta] \\
  y_i^{(l)} &= r_{in} \cdot \cos[(i-1)\theta] + r_{via} \cdot \sin[\pi - \beta - (i-1)\theta] \\
  z_i^{(l)} &= -h_{via}
\end{align*}
\]  

(5.1.11) (5.1.12) (5.1.13)

where \( \beta = \theta - \phi \), and the orientation of the lower trace 'i' is equal to:

\[
  Or_i^{(l)} = -(i-1)\theta - \beta
\]

(5.1.14)

The geometrical construct of a 20 turn air-core inductor based on the geometry outlined above is presented in Figure 5.1.1. The geometrical parameters which can be independently adjusted are as follows: (a) the number of turns (N), (b) the ratio of the outer and inner radii \( r_{out}/r_{in} \), and (c) the ratio of the outer and inner via radii \( r_{out}^{\text{via}}/r_{in}^{\text{via}} \); the values of the inner radius \( r_{in} \) and inner via radius \( r_{in}^{\text{via}} \) are constrained by the total number of turns selected.

Qualitative conclusions can be drawn about the designed air-core inductors by adjusting these three independent parameters (N, \( r_{out}/r_{in} \), \( r_{out}^{\text{via}}/r_{in}^{\text{via}} \)), but only with the help of an air-core inductor circuit model. To this effect, a "per-turn" model was developed.
5.2 Per-Turn Model of the Toroidal Air-Core Inductor

To better account for the inductor non-idealities, a "per-turn" model that includes the interwinding capacitance and the frequency dependent copper loss is introduced. The per-turn model is obtained by considering each individual winding as a separate inductor with self inductance and mutual inductance due to all the other windings.

The circuit model for a three winding air-core inductor is presented in Figure 5.2.1. Interwinding capacitances are associated with every two-turn combination, mutual inductances exist between all pairs of turns, and a resistive term is associated with each individual winding.

![Circuit diagram of the per-turn model for a three turn air-core inductor](image)

Figure 5.2.1: Circuit diagram of the per-turn model for a three turn air-core inductor

The voltage relationship for a single winding can be described based on the following equation:

\[
v_i(t) = L_i \frac{d i_i(t)}{dt} + \sum_{j=0}^{N} M_{ij} \frac{d i_j(t)}{dt}, \quad \text{for} \quad i \neq j
\]  

(5.2.1)

where \( L_i \) is the self inductance and \( M_{ij} \) represents the mutual inductance. If the convention
\( M_{ii} = L_i \) is assumed, then equation 5.2.2 can be rewritten as:

\[
v_i(t) = \sum_{j=0}^{N} M_{ij} \frac{d i_j(t)}{dt}
\] (5.2.2)

The equation for the voltage across the entire inductor can thus be written as:

\[
v_L(t) = \sum_{i=0}^{N} v_i(t) = \sum_{i=0}^{N} \sum_{j=0}^{N} M_{ij} \frac{d i_j(t)}{dt}
\] (5.2.3)

which in phasor form is equal to:

\[
V_L = \sum_{i=0}^{N} V_i(t) = j\omega \sum_{i=0}^{N} \sum_{j=0}^{N} M_{ij} I_j
\] (5.2.4)

### 5.2.1 Inter-winding Capacitance of Per-Turn Model

For a toroidal geometry, every set of traces has associated with it a distributed capacitance. However, this distributed capacitance becomes difficult to compute and impossible to use outside of large scale simulations based on the Finite Element Method (FEM) or the Finite Volume Method (FVM). In order to simplify our computations and obtain a "per-turn" approximate model, we will focus only on the overall capacitance between two toroidal turns as shown in Figure 5.2.2. The model presented here is valid below frequencies for which transmission line effects become apparent. The capacitance between two loops can be approximated as follows:

- Divide each loop into four elements: inner and outer vias, upper and lower traces.
- Compute the total capacitance for every pair of elements and add the results together.

The computation will be done for only four conductor pairs: the inner and outer vias and the upper and lower traces.

The total inter-winding capacitance will be equal to:

\[
C_{inter} = C_{\text{in}}^{(\text{via})} + C_{\text{out}}^{(\text{via})} + 2 \cdot C_{tr}
\] (5.2.5)
Figure 5.2.2: Two adjacent turns for the air core inductor

where $C^{(via)}_{in}$ is the capacitance between the two inner vias, $C^{(via)}_{out}$ is the capacitance between the two outer vias, and $C_{tr}$ is the capacitance between two traces. The distance between the inner vias is equal to:

$$d_{in} = \sqrt{R_{in}^2 + r_{in}^2 - 2r_{in}^2 \cdot \cos(\theta)} = r_{in} \sqrt{2[1 - \cos(\theta)]} \quad (5.2.6)$$

Similarly, the distance between the outer vias is equal to:

$$d_{out} = r_{out} \sqrt{2[1 - \cos(\theta)]} \quad (5.2.7)$$

The capacitance of two parallel and infinitely long wires of radius 'a', that are a distance 'd' apart, was computed analytically [36], and is equal to:

$$C_{wires} = \frac{\rho}{V_1 - V_2} = \frac{\pi \epsilon}{\ln \left( \frac{d}{a} \right)} \quad (5.2.8)$$

This is a reasonable approximation if the length 'l' of the two cylinders is very large when compared with their separation distance 'd' - in this particular case, the validity of the approximation depends on the toroid inner and outer radii and the number of turns. For computing the
capacitance of a pair of wires of length \( l \), an approximate equation as a function of length is used, which is equal to [36]:

\[
C_{\text{wires}} = \frac{\pi \varepsilon l}{\ln \left( \frac{d}{2a} + \sqrt{\frac{d^2}{4a^2} + 1} \right)}
\] (5.2.9)

Equation 5.2.9 will be used to compute the capacitance between the inner and outer vias \( C_{\text{via}}^{\text{in}} \) and \( C_{\text{via}}^{\text{out}} \) respectively). The capacitance between the upper and lower traces \( C_{tr} \) is computed with the help of MATLAB code due to the fact that the distance between the two traces changes depending on your position along either trace.

As an example, for two adjacent loops of a toroid with \( N = 20 \), \( r_{\text{in}} = 2.5\, \text{mm} \) and \( r_{\text{out}} = 6.5\, \text{mm} \), the computed capacitance between the inner vias is equal to 0.66pF, the computed capacitance between the upper and lower traces is equal to 0.17pF, and the computed capacitance of the outer vias is 0.32pF for a total interwinding capacitance of 1.3pF.

### 5.2.2 Resistance Per-Turn Loss

The loss associated with each turn, is due to the copper loss in the traces and vias:

\[
R_L = 2 \cdot R_{tr} + R_{\text{via}}^{\text{(in)}} + R_{\text{via}}^{\text{(out)}}
\] (5.2.10)

where \( R_{tr} \) is the resistance associated with the upper and lower traces, and \( R_{\text{via}}^{\text{(in)}} \), \( R_{\text{via}}^{\text{(out)}} \) are the resistive loss terms associated with the inner and outer vias. Since the inductors should be operated at MHz frequencies, the resistive term \( R_L \) is dependent on the skin depth of copper, which can be approximated by the following formula:

\[
\delta_{Cu} = \sqrt{\frac{2 \cdot \rho_{Cu}}{\omega \cdot \mu_0}}
\] (5.2.11)
where $\rho_{Cu}$ is the resistivity of copper. At 1MHz, the skin depth of copper is equal to approximately 65$\mu$m. The distribution of current density within the copper trace is given by the following formula:

$$J_{tr} = J_s e^{-d/\delta_{Cu}}$$  \hspace{1cm} (5.2.12)

where $J_s$ is the surface value of the current density. This implies that the use of integrals is necessary to extract the AC resistance of the copper traces. In order to simplify the loss calculations, the concept of effective thickness is employed. The assumption made is that the current flux through the copper path is constant (DC conditions), and that the thickness of the traces and vias is equal to one skin depth (if the thickness is greater than one skin depth). The DC equivalent resistance obtained in this manner is a good approximation to the AC resistance of the system at a single frequency, which is a good approximation for the current model. The resistive values of the inner and outer vias are equal to:

$$R_{via} = \frac{h_{tr}}{\pi \left(r_{via}^2 - (r_{via} - \delta_{Cu})^2\right)} \cdot \rho_{Cu}$$  \hspace{1cm} (5.2.13)

and the resistance associated with the PCB trace is equal to:

$$R_{tr} = \int_0^D \frac{\rho_{Cu}}{r_{via} + \left(\frac{r_{via}^{(in)} + r_{via}^{(out)}}{2} \right) \cdot x} \cdot \delta_{Cu} \cdot dx$$  \hspace{1cm} (5.2.14)

Equations 5.2.13 and 5.2.14 are valid when the skin depth of copper is smaller than the trace of the thickness ($\delta_{Cu} < t_{tr}$). If this is not the case, then replace $\delta_{Cu}$ with $t_{tr}$ in equations 5.2.13 and 5.2.14.
5.2.3 Per-Turn Model Analytical Solution

The voltage-current relationship for each loop can be expressed as follows:

\[ V_{Li} = j\omega \sum_{N} M_{ij} I_i \]  
(5.2.15)

Since the loops are identical, the inductances, capacitances and resistances associated with each loop are the same. Because of this, the subscripts from the impedance notations are dropped, and \( L', R' \) and \( C' \) are used instead. This changes equation 5.2.15 to the following:

\[ V_{Li} = j\omega L' \sum_{N} I_i \]  
(5.2.16)

This equation is the same for the voltage across every inductor turn which suggests that \( V_{Li} = V_{Lj} \), or that the voltage drop across the inductance associated with every turn is equal. A voltage source \( V_{in} \) is assumed to be connected to the input terminals, and based on the per-turn model, equations are obtained for the currents flowing through each individual turn.

The first step in obtaining a solution for the per-turn model is to compute the voltages at every node (\( V_1, V_2, ..., V_{N-1} \)). The voltage at the input node is set by the voltage source \( V_0 = V_{in} \). Performing KCL at the first node (\( V_1 \)), results in the following equation:

\[ (V_{in} - V_{L1} - V_1)R'^{-1} = (V_1 - V_{L2} - V_2)R'^{-1} + j\omega R'C'(V_1 - V_3) \]  
(5.2.17)

Since \( V_{L1} = V_{L2} \), equation 5.2.17 can be rearranged as follows:

\[ V_{in} = V_1(2 + j\omega R'C') + V_2(-1) + V_3(-j\omega R'C') \]  
(5.2.18)
The KCL equation at the second node is presented below:

\[
V_{in} = V_1(-j\omega R'C')^{-1} + V_2(1 + j\omega R'C') \cdot (j\omega R'C')^{-1} + V_3(-j\omega R'C')^{-1} + V_4(-1)
\]

(5.2.19)

For every other node denoted as i, except for N-1, the equation obtained from the KCL equation is equal to:

\[
0 = V_{i-2}(-j\omega R'C') + V_{i-1}(-j\omega R'C') + V_i(2 + 2j\omega R'C') + V_{i+1}(-1) + V_{i+2}(-j\omega R'C')
\]

(5.2.20)

All of these N-1 equations can be rearranged in matrix form which will provide a relationship of the following form:

\[
\begin{bmatrix}
V_{in} \\
V_{in} \\
0 \\
... \\
0
\end{bmatrix}
= M
\begin{bmatrix}
V_1 \\
V_2 \\
V_3 \\
... \\
V_{N-1}
\end{bmatrix}
\]

(5.2.21)

where \(M\) is a N-1 \(\times\) N-1 matrix equal to:

\[
M = \begin{bmatrix}
2 + j\omega R'C' & -1 & -j\omega R'C' & 0 & 0 & ... \\
-j\omega R'C' & 2(1 + j\omega R'C') & -j\omega R'C' & -1 & 0 & ... \\
-j\omega R'C' & -1 & 2(1 + j\omega R'C') & -1 & -j\omega R'C' & ... \\
... & ... & ... & ... & ... & ... \\
\end{bmatrix}
\]

(5.2.22)

Inverting matrix \(M\) and multiplying it to the input voltage vector will generate the nodal volt-
The next step in solving the system is obtaining an expression for the current through each loop \( I_1, I_2, ... I_N \) in terms of the nodal voltages. The equation of each current can be expressed in terms of the nodal voltages and the current in the previous loop, as follows:

\[
I_2 = I_1 - j\omega C'(V_1 - V_3) \\
I_3 = I_2 + j\omega C'(V_{in} - 2V_2 + V_4) \\
I_4 = I_3 + j\omega C'(V_1 - 2V_3 + V_5) \\
... I_i = I_{i-1} + j\omega C'(V_{i-3} - 2V_{i-1} + V_{i+1})
\]

Thus, the sum of the per-loop currents can be written in the following form:

\[
\sum_{<N>} I_i = N \cdot I_1 + f(V, V_{in})
\]

where \( f(V, V_{in}) \) is a function of the node voltages obtained by the recursive substitution of \( I_{i+1} \) into \( I_i \) and their summation. The function \( f(V, V_{in}) \) is computed in this manner and it is equal to:

\[
f(V, V_{in}) = N j\omega C'(-V_1 - V_2 + V_{N-1} + V_{in})
\]

The voltage across the per-turn inductance can be expressed as follows:

\[
V_L' = j\omega L'(N \cdot I_1 + f(V, V_{in}))
\]
and using KVL, the following relationship can be extracted:

\[ V'_L = V_{in} - I_1R' - V_1 \]  \hfill (5.2.31)

Equations 5.2.30 and 5.2.31 are combined to provide the following expression for the current \( I_1 \):

\[ I_1 = \frac{-j\omega L' f(V, V_{in}) + V_{in} - V_1}{N \cdot j\omega L' + R'} \]  \hfill (5.2.32)

and by substituting \( f(V, V_{in}) \) from expression 5.2.29, the equation for \( I_1 \) becomes:

\[ I_1 = \frac{(1 + \omega^2 NL'C')(V_{in} - V_1) - \omega^2 NL'C'(V_2 - V_{N-1})}{N \cdot j\omega L' + R'} \]  \hfill (5.2.33)

With the currents per turn determined analytically, the performance of the air-core inductor can be gauged.

### 5.2.4 Comparison of Per-Turn Model with Lumped Inductor Model with Parasitics

The classical lumped inductor model with parasitics is shown in Figure 5.2.3. The inductor

L represents the inductance of the inductor, and \( R_L \) represents the losses of the system (DC resistive loses, AC skin effect loss and dielectric losses). The capacitance in parallel with \( R_L \) and L represents the equivalent capacitance seen between the two terminals of the inductor. The impedance plot of the lumped inductor model with parasitics as a function of frequency
can be seen in Figure 5.2.4. The chosen values were as follows: \( C_L = 1 \text{nF}, L = 1 \mu \text{H}, R_L = 1 \text{m\Omega} \).

![Figure 5.2.4: Impedance plot as a function of frequency of the classic parasitic model](image)

Note that for frequencies lower than the resonant point, the device behaves as an inductor. However, after the resonant frequency (\( \omega_R = 1/\sqrt{L \cdot C_L} \)), the device impedance drops with 20dB per decade; at this point, the device behaves like a capacitor.

The impedance of a toroidal air-core inductor modeled with the per-turn model is presented in Figure 5.2.5, for the following inductor specifications: \( R_{in} = 2.5 \text{mm}, R_{out} = 6.5 \text{mm}, h_{via} = 5 \text{mm} \) and \( N=20 \). Note that the value of the resonant frequency is in the 100’s of MHz region(\( \approx 160 \text{MHz} \)), which suggests that the inter-winding capacitance does not play an important role.

![Figure 5.2.5: Impedance plot as a function of frequency of the ”per-turn” inductor model](image)
for the frequencies of interest (100kHz-10MHz). The agreement of the impedance plot shown in Figure 5.2.5 with the classical lumped model with parasitics (example provided in Figure 5.2.4) suggests that the "per-turn" model provides reasonable predictions of the behavior of a toroidal air-core inductor.

### 5.2.5 Inductor Figures of Merit

The most important figure of merit when assessing high frequency inductors is the quality factor $Q$, defined as follows:

$$Q = \frac{\omega L}{R_L}$$

While the inter-winding capacitance is not included in this definition, in practice it is taken into account since the $Q$ factor is computed as:

$$Q = \frac{\text{Imag}(Z_L)}{\text{Real}(Z_L)}$$

where $Z_L$ represents the impedance of the system, and is affected by the inter-winding capacitance.

Figure 5.2.6 presents the quality factor of the inductor as a function of the ratio of the outer via radius to the inner via radius. The inner via radius is kept constant (0.25mm) while the outer via radius is changed. Note that increasing the radius of the outer vias will increase the quality factor; this is achieved because of the reduction in the copper resistive loss. The benefit of increasing the outer via radius becomes less important for larger $\frac{r_{\text{out}}}{r_{\text{via}}}$ ratios. The outer via radii cannot be increased indefinitely, since they are constrained by the number of turns and the radius of the outer loop. If a separation of $\beta$ mm between adjacent vias is desired, then the following constraint must be met:

$$2 \cdot r_{\text{via}} > r_{\text{out}} \sqrt{2[1 - \cos(\theta)]} - \beta$$

(5.2.36)
As an example, for a 20 turn inductor, with $r_{\text{out}} = 6.5\,\text{mm}$, the radius of the outer vias cannot be larger than approximately 1mm for $\beta = 0.1\,\text{mm}$. If the inner via radius was set to 0.25mm with $\beta = 0.1\,\text{mm}$, then the ratio of the outer to inner via radii cannot exceed 4.

Figure 5.2.7 displays the Q factor of the inductor as a function of the ratio $r_{\text{out}}/r_{\text{in}}$. The quality factor increases with an increase in the outer radius. Similar to Figure 5.2.6, there are diminishing returns to increasing $r_{\text{out}}$ further. A different figure of merit presented in Figure 5.2.8 is defined as follows:

$$FoM = \frac{Q}{r_{\text{out}}} \quad (5.2.37)$$
5.3 Analytical Expression for Computing Inductance of a Toroidal Air-Core Inductor

The inductance of a toroid with $N$ windings has been computed analytically (assuming no leakage fields, or interwinding capacitance) [36], and it is equal to:

$$L_{\text{tor}} = N^2 \mu \cdot \frac{h_{\text{via}}}{2\pi} \ln \left( \frac{r_{\text{out}}}{r_{\text{in}}} \right)$$

(5.3.1)

This formula is a good approximation for a "tightly" wound, single layer toroid with a "large" number of windings. If these conditions are not met, then a slightly modified formula can be
used to obtain the inductance of the system:

\[ L_{\text{eff}} = L_{\text{tor}} - L_{\text{corr}} \]  

(5.3.2)

where \( L_{\text{tor}} \) is given in equation 5.3.1 and \( L_{\text{corr}} \) is obtained from [37]:

\[ L_{\text{corr}} = \frac{\mu}{2\pi} \cdot N \cdot 2(h_{\text{via}} + r_{\text{out}} - r_{\text{in}}) \cdot (G + H) \]  

(5.3.3)

where \( G \) is a figure of merit based on the ratio of the wire diameter and pitch (the spacing between the copper wires), and \( H \) is a correction term based on the total number of turns \( N \). The corrective inductance has a large impact on the effective inductance of the system for loosely wound toroidal structures (large pitch) or for tightly wound inductors with small wire diameter. However, the corrective factor is computed for a fixed value of pitch, which is not the situation for the proposed toroidal geometry since the pitch changes continuously, from the inner to the outer radius (as seen in Figure 5.1.1). The corrective term will be computed with the inner and outer radius pitch separately, and the two results will be averaged. As an example, an air-core inductor with \( N=20 \), \( r_{\text{via}} = 0.25\,\text{mm} \), \( r_{\text{in}} = 2.5\,\text{mm} \), \( r_{\text{out}} = 6.5\,\text{mm} \) and \( h_{\text{via}} = 5\,\text{mm} \) has an inductance of approximately 380nH. The ratio of the diameter to the pitch of the windings for the outer radius is equal to:

\[ \text{pitch} = \frac{2r_{\text{via}}}{r_{\text{out}} \sqrt{2[1 - \cos(\theta)]}} = 0.123 \]  

(5.3.4)

The value of the correction term \( G_{\text{out}} \) is extracted from a look-up table, and is equal to -1.5634. Similarly, the value of \( H \) is equal to 0.2964. This results in a corrective inductance equal to \( L_{\text{corr}}^{(\text{out})} = 72 \cdot (-1.5634 + 0.2964) = -91\,\text{nH} \). Performing a similar calculation on the inner radius of the inductor we obtain that \( G_{\text{in}} = 0.1106 \) and the corrective term is equal to \( L_{\text{corr}}^{(\text{in})} = \)
The averaged corrective term is therefore equal to:

\[ L_{corr} = \frac{L_{corr}^{(out)} + L_{corr}^{(in)}}{2} = -31nH \]  

(5.3.5)

As shown in the example, the corrective term can vary significantly for different pitch values, and it cannot be ignored since it can represent a significant percentage of the analytically computed inductance.

### 5.4 COMSOL Model of Toroidal Air-Core Inductor

The COMSOL 4.3 multi-physics engine was employed to model the inductor behavior, and compare the obtained results with those extracted with the per-turn model and the modified analytical expression presented in section 5.3. The Magnetic and Electric Fields physics model within COMSOL was used to simulate the fields created by the inductor. The equations used to solve the FEM system are as follows:

\[ \nabla \cdot (\sigma \nabla V - \vec{J}_e) = 0 \]  
\[ \nabla \times \nabla \times \vec{A} + \sigma \nabla V = \vec{J}_e \]  

(5.4.1)  
(5.4.2)

where \( \vec{A} \) is the magnetic vector potential and \( \vec{J}_e \) is the externally generated current density.

A fixed voltage or current is imposed at one of the inductor terminals, while the other terminal is set as ground (\( V = 0V \)). The inductance of the system is extracted based on the admittance computed between the two terminals of the system (\( Y_{tor} \)):

\[ L_{tor} = \text{Im} \left( \frac{1}{\omega Y_{tor}} \right) \]  

(5.4.3)

Figure 5.4.1 presents the voltage profile and magnetic flux density lines for a 20 turns air-core inductor. Note that the voltage drop is uniform across the inductor and that the leakage flux is
Figure 5.4.1: COMSOL 4.3 simulation results for 20 turn inductor with magnetic field lines: (a) perspective and (b) top view (dimensions in mm)

small compared to the magnetic flux close to the inner radius $r_{in}$.

Table 5.4.1 presents the results of several COMSOL simulations for different geometrical parameters. The self inductance computed by COMSOL is presented in the $L_{torC}$ column, while the inductance calculated based on the per-turn model is in the second last column of

<table>
<thead>
<tr>
<th>#</th>
<th>N</th>
<th>$r_{in}$</th>
<th>$r_{out}$</th>
<th>$h_{via}$</th>
<th>$h_{trace}$</th>
<th>freq</th>
<th>$L_{torC}$</th>
<th>$L_{torA}$</th>
<th>$\Delta L$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>7</td>
<td>2 mm</td>
<td>10 mm</td>
<td>5 mm</td>
<td>0.15 mm</td>
<td>100kHz</td>
<td>115 nH</td>
<td>79 nH</td>
<td>-45.75%</td>
</tr>
<tr>
<td>2</td>
<td>10</td>
<td>2 mm</td>
<td>5 mm</td>
<td>5 mm</td>
<td>0.3 mm</td>
<td>5MHz</td>
<td>100 nH</td>
<td>92 nH</td>
<td>-9.17%</td>
</tr>
<tr>
<td>3</td>
<td>10</td>
<td>2.5 mm</td>
<td>10 mm</td>
<td>5 mm</td>
<td>0.15 mm</td>
<td>100kHz</td>
<td>171 nH</td>
<td>139 nH</td>
<td>-23.4%</td>
</tr>
<tr>
<td>4</td>
<td>10</td>
<td>2.5 mm</td>
<td>8 mm</td>
<td>5 mm</td>
<td>0.15 mm</td>
<td>100kHz</td>
<td>138 nH</td>
<td>116 nH</td>
<td>-18.5%</td>
</tr>
<tr>
<td>5</td>
<td>10</td>
<td>2.5 mm</td>
<td>7 mm</td>
<td>5 mm</td>
<td>0.15 mm</td>
<td>100kHz</td>
<td>119 nH</td>
<td>103 nH</td>
<td>-15.5%</td>
</tr>
<tr>
<td>6</td>
<td>16</td>
<td>2.5 mm</td>
<td>7 mm</td>
<td>5 mm</td>
<td>0.5 mm</td>
<td>1MHz</td>
<td>253 nH</td>
<td>264 nH</td>
<td>4.0%</td>
</tr>
<tr>
<td>7</td>
<td>16</td>
<td>2.5 mm</td>
<td>6 mm</td>
<td>5 mm</td>
<td>0.5 mm</td>
<td>1MHz</td>
<td>223 nH</td>
<td>224 nH</td>
<td>0.5%</td>
</tr>
<tr>
<td>8</td>
<td>16</td>
<td>2.5 mm</td>
<td>7 mm</td>
<td>7.5 mm</td>
<td>0.5 mm</td>
<td>1MHz</td>
<td>385 nH</td>
<td>395 nH</td>
<td>2.6%</td>
</tr>
<tr>
<td>9</td>
<td>16</td>
<td>2.5 mm</td>
<td>7 mm</td>
<td>7 mm</td>
<td>0.5 mm</td>
<td>5MHz</td>
<td>320 nH</td>
<td>369 nH</td>
<td>13.3%</td>
</tr>
<tr>
<td>10</td>
<td>16</td>
<td>2.5 mm</td>
<td>6 mm</td>
<td>7.5 mm</td>
<td>0.5 mm</td>
<td>1MHz</td>
<td>326 nH</td>
<td>336 nH</td>
<td>3.0%</td>
</tr>
<tr>
<td>11</td>
<td>20</td>
<td>2.5 mm</td>
<td>7 mm</td>
<td>6 mm</td>
<td>0.3 mm</td>
<td>5MHz</td>
<td>446 nH</td>
<td>495 nH</td>
<td>9.8%</td>
</tr>
<tr>
<td>12</td>
<td>20</td>
<td>2.5 mm</td>
<td>7 mm</td>
<td>5 mm</td>
<td>0.3 mm</td>
<td>5MHz</td>
<td>407 nH</td>
<td>412 nH</td>
<td>1.2%</td>
</tr>
<tr>
<td>13</td>
<td>20</td>
<td>2.5 mm</td>
<td>6.5 mm</td>
<td>5 mm</td>
<td>0.3 mm</td>
<td>5MHz</td>
<td>367 nH</td>
<td>383 nH</td>
<td>4.0%</td>
</tr>
<tr>
<td>14</td>
<td>20</td>
<td>2.5 mm</td>
<td>6.5 mm</td>
<td>5 mm</td>
<td>0.3 mm</td>
<td>5kHz</td>
<td>382 nH</td>
<td>383 nH</td>
<td>0.2%</td>
</tr>
</tbody>
</table>

Table 5.4.1: Inductor values obtained with COMSOL 4.3 simulations
the table \((L_{torA})\). The last column presents the percentage difference between the COMSOL computed inductance and the per-turn computed inductance, which is equal to:

\[
\Delta L = \left(\frac{L_{torA} - L_{torC}}{L_{torA}}\right) \cdot 100
\]  

(5.4.4)

The discrepancy between the inductance value computed with COMSOL and the per-turn model is larger for a lower number of turns. This is expected, since the per-turn model requires a ‘large’ number of turns to provide accurate predictions. Another important aspect to note is that the agreement between COMSOL simulations and the per-turn model is greater when the ratio of the outer to inner radius of the inductor is reduced (see simulation examples 3-4 and 6-7 in Table 5.4.1). Finally, the COMSOL and per-turn results show better agreement when \(L_{torC}\) is extracted at lower frequencies (see test examples 8-9 or 13-14 in Table 5.4.1).

Table 5.4.2 presents a comparison between the adjusted analytical inductance values \((L_{eff}\) - see equation 5.3.2) and the inductance values computed with the help of COMSOL. The G and H parameters used to compute equation 5.3.2 are extracted and displayed in Table 5.4.2. Since the value of G is dependent on the ratio of the wire diameter and the pitch (or distance between consecutive windings), two values of G have been computed for each case (one for the inner radius \(G_{in}\) and one for the outer radius \(G_{out}\)), and an average of the two has been used.

Note that when comparing \(\Delta L\) in Table 5.4.1 to \(\Delta L\) in Table 5.4.2, the difference between the two computed sets of inductances is reduced for the first 5 cases (with \(N=7\) and \(N=10\)), but is increased for the rest (\(N=16\) and \(N=20\)). This suggests that the modified analytical expression should be used for a reduced number of turns \(N <= 10\), and the per-turn model should be used for a larger number of turns \(N >= 16\).

The magnetic field generated by the inductor is in large part constrained within the toroidal structure; this is one of the main advantages provided by the toroidal structure chosen - reduced leakage fields. This fact can be seen in the simulation results displayed in Figure 5.4.2 which shows the magnitude of the magnetic flux density vector \(|\vec{B}|\) for a side cross-section through
Table 5.4.2: Inductance calculations comparisons for air core inductors

<table>
<thead>
<tr>
<th>#</th>
<th>N</th>
<th>$G_{in}$</th>
<th>$G_{out}$</th>
<th>H</th>
<th>$L_{tor A}$</th>
<th>$L_{corr}$</th>
<th>$L_{eff}$</th>
<th>$L_{tor C}$</th>
<th>ΔL</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>7</td>
<td>-1.1</td>
<td>-1.97</td>
<td>0.24</td>
<td>79 nH</td>
<td>-47 nH</td>
<td>126 nH</td>
<td>115 nH</td>
<td>8.8%</td>
</tr>
<tr>
<td>2</td>
<td>10</td>
<td>0.11</td>
<td>-0.83</td>
<td>0.27</td>
<td>92 nH</td>
<td>-3 nH</td>
<td>95 nH</td>
<td>100 nH</td>
<td>-5.3%</td>
</tr>
<tr>
<td>3</td>
<td>10</td>
<td>-0.68</td>
<td>-2.44</td>
<td>0.27</td>
<td>139 nH</td>
<td>-65 nH</td>
<td>204 nH</td>
<td>171 nH</td>
<td>16.2%</td>
</tr>
<tr>
<td>4</td>
<td>10</td>
<td>-0.58</td>
<td>-1.97</td>
<td>0.27</td>
<td>116 nH</td>
<td>-42 nH</td>
<td>158 nH</td>
<td>138 nH</td>
<td>12.7%</td>
</tr>
<tr>
<td>5</td>
<td>10</td>
<td>-0.58</td>
<td>-1.75</td>
<td>0.27</td>
<td>103 nH</td>
<td>-34 nH</td>
<td>137 nH</td>
<td>119 nH</td>
<td>13.1%</td>
</tr>
<tr>
<td>6</td>
<td>16</td>
<td>0.11</td>
<td>-0.83</td>
<td>0.29</td>
<td>264 nH</td>
<td>-4 nH</td>
<td>268 nH</td>
<td>253 nH</td>
<td>5.5%</td>
</tr>
<tr>
<td>7</td>
<td>16</td>
<td>-0.12</td>
<td>-1.16</td>
<td>0.29</td>
<td>224 nH</td>
<td>-19 nH</td>
<td>243 nH</td>
<td>223 nH</td>
<td>8.2%</td>
</tr>
<tr>
<td>8</td>
<td>16</td>
<td>-0.12</td>
<td>-1.00</td>
<td>2.29</td>
<td>395 nH</td>
<td>-21 nH</td>
<td>416 nH</td>
<td>385 nH</td>
<td>7.5%</td>
</tr>
<tr>
<td>9</td>
<td>16</td>
<td>-0.12</td>
<td>-1.16</td>
<td>0.29</td>
<td>369 nH</td>
<td>-26 nH</td>
<td>395 nH</td>
<td>320 nH</td>
<td>18.9%</td>
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<tr>
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<td>16</td>
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<td>-1.00</td>
<td>0.29</td>
<td>336 nH</td>
<td>-19 nH</td>
<td>355 nH</td>
<td>326 nH</td>
<td>8.2%</td>
</tr>
<tr>
<td>11</td>
<td>20</td>
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<td>-1.16</td>
<td>0.30</td>
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<td>-29 nH</td>
<td>523 nH</td>
<td>446 nH</td>
<td>14.7%</td>
</tr>
<tr>
<td>12</td>
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<td>0.11</td>
<td>-0.91</td>
<td>0.3</td>
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<td>-8 nH</td>
<td>420 nH</td>
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<tr>
<td>13</td>
<td>20</td>
<td>0.11</td>
<td>-0.83</td>
<td>0.3</td>
<td>382 nH</td>
<td>-4 nH</td>
<td>386 nH</td>
<td>367 nH</td>
<td>5.0%</td>
</tr>
<tr>
<td>14</td>
<td>20</td>
<td>0.11</td>
<td>-0.83</td>
<td>0.3</td>
<td>382 nH</td>
<td>-4 nH</td>
<td>386 nH</td>
<td>382 nH</td>
<td>1.0%</td>
</tr>
</tbody>
</table>

Figure 5.4.2: Plot of $|\vec{B}|$ for a side cross-section through the inductor
the inductor. Note that most of the field is concentrated close to the inner radius, which is as expected.
Chapter 6

Mutual Branch Topology Experimental Results

This section will present the experimental results obtained with customized air-core inductors and the MBT implementation. The first set of tests presented are impedance measurements for stand-alone air core inductors and for a MBT implementation. The second set of tests presented are for two resonant converter implementations, one with a two winding transformer topology, the other with the MLCID and MBT hybrid component. The two resonant switching networks are identical in order to compare the efficiency of the two winding transformer topology with that of the hybrid passive component (MLCID cascaded with the MBT).

6.1 Stand-Alone Inductor Measurements

The PCB design of the air-core inductors was done with the help Altium Designer 10. The purpose of manufacturing stand alone PCB air core inductors is to compare the theoretical and experimentally measured inductance and resistance and account for any difference between the two.

The geometry of two stand-alone inductors is presented in Figure 6.1.1. Note that the first inductor \((L_1)\) has the same radius for the inner and outer vias \((r_{\text{via}}^{\text{in}} = r_{\text{via}}^{\text{out}})\) while the second
Figure 6.1.1: PCB implementation of two stand-alone inductors; $L_1$ on the left hand side and $L_2$ on the right hand side.

The second inductor was built in order to assess how the ratio of the inner to outer via radius affects the total resistance of the inductor. The PCB has a height of 3.1mm and 3oz copper weight (105µm trace thickness). The inner and outer radius of both toroidal structures are 2.5mm and 6.5mm respectively - these two radii are selected in order to obtain a ratio of $r_{\text{out}}/r_{\text{in}}$ close to 2.6 (as shown in Figure 5.9, this ratio provides “optimal” results in terms of quality factor/efficiency). The inner vias have a hole size diameter of 0.25mm and a total diameter (with copper trace) of 0.5mm.

The per-turn model developed in the previous section is used to compute the inductance of the two inductors shown in Figure 6.1.1. The obtained inductance is equal to approximately 230nH for both $L_1$ and $L_2$.

The equivalent resistance of the inductors is also estimated with the per-turn model. The resistance associated with each turn is broken down into 4 components: the resistance asso-
associated with the top and bottom traces, and the resistance associated with the inner and outer radius:

\[ R_{\text{turn}} = 2 \cdot R_{\text{tr}} + R_{\text{via}}^{(\text{in})} + R_{\text{via}}^{(\text{out})} \]  

(6.1.1)

The AC resistances of the traces and vias is computed with the help of equations 6.1.2 and 6.1.3:

\[ R_{\text{via}} = \frac{h_{\text{tr}}}{\pi (r_{\text{via}}^2 - (r_{\text{via}} - \delta_{\text{Cu}})^2)} \cdot \rho_{\text{Cu}} \]  

(6.1.2)

\[ R_{\text{tr}} = \int_{0}^{D} \frac{\rho_{\text{Cu}}}{\left[ r_{\text{via}}^{(\text{in})} + \frac{r_{\text{via}}^{(\text{in})} + r_{\text{via}}^{(\text{out})}}{2D} \right] \cdot x} \cdot dx \]  

(6.1.3)

For \( r_{\text{via}}^{(\text{in})} = r_{\text{via}}^{(\text{out})} \), the equivalent per turn resistance is equal to 3.4m\(\Omega\) at 100kHz and 5.2m\(\Omega\) at 1MHz. For the 20 turn air core inductor, this translates into a total equivalent resistance of 62m\(\Omega\) at 100kHz and 104m\(\Omega\) at 1MHz. Similarly, for the second stand alone inductor with \( r_{\text{via}}^{(\text{out})} = r_{\text{via}}^{(\text{in})} \cdot 3 \), the per turn resistance is equal to 2.7m\(\Omega\) at 100kHz and 4.2m\(\Omega\) at 1MHz; the total resistance is then equal to 54m\(\Omega\) at 100kHz and 84m\(\Omega\) at 1MHz.

Impedance measurements for the inductors shown in Figure 6.1.1 are presented in tables 6.1.1 and 6.1.2. The value recorded with the LCR meter is approximately 70-80nH larger for both \( L_1 \) and \( L_2 \). This difference between theoretical and measured inductance is attributed to the inductance introduced by the input/ground traces together with the leads from the input connector to the measurement device (the inductance of a connector and leads was approximately 40-50nH in a stand-alone measurement). For both inductors, the measured inductance drops slightly with an increase in frequency. However, the inductance does increase for the last frequency measurement (10MHz); this increase is consistent with all measurements performed on air core PCB inductors and is most likely due to resonance with the parasitic capacitance of the entire system (PCB air core inductor and connectors).

The inductor with the larger outer via radii has a lower equivalent resistance (\( R_1 \) compared to \( R_2 \)), as predicted by the per-turn model, but it does not have a significantly larger quality
factor (Q), because the inductance of the toroid decreases for the larger outer to inner via radii ratio case. The measured resistance of the inductors is larger than the theoretically computed resistance. This discrepancy is due to the wires and connectors used to interface the air-core inductors with the LCR measurement unit, due to proximity effects in the inner vias, and due to the via-trace connections which create 90 angles in the winding structures (causing the current to concentrate towards the inner edge of the bends). The quality factor is poor in the kHz range, but it does improve in the MHz range, as expected from air-core inductors.

Several industry manufactured inductors were tested with the LCR meter to provide a baseline for the PCB air-core inductor measurements. Table 6.1.3 presents one such set of impedance measurements, for a 2.2\(\mu\)H ferrite core inductor. Observe that past 1MHz there is a large increase in the measured resistance of the inductor, due to increased core losses, as discussed in Chapter 1. The increase in measured inductance observed at 4MHz and 10MHz is

| freq  | \(L_1\) nH | \(R_1\) m\(\Omega\) | \(Q_1\) | \(|Z_1|\) m\(\Omega\) |
|-------|------------|----------------|--------|-----------------|
| 100 kHz | 310 | 80 | 2.4 | 210 |
| 200 kHz | 309 | 84 | 4.6 | 398 |
| 400 kHz | 306 | 94 | 8.2 | 774 |
| 1 MHz | 300 | 130 | 14.5 | 1,889 |
| 2 MHz | 298 | 163 | 23 | 3,746 |
| 4 MHz | 297 | 209 | 35.7 | 7,463 |
| 10 MHz | 305 | 312 | 61.4 | 19,156 |

Table 6.1.1: Measurements for inductor with \(r_{\text{via}}^{(\text{out})}/r_{\text{via}}^{(\text{in})} = 1\)

| freq  | \(L_2\) nH | \(R_2\) m\(\Omega\) | \(Q_2\) | \(|Z_2|\) m\(\Omega\) |
|-------|------------|----------------|--------|-----------------|
| 100 kHz | 304 | 72 | 2.7 | 204 |
| 200 kHz | 303 | 77 | 4.9 | 388 |
| 400 kHz | 302 | 86 | 9.1 | 763 |
| 1 MHz | 300 | 117 | 16.1 | 1,888 |
| 2 MHz | 295 | 144 | 25.7 | 3,707 |
| 4 MHz | 289 | 187 | 38.8 | 7,262 |
| 10 MHz | 294 | 291 | 63.4 | 18,465 |

Table 6.1.2: Measurements for inductor with \(r_{\text{via}}^{(\text{out})}/r_{\text{via}}^{(\text{in})} = 3\)
most likely due to resonance with a parasitic capacitance of the measurement/device setup.

| freq    | $L_{2R2K}$ nH | $R_{2R2K}$ mΩ | $Q_{2R2K}$ | $|Z_{2R2K}|$ mΩ | $\theta_{2R2K}$ (deg) |
|---------|---------------|---------------|------------|----------------|----------------------|
| 100 kHz | 2162          | 36.6          | 37.9       | 1,359          | 88.5°                |
| 200 kHz | 2139          | 60.5          | 45.1       | 2,689          | 88.7°                |
| 400 kHz | 2122          | 98            | 55.0       | 5,334          | 88.95°               |
| 1 MHz   | 2109          | 199           | 69.3       | 13,247         | 89.14°               |
| 2 MHz   | 2110          | 410           | 66.2       | 26,515         | 89.13°               |
| 4 MHz   | 2135          | 1,600         | 33.6       | 53,690         | 88.3°                |
| 10 MHz  | 2187          | 12,900        | 10.6       | 138,000        | 84.6°                |

Table 6.1.3: Measurements for inductor AIRD-01-2R2K

### 6.2 MBT Impedance Measurements

The first MBT implementation attempted was for a 4:1 step-down configuration. The optimized design parameters obtained with the optimization algorithm shown in Appendix D are:

$L_1 = 300nH$, $L_2 = 50nH$, $k_{12} = 0.7$, where $L_1$ is the series inductor and $L_2$ is the parallel inductor. These are the values used for the 5MHz test case presented in section 4.3. A two core toroid design is performed in the following manner:

- The top, larger toroid shown in Figure 6.2.1 contains part of the windings for inductor $L_1$ and the windings for inductor $L_2$. This first toroid will ensure that the required mutual coupling ($M_{12} = k_{12} \sqrt{L_1 \cdot L_2} \ nH$) is achieved and that the correct value of the self inductance for $L_2$ is obtained.

- The second toroid is used to increase the self inductance value of $L_1$ to the desired 300nH value.

In short, $L_1$ is composed from part of the windings of toroid #1 and toroid #2. The second inductor $L_2$ is composed of the remaining windings on toroid #1 that are not "used" for $L_1$.

The geometrical parameters of the PCB design are as follows:

- The thickness of the board is set based on the available thickness provided by PCB manufacturers - $h_{via} = 3.1\ mm$. 
Figure 6.2.1: Mutual Branch Topology implementation on PCB - top and perspective views

- The first toroid is constructed based on the following values: \( N = 22, \ r_{in} = 2.5\text{mm}, \) and \( r_{out} = 8.5\text{mm}. \) 14 of the 22 windings are part of inductor \( L_1 \) and the remaining 8 are part of inductor \( L_2. \)

- The second toroid is constructed based on the following specifications: \( N = 16, \ r_{in} = 2.5\text{mm} \) and \( r_{out} = 6.5\text{mm}. \)

Two inductor networks were built based on these specifications. One MBT was built with \( r_{via}^{(out)}/r_{via}^{(in)} = 1, \) and a second inductor network with \( r_{via}^{(out)}/r_{via}^{(in)} = 3. \) To differentiate between the two networks, the upper-scripts \(^{(1)}\) and \(^{(3)}\) will be used, respectively. Two sets of measurements were performed with the LCR meter and are presented in tables 6.2.1 and 6.2.2.

The equations describing the behavior of the inductor networks are provided below:

\[
V_1 = j\omega L_1 \cdot I_1 + j\omega M \cdot I_2 \quad (6.2.1)
\]

\[
V_2 = j\omega M \cdot I_1 + j\omega L_2 \cdot I_2 \quad (6.2.2)
\]

\[
V_{appl} = V_1 + V_2 = j\omega (L_1 + M)I_1 + j\omega (M + L_2)I_2 \quad (6.2.3)
\]
Since \( I_1 = I_2 \), the equivalent measured inductance should be equal to:

\[
L_{eq} = L_1 + 2M + L_2 \approx 300nH + 2 \cdot 85nH + 50nH = 520nH
\]  

(6.2.4)

The obtained impedance measurements for \( V_{in}^{(3)} - V_{gnd}^{(3)} \) are in the 540-580nH range while the impedance measurements for \( V_{in}^{(1)} - V_{gnd}^{(1)} \) are in the 590-610nH range. The measured values are larger than the theoretical value (520nH) because of the additional inductance associated with the input traces and the connectors, and because of the unaccounted leakage inductance.

The additional inductance is similar to the \( \Delta L \) obtained in section 6.1 since the geometry of the connector and the windings is similar. Equating \( \Delta L \) to 70nH provides us with an equivalent measured inductance of approximately 500nH value which is fairly close to the theoretical predicted value.

The impedance measurements obtained for both stand-alone air-core inductors and MBTs confirm the fact that the MBT and air core inductor models developed provide accurate predic-
Chapter 6. Mutual Branch Topology Experimental Results

6.3 Converter Specifications and Design

Two resonant converters were built on the same PCB: one converter has a two-winding air-core transformer with a 4:1 step down ratio, while the other converter uses the MBT-MLCID hybrid to provide the required galvanic isolation and 4:1 step down configuration. The resonant converters are DC-AC full bridge inverters operated at 1MHz. Figure 6.3.1 display the circuit setup for the two resonant converters with (a) classical transformer and (b) MBT and MLCID components. It is important to note that the switching networks of the two resonant converters (full bridge implementation, half bridge gate drivers, traces) are completely identical. This is to ensure that the comparison made between the efficiency of the two winding transformer and the MBT-MLCID hybrid component is fair.

Figure 6.3.1: Diagram of converter with (a) classical transformer and (b) MBT with MLCID
The switching network used for both converters is shown in Figure 6.3.2. To ensure that ZVS is achieved for the full bridge converter implementations presented in Figure 6.3.1, two auxiliary inductors (\(L_{R1}\) and \(L_{R2}\)) were used. Details on the resonant converter switching can be found in [38]. The legs of the full bridge resonant converter were controlled by two half-bridge gate drivers. As in the case of the MLCID standalone tests presented in section 3.5, the half-bridge gate drivers were controlled with phase shifted gating signals generated at 1MHz with the help of an Altera DE2 board. The list of relevant components used for the two converter implementations are presented in Table 6.3.1.

![Figure 6.3.2: Switching network for the two resonant converters](image)

<table>
<thead>
<tr>
<th>Manufacturer Part #</th>
<th>Description</th>
<th>Usage</th>
</tr>
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<tbody>
<tr>
<td>SD101AW</td>
<td>Schottky diode</td>
<td>High side gate driver</td>
</tr>
<tr>
<td>445-1316-1</td>
<td>Ceramic capacitor 0.1(\mu)F</td>
<td>Bootstrap capacitor</td>
</tr>
<tr>
<td>TMK107BJ105KA0</td>
<td>Ceramic capacitor 1 (\mu)F</td>
<td>(C_{DC1}) and (C_{DC2})</td>
</tr>
<tr>
<td>08055C5011MAT2A</td>
<td>Ceramic capacitor 0.5nF</td>
<td>In parallel with MOSFETs</td>
</tr>
<tr>
<td>SRN8040-R50Y</td>
<td>Power inductor</td>
<td>(L_{R1}) and (L_{R2})</td>
</tr>
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<td>ED1947</td>
<td>2 Pin conn. 3.81mm</td>
<td>Gating signals and MLCID connection</td>
</tr>
<tr>
<td>ED2454</td>
<td>2 Pin plug 3.81mm</td>
<td>Gating signals and MLCID connection</td>
</tr>
<tr>
<td>LTC4449</td>
<td>Half bridge gate driver</td>
<td>MOSFET switching</td>
</tr>
<tr>
<td>RA 13V1</td>
<td>Schottky diode</td>
<td>Output rectification</td>
</tr>
<tr>
<td>IRLML2030</td>
<td>N-Channel MOSFET</td>
<td>Full bridge inverter</td>
</tr>
</tbody>
</table>

Table 6.3.1: List of relevant components for the two resonant converters

The MBT and two-winding transformer specifications are presented in Table 6.3.2. Note
that the MBT implementation chosen for the resonant converter is different from the one used for experimental impedance measurements presented in section 6.2. A different MBT implementation was chosen in order to obtain a similar footprint for the MBT and two-winding transformer (as shown in Table 6.3.2, most geometrical parameters for the two winding transformer and MBT are identical). Although the chosen MBT parameters (self inductances and mutual inductances) are not "optimal", they result in an MBT-MLCID combination which provides the desired 4:1 step-down ratio. The computed resistance associated with winding $L_1$

<table>
<thead>
<tr>
<th>Classical transformer</th>
<th>$h_{via}$</th>
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<th>1200nH</th>
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<td>5mm</td>
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</tr>
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<td>$M$</td>
<td>300nH</td>
<td></td>
</tr>
<tr>
<td>$r_{via}$</td>
<td>0.25mm</td>
<td>$R_{MLT}$</td>
<td>13.3 mΩ</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Mutual Branch Topology</th>
<th>$h_{via}$</th>
<th>3.1mm</th>
<th>$L_x$</th>
<th>1000nH</th>
</tr>
</thead>
<tbody>
<tr>
<td>$r_{in}$</td>
<td>5mm</td>
<td>$L_y$</td>
<td>110nH</td>
<td></td>
</tr>
<tr>
<td>$r_{out}$</td>
<td>17.5mm</td>
<td>$M_{xy}$</td>
<td>300nH</td>
<td></td>
</tr>
<tr>
<td>$r_{via}$</td>
<td>0.25mm</td>
<td>$R_{MLT}$</td>
<td>13.3 mΩ</td>
<td></td>
</tr>
</tbody>
</table>

Table 6.3.2: Toroidal air-core inductor network specifications

is equal to approximately 540mΩ while the resistance associated with $L_2$ is approximately 150mΩ (for the two winding transformer). The computed resistance of $L_x$ is equal to 470mΩ while the resistance associated with $L_y$ is approximately 230mΩ (for the MBT).

One set of simulation results obtained for the two converters is shown in Figure 6.3.3. The simulation results were obtained with the help of MATLAB Simulink SimPowerSystems, for an output load of 5Ω and assuming the switching network generates a 1MHz 12V peak sinusoidal voltage waveform. The two winding transformer and MBT specifications used are those presented in Table 6.3.2. Note that the input current for the two-winding transformer ($I_{in}$ (a)) is larger when compared to the MBT input current ($I_{in}$ (b)), which results in larger losses for the classical transformer implementation. The output currents for both topologies ($I_{out}$ (a) and $I_{out}$ (b)) are very close in magnitude, as expected.
6.4 Experimental Results

The two implemented converters were operated with several different loads, at 1MHz, and an input DC voltage of 12V. Figure 6.4.1 displays the PCB traces of the two resonant converters. Note that the MBT and transformer have identical geometries (but different number of turns per winding and winding connections) and that the rectifiers, MLCID and loads are connected off board. The figure also highlights where the rectifier and load (or the MLCID plus rectifier and load in the case of the MBT) is connected.

Figure 6.4.2 displays the output converter voltage obtained, for a 20Ω load, for the MBT-MLCID implementation. The output converter voltage has a magnitude of approximately 3V, which exemplifies the 4:1 ratio of the obtained with the MBT-MLCID hybrid component.

The experimental results for the efficiency of the two converters are shown in Figure 6.4.3. The efficiencies were obtained by measuring the voltage drop across the output load, computing
Figure 6.4.1: Layout of the two resonant converters with the transformer and MBT topology

Figure 6.4.2: Output converter voltage across 20Ω load for MBT-MLCID implementation, 1V/div, 500ns/div
the output power, and dividing it by the total input power. Lower values of output resistance were not tested due to the current rating limitation on the MLCID (2A). Note that while the efficiencies are relatively low for both topologies (due to the increased resistance associated with the copper traces and converter losses), the MBT model has better overall efficiency, especially for lighter loads.

This is as predicted by the developed MBT model, and it shows that the hybrid component made up of the MLCID isolation device and the MBT air core inductor network has lower overall losses when compared to the two winding transformer implementation.

Figure 6.4.3: Efficiency measurements for the classic transformer and MBT-MLCID hybrid
Chapter 7

Conclusions

The focus of this thesis has been the development of a high frequency hybrid component comprised of a dielectric isolation device denoted as the Multi-Layer Ceramic Isolation Device (MLCID) and an air core coupled inductor topology denoted as the Mutual Branch Topology (MBT).

The design, modeling, simulation and experimental characterization of the MLCID was the focus of chapters 2 and 3. The MLCID is a four port interleaved planar structure constructed with a sandwich of two different dielectric media. The characteristics of the MLCID were experimentally verified with impedance measurements, voltage transfer function measurements and circuit tests. The MLCID is able to provide high coupling efficiency (high 90% range), ease of manufacturing due to the planar design and good matching between the active and return paths which results in reduced common mode currents.

The advantages of the MBT over a classical two winding transformer are higher efficiency (especially at lighter loads) and lower input currents. These advantages were presented in a set of simulation scenarios presented in Chapter 4. Chapter 5 detailed the modeling of the of air-core inductors along with simulation results. The MBT was designed and created by using traces and vias directly on the printed circuit board and impedance measurements tests were presented to confirm the validity of the model. Finally, galvanic isolation and a 4:1 voltage
step down ratio was achieved by cascading the MBT and MLCID and connecting this hybrid passive component to a resonant converter and load. Efficiency measurements performed for several different loads confirm the modeling and simulation results regarding the MBT-MLCID operation. Although the final converter efficiency was relatively low (65-80%), it was better than the classical two winding transformer implementation, which was the main purpose of the comparison.

The contributions to the field of electrical engineering of the work presented in this thesis are outlined below in point form:

- Modeling and development of a Multi-Layer Ceramic Isolation Device, which is a new type of dielectric isolation device.
- Manufacturing and experimental verification of the MLCID, proving that the device can be used in practical implementations.
- Modeling, development, manufacturing and experimental verification of the Mutual Branch Topology, which is an inductor network topology that provides lower input currents and higher efficiencies when compared to classical transformers, for high operating frequencies.
- Validating the improved performance of the MLCID-MBT hybrid component.
- Development of two Graphical User Interfaces to aid with the design of the MLCID and MBT devices and establishing design procedures for designing such devices.

Future work will include the design and testing of MLCID-MBT devices that will operate at higher frequencies (10-20MHz range), and improving the efficiency of the air-core windings at high frequencies. The technical challenges encountered when operating in the 10-20MHz range are increased losses due to skin and proximity effects, and the lack of appropriate components (MOSFETs, gate drivers) with small turn on/off times. GaN devices in specific circuit
configurations may be able to exploit the benefits of the MBT-MLCID topology at these high switching frequencies.
Bibliography


Appendix A

Resonant Converter Basics

Resonant converters are used for high frequency DC-AC or DC-AC-DC conversion. The main advantage resonant converters provide over traditional hard switched converters is a significant reduction in the switching losses of the circuit. This is particularly important for higher operating frequencies since switching losses \( P_{\text{sw}} \) scale with the square of the converter switching frequency \( f_{\text{sw}} \): \( P_{\text{sw}} \propto f_{\text{sw}}^2 \). The basic configuration for a resonant converter can be broken down into two components: a) the switching network and b) the resonant tank.

The switching network is used to create a square wave voltage waveform with no DC component. This is achieved with the help a full bridge or half bridge inverter. In practice, the switch realization is usually achieved using power MOSFETs; Figure A.1.1 shows a full bridge implementation. The resonant tank is a L-C network which has to be operated around its resonant frequency.

A.1 Converter Operation

The square wave which is generated at the output of the switching inverter has a fundamental frequency which is close to the resonant point of the L-C tank. Thus, the L-C network will act like a filter which will dampen the higher order harmonics of the square wave. This will create output current and voltage waveforms which are sinusoidal, and at the fundamental frequency
Soft switching refers to turning the transistors on/off on the zero-crossing of the current or voltage waveforms. There are two different types of soft switching operation: zero voltage switching (ZVS) or zero current switching (ZCS). Whether you can use ZVS or ZCS in your systems depends on the input load reactance. If the input load is inductive, then ZVS can be applied, while if the input load is capacitive, then ZCS can be applied.

ZVS is best used when the switches are majority carrier devices such as MOSFETs and
Schottky diodes, while ZCS provides better results for minority carrier devices such as BJTs, thyristors, and diffused junction diodes [39]. Figure A.1.2 presents the output current and voltage waveforms of the converter using ZCS. Note that for ZCS, the transistors have a "hard" turn-on and "soft" turn-off, while for ZVS it’s vice-versa. For majority carrier devices, it is preferred to have the "soft" turn-on because the loss associated with the reverse recovery charge of the anti-parallel diodes can be eliminated. This is why ZVS is preferable for MOSFET inverters.

### A.2 Resonant Tank Design

There are several topologies that can be used for the resonant tank of the converter. The most commonly used topologies are the series and parallel L-C, along with the L-C-C and L-L-C topologies, which are shown in Figure A.2.1. The choice of resonant tank topology is usually based on the choice of operating frequency and load profile.

![Resonant Tank Topologies](image)

Figure A.2.1: (a) Series L-C, (b) parallel L-C, (c) L-C-C, and (d) L-L-C resonant tank topologies
Resonant Tank Load Profile

An important part of MOSFET resonant converter design is ensuring that the resonant tank topology and discrete element values are selected such that the transistor conduction losses are minimized at light load, that ZVS is obtained, and that the appropriate voltage output magnitude is achieved. This can be observed for the following parallel L-C tank example.

The frequency profile of the input impedance of the system is shown in Figure A.2.2 for the two output load extremes: short circuit ($|Z_{0}(p)|$) and open circuit ($|Z_{\infty}(p)|$). Note that the two impedance cases ($|Z_{0}(p)|$ and $|Z_{\infty}(p)|$) intersect at a frequency below resonance, denoted as $f_{int}$.

![Figure A.2.2: Input impedance for a L-C parallel tank](image)

If we choose to operate below resonance, and below $f_{int}$, then the input impedance of the converter will be larger for light loads. This is desirable, since it translates into a larger overall impedance, and consequently, lower resonant currents for light loads. However, operation below resonance means that zero-voltage switching cannot be achieved, since the input load is capacitive. If converter operation above resonance is desired, then the converter has lower input impedance for the light load scenario, and as such, the load-efficiency profile will be poor. Therefore, the parallel resonant L-C tank is a poor choice if both ZVS and low conduction losses at light loads are desired.

On the other hand, a series L-C tank is a good choice in terms of load profile, since $|Z_{\infty}^{(s)}| \approx$
\( \infty \) and \( |Z_0^{(s)}| = |Z_\infty^{(p)}| \). This means that for any operating frequency, the light load resonant currents will be smaller than for heavier loads. In conclusion, operation above resonance of the series L-C tank, ensures that ZVS is achieved and that a good load-efficiency profile is obtained. The resonant frequency of the L-C-C topology is dependent on the output load. This can be seen in Figure A.2.3, which displays the open circuit and short circuit input impedance of the L-C-C tank plus output load. Note that if we try to operate above the open circuit resonant frequency (denoted as \( f_{\text{res}}^O \) in Figure A.2.3), then the resonant converter will be able to operate with zero-voltage switching, but the resonant currents will be larger for lighter loads, which is undesirable. The L-C-C configuration has the same design problems as the parallel L-C resonant tank (poor efficiency at light loads).

Lastly the L-L-C resonant tank is an improvement over the series L-C tank since it can operate over a wide load range with very little frequency change, and it can provide a voltage output larger than the voltage input.

**The effect of parasitics on the Resonant Tank**

The resonant tank and the switching network will have parasitics associated with the overall circuit layout, and with the individual lumped elements. These elements will affect the behavior of the resonant tank, as well as potentially change the resonant frequency \( f_{\text{res}} \).
Figure A.2.4 displays a series L-C tank with parasitics. The introduced parasitics are as follows:

- $L_{par}$, which represents the inductance associated with the main current loop, together with the parasitic inductance associated with the lumped capacitor element.

- $R_{loss}$, which is used to symbolize the turn-on resistance of the switches ($R_{DSon}$), together with the winding resistance associated with the inductor and with the equivalent series resistance of the lumped capacitor (ESR), which accounts for wire resistance and dielectric losses.

The capacitance associated with the inductor loops is disregarded due to the fact that it will be insignificant at frequencies around 1MHz. Note that for the series L-C case, the inductance parasitics are in series with the lumped inductor, and as such, do not create new resonant points. The resistance associated with the loss in the system does not influence $f_{res}$, but it does create attenuation between the input and output terminals. In conclusion, $f_{res}$ changes due to the parasitic inductance, but there are no new resonant points created. If the lumped inductor has a value $> 1 \mu H$ and $L_{par} < 10 nH$, then the resonant frequency will not drop more than 0.5%.

For the parallel L-C, L-C-C, or L-L-C topologies, new resonant points are introduced in the load profile due to the parallel branch element. The rest of the parasitics have a similar influence on the circuit as in the series L-C case, with the footnote that the total parasitic series inductance will be lower for the L-C parallel topology. If the new resonant frequency is more
than a decade away from our operating point, then it can disregarded for practical purposes.

This can be ensured by selecting a lumped inductor with a larger value, while proportionally reducing the value of the lumped output capacitance. \( f_{\text{res}} \) will not change, but due to the lower output capacitance (assuming similar parasitic series inductance values), the parasitic resonant frequency will increase.

### A.3 Switching Network Design

The switching network used for the resonant converter is a full bridge bipolar configuration. For lower frequency switching applications, the most important figure of merit for a MOSFET is the turn-on resistance (\( R_{DS(on)} \)), which dominates the converter losses. However, for higher frequencies (above 100’s of kHz), the switching losses start to be a significant component of the total loss.

There are several lumped circuit models available to characterize how MOSFET’s operate, dependent on the type of operation required. The switching dynamics of the device are the main focus due to the fact that for higher frequencies, the switching on-off times become the limiting factor for performance. Figure A.3.1 shows a MOSFET model that is usually used to assess its switching performance.

In most switching applications, the desirable goal is to have the semiconductor switch change between the lowest and highest resistance states in the shortest amount of time possible. The finite practical switching times (\( \approx 10 - 60 \) ns) of a MOSFET [40], are mostly due to the parasitic capacitances, which can be seen in Figure A.3.1. Thus, the switching performance will be determined by how quickly the voltage drops across these parasitic capacitors can be changed. The \( C_{GS} \) and \( C_{GD} \) capacitors can be derived directly from the physical geometry of the MOSFET, while the \( C_{DS} \) capacitor is associated with the body diode effect.

The gate-source capacitance is determined by the overlap between the source-channel region and the gate insulated electrode. In the triode switching region, the value of this capacitor
Appendix A. Resonant Converter Basics

Figure A.3.1: High frequency MOSFET model [40]

is equal to:

\[ C_{GS} = \frac{1}{2} WLC_{ox} \]  \hspace{1cm} (A.3.1)

where \( W \) and \( L \) are the width and length of the channel region, and \( C_{ox} \) represents the electrode capacitance per area [41].

While the \( C_{GS} \) capacitor can be approximated as linear and independent of the applied voltage, \( C_{GD} \) and \( C_{DS} \) are nonlinear capacitors, dependent on the drain to source voltage (\( V_{DS} \)). These capacitors can be approximated by the following two formulas:

\[ C_{GD} \approx \frac{C_{GD0}}{1 + K_1 \sqrt{V_{DS}}} \]  \hspace{1cm} (A.3.2)

\[ C_{DS} \approx \frac{C_{DS0}}{1 + K_2 \sqrt{V_{DS}}} \]  \hspace{1cm} (A.3.3)

where \( C_{GD0} \) and \( C_{DS0} \) are the 0V bias capacitance values, and \( K_1, K_2 \) are constants based on the geometry and doping of the device regions.

However, these three capacitances are usually not specified in MOSFET datasheets. What is usually specified are capacitances \( C_{ISS}, C_{OSS} \) and \( C_{RSS} \). \( C_{ISS} \) is measured when the drain and source terminals are shorted together, \( C_{OSS} \) measurements have the gate and source shorted,
while $C_{RSS}$ has all three terminals (gate, source and drain) shorted. These three figures of merit can be used to obtain an approximation for the three physical capacitances:

\[
C_{GS} = C_{ISS} - C_{RSS} \quad (A.3.4)
\]
\[
C_{GD} = C_{RSS} \quad (A.3.5)
\]
\[
C_{DS} = C_{OSS} - C_{RSS} \quad (A.3.6)
\]

These capacitances cannot be used at the given values because they are obtained for a fixed bias ($V_{DS}$) condition. As seen from equations A.3.2 and A.3.3, $C_{GD}$ and $C_{DS}$ are dependent on the bias voltage. In order to obtain an effective capacitance value, the following adjustments to the above formulae are required:

\[
C_{eff}^{GS} = 2 \cdot C_{RSS} \cdot \sqrt{\frac{V_{DS,spec}}{V_{DS,off}}} \quad (A.3.7)
\]
\[
C_{eff}^{DS} = 2 \cdot (C_{OSS} - C_{RSS}) \cdot \sqrt{\frac{V_{DS,spec}}{V_{DS,off}}} \quad (A.3.8)
\]

The gate to drain capacitance is the most important capacitance parameter for switching applications because it provides a feedback loop between the output and the input. $C_{GD}$ is also known as the Miller capacitance.

**MOSFET Parasitic Inductance**

For high frequency applications (>100kHz), the parasitic source and drain inductance ($L_S$ and $L_D$) can limit the switching performance of the device. The $L_S$ and $L_D$ values are sometimes listed in data sheets and are mainly dependent on the packaging of the power MOSFET. These inductances need to be added to the external parasitic inductances associated with the overall circuit.
Detailed Switch-ON Transistor Behavior

The waveforms for $V_{GS}$, $V_{DS}$, $I_G$ and $I_D$ associated with the turn on dynamics are shown in Figure A.3.2. The switching-on cycle begins with $V_{GS} \approx 0$, $V_{DS} \approx V_{DD}$ and $I_{DS} \approx 0$. Once a gate voltage is applied, the driver starts to charge the $C_{GS}$ capacitance which causes the $V_{GS}$ voltage to slowly rise, until it reaches the threshold voltage $V_t$. During this time interval, also known as the turn-on delay time, the drain current and the voltage across the MOSFET remain unchanged.

In the second time interval (between $t_1$ and $t_2$), $V_{GS}$ rises from the threshold value to the Miller Plateau voltage. The drain current starts increasing linearly with the $V_{GS}$ voltage.

In the third interval, between $t_2$ and $t_3$, the gate-source voltage remains constant, while $V_{DS}$ begins to drop. $V_{GS}$ remains constant because all the gate current from the driver circuit is used to discharge the $C_{GD}$ capacitor which in turn drops the $V_{DS}$ voltage [42]; this time period is the Miller Plateau time interval.

Once $V_{DS}$ drops close to zero, $V_{GS}$ starts increasing to the voltage input value of the driver.
circuit ($V_{DRV}$). This region, between $t_3$ and $t_4$, is characterized by an increase in $V_{GS}$ and a decrease in the gate current $I_G$.

The turn-off procedure will not be covered since it is very similar to the turn-on procedure in reverse. The integral of $I_G$ over this entire switching cycle results in the total gate charge, $Q_G$, required to turn-on the transistor.

**Assessing Switching Performance**

For a 1MHz converter, the sum of the switch turn-on and turn-off times should not be larger than 200ns [43]. The total turn-on and turn-off time can be approximated based on the information extracted from the MOSFT data sheet, by summing together the values given for the turn-on delay time, rise time, turn-off delay time, and fall time:

$$t_{TOT} = t_{d(on)} + t_r + t_{d(off)} + t_f$$  \hspace{1cm} (A.3.9)

However, this does not take into account the Miller Plateau, which is usually larger than the turn-on delay and rise time together. In order to get an appropriate figure of merit for total switch on and switch off times, we can approximate the time interval for the Miller Plateau as twice the turn-on delay and rise time, which will result in a total effective switching time of:

$$t_{eff} = 3 \cdot t_{TOT}$$  \hspace{1cm} (A.3.10)

If $t_{eff} < 200\text{ns}$, then the chosen power MOSFET should be able to provide switching at 1MHz, given the conservative effective switch time estimate. Another figure of merit which can be used to assess the switch performance is the total gate charge.
Gate Charge

The gate charge, $Q_G$, represents the minimum charge required to switch the device on, which corresponds to charging or discharging capacitors $C_{GD}$ and $C_{GS}$:

$$Q_G = Q_{GS} + G_{GD}$$  \hspace{1cm} (A.3.11)

The gate charge value can be used to compute the current required from the gate driver to switch the device on in a certain period of time, or compute the time given a fixed current. This computation is possible due to the following approximation:

$$Q_G = I_{\text{driver}} \cdot t_{\text{ON}}$$  \hspace{1cm} (A.3.12)

This estimation can be used in choosing an appropriate gate driver once the power MOSFET’s are selected.
Appendix B

Review of Capacitor Technologies

Capacitors can be grouped according to the following four technologies:

1. Laminar Dielectric Capacitors
2. Electrolytic Capacitors
3. Double-Layer or Electrochemical Capacitors
4. Multi Layer Ceramic Capacitors

A short review for each capacitor technology will be presented in the following subsections along with any advantages or disadvantages they present.

Laminar Dielectric Capacitors

There are several technologies used to manufacture laminar dielectric capacitors:

1. Foil-laminar dielectric capacitors.
2. Soggy electrode self clearing impregnated high voltage capacitors.
**Foil-Laminar Dielectric Capacitor (FLDC)**

Foil film capacitor designs are usually used for specialized applications such as power systems due to the requirements for high energy density, large discharge currents and low self inductance [44]. However, foil-film technology is not self clearing, which requires operation well below the electric breakdown field. FLDC’s present advantages over metalized film capacitors in high current applications or for designs where a low inductance is required. The low inductance is achieved with the help of a tabbed winding design where the currents in adjacent foils flow in opposite directions, reducing the flux linkage.

Currently, FLDCs are usually made using only foil and polymer film and their main application is for power factor correction devices. In terms of the metallic foils used, the usual choices are either aluminum (as thin as 4µm) and tin/tin alloy (5µm). The thickness of the dielectric is in the range of 8-25µm. There are two main topologies that FLDCs are manufactured in:

- Tabbed windings design.
- Extended foil windings.

The tabbed winding design has metallic tabs (tab ribbons) connected to each metallic foil, for every separate winding. The tab ribbons from each foil are then connected together to form the two ports of the capacitor. The main advantage of this design is the low inductance obtained. The currents from adjacent foils flow in opposite directions within the winding which cancels the magnetic field and thereby reduces the inductance.

In the extended foil design, the metallic layers are offset inwards from the edge of the dielectric (alternating in one direction or another). All of the metallic foils offset in one direction are connected together forming one terminal while all the foils offset in the opposite direction are soldered to form the other capacitor terminal. The main advantage of the extended foil design is that it can tolerate very high current peaks, and as such, it is very useful in pulsed current applications. The achievable peak current is however limited by the larger inductance.
of the design.

Failure of the foil laminar dielectric capacitors usually occurs at the foil edges. When impregnated FLDC’s are overstressed, discharge at the foil edges occurs which creates gas bubbles that promote further discharge and can result in total failure of the device.

**Soggy Electrode Capacitors**

In soggy electrode capacitors, the electrodes are made from metalized paper while the dielectric used is either paper or polymer film impregnated with a dielectric fluid. When electrical breakdown occurs, the metallization of the paper is either evaporated or oxidized, which provides clearing of the breakdown current and allows the device to be operated at higher voltage ratings than non-clearing designs. Soggy electrode capacitors have been mostly replaced by metalized film capacitors, although there is still active research for high energy density devices with respect to this design approach.

**Metalized Film Capacitors (MFC)**

Metalized film capacitors (MFCs) are made from a wide range of polymer films. The polymers are usually low dielectric materials ($\varepsilon_r = 2.2-15$), but have very high breakdown fields (>700 V/µm). The major advantage of metalized polymer film capacitor technology is the fact that the breakdown current is self-clearing [45]. As a result, similar to soggy electrode capacitors, MFCs can be operated at higher voltage ratings, and complete failure of the device is rare. If the dielectric experiences significant carbonization during the breakdown process, then self-clearing is more difficult to achieve. Due to this, some dielectrics have better self-healing properties than others. Furthermore, increasing the metallization resistivity increases the ESR, but it also decreases the clearing energy required.

The terminal connections are the weakness of metalized film capacitor technology. They are usually implemented by a wire arc metal spray at the capacitor ends. The metal spray particles are in liquid form and tend to ”splash” into the small gap between polymer films and
it is believed to cause shrinkage of the film. Furthermore, the metal spray, which is usually Zn or Zn alloy, does not bond well with the aluminum metallization of the film.

Laminar dielectric technology can offer good performance at high operating frequencies and has high breakdown field strength, with the possibility of recovery (self-clearing breakdown current for MFCs). The major disadvantage for the design of the high frequency isolation structure attempted in this thesis is the low permittivity range for laminar dielectrics and the added difficulty of using more than one dielectric in the design of an integrated structure.

**Electrolytic Capacitors**

The aluminum electrolytic capacitors size and voltage rating has increased over the past few years. The obvious limitation regarding electrolytics is the unipolar nature of the device. They also experience significant leakage current and the operating voltage is usually limited to 1kV due to the inability to create a thicker coating of aluminum oxide [46]. This type of capacitor technology will be disregarded for the design of the dielectric isolation device due to the poor high frequency performance it offers.

**Double-Layer Capacitors**

Double-layer or electrochemical capacitors are based on the electric double-layer capacitance formed between ionic conductors and electrons which results in a capacitance per unit volume that is unmatched by any other technology. However, due to the electrochemical process which governs its operation, these capacitors can only be operated at very low frequencies, and as a result, they are mostly used to complement or replace batteries in applications that have rapidly varying loads. The inability to operate at higher frequencies makes double-layer dielectrics unusable in the dielectric isolation device design.
Multi Layer Ceramic Capacitors

The multilayer ceramic capacitor (MLCC) is the most widely used passive device in modern electronics [47]. The multi-layer aspect allows large capacitances to be obtained in a relatively small volume. MLCCs are used mainly for two purposes:

- As passive elements in resonant circuits and filters.
- In power supplies for bypass and decoupling.

The ceramic dielectric materials have a wide range of dielectric properties, with relative permittivity values ranging from as low as 5 to 20,000 and with highly varying temperature dependence. The commercially available ceramics are divided into three main categories:

1. Class I dielectrics have low $\varepsilon_r$ values and very low dissipation factor ($\gg 0.01$). The temperature coefficient is also very low (ppm/$^\circ C$) and linear. Alumina is a class I ceramic dielectric.

2. Class II dielectrics have high $\varepsilon_r$ values (1000 - 20,000) based on ferroelectric ceramics with dissipation factors in the range of 0.01 to 0.03. This type of ceramic has a dielectric constant with moderate-to-high temperature dependence. Barium Strontium Titanate is a class II ceramic and the most commonly used ceramic dielectric material.

3. Class III dielectrics are called barrier layer capacitors. Through a redox process, each grain in the dielectric is made up of a conductive core with a thin insulating shell, or barrier layer. When voltage is applied, the electric field concentrates in the thin insulating shell, resulting in very high capacitance, but low operating voltage, due to the low dielectric breakdown.

The main limitation of ceramics is the difficulty encountered in manufacturing and operating large scale high voltage capacitors. Furthermore, since ceramic capacitors are not "self-clearing devices", they require higher operating safety margins in order to ensure reliable operation. Even though they are not "self-clearing devices", the high range of dielectric permittivity
values (class I and class II), together with the fact that they can be easily used in an integrated structure makes ceramics the best capacitor technology candidate for our dielectric isolation device.

## B.1 Ceramic Capacitor Technology Details

The main advantage of ceramics as insulators is their capability for high-temperature operation without a hazardous degradation in their chemical, mechanical or dielectric properties [47]. To determine the insulation and dielectric characteristics of the material, the following information is required:

1. Relative permittivity or dielectric constant ($\varepsilon_r$).
2. Electrical resistivity $\rho$.
3. Dissipation factor $\tan(\delta)$.
4. Dielectric Strength (DS).

For an AC field, the electrical resistivity, the dielectric constant and the dissipation factor are related by the following formula:

$$\frac{1}{\rho} = \omega \varepsilon_0 \varepsilon_r \tan\delta$$  \hspace{1cm} (B.1.1)

Table B.1.1 presents parameters such as relative permittivity, loss tangent, resistivity and dielectric strength of several type 1 ceramics. These parameters are influenced by several factors such as dielectric thickness, frequency, temperature, humidity and microstructural features such as flaws, cracks or porosity. Permittivity measurements can also be heavily influenced by measurement conditions such as electrode configuration.

The most common dielectric failure of ceramic insulators is due to thermal breakdown. The causes for failure are generally attributed to local heating or conduction losses which produce heat at a faster rate than it can be removed. The thermal gradients that are created in the dielectric can cause cracks to appear which leads to failure of the ceramic.
### Thermal and Mechanical Properties of Ceramics

A material with good thermal conductivity allows heat to be transported effectively, and hence the temperature gradient across the material is low. In the case of ceramics, the highest thermal conduction is obtained for dense, single phase oxides such as BeO, MgO, $\text{Al}_2\text{O}_3$. Microstructural features such as porosity, cracks and second phases generally degrade thermal conduction.

Thermal stresses usually develop in ceramics due to thermal or expansion gradients. Unaddressed thermal stresses can lead to mechanical and dielectric degradation of the ceramic or even complete failure. In order to resist thermal stresses, it is desirable for ceramics to possess high thermal conductivity and high specific heat capacity (increasing the specific heat capacity allows for smaller temperature changes for the same amount of heat generated).

### Dielectric Strength of Ceramics

All insulators lose their insulating properties if the applied field $\vec{E}$ field exceeds a certain value. Dielectric strength is therefore defined as the maximum potential gradient to which a material can be subjected without breakdown occurring:

$$DS = \frac{V_B}{d}$$ (B.1.2)
where $V_B$ is the breakdown voltage and $d$ is the thickness of the sample. Dielectric breakdown usually occurs due to photoionization and collision of electrons with gaseous atoms leading to further ionization and creating an avalanche process. There are three main mechanisms for dielectric breakdown: intrinsic, thermal and ionization.

For high applied fields, electrons can either be ejected from the electrodes or they may be moved to the conduction band from the valence band. These ejected electrons are accelerated through the crystal and some make electron-phonon interactions, generating heat in the process. The electrons colliding with the ions or atoms "knock" out electrons, moving them to the conduction band. These are in turn accelerated and collide with atoms, releasing more electrons. This cascade of electrons being released creates an avalanche of conducting electrons over a narrow area, forming a conducting path through the material - which is what causes the dielectric breakdown. Intrinsic breakdown usually requires very high electric fields ($10^8 - 10^9 V/m$). Due to the high field requirement, usually other breakdown mechanisms are initiated before electronic breakdown.

Thermal breakdown is the most common failure for ceramic insulators. It usually occurs due to excessive local heating generated by losses within the device. The high electric fields increase the temperature in local areas of the ceramic causing temperature gradients to develop. Thermal gradients create thermal stresses that can create cracks or fissures around the hotspot. The local temperature can increase to the point of melting the ceramic or even causing localized evaporation. The combination of ionized high temperature gasses and increased conduction eventually leads to dielectric breakdown.

Ionization breakdown usually occurs in inhomogeneous dielectric solids through the mechanism of partial discharge. Ionization of gases inside the porous structure of ceramics, due to high electric fields, can cause heat generation which is transmitted to the surrounding ceramic, creating a temperature gradient. This causes high thermal stresses, increased dielectric losses and increased local conduction. These stresses can cause cracks leading to further ionization, until breakdown occurs due to a thermal runaway process. Therefore, the presence of porosity
in an insulator is usually detrimental to high dielectric strength materials.

**Polarization in Ceramics**

The macroscopic behavior of a dielectric in an electric field can be described in terms of three vector quantities: the dielectric displacement $\vec{D}$, the electric field $\vec{E}$ and the polarization $\vec{P}$ which are related to the material properties by the following relationship:

$$\vec{D} = \varepsilon_0 \varepsilon_r \vec{E} = \varepsilon_0 \vec{E} + \vec{P} \quad (B.1.3)$$

In a linear isotropic medium, the polarization vector is equal to:

$$\vec{P} = \varepsilon_0 (\varepsilon_r - 1) \vec{E} = \varepsilon_0 \chi \vec{E} \quad (B.1.4)$$

where $\chi$ is defined as the electric susceptibility that relates the polarization of a linear dielectric material to the applied field. Polarization can also be described in terms of a bound charge (surface) density related to the dielectric constant that opposes the surface charge density $\sigma_S$ created by the applied field:

$$P = \sigma_S \left(1 - \frac{1}{\varepsilon_r}\right) \quad (B.1.5)$$

Polarization can also be defined in terms of the number of dipoles created in the material per unit volume:

$$\vec{P} = \alpha N \vec{E}' \quad (B.1.6)$$

where $N$ represents the number of dipoles per unit volume, $\alpha$ is a material property named polarizability and $\vec{E}'$ represents the local field created inside the dielectric which for a linear material is equal to:

$$\vec{E}' = \frac{\varepsilon_r + 2}{3} \vec{E} \quad (B.1.7)$$
Equations B.1.4, B.1.6 and B.1.7 can be combined to create the Clausius-Mosotti equation which relates the dielectric constant to the polarizability of the material:

$$\frac{\varepsilon_r - 1}{\varepsilon_r + 2} = \frac{N\alpha}{3\varepsilon_0}$$

(B.1.8)

The polarizability $\alpha$, which is a true material property, can be decomposed into several terms, each related to a different phenomenon of polarization:

$$\alpha = \alpha_e + \alpha_i + \alpha_o + \alpha_s$$

(B.1.9)

where $\alpha_e$, $\alpha_i$, $\alpha_o$ and $\alpha_s$ represent the electronic, ionic, orientational and space charge polarizabilities respectively.

**Dielectric Relaxation in Ceramics**

When a dielectric is introduced into a capacitor while the external applied voltage is held constant, the energy stored in the capacitor is increased. If a DC electric field, $\vec{E}_{app}$, is applied to the dielectric, then the equilibrium relationship between polarization $\vec{P}_{eq}$ and $\vec{E}_{app}$ is as follows:

$$\vec{P}_{eq} = (\varepsilon_s - 1) \cdot \vec{E}_{app}$$

(B.1.10)

Equilibrium implies that the electric field has been constant for a "long enough" time. If however, $\vec{E}_{app}$ changes with time, then the polarization vector will differ from the equilibrium value: $\vec{P}(t) \neq \vec{P}_{eq}$.

If we make the assumption that the rate of change of the polarization vector as it approaches the equilibrium value is governed by a first order differential equation, then the relationship between $\vec{P}(t)$ and $\vec{P}_{eq}$ can be written as:

$$\tau \frac{d\vec{P}(t)}{dt} = \vec{P}_{eq} - \vec{P}(t)$$

(B.1.11)
where \( \tau \) is referred to as the relaxation constant. This first order differential equation assumption turns out to be a very good approximation for describing the macroscopic behavior of the dielectric.

There are several polarization mechanisms such as electronic, dipolar, ionic or orientational. Electronic polarization is a process which displaces the electronic cloud surrounding an individual atom, creating a dipole moment. The resonant frequency of electronic polarization occurs in the ultraviolet region which suggests that for most electrical and electronic measurements, the time delay between the electrical and polarization fields is negligible. This allows \( \vec{P}(t) \) to be rewritten as follows:

\[
\vec{P}(t) = \vec{P}_D(t) + \vec{P}_\infty
\]

where \( \vec{P}_\infty \) is the electronic polarization vector and \( \vec{P}_D(t) \) represents the remaining polarization processes (dipolar, ionic and orientational). This separation of processes allows for the introduction of electronic permittivity \( \varepsilon_\infty \) as follows:

\[
\vec{P}_\infty = \varepsilon_\infty \cdot \vec{E}_{app}
\]

Equation B.1.13 can be used to rewrite B.1.11 as follows:

\[
\tau \frac{d\vec{P}_D(t)}{dt} + \vec{P}_D(t) = (\varepsilon_s - \varepsilon_\infty)\vec{E}_{app}(t)
\]

Formula B.1.14 is analogous to the differential equation obtained for the charge on a capacitor which is in series with a resistor. Solving this differential equation leads to the complex Debye equations for permittivity as a function of frequency:

\[
\varepsilon'_r = \varepsilon_\infty + \frac{\varepsilon_s + \varepsilon_\infty}{1 + \omega^2 \tau^2}
\]
\[
\varepsilon''_r = \frac{(\varepsilon_s - \varepsilon_\infty)\omega \tau}{1 + \omega^2 \tau^2}
\]
This shows the dispersive behavior of the dielectric material as a function of frequency. Obtaining a good microscopic description of the polarization dynamics is difficult mainly because the dipole moments created in the material influence one another mutually. A dipole within the dielectric is not only subject to the influence of the applied field, but also to other dipoles surrounding it. This mutual influence makes the response of the molecular assembly dependent upon the size, shape and structural arrangement of the dielectric. Because of this, the field "seen" by a dipole inside an insulator is not the applied electric field, but a local or effective field which is usually larger than the applied one.

For the barium strontium titanate and alumina layers used, we assume linear isotropic materials.

**Dielectric Constant and Dielectric Loss**

The charge stored on the electrodes of a parallel plate capacitor can be computed by the formula:

\[ Q = C \cdot V = \epsilon_0 \epsilon_r \frac{A}{d} V \]  

(B.1.16)

where \( \epsilon_r \) is the dielectric material property, while \( A \) and \( d \) are the capacitor dimensions. If we consider an AC field, then equation B.1.16 can be written in phasor form as:

\[ Q = CV_0 e^{j\omega t} \]  

(B.1.17)

The current flowing through the capacitor can then be written as:

\[ I = \frac{dQ}{dt} = j\omega CV \]  

(B.1.18)

For a real capacitor, the current "I" is comprised of two components, defined as \( I_R \) and \( I_C \). \( I_R \) represent the conduction current in phase with the applied voltage \( V \), while \( I_C \) represents a capacitive current proportional to the charged stored on the electrodes. The loss term is due
to the hysteresis between the polarization field and the electric field. The conduction current can be represented by introducing the concept of complex permittivity (only valid for low field strengths), as shown in equation B.1.19:

\[
I = j\omega\varepsilon_0(\varepsilon'_r - j\varepsilon''_r)\frac{A}{d}V = j\omega\varepsilon_0\varepsilon'_r\frac{A}{d}V + \omega\varepsilon_0\varepsilon''_r\frac{A}{d}V = I_C + I_R
\]

The dissipation factor, \(\tan\delta\), is defined as the ratio of the conduction and capacitive current:

\[
\tan\delta = \left| \frac{I_R}{I_C} \right| = \frac{\varepsilon''_r}{\varepsilon'_r}
\]

The dielectric materials used in the manufacturing of the dielectric isolation device prototypes will be characterized based on the loss tangent provided by TRS Technologies Inc. and on the performed impedance measurements.
Appendix C

Models of Dielectric Coupling

C.1 Four plate uniaxial device operation

The basic geometry of the Four Plate Uniaxial Device (FPUD) is displayed in Figure C.1.1. The insulating material between the four conductors is a uniaxial dielectric, which has two different permittivity values associated with it: one permittivity value is encountered in a certain direction, while the other permittivity is encountered in the plane perpendicular to the first direction. The uniaxial dielectric is represented by the grey region between two primary parallel plates denoted as A and A’ and between two secondary parallel plates denoted as B and B’.

The following assumptions will be made in modeling the behavior of this device:

- The dielectric material is lossless and it displays linear polarization behavior.

- Fringing fields between adjacent plates are ignored. This approximation can be made with little loss in accuracy for high permittivity dielectrics (similar to ignoring leakage inductance for high permeability magnetic cores).

- The $\vec{D}$-$\vec{E}$ fields appearing between the four conductor plates are only coupled with the help of the uniaxial material. This assumption implies that in the absence of the uniaxial dielectric, the electric field lines will be perpendicular to the surface of the conductor.
If an input current is applied to the two primary plates (A and A’) it will create a field intensity vector in the z-direction. This also generates an electric field $E_z$ in the z-axis direction which will have to be determined. The equation which relates the input current $i_z(t)$ to the field intensity vector $D_z$ is as follows:

$$i_z(t) = \frac{\partial Q}{\partial t} = S_z \frac{\partial D_z}{\partial t}$$  \hspace{1cm} (C.1.1)

Therefore, the field $D_z$ can be expressed as:

$$D_z = \int i_z(t) dt$$  \hspace{1cm} (C.1.2)

The uniaxial dielectric material can be described by the following second rank susceptibility tensor in the k-y-l coordinate system:

$$\bar{\chi} = \begin{bmatrix} \chi_1 & 0 & 0 \\ 0 & \chi_1 & 0 \\ 0 & 0 & \chi_2 \end{bmatrix}$$  \hspace{1cm} (C.1.3)

The geometry of the applied field and the susceptibility tensor can be seen in Figure C.1.2,
as well as the breakdown of the $E_z$ and $E_x$ electric fields into their k-l components. To de-

compose the $z$-electric field in the k-y-l coordinate system, the matrix $\Omega_{xz-kl}$ is used for the transformation:

$$\Omega_{xz-kl} = \begin{vmatrix} \cos\delta & 0 & \sin\delta \\ 0 & 1 & 0 \\ -\sin\delta & 0 & \cos\delta \end{vmatrix} \quad (C.1.4)$$

Thus, the $E_z$ electric field expressed in the k-y-l coordinate system is equal to:

$$\vec{E}_z^{(kyl)} = \Omega_{xz-kl} \vec{E}_z^{(xyz)} = \begin{vmatrix} \cos\delta & 0 & \sin\delta \\ 0 & 1 & 0 \\ -\sin\delta & 0 & \cos\delta \end{vmatrix} \cdot \begin{pmatrix} 0 \\ 0 \\ E_z \end{pmatrix} = [\hat{a}_k \sin(\delta) + \hat{a}_l \cos(\delta)] \cdot E_z \quad (C.1.5)$$
The dielectric polarization vector is obtained by multiplying the electric field by the $\bar{\chi}$ tensor:

$$
\vec{P}_{Dz}^{(kyl)} = \begin{vmatrix} \chi_1 & 0 & 0 \\ 0 & \chi_1 & 0 \\ 0 & 0 & \chi_2 \end{vmatrix} \begin{bmatrix} \sin(\delta)E_z \\ 0 \\ \cos(\delta)E_z \end{bmatrix} = [\hat{a}_k\chi_1 \sin(\delta) + \hat{a}_l\chi_2 \cos(\delta)]E_z
$$

which expressed in the x-y-z Cartesian coordinate system is:

$$
\vec{P}^{(xyz)}_{Dz} = \Omega_{xz-kl}^{-1}\vec{P}^{(kyl)}_{Dz} = \begin{vmatrix} \cos\delta & 0 & -\sin\delta \\ 0 & 1 & 0 \\ \sin\delta & 0 & \cos\delta \end{vmatrix} \cdot \begin{bmatrix} \chi_1 \sin(\delta) \\ 0 \\ \chi_2 \cos(\delta) \end{bmatrix} E_z
$$

Using the notation $\Delta \chi = \chi_2 - \chi_1$ and simple trigonometric identities, equation C.1.7 is rewritten as:

$$
\vec{P}_{Dz} = [-\hat{a}_x\Delta \chi \sin(\delta) \cos(\delta) + \hat{a}_z(\chi_2 - \Delta \chi \sin^2(\delta))]E_z
$$

$$
\vec{P}_{Dz} = [-\hat{a}_x\chi_{xz} + \hat{a}_z\chi_{zz}]E_z
$$

where $\chi_{xz} = \Delta \chi \sin(\delta) \cos(\delta)$ and $\chi_{zz} = \chi_2 - \Delta \chi \sin^2(\delta)$ are the susceptibilities “seen” by the electric field from the z-direction. Equation C.1.8 emphasizes the fact that the material polarization has vector components in the x and z directions. Note that if the dielectric material is isotropic ($\chi_1 = \chi_2$), then $\chi_{xz} = 0$ and equation C.1.8 simplifies to the established linear relationship for isotropic media: $\vec{P}_{Dz} = \chi_1 \vec{E}_z$.

The electric field generated in the x-direction by the flux intensity vector $D_x$ (which is yet to be determined) can also be broken down into its k-l components:

$$
\vec{E}_{x}^{(kyl)} = \Omega_{xz-kl}\vec{E}_{x}^{(xyz)} = \begin{vmatrix} \cos\delta & 0 & \sin\delta \\ 0 & 1 & 0 \\ -\sin\delta & 0 & \cos\delta \end{vmatrix} \cdot \begin{bmatrix} E_x \\ 0 \\ 0 \end{bmatrix} = [\hat{a}_k \cos(\delta) - \hat{a}_l \sin(\delta)] \cdot E_x
$$
The polarization vector created by $E_x$ will be equal to:

$$\vec{P}_{Dx}^{(kyl)} = \begin{bmatrix} \chi_1 & 0 & 0 \\ 0 & \chi_1 & 0 \\ 0 & 0 & \chi_2 \end{bmatrix} \begin{bmatrix} \cos(\delta)E_x \\ 0 \\ -\sin(\delta)E_x \end{bmatrix} = [\hat{a}_k\chi_1 \cos(\delta) - \hat{a}_l\chi_2 \sin(\delta)]E_x$$

(C.1.10)

If we express this in the x-y-z system:

$$\vec{P}_{Dx}^{(xyz)} = \Omega_{kz-l}^{-1} \vec{P}_{Dx}^{(kyl)} = \begin{bmatrix} \cos\delta & 0 & -\sin\delta \\ 0 & 1 & 0 \\ \sin\delta & 0 & \cos\delta \end{bmatrix} \begin{bmatrix} \chi_1 \cos(\delta) \\ 0 \\ -\chi_2 \sin(\delta) \end{bmatrix} E_x$$

(C.1.11)

which is equal to:

$$\vec{P}_{Dx} = [\hat{a}_x(\chi_2 - \Delta\chi \cos^2(\delta)) - \hat{a}_z \Delta\chi \sin(\delta) \cos(\delta)]E_x = [\hat{a}_x\chi_{xx} - \hat{a}_z\chi_{xz}]E_x$$

(C.1.12)

Equations C.1.8 and C.1.12 can be used to express the x and z components of the $\vec{D}$ field:

$$D_x = \varepsilon_0 E_x + P_{Dx} = [\varepsilon_0 + \chi_{xx}]E_x - \chi_{xz}E_z$$

(C.1.13)

$$D_z = \varepsilon_0 E_z + P_{Dz} = [\chi_{zz} + \varepsilon_0]E_z - \chi_{xz}E_x$$

(C.1.14)

Equations C.1.13 and C.1.14 provide the description of the $\vec{D}$ field in terms of the electric fields. These expressions will be used in order to determine the circuit equations describing the operation of the Four Plate Uniaxial Device (FPUD).

**Current-Voltage Relationship of FPUD**

As defined in equation C.1.14, the electric flux intensity vector in the z-direction is equal to:

$$D_z = [\chi_{zz} + \varepsilon_0]E_z - \chi_{xz}E_x$$

(C.1.15)
and if $D_z$ is substituted from equation C.1.2, the following formula is obtained:

$$\frac{\int i_z(t)dt}{S_z} = \varepsilon_z E_z - \chi_{xz} E_x$$

(C.1.16)

Taking the first derivative with respect to time of equation C.1.16 will create an expression for the current flowing in plate A and out of plate A’:

$$i_z(t) = S_z \varepsilon_z \frac{\partial}{\partial t} E_z - S_z \chi_{xz} \frac{\partial}{\partial t} E_x$$

(C.1.17)

The voltage appearing across the plates A-A’, denoted as $v_z(t)$, it attained by integrating the electric field $E_z$ (assuming no fringing fields):

$$v_z(t) = -\int_b^a \vec{E}_z d\vec{l} = \int_b^a E_z dz = E_z(a - b) = E_z d_z$$

(C.1.18)

In a similar manner, the voltage appearing across plates B-B’ is equal to:

$$v_x(t) = -\int_d^c \vec{E}_x d\vec{l} = \int_d^c E_x dx = E_x d_x$$

(C.1.19)

Using the results from C.1.18 and C.1.19, re-write C.1.17 as follows:

$$i_z(t) = \varepsilon_z S_z \frac{\partial}{\partial t} d_z E_z - \chi_{xz} \varepsilon_z \frac{\partial}{\partial t} d_x E_x = \varepsilon_z S_z \frac{d}{d_z} \frac{d}{dt} v_z(t) - \chi_{xz} \varepsilon_z \frac{d}{d_x} \frac{d}{dt} v_x(t)$$

(C.1.20)

which can be represented as:

$$i_z(t) = C_z \frac{d}{dt} v_z(t) - C_{zx} \frac{d}{dt} v_x(t)$$

(C.1.21)

where $C_z = \frac{\varepsilon_z S_z}{d_z}$ and $C_{zx} = \frac{\chi_{xz} \varepsilon_z}{d_x}$ are the self and mutual capacitances.
In the x-direction, the electric flux intensity vector is expressed as follows:

\[
D_x = (\varepsilon_0 + \chi_{xx})E_x - \chi_{xz}E_z
\]  
(C.1.22)

which by using the charge conservation law, transforms into:

\[
\frac{\int i_x(t)dt}{S_x} = \varepsilon_x E_x - \chi_{xz}E_z
\]  
(C.1.23)

Using a similar method as used for deriving equation C.1.21:

\[
i_x(t) = C_x \frac{d}{dt}v_x(t) - C_{xz} \frac{d}{dt}v_z(t)
\]  
(C.1.24)

where \(C_x = \frac{\varepsilon_x S_x}{d_x}\) and \(C_{xz} = \frac{\chi_{xz} S_x}{d_x}\).

Equations C.1.21 and C.1.24 describe the operation of the four plate device, which is similar to the equivalent voltage equations describing the operation of a transformer. If phasor representation is used, the following equations are obtained:

\[
I_x = j\omega C_x V_x - j\omega C_{xz} V_z
\]  
(C.1.25)

\[
I_z = -j\omega C_{zx} V_x + j\omega C_z V_z
\]  
(C.1.26)

which in matrix form is:

\[
\begin{bmatrix}
I_x \\
I_z
\end{bmatrix}
= j\omega
\begin{bmatrix}
C_x & -C_{xz} \\
-C_{zx} & C_z
\end{bmatrix}
\begin{bmatrix}
V_x \\
V_z
\end{bmatrix}
\]  
(C.1.27)

By taking the inverse of the capacitance matrix and multiplying both sides of C.1.27, the fol-
Following is obtained:

\[
\begin{bmatrix}
V_x \\
V_z \\
\end{bmatrix}
= \frac{1}{j\omega(C_x C_z - C_x C_{xz})}
\begin{bmatrix}
C_x & C_{xz} \\
C_{zx} & C_x \\
\end{bmatrix}
\begin{bmatrix}
I_x \\
I_z \\
\end{bmatrix}
\] (C.1.28)

The geometry of the device imposes two relationships between the plate conductor surface area and the separation distance:

\[S_x = d_z \cdot d_y\] (C.1.29)

\[S_z = d_x \cdot d_y\] (C.1.30)

where \(d_y\) represents the thickness of the device in the y-direction. Therefore, the mutual capacitances \(C_{xz}\) and \(C_{zx}\) are equal to each other:

\[C_{xz} = \frac{S_y \chi_{xz}}{d_z} = d_y \chi_{xz}\] (C.1.31)

\[C_{zx} = \frac{S_y \chi_{zx}}{d_x} = d_y \chi_{xz}\] (C.1.32)

### Development of Capacitive Coupling Circuit Model

The development of the capacitive circuit element follows a similar trend to the development of the transformer model. Define the current \(I'_x\) as follows:

\[I'_x = I_x - j\omega C_1 V_x\] (C.1.33)

where \(C_1\) is an unknown capacitance. The condition imposed on \(I'_x\) is as follows:

\[T \cdot I'_x = -I_z\] (C.1.34)
where \( T \) is a constant. This constraint provides the following relationship:

\[
T[(C_x - C_1)V_x - C_{xz}V_z] = C_{xz}V_x - C_zV_z \tag{C.1.35}
\]

In order for this relationship to hold, the coefficients of \( V_x \) and \( V_z \) on both sides of the equality must be the same:

\[
T(C_x - C_1) = C_{xz} \tag{C.1.36}
\]

\[
T \cdot C_{xz} = C_z \tag{C.1.37}
\]

This system of two equations and two unknowns (\( T \) and \( C_1 \)) generate the next results:

\[
T = \frac{\varepsilon_zS_z}{\chi_{xz}S_x} \tag{C.1.38}
\]

\[
C_1 = \frac{S_x[\varepsilon_x\varepsilon_z - \chi_{xz}^2]}{d_x\varepsilon_z} \tag{C.1.39}
\]

A similar relationship has to be obtained between the voltages \( V_z \) and \( V_x \). For this purpose, \( V_z' \) is introduced as:

\[
V_z' = V_z - KCAI_z \tag{C.1.40}
\]

\[
T \cdot V_z' = V_x \tag{C.1.41}
\]

where \( CA \) is a capacitance that needs to be determined and \( K = \frac{1}{j\omega(C_z - C_{xz})} \). Once the constraint from equation C.1.41 is applied:

\[
T \cdot C_{xz} = C_z \tag{C.1.42}
\]

\[
T \cdot (C_x - CA) = C_{xz} \tag{C.1.43}
\]
Expanding equation C.1.42, the following is obtained for $T$:

$$T = \frac{C_z}{C_{xz}} = \frac{\varepsilon_z S_z}{\chi_{xz} S_x} \quad (C.1.44)$$

which is the same result as the one obtained in C.1.38. The value of $C_A$ is therefore equal to:

$$C_A = C_x - \frac{C_{xz}}{T} = \frac{\varepsilon_x S_x}{d_x} - \frac{\chi_{xz} S_x}{d_x \varepsilon_z} = \frac{S_x (\varepsilon_x \varepsilon_z - \chi_{xz}^2)}{d_x \varepsilon_z} \quad (C.1.45)$$

With the help of C.1.45, the value of the impedance $KCA$ can now be computed:

$$KCA = \frac{d_x d_z}{j \omega S_x S_z (\varepsilon_x \varepsilon_z - \chi_{xz}^2)} \cdot \frac{S_x (\varepsilon_x \varepsilon_z - \chi_{xz}^2)}{d_x \varepsilon_z}$$

$$KCA = \frac{1}{j \omega \varepsilon_x \varepsilon_z} = \frac{1}{j \omega C_z} \quad (C.1.46)$$

All the required tools for developing a capacitive coupling circuit element are now available. The circuit model is based on the next four equations:

$$I'_x = I_x - j \omega C_1 V_x \quad (C.1.47)$$

$$V'_z = V_z - \frac{I_z}{j \omega C_z} \quad (C.1.48)$$

$$T \cdot I'_x = -I_z \quad (C.1.49)$$

$$T \cdot V'_z = V_x \quad (C.1.50)$$

The first two formulae include two capacitive impedances in the model: one parallel connection for $\frac{1}{j \omega \chi_1}$ on the primary ($x$) side, and one series connection for $\frac{1}{j \omega \chi_z}$ on the secondary ($z$) side. The last two formulae provide the relationship between the input currents and voltages of an ideal transformer. The resulting circuit element is shown in figure C.1.3. Note that it is a circuit with an ideal transformer with turn ratios $T:1$ and two capacitive elements. The turns ratio can be either positive or negative (depending on the sign of the dielectric anisotropy $\Delta \chi = \chi_2 - \chi_1$).
and is given by the following formula:

\[
T = \frac{S_z(\Delta \chi \cos^2 \delta + \chi_2)}{S_x \Delta \chi \cos \delta \sin \delta}
\]  
(C.1.51)

**Simulation Results**

If the x-side of the terminals is used to connect a load and the z-side to connect a current source, then everything can be referred to the z-side of the ideal transformer. The original circuit and the equivalent circuit with all impedances referred to the primary side is presented in figure C.1.4.

---

Figure C.1.3: Circuit element for a balanced four plate capacitive coupling device

Figure C.1.4: a) FPUD connected to a resistive load and a source b) Simplified circuit with all loads referred to primary side
The main point to notice about this circuit is that if \( R_{\text{out}} \ll \frac{1}{|\omega C_1|} \) and \( \frac{R_{\text{out}}}{T_2} \ll \frac{1}{|\omega C_z|} \), then there will be a large voltage drop across the capacitor \( C_z \). Thus, in order to transfer power to the load, a very large input voltage \( V_z \) is required. Alternatively, an inductor can be inserted between the source and the FPUD in order to reduce the large voltage drop across the capacitor \( C_z \) and to reduce the reactive power drawn from the source. This will also increase the power factor of the device. The simulation results presented in the following two graphs are obtained by using the input parameters displayed in Table C.1.1. The power output obtained by varying the dielectric susceptibility \( \chi_1 \) and the inclination angle \( \delta \) is shown in Figure C.1.5. Figure C.1.6 shows the required input inductance that would make the source generate no reactive power, for the same dielectric susceptibility and inclination angles. Figures C.1.5 and C.1.6 show that maximum power transfer occurs for the highest dielectric anisotropy and for an angle \( \delta \approx 20^\circ \). The input inductance required for such a device is around 0.7mH. This inductance can be further reduced by increasing the surface of the plates \((S_x \text{ and } S_z)\). An increase in the surface of the plates by a factor of 10 causes a reduction in the inductor size by approximately the same factor. Increasing the frequency also causes a reduction in the requirements for the inductor, while a decrease in frequency has the opposite effect. This change is proportional to the square of the frequency. One issue of note is that the device has to be operated at a high frequency (10-100MHz) to maintain an acceptable inductor size for the given geometrical parameters. If, for example, the device is operated at 1MHz, the inductor size will be on the order of Henries.

The required large inductive element, together with the lack of uniaxial materials with large relative permittivity values and low losses (high losses appear in large permittivity uniaxial dielectrics due to relaxation modes such as the Goldstone relaxation mode in ferroelectric liquid
crystals) has made the manufacturing of a FPUD impractical.
C.2 State Space Model for a Four Parallel Plate Interleaved Structure

Figure C.2.1 presents the system under study, where a current source is used as the input to our capacitor network, used to represent a four parallel plate interleaved structure.

The three state variables and the input are as follows: \( x_1 = v_1, x_2 = v_2, x_3 = v_3 \), and \( u = i_S \).

The three equations describing the behavior of the system are the three KCL equations at nodes 1, 2 and 3 respectively:

\[
\begin{align*}
    u - C_{1g} \dot{x}_1 - C_{12} (\dot{x}_1 - \dot{x}_2) &= 0 \\
    C_{12} (\dot{x}_1 - \dot{x}_2) - C_{2g} \dot{x}_2 - C_{23} (\dot{x}_2 - \dot{x}_3) - R_L^{-1} (x_2 - x_3) &= 0 \\
    -C_{g3} \dot{x}_3 + C_{23} (\dot{x}_2 - \dot{x}_3) + R_L^{-1} (x_2 - x_3) &= 0
\end{align*}
\]

In matrix form, these equations are represented as follows:

\[
\begin{bmatrix}
    -C_{1g} - C_{12} & C_{12} & 0 \\
    C_{12} & -C_{12} - C_{2g} - C_{23} & C_{23} \\
    0 & C_{23} & -C_{g3} - C_{2g}
\end{bmatrix}
\begin{bmatrix}
    \dot{x}_1 \\
    \dot{x}_2 \\
    \dot{x}_3
\end{bmatrix}
= \begin{bmatrix}
    0 & 0 & 0 \\
    0 & R_L^{-1} & -R_L^{-1} \\
    0 & -R_L^{-1} & R_L^{-1}
\end{bmatrix}
\begin{bmatrix}
    x_1 \\
    x_2 \\
    x_3
\end{bmatrix}
+ \begin{bmatrix}
    -1 \\
    0 \\
    0
\end{bmatrix}
\begin{bmatrix}
    x_1 \\
    x_2 \\
    x_3
\end{bmatrix}
\]

\[u, \quad (C.2.4)\]
We now have a state equation of the form:

\[ H_3 \dot{x} = P_3 x + Q_3 u \]  
(C.2.5)

Matrix \( H_3 \) on the right side of equation C.2.5 is invertible since all the column vectors are linearly independent. To obtain the system of equations in standard form, we multiply both sides of equation C.2.4 by \( H_3^{-1} \):

\[ \dot{x} = H_3^{-1} P_3 x + H_3^{-1} Q_3 u \]  
(C.2.6)

Since matrix \( P_3 \) is singular, the resulting matrix \( H_3^{-1} P_3 \) will also be not invertible.

**Transfer Function of the Four Parallel Plate Interleaved Structure State Space System**

In order to obtain the input to output current transfer function for the three state variable system, we use the \texttt{ss2tf} function in MATLAB. This function has as input the \((A, B, C, D)\) matrix pair and outputs the nominator and denominator coefficients of the transfer function. The capacitor values used were computed by using the current information given by TRS technologies (dielectric thickness of 150µm, relative permittivity values of 1300 and 9).

The transfer function corresponding to the 3 state variable system is equal to:

\[ G_3(s) = \text{ss2tf}(A_3, B_3, C_3, D_3) = \frac{4.682 \cdot 10^8 s^2}{s^3 + 4.747 \cdot 10^8 s^2} \]  
(C.2.7)

where \( A_3 = H_3^{-1} P_3 \), \( B_3 = H_3^{-1} Q_3 \), \( C_3 = \begin{bmatrix} 0 & R_L^{-1} & -R_L^{-1} \end{bmatrix} \) and \( D_3 = 0 \).

The bode plot of transfer function \( G_3(s) \) is shown in Figure C.2.2. Note that the magnitude of the transfer functions is close to 0dB, which is as expected. This means that most of the input current from the source will flow through the output load.
Figure C.2.2: Bode plot for the $G_3$ transfer function
Appendix D

Graphical User Interfaces and Code Optimization

D.1 MLCID Graphical User Interface

The MLCID GUI is a MATLAB applet which allows the user to simulate the behavior of a multi-layer capacitor. The user has control over a series of parameters pertaining to the multi layer dielectric coupling device such as:

- The total area of the electrode plates ($mm^2$).
- The dielectric thickness or spacing between the plates ($\mu m$).
- The plate overlap between the set of input and output plates (%).
- The values of the voltage source inductor (nH) and resistor ($m\Omega$).
- The equivalent series resistance ($m\Omega$) and inductance(nH) which appears between each adjacent set of electrodes.
- The relative permittivity of the two different dielectrics used.
- The number of 4 electrode stacks which form the device.
The user also has control over the type of input source used (voltage or current source) as well as the magnitude of the input voltage (V) or current (A) and the magnitude of the output load (Ω). Once the above parameters are set, the user has the option of displaying a series of graphs such as:

- The input to output magnitude of the voltage $G_{io}^v$ and current $G_{io}^i$ transfer function.
- The ratio between the input and output real power both with and without a resonant inductor placed in parallel with the output load in order to increase this ratio.
- The magnitude of the input and output voltage, as well as the total output power, with or without the resonant inductor.

Finally, the GUI allows for the transfer functions to be plotted as a logarithmic function of frequency or as a function of the output load. The MLCID GUI is shown in Figure D.1.1, which displays the $G_{io}^v$ and $G_{io}^i$ of a given multi-layer capacitor configuration.

![Figure D.1.1: Main display window of the MLCID GUI](image)

**MLCID GUI Modeling Details**

The computations performed by the MLCID GUI are based on a main function called 'compute_parameters’ which is called whenever a change is made to the design parameters. When
'compute parameters' is called, the physical parameters related to the design of the MLCID are stored in variables (such as the thickness of the dielectric and their permittivity values, the surface of the plates, and the type of sweep - load or frequency). Once these design parameters are retrieved, the function computes all the capacitances present in the capacitor network by using the following formulas:

\[
\begin{align*}
C_{1g} &= \varepsilon_{\text{low}} \cdot \left(1 - \frac{\text{plate overlap}}{\text{surface area}} \right) \cdot \frac{2 \cdot t_{\text{dielectric}}}{t_{\text{dielectric}}} \\
C_{12} &= \varepsilon_{\text{high}} \cdot \frac{\text{plate overlap} \cdot \text{surface area}}{t_{\text{dielectric}}} \\
C_{2g} &= \varepsilon_{\text{low}} \cdot \frac{\text{plate overlap} \cdot \text{surface area}}{t_{\text{dielectric}}} \\
C_{g3} &= \varepsilon_{\text{high}} \cdot \frac{\text{plate overlap} \cdot \text{surface area}}{t_{\text{dielectric}}} \\
C_{23} &= \varepsilon_{\text{low}} \cdot \left(1 - \frac{\text{plate overlap}}{\text{surface area}} \right) \cdot \frac{2 \cdot t_{\text{dielectric}}}{t_{\text{dielectric}}} 
\end{align*}
\] (D.1.1)

The equivalent series inductance (ESL) as well as the loss tangent are extracted from the user input. The function then checks if the user requires frequency or load sweep plots - and defines the required frequency or load array for the sweep.

The equivalent series resistance (ESR) associated with all capacitors from the capacitor network is computed next (based on the loss tangent of the device and the surface area of the plates) as well as the impedances associated with every branch:

\[
\begin{align*}
Z_{1g} &= \frac{1}{i \omega_0 C_{1g}} + i \omega_0 \text{ESL} + \text{ESR}_{1g} \\
Z_{12} &= \frac{1}{i \omega_0 C_{12}} + i \omega_0 \text{ESL} + \text{ESR}_{12} \\
Z_{2g} &= \frac{1}{i \omega_0 C_{2g}} + i \omega_0 \text{ESL} + \text{ESR}_{2g} \\
Z_{g3} &= \frac{1}{i \omega_0 C_{g3}} + i \omega_0 \text{ESL} + \text{ESR}_{g3} \\
Z_{23} &= \frac{1}{i \omega_0 C_{23}} + i \omega_0 \text{ESL} + \text{ESR}_{23} 
\end{align*}
\] (D.1.2)
The function then checks whether the input source is a current or a voltage source, and assigns variables for input parameters such as the input resistance and inductance, magnitude of the input source and output load. Once all the required parameters have been assigned to temporary variables and the impedance for each branch has been computed, the function creates a matrix which describes the input-output relationship of the device.

### The Input-Output Matrix M

If a current source configuration of \(n\) stacks is considered, the parameter matrix \(M_I\) is represented as shown in equation D.1.3.

\[
M_I = \begin{pmatrix}
(2n - 1)Z_{1g}^{-1} + nZ_{12}^{-1} + (n - 1)Z_{2g}^{-1} & -nZ_{12}^{-1} & -(n - 1)Z_{2g}^{-1} \\
-nZ_{12}^{-1} & nZ_{12}^{-1} + (2n - 1)Z_{23}^{-1} + Z_L^{-1} & -(2n - 1)Z_{23}^{-1} - Z_L^{-1} \\
-(n - 1)Z_{2g}^{-1} & -(2n - 1)Z_{23}^{-1} - Z_L^{-1} & (n - 1)Z_{2g}^{-1} + nZ_{12}^{-1} + (2n - 1)Z_{23}^{-1} + Z_L^{-1}
\end{pmatrix}
\] (D.1.3)

Increasing the number of stacks for a MLCID device increases the total capacitance values, and as a result it decreases the total reactive impedance of the system. This will, in theory, allow for the design of MLCID devices that operate below the MHz range if enough stacks are used \((< 20)\). For a voltage source input, the parameter matrix \(M_V\) for an \(n\)-stack configuration is shown in equation D.1.4. The only difference between matrices \(M_I\) and \(M_V\) appears on the first row, due to the input series inductance and resistance, and because the input to our system is a voltage source, not a current source. In order to solve for the voltage and currents in the system, we invert matrix \(M\) as follows:

\[
\begin{bmatrix}
V_1 \\
V_2 \\
V_3
\end{bmatrix} = \begin{bmatrix}
M_n^{-1}
\end{bmatrix} \begin{bmatrix}
u \\
0 \\
0
\end{bmatrix}
\] (D.1.5)
where 'u' represents the input source which can either be $V_{in}$ or $I_{in}$.

In the MATLAB GUI implementation, the value of every matrix element $M$ is computed separately in variables defined as '$a_{ij}$'. These matrix element variables are then used to compute the determinant of the matrix as follows:

$$
det_{M} = a_{11}(a_{33}a_{22} - a_{32}a_{23}) - a_{21}(a_{33}a_{12} - a_{32}a_{13}) + a_{31}(a_{23}a_{12} - a_{22}a_{13}) \tag{D.1.6}
$$

Only 3 matrix elements are computed for the inverse matrix $M^{-1}$:

$$
b_{11} = \frac{a_{33}a_{22} - a_{32}a_{23}}{det_{M}} \\
b_{21} = -\frac{a_{33}a_{21} - a_{31}a_{23}}{det_{M}} \\
b_{31} = \frac{a_{32}a_{21} - a_{31}a_{22}}{det_{M}} \tag{D.1.7}
$$

These are the only elements required from the inverse matrix in order to determine the voltages at every node and the current in every branch for both the current or voltage source configurations:

$$
V_{1} = b_{11} \cdot u \\
V_{2} = b_{21} \cdot u \\
V_{3} = b_{31} \cdot u \tag{D.1.8}
$$

If the design parameters for the PCB board are used, without any parasitics, then the input-output voltage transfer function can be seen in Figure D.1.2.

Introducing an equivalent series inductance for every capacitor branch in the capacitor network, will cause the transfer function to change, as shown in Figure D.1.3.

The shape of the transfer function in this particular case is similar to the results obtained for the interleaved parallel plate PCB board with the 4695A Network Analyzer from Agilent. The transfer function obtained with the help of the network analyzer is shown in Figure D.1.4 for comparison purposes.
If mutual inductance is introduced between the ESL present in every branch, then the system can be solved by mesh analysis. The system is setup in a similar manner to the previous section, except that the parameter matrix will be $4 \times 4$ (denoted by $H$). The system of equations has the
Figure D.1.4: Input-output transfer function of PCB board obtained using an Agilent 4395A network analyzer

Following form:

\[
\begin{bmatrix}
I_A \\
I_B \\
I_C \\
I_D
\end{bmatrix} = H^{-1} \begin{bmatrix}
u \\
0 \\
0 \\
0
\end{bmatrix}
\] (D.1.9)

where \(I_A-I_D\) represent the mesh currents and \(u\) represents the voltage input.

The new parameter matrix \(H\) will be equal to the following:

\[
H = \begin{bmatrix}
Z_{1g} & -Z_{1g} - 2i\omega M & i\omega M & 0 \\
-Z_{1g} - 2i\omega M & 4i\omega M + Z_{1g} + Z_{12} + Z_{2g} & -Z_{2g} - 2i\omega M & i\omega M \\
i\omega M & -Z_{2g} - 2i\omega M & 4i\omega M + Z_{g3} + Z_{2g} + Z_{23} & -Z_{23} - 2i\omega M \\
0 & i\omega M & -Z_{23} - 2i\omega M & Z_{23} + Z_{out}
\end{bmatrix}
\] (D.1.10)
As in the case of the $3 \times 3$ matrix, $H$ will have to be inverted in order to obtain the mesh currents $I_A - I_D$. This inversion is done manually, by computing the matrix elements $a_{ij}$ individually and then generating specific elements of the inverted matrix ($b_{11} - b_{41}$). Only 4 elements are required of the inverted $H$ matrix to solve for the mesh currents, as seen from equation D.1.9. The following equation is used to compute the voltage TF:

$$G_{io}^v = b_{41} \cdot Z_{out}$$  \hspace{1cm} (D.1.11)

since $I_D = b_{14} \cdot u$ and $V_{out} = I_D \cdot Z_{out}$.

The $G_{io}^v$ is plotted as a function of frequency in Figure D.1.5.

Note that the transfer function is slightly different when using mutual coupling between the ESLs, since it has an additional pair of complex zeros and poles. However, the location of the local minima (complex zero frequencies) have not shifted in frequency in any significant manner if we compare them to the ones in Figure D.1.3. This is because the mutual inductances do not alter the ESL values of the matrix elements. We can thus disregard mutual coupling between the equivalent series inductances.
Mutual Inductance Loops

In the previous mutual inductance simulations, mutual inductance was assigned between the different ESLs. However, inductances are associated with loops, not with individual branches. Note that each of the four loops has an inductance associated with it, and that each of these inductances have mutual coupling with each other. This setup can also be solved by setting up the equations in matrix form as follows:

\[
\mathbf{H} \begin{bmatrix} I_A \\ I_B \\ I_C \\ I_D \end{bmatrix} = \begin{bmatrix} u \\ 0 \\ 0 \\ 0 \end{bmatrix}
\]  \hspace{1cm} (D.1.12)

where \( \mathbf{H} \) is the parameter matrix.

In the case of no mutual coupling between the loops, the \( G_{io}^V \) transfer function is displayed in Figure D.1.6, along with the root locus of the system. This system has 8 poles (4 complex pairs) and one zero at the origin.

![Root Locus and Transfer Function](image)

Figure D.1.6: Voltage TF with no mutual coupling

The results of this simulation show large discrepancy when compared to the PCB TF ob-
tained with the network analyzer. By adding mutual inductance branches, the number of zeroes in $G_{iv}$ increases, as expected. However, the corner frequencies of the pole/zero pairs are in the 100’s of MHz range, unless a very large inductance ($L$) is used. Mutual inductances between different current loops can therefore be disregarded in the analysis of the dielectric coupling device.

**Efficiency and Ideal Power Transfer**

A MLCID can transfer power from the input to output with a certain efficiency. This efficiency represents the ratio of the output to input power and is dependent on both the operating frequency and on the value of the output load. The factors which affect this power ratio are the losses associated with the dielectrics and the Au/Cr electrodes. The dielectric losses can be computed based on the loss tangent of the ceramic materials and the input frequency, while the conductor losses can be estimated based on the geometry and conductance of the electrodes, along with the resistance of the input voltage source.

This information, together with the developed circuit model, allows for the generation of efficiency meshes with the help of the MLCID GUI, as shown in Figure D.1.7. The x-axis represents the logarithm base 10 of the output resistance while the y-axis represents the logarithm base 10 of the input frequency. Note that the efficiency is high for certain load/frequency ranges, which forms a ”diagonal band” across the mesh. The position of this band is affected by factors such as the effective capacitance values between different plates. Thus, if we increase the area of the plates or decrease the dielectric thickness, the high efficiency band will shift towards lower frequencies. The same behavior can be observed if the permittivity of the layers are increased (as long as the permittivity ratio remains the same) or if the number of dielectric stacks is increased. The width of the high efficiency band is determined by 2 parameters of the MLCID: the permittivity ratio of the dielectric, and the loss tangents of the ceramics. If the permittivity ratio is decreased or the loss tangent increased, then the high efficiency band becomes narrower.
Figure D.1.7: 20 Layer MLCC efficiency as a function of load and frequency

The main conclusion that can be drawn from these simulations is that good efficiency can be obtained even for lower frequencies (100kHz range) by changing the geometry of the device. On the other hand, increasing the efficiency band width is harder to achieve because it requires tweaking of parameters that are related to material properties (permittivity and loss tangent) rather than to the geometry of the design.
D.2 MBT Graphical User Interface

The MBT Graphical User Interface is used to assess the MBT capability to step-up/step-down the voltage over a given load/frequency range, as well as observe the magnitudes of the series and parallel branch currents over the same load/frequency range. The MBT GUI cannot be used as a stand-alone tool, since it cannot provide the user with an optimized MBT design for a given set of parameters. This optimized MBT design is achieved with the help of the optimization algorithm presented in Appendix D.3. However, the MBT GUI allows the user to determine the selected MBT behavior over a frequency/load range, which the optimization algorithm is unable to do. Figure D.2.1 shows the layout of the MBT GUI.

Figure D.2.1: Mutual Branch Topology Graphical User Interface

The input parameters for the MBT GUI are as follows:

- The series inductance $L_x$.
- The parallel inductance $L_y$.
- The mutual coupling between the two inductors $k_{xy}$.
- The magnitude of the input voltage $V_{in}$. 
The GUI uses the circuit model developed in Chapter 4, and can provide the following surface plots:

- The output voltage $V_{out}$.
- The required input current $I_{in}$.
- The parallel branch current $I_m$.

### D.3 MBT Optimization Code

The MBT optimization code is used to obtain the optimal inductance values for the MBT inductor network. The code used to obtain the "best" $L_x$, $L_y$ and $M_{xy}$ values is shown below:

```matlab
%MBT OPTIMIZATION CODE
%----------------------------------------------
%Material Constants
mu_0 = 4*pi*10^-7;
Rho_Cu = 1.68*10^-8;
perm_high =1300 *8.85*10^-12;
perm_low = 9*8.85*10^-12;
l1 = 0.15; l2 = 0.68;

%Operational Parameters of Simulation
V_in = 10; Input_Vector = [V_in, 0, 0]'; %Input voltage
freq = 5*10^6; w0 = 2*pi*freq; % frequency of operation
Z_out = 10; %Output Load
d_1 = 10^-2; d_2 = 10^-2; %Inductor trace length
width_1 = 10^-3; width_2 = 10^-3; l_g = 10^-3; %Initial Inductor trace dimensions
skin_d = sqrt(2*Rho_Cu / (w0 * mu_0)); %Skin depth
R_out = 6.5e-3; R_in = 2.5e-3; h_via = 3e-3;
r_via = 0.25e-3; r_via_2 = 0.75e-3; th_trace = 70e-6;

if (skin_d>r_via) cyl_skin = 0; else cyl_skin = r_via - skin_d; end
if (skin_d>r_via_2) cyl_skin_2 = 0; else cyl_skin_2 = r_via_2 - skin_d; end

%Temperature consideration for width of inductor copper trace
b = 0.44; k =0.048; c = 0.725; delta_T = 25;
```
k_T = (k*delta_Tˆb)ˆ(1/c)*skin_d*39.37;

% Geometry of MLCID
thickness_diel = 150*10^-6;
surface_area = 10^-4;
plate_overlap = 1;
n = 5; % number of stacks

% Capacitances of the capacitance matrix for MLCID
C_1g = perm_low .* (1-plate_overlap) .* surface_area./(2.* thickness_diel);
C_12 = perm_high .* plate_overlap .* surface_area ./thickness_diel;
C_2g = perm_low .* plate_overlap .* surface_area./(3.33333*thickness_diel);
C_g3 = perm_high .* plate_overlap .* surface_area ./thickness_diel;
C_23 = perm_low .* (1-plate_overlap) .* surface_area./(2.* thickness_diel);

% MLCID Resistive Losses due to loss tangent (lt1, lt2) and electrodes
ESR_1g = lt1*10^(-2)./(w0.*C_1g);
ESR_12 = lt2*10^(-2)./(w0.*C_12);
ESR_2g = lt1*10^(-2)./(w0.*C_2g);
ESR_g3 = lt2*10^(-2)./(w0.*C_g3);
ESR_23 = lt1*10^(-2)./(w0.*C_23);

% Impedance of main branches in MLCID Stack
Z_1g = 1./(i.*w0.*C_1g)+ ESR_1g;
Z_12 = 1./(i.*w0.*C_12)+ ESR_12;
Z_2g = 1./(i.*w0.*C_2g)+ ESR_2g;
Z_g3 = 1./(i.*w0.*C_g3)+ ESR_g3;
Z_23 = 1./(i.*w0.*C_23)+ ESR_23;

% Initialization of values
W_best = 1000; L_b1 = 0; L_b2 = 0; M_b = 0; Ratio_Rec = 0;

for dL2 = 50 : 5 : 300
    % Value of L2 and computation of Resistive loss of Inductor
    L_2 = dL2*10^(-9);
    N_2 = sqrt (L_2*2*pi/(mu_0*h_via)/log(R_out/R_in));
    theta_2 = 2*pi./N_2;
    D_2 = R_out^2 + R_in^2 - 2*R_in*R_out*cos(theta_2/2);
    R_L2 = N_2*(2*D_2./((2*r_via + (r_via_2-r_via)/2) * skin_d) * Rho_Cu + h_via./(pi*abs((r_via_"2 - cyl_skin."2)) * Rho_Cu) + h_via./(pi*(r_via_2."2 - cyl_skin_2."2)) * Rho_Cu);

    for dL1 = dL2 : 5 : 300
        % Value of L1 and computation of Resistive loss of Inductor
        L_1 = dL1*10^(-9);
        N_1 = sqrt (L_1*2*pi/(mu_0*h_via)/log(R_out/R_in));
        theta_1 = 2*pi./N_1;
        D_1 = R_out^2 + R_in^2 - 2*R_in*R_out*cos(theta_1/2);
\[ R_{L1} = N_1 \times \frac{2 \times D_1}{(2 \times r_{via} + (r_{via_2} - r_{via})/2) \times \text{skin_d}} \times Rho_Cu + \frac{h_{via}}{(\pi \times \text{abs}(r_{via}^2 - \text{cyl_skin}^2))} \times Rho_Cu + \frac{h_{via}}{(\pi \times (r_{via}^2 - \text{cyl_skin}^2))} \times Rho_Cu; \]

for Mut_Per = -90: 0
% Mutual inductance between L1 & L2
Mut = (Mut_Per - 1) \times \sqrt{L_1 \times L_2} / 100;

% Impedance Matrix Elements of the System
\[ a_{11} = \frac{(L_1 + L_2 + 2 \times \text{Mut}) - w_0^2 \times (L_1 \times L_2 - \text{Mut}^2) \times (2n - 1) \times C_{1g} + n \times C_{12})}{L_2 + \text{Mut}}; \]
\[ a_{12} = \frac{n \times w_0^2 \times (L_1 \times L_2 - \text{Mut}^2) \times C_{2g}}{L_2 + \text{Mut}}; \]
\[ a_{13} = \frac{(n - 1) \times w_0^2 \times (L_1 \times L_2 - \text{Mut}^2) \times C_{2g}}{L_2 + \text{Mut}}; \]
\[ a_{21} = -\frac{n}{Z_{12}}; \]
\[ a_{31} = -\frac{n - 1}{Z_{2g}}; \]
\[ a_{22} = \frac{n \times Z_{12} + n \times Z_{2g} + (2n - 1)/Z_{23} + 1/Z_{24}}{L_2 + \text{Out}}; \]
\[ a_{23} = -\frac{(2n - 1)/Z_{23} - 1/Z_{24}}{L_2 + \text{Out}}; \]
\[ a_{32} = -\frac{(2n - 1)/Z_{23} - 1/Z_{24}}{L_2 + \text{Out}}; \]
\[ a_{33} = \frac{(n \times Z_{12} + (2n - 1)/Z_{23} + (n - 1)/Z_{2g}) + 1/Z_{24}}{L_2 + \text{Out}}; \]

Mat = [a_{11}, a_{12}, a_{13}; a_{21}, a_{22}, a_{23}; a_{31}, a_{32}, a_{33}];
Matrix = inv(Mat);

% Computing Node Voltages
Voltage_Vector = Matrix \times \text{Input_Vector}; \quad V_1 = \text{Voltage_Vector}(1);

% Computing Currents flowing through inductors
\[ I_1 = \frac{(-V_{in} \times i \times w_0 \times L_2 + V_1 \times i \times w_0 \times (\text{Mut} + L_2))}{(w_0^2 \times (L_1 \times L_2 - \text{Mut}^2))}; \]
\[ I_2 = \frac{(V_{in} \times i \times w_0 \times \text{Mut} - V_1 \times i \times w_0 \times (\text{Mut} + L_1))}{(w_0^2 \times (L_1 \times L_2 - \text{Mut}^2))}; \]

% Computing total loss due to inductors
\[ W_{loss} = R_{L1} \times \text{abs}(I_1)^2 + R_{L2} \times \text{abs}(I_2)^2; \]
width_1 = \text{abs}(I_1) / k_T / 39.37 \times 10^{-6};
width_2 = \text{abs}(I_2) / k_T / 39.37 \times 10^{-6};
if width_1 > 5e-4
  width_1 = 5e-4;
end
if width_2 > 5e-4
  width_2 = 5e-4;
end
% Voltage ratio of the step down MLCID transformer
ratio = V_{in} / \text{abs}(\text{Voltage_Vector}(2) - \text{Voltage_Vector}(3));

% Check if ratio is within acceptable limits
if (3.9 < ratio)
  if (4.1 > ratio)
% If the loss of the current configuration is lower than the
% best case so far, make this the best case
if W_loss < W_best
    I_b1 = I_1; I_b2 = I_2; L_b1 = L_1; L_b2 = L_2;
    M_b = Mut_Per; W_best = W_loss; Ratio_Rec = ratio;
end
end
end
end
end

display(['L_1 = ' num2str(L_b1*1e9) 'nH; L_2 = ' num2str(L_b2*1e9) 'nH; M = ' num2str(M_b);
    I_1 = ' num2str(abs(I_b1)) 'A; I_2 = ' num2str(abs(I_b2)));
display(['W_loss = ' num2str(W_best) 'W; Width_1 = ' num2str(width_1*1e3) 'mm;
    Width_2 = ' num2str(width_2*1e3) 'mm; ']);
Appendix E

Equivalent T-model Implementation of Transformer

E.1 Transfer Function Derivation

For a two winding transformer presented in Figure E.1.1(a), the following equations can be used to describe its behavior:

\[ V_{in} = j\omega L_1 I_1 + j\omega M I_2 \]  \hspace{1cm} (E.1.1)

\[ V_{out} = j\omega M I_1 + j\omega L_2 I_2 \]  \hspace{1cm} (E.1.2)

\[ I_{out} = -\frac{V_{out}}{R_{out}} \]  \hspace{1cm} (E.1.3)

Substituting equation E.1.3 into E.1.2, we obtain:

\[ V_{out} = j\omega M I_1 - j\omega L_2 \frac{V_{out}}{R_{out}} \]  \hspace{1cm} (E.1.4)
Rearranging equation E.1.4 results in an expression for current $I_1$ in terms of $V_{out}$:

$$I_1 = \frac{R_{out} + j\omega L_2}{j\omega M \cdot R_{out}} \cdot V_{out} \quad (E.1.5)$$

Substituting equations E.1.3 and E.1.5 into equation E.1.1 results in:

$$V_{in} = j\omega L_1 \cdot \frac{R_{out} + j\omega L_2}{j\omega M \cdot R_{out}} V_{out} - j\omega M \cdot \frac{V_{out}}{R_{out}} \quad (E.1.6)$$

$$V_{in} = \frac{L_1 \cdot R_{out} + j\omega (L_1 \cdot L_2 - M^2)}{R_{out} \cdot M} \quad (E.1.7)$$

If perfect coupling is assumed ($M = \sqrt{L_1 \cdot L_2}$), then equation E.1.7 can be simplified to:

$$V_{in} = \frac{L_1 \cdot R_{out}}{M \cdot R_{out}} \cdot V_{out} = \frac{L_1}{M} V_{out} \quad (E.1.8)$$

Since $L_1 \approx N_1^2$ and $M \approx N_1 \cdot N_2$, we obtain that:

$$V_{in} = \frac{N_1}{N_2} V_{out} \quad (E.1.9)$$

This result is the expected turns ratio for an ideal transformer. If leakage inductance is introduced in the system, the input/output voltage ratio will be slightly different, since $M < \sqrt{L_1 \cdot L_2}$ and two new series inductors (accounting for leakage) are introduced in the electrical circuit.
representation.

The T-model implementation introduced in this thesis mimics the operation of the standard transformer, but does so with the help of three separate components rather than a pair of coupled windings. The inductance value of the three components is equal to:

\[ L_A = L_1 - M \]  
\[ L_B = L_2 - M \]  
\[ L_M = M \]  
(E.1.10) \hspace{0.5cm} (E.1.11) \hspace{0.5cm} (E.1.12)

Note that for non-unity turn-ratios, one of the series inductors (\( L_A \) or \( L_B \)) will have a negative value which suggests the usage of a capacitor in a practical physical implementation. The T-model circuit representation is shown in Figure E.1.1(b). Applying KCL, we obtain:

\[ \frac{V_{in} - V_M}{j\omega L_A} = \frac{V_M}{j\omega L_M} + \frac{V_M - V_{out}}{j\omega L_B} \]  
(E.1.13)

\[ V_{in} = V_M \frac{L_M \cdot L_B + L_A \cdot L_B + L_M \cdot L_A}{L_M \cdot L_B} - V_{out} \frac{L_A}{L_B} \]  
(E.1.14)

Since current \( I_B \) can be expressed in two different ways, we have that:

\[ I_B = \frac{V_M - V_{out}}{j\omega L_B} = \frac{V_{out}}{R_{out}} \]  
(E.1.15)

which results in the following relationship between \( V_M \) and \( V_{out} \):

\[ V_M = \frac{j\omega L_B + R_{out}}{R_{out}} \cdot V_{out} \]  
(E.1.16)

Substitution of equation E.1.16 into E.1.14 results in:

\[ V_{in} = \left[ \frac{L_M \cdot L_B + L_A \cdot L_B + L_M \cdot L_A}{L_M \cdot L_B} \cdot \left( \frac{j\omega L_B + R_{out}}{R_{out}} \right) - \frac{L_A}{L_B} \right] \cdot V_{out} \]  
(E.1.17)
If the three separate inductors ($L_A$, $L_B$ and $L_M$) are selected based on equations E.1.10-E.1.12, then equation E.1.14 becomes:

$$V_{in} = \left[ \frac{L_1 \cdot L_2 - M^2}{M \cdot (L_2 - M)} \right] \left( \frac{j\omega(L_2 - M) + R_{out}}{R_{out}} \right) \left( L_1 - M \right) \cdot V_{out}$$  \hspace{1cm} (E.1.18)

$$V_{in} = \left[ \frac{j\omega(L_1 \cdot L_2 - M^2)}{M \cdot R_{out}} + \frac{L_1 \cdot R_{out}}{M \cdot R_{out}} \right] \cdot V_{out}$$  \hspace{1cm} (E.1.19)

The final result for the input-output voltage relationship is the same as the one obtained for the two winding transformer formulation:

$$V_{in} = \frac{L_1 \cdot R_{out} + j\omega(L_1 \cdot L_2 - M^2)}{R_{out} \cdot M} \cdot V_{out}$$  \hspace{1cm} (E.1.20)

which suggests that the two circuits will have exactly the same behavior (at a given frequency) given ideal conditions (no losses, perfect coupling).