SINGLE-INDUCTOR 4-OUTPUT DC/DC BUCK CONVERTER WITH COMPARATOR-BASED FIXED-FREQUENCY SINGLE-DISCHARGE CONTROL

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A thesis submitted in conformity with the requirements for the degree of Master of Applied Science
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Abstract

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With ever increasing demand of portable electronics, Single-Inductor Multiple-Output (SIMO) converters are becoming a popular option to design DC/DC converters to reduce cost and maintain long battery life. Single-discharge (SDC) control scheme is proposed to simplify the SIMO design, achieve low cross-regulation, and to support wide range of loads. The proposed converter with 4 outputs is prototyped using TSMC 0.18 µm BCD Gen II process. The chip is tested for its functionality, capable of converting 2.7 to 3.7 V input to 1, 1.2, 1.5, and 1.8 V outputs. The load regulation and efficiency performance of the converter is less than expected due to the unforeseen layout and bond wire parasitics. The peak efficiency of the converter is 73.2%, with the cross regulation of 0.143 mV/mA. The converter prototype is able to support wide range of loads, from disconnected loads to total output power of 1W.
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<th>Description</th>
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<td>SIMO</td>
<td>Single-inductor multiple-output</td>
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<td>HS</td>
<td>Gate drive signal for the high-side transistor</td>
</tr>
<tr>
<td>LS</td>
<td>Gate drive signal for the low-side transistor</td>
</tr>
<tr>
<td>RC</td>
<td>Gate drive signal for the recycling transistor</td>
</tr>
<tr>
<td>FW</td>
<td>Gate drive signal for the inductor freewheeling transistor</td>
</tr>
<tr>
<td>S1</td>
<td>Gate drive signal for the output 1 transistor</td>
</tr>
<tr>
<td>S2</td>
<td>Gate drive signal for the output 2 transistor</td>
</tr>
<tr>
<td>S3</td>
<td>Gate drive signal for the output 3 transistor</td>
</tr>
<tr>
<td>S4</td>
<td>Gate drive signal for the output 4 transistor</td>
</tr>
<tr>
<td>SDC</td>
<td>Single discharge control scheme proposed in this thesis</td>
</tr>
<tr>
<td>DCO</td>
<td>Duration-controlled oscillator</td>
</tr>
<tr>
<td>VCD</td>
<td>Voltage-controlled duration</td>
</tr>
<tr>
<td>FSM</td>
<td>Finite state machine</td>
</tr>
<tr>
<td>PLL</td>
<td>Phase-locked loop</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage-controlled oscillator</td>
</tr>
<tr>
<td>DBB</td>
<td>Dynamic bulk bias circuit</td>
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<td>CNTL_RST</td>
<td>FSM controller reset</td>
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<td>EN_ICNTL</td>
<td>Enable for internal controller connection to the internal output stage</td>
</tr>
<tr>
<td>SUPDATE</td>
<td>Shift register update bit</td>
</tr>
<tr>
<td>SRST</td>
<td>Shift register reset bit</td>
</tr>
<tr>
<td>SCLK</td>
<td>Shift register clock</td>
</tr>
<tr>
<td>SDATA</td>
<td>Shift register data bit</td>
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1 Power Supplies for Portable Electronics

This chapter provides introduction to power supplies used for portable devices. Section 1.1 describes the overall trend of the electronics industry, with increasing market share for portable electronics. Section 1.2 illustrates traditional methods of power regulation used in these devices. Lastly, Section 1.3 outlines single-inductor multiple-output (SIMO) power converters which provide new cost-efficient way of designing the power supplies.

1.1 Rising Demand in Portable Devices

As technology advances, there is fast growing demand for inexpensive, feature rich and yet compact portable electronics. Computers used to cost tens of thousands of dollars, capable of doing only simple arithmetic. As time went by, they became personalized and capable of many complex tasks, and in a small desktop form factor. This has then progressed to the laptop format and nowadays as portable handheld devices. While the size of the devices decreased dramatically, their capability has increased continuously. Modern smartphones can perform a variety of functions including phone calls, video chat, 3D gaming, GPS navigation, web browsing, fingerprint authentication, bio-monitoring and more. This is possible by decreasing the footprint of the electronics required and developing more advanced sensors and Integrated Circuits (IC) to support additional features that the consumers may not even think of.
At present, mobile devices are leading the electronics industry as shown in Figure 1.1 [1], [2]. Ownership of the smartphones and tablets is increasing every day as they become more affordable with many features that were only available in previously premium devices. As these portable devices become a large part of many electronics companies’ revenues, they focus their research and development in packing more functionality into a smaller form factor and at a lower cost.
1.2 Traditional Power Regulation

As previously mentioned, many modern portable devices are capable of various tasks. These tasks are possible by use of wide variety of peripherals, such as CPU, GPU, LCD display, touch sensors, GPS, accelerometers, gyroscopes, audio amplifiers and cameras. All these peripherals require independent well-regulated voltage supplies, drawing different amounts of current at any given time. Voltage regulators (or power converters), which convert electrical power from one voltage level to another are used to achieve this task. This is becoming increasingly difficult as more peripherals are incorporated into a smaller and smaller form factor. Since the power source in portable devices is usually a single rechargeable battery, multiple power converters such as those outlined in Figure 1.2, must be used to regulate various voltages and currents independently for different loads. Traditionally, there are two common ways to provide
regulated voltage supply to a load: using a Low-Dropout Regulator (LDO), or using a Switched Mode Power Supply (SMPS). The characteristics of these circuits are briefly described in the next two sections.

1.2.1 **Low Dropout Regulators (LDO)**

![Typical design of a LDO](image)

Figure 1.3. Typical design of a LDO.

A typical Low-Dropout Regulator (LDO) can provide a regulated output voltage smaller than its input. A simple example of LDO is presented in Figure 1.3 consisting of a transistor $M_1$, and an opamp. $M_1$ is biased such that it acts like a variable resistor. This creates a simple voltage divider as follows:

$$V_{out} = V_{in} \frac{R_{load}}{R_{load} + R_{m1}}$$

where $R_{m1}$ is the equivalent variable resistance presented by transistor $M_1$. 


The opamp is connected in a negative feedback configuration to control this variable resistance. With sufficient gain, the opamp forces the voltage at both of the input terminals to be equal by adjusting the gate voltage of \( M_1 \). Therefore, when a desired \( V_{\text{ref}} \) is chosen, the output voltage follows.

Due to the large opamp gain within the negative feedback, a small Miller capacitor is often added to the gate of \( M_1 \) to stabilize the circuit. Since the LDO circuit has poles governed by these small capacitors, the bandwidth of the feedback loop is often large and is capable of excellent voltage regulation at high frequencies. However, during heavy load operation, the active series resistance of the transistor dissipates significant amount of energy. Therefore, the use of LDO is often restricted to light or medium load operations and when the power conversion efficiency of the converter is not the primary concern.
1.2.2 Switched Mode Power Supplies (SMPS)

For heavy load (high output current) operations, where power conversion efficiency is of high importance, SMPS is often used. A typical design of SMPS is as shown in Figure 1.4. This SMPS consists of a network of transistors, $M_{hs}$, and $M_{ls}$, connected to an inductor, $L_1$, and a capacitor, $C_1$. Unlike the series transistor used in LDO, the transistors in SMPSs are used as on-off switches with very low resistances. These transistors are switched on and off in complementary fashion every cycle causing the node LXP to change between $V_{in}$ and ground. $L_1$ and $C_1$ acts as a low-pass filter, making the output $V_{out}$ the time averaged version of the voltage at node LXP. Therefore, output voltage is simply:

$$V_{out} = D \times V_{in}$$ (2)
where $D$ is the duty cycle of the switching pulse. The PID compensator is often used to compare $V_{out}$ against the desired $V_{ref}$. The compensator as part of the negative feedback loop adjusts the duty cycle until $V_{out}$ is equal to $V_{ref}$. Since all components in the power delivery path have low resistance, the conduction loss of the SMPS is much smaller than the LDO.

### 1.2.3 Disadvantages of SMPS

A major drawback of SMPS is the cost and footprint associated with the inductor. Also, the switching frequency of SMPS is often restricted to a few MHz to limit gate driver loss, leading to a loop bandwidth that is much smaller than the typical LDO. Finally, because of the switching operation, a slightly larger voltage ripple can be observed at the output node.
Due to these factors, LDO is often preferred over SMPS where tight voltage regulation is required, and power conversion efficiency is not of utmost importance. LDOs are much simpler designs, uses very little area, can regulate voltage even with high frequency transients, has low noise output, and saves significant cost in manufacturing. This is clearly visible from Table 1.1, a list of power regulators inside the PMM8920, which is a power management IC (PMIC) often used
for portable electronics [4]. PMM8920 employs 8 SMPS converters with 29 LDOs inside a single chip. Seven out of 29 LDOs are rated more than 500mA of current, with 5 of them providing output currents of up to 1.2A. If SMPS were used in these cases, the battery life could be extended significantly. However, area usage and cost increase from using seven more inductors as well as other undesirable effects outlined above make this difficult to realize. This issue is also evident from Figure 1.5, which depicts a PCB layout for an iPhone 6S. PMICs labeled on the PCB has numerous capacitors and inductors taking up space nearby. Adding more inductors for the benefit of power efficiency would dramatically increase the PCB area and would increase the cost.

![Figure 1.5. PCB from iPhone 6S [5]. PMICs are surrounded by capacitors and inductors.](image-url)
1.3 Single Inductor Multiple Output (SIMO) Converters

To tackle the disadvantages outlined in Section 1.2.3, along with the demand for a longer battery life in portable devices, Single Inductor Multiple Output (SIMO) converters were introduced [7]. SIMO converters time-multiplex the inductor charge/discharge cycles in SMPS to provide energy to several different outputs. By using single inductor for multiple outputs, it resolves the main disadvantage of using SMPS over LDO. By maintaining similar efficiency to SMPS, SIMO designs aim to replace LDOs in medium load conditions, ultimately providing longer battery life while keeping the cost down. Since the first patent of this design in 1995 by D. Goder et al. [8], variety of methods to regulate numerous outputs have been developed. A popular implementation example is as shown in Figure 1.6 from D. Ma et al. [6]. The converter divides
the switching cycle into two phases, where the inductor charges and discharges in each phase for its respective outputs. These phases are given enough dead-time in between to eliminate the cross-regulation effect which will be discussed in the next section. An example of a physical implementation of a Single-Inductor 4-Output converter is as shown in Figure 1.7, utilizing much less area of PCB compared to conventional SMPS implementation. The corresponding schematic of the converter is found in Figure 2.6.

![Figure 1.7. Typical PCB for SIMO with four outputs [9].](image)

### 1.3.1 Problems with SIMO

![Figure 1.8. Cross regulation observed on Single-Inductor 2-Output converter [10].](image)

Although SIMO can achieve higher efficiency than a LDO, it is still not widely used in industry. This is mainly due to the issue with cross regulation as illustrated in Figure 1.8. This is a phenomenon observed when a load transient in one output causes a variation in adjacent outputs.
The cross regulation problem occurs since different outputs share the same inductor. When an output experiences load transient, the converter acts by changing the magnitude of inductor current to compensate. However, since the inductor is shared, other outputs also experience small changes in its power delivered even if it does not have any load transient.

Another problem of SIMO is that it is often less power efficient than a regular SMPS due to the need for additional power transistors to direct inductor current. The efficiency is still much better than that of an LDO, and recent papers were able to achieve up to 88.7% efficiency [11]. Therefore, this problem is becoming less significant compared to cross regulation. Finally, SIMOs suffer from a very complex and constrained design. SIMOs sometimes require significantly more complex circuits, such as multiple-input multiple-output compensators, to properly compensate for all outputs to eliminate cross-regulation [12]. Many research papers, including the design shown in Figure 1.6, are often limited to a small range of load to simplify their circuit as much as possible.

This thesis proposes a simple SIMO converter design, utilizing comparators to regulate output voltages, while a Phased-Locked Loop (PLL) in combination with charge recycling keeps the switching frequency constant. The resulting design suppressed cross-regulation effects, maintained reasonable efficiency, while supporting wide range of load currents.

Chapter 2 provides details on the non-ideal performance of SIMOs by reviewing previously published literature. Chapter 3 explains the proposed SIMO converter design, showing detailed design steps and simulation results. Chapter 4 shows the testing methodology as well as actual testing results, verifying the functionality of the proposed design. Finally, the conclusions in Chapter 5 summarizes the proposed SIMO design and provides suggestions for future improvements.
2 Literature Review

This chapter discusses previous designs of SIMO converters. In Section 2.1, the first generation of converters using time-multiplexed PWM control scheme is introduced and analyzed in terms of their advantages and disadvantages. In Section 2.2, more advanced control scheme with flexible switching frequency is discussed, improving upon the preceding designs. In the last section, summary of designs is presented, along with how the proposed converter compares.

2.1 Fixed Frequency SIMO Converters

When the first generation of SIMO converters was introduced, researchers approached the design as an extension of existing SMPS [13]. Pulse-Width-Modulation (PWM) was the most popular control scheme to support multiple outputs.

![Diagram of Conventional SMPS and SIMO Inductor Currents](image)

Figure 2.1. The inductor current in a conventional SMPS (top), and in the 3-output time-multiplexed SIMO (bottom).

An example of this simple extension is illustrated in Figure 2.1, where the conventional switching cycle is time-multiplexed. Each phase, $\Phi_a$, $\Phi_b$, and $\Phi_c$ would regulate the inductor current to supply its own output.
Figure 2.2. Cross regulation of simple time-multiplexed SIMO.

However, this technique was not a practical design solution. For example, Figure 2.2 depicts a case where the first output undergoes light-to-heavy load transient. A conventional SMPS would increase the duty cycle of the PWM signal to increase the magnitude of inductor current flowing to the output. For the time-multiplexed SIMO, the same action would take place for the first output, where the duty cycle of $\Phi_a$ increases. However, since the inductor current is shared, the subsequent outputs governed by $\Phi_b$, and $\Phi_c$ receive much more current than needed temporarily, causing their output voltages to overshoot.

In order to address this problem, many SIMO designs explored techniques to improve the PWM control scheme, and reduce cross-regulation as much as possible. As outlined in a popular summary of PWM SIMO converter designs [7], there are mainly two types: Multiple Energizing, and Single Energizing converters. Multiple energizing SIMOs aim to improve the time-multiplexing scheme with few minor changes. Single energizing designs try to time-multiplex only the falling slope of inductor current, in order to maximize efficiency while introducing new techniques to reduce cross-regulation.
2.1.1 Multiple Energizing SIMO Converters

Multiple Energizing SIMO converters are similar to the examples introduced in Section 1.3. These converters operate as a combination of multiple sub-converters. Each phase is designated for an output, which charge and discharge inductor current for its needs. Figure 2.3 shows the implementation of this type of converter in Discontinuous Conduction Mode (DCM), designed by D. Ma et al. [6]. In the first phase $\Phi_a$, $S_i$ closes to charge the inductor, and discharge to the output $V_{oa}$ through $S_a$. After a preset dead-time, the second phase $\Phi_b$ commences to charge and discharge the energy to the output $V_{ob}$. The duty cycle of the inductor charging phase is determined by the error voltage between the corresponding output and its reference voltage. The dead-time between two phases is implemented by shorting the inductor when it reaches zero.

Figure 2.3. Typical Multiple Energizing SIMO Converter operating in DCM is shown [6].
current. This dead-time introduces isolation between the two sub-converters from interacting with each other. Provided this dead-time is long enough, it prevents other sub-converter from being influenced with cross-regulation when load step occurs. Additionally, the compensator is easy to design as the sub-converter loop dynamic is equivalent to that of a DCM boost converter. DCM boost converter is a special case in SMPS design where it has a first order transfer function with an open loop gain equal to $\frac{V_{out}}{D_{in}}$. Therefore, a mere Proportional-Integral (PI) compensator is sufficient to stabilize multiple loops in this case.

Although the converter eliminates the cross-regulation problem, the efficiency and load range are problematic. Since the operation relies on the dead-time between the two phases as a buffer for load changes, cross-regulation can occur when load change eliminates the dead-time.

![Graph showing load step in output 1 eliminating the dead-time causes cross-regulation in output 2.](image)

This is illustrated in Figure 2.4, where the output 1 undergoes light-to-heavy load transient. If the load step is large enough, the resulting inductor current after the first phase is not zero. This causes the output 2 to gain more charge while keeping the same duty cycle. Therefore, the converter must have a sufficient dead-time for nominal loads. As a result, the maximum load that can be supported is significantly reduced even when comparing to other DCM converter designs.
In addition, the converter requires at least 3 switching phases per sub-converter: charging/discharging inductor, and freewheeling. For example, for a 4-output SIMO converter, there are 12 switching events in one cycle. Due to this, the converter suffers from very low efficiency at light loads. Additionally, the switching frequency of the converter becomes limited in order to keep reasonable on-time for the switches.

![Diagram](image)

**Figure 2.5.** Multiple Energizing Converter operating in PCCM [14].

In order to address the load flexibility issues, D. Ma *et al.*, proposed a Pseudo-Continuous Conduction Mode (PCCM) design as illustrated in Figure 2.5 [14]. This design has identical operation as in the DCM case, but the freewheeling switch is turned on at a particular $I_{dc}$ rather than a zero current. By dynamically configuring $I_{dc}$ according to the overall load condition, cross regulation is again eliminated while being able to support larger loads. However, since significant amount of current may flow through the freewheeling switch, this design suffers from poor power conversion efficiency at heavy loads. Also, for large load transients, cross regulation is still problematic as the inductor current waveform may simply overstep the dead-time between sub-converters, before $I_{dc}$ could compensate by changing its value.
To tackle the efficiency and load flexibility issues, there has been effort to suppress the cross-regulation while removing dead-time between sub-converters. D. Trevisan et al. attempted to integrate sub-converters while completely removing the dead-time between the phases [12]. In order to address the cross-regulation problem, the proposed converter implements Multiple-Input Multiple-Output (MIMO) proportional-integral-derivative (PID) controllers to compensate for changes in other loads. However, the complexity of the compensator increases exponentially with the number of outputs, leaving the design undesirable for more than 2 outputs.

### 2.1.2 Single Energizing SIMO Converters

![Diagram of the OPDC converter proposed by Le et al. [9]]
In 2007, Le et al. proposed the Ordered-Power-Distributive-Control (OPDC) SIMO converter [9]. The OPDC operates by first energizing the inductor current in a single phase, then distributing the charged energy into multiple outputs one by one as illustrated in Figure 2.7. As shown in Figure 2.6, the converter utilized a comparator-based controller that measures whether each output has reached a voltage reference. It then proceeds onto the next output. The last output is sampled by a PID controller. It then calculates the charge duration of the inductor in the next cycle. This became the basis of the single energizing SIMO converters, where the inductor is charged once and is discharged to all the outputs.

This process significantly reduced the complexity of the design as you only needed to design one PID controller for any number of outputs. Also, the number of switching events was reduced to N+1, where N is the number of outputs. This is much smaller when compared to 3 times N for the case of most multiple energizing converters. This also improved the light load efficiency of the converter, and allowed the converter to switch at higher frequencies. Finally, the design had
minimal cross regulation with small load changes due to the comparator-based operation. With the exception for the last output, all outputs received current until its output voltage was greater or equal to the reference voltage, thereby removing any regulation problems.

![Figure 2.8. Light-to-heavy (top) and heavy-to-light (bottom) load step causing cross regulation in other outputs for OPDC [9].](image)

However, the last few trailing outputs are susceptible to cross regulation from fixed time-period in OPDC. Figure 2.8 demonstrates a light-to-heavy load step in one output. The succeeding outputs receive limited current due to the fixed time period, and therefore causes a temporary output voltage drop. Similarly, it is true for heavy-to-light load step, where the succeeding outputs gain overflow of current, causing an overshoot in output voltage. If the magnitude of load step was large enough, a load step in the first output would also be able to cause cross-regulation in all other outputs.

Despite this cross regulation issue in single energizing SIMOs, it is more widely adopted compared to multiple energizing designs. This is because of the scope of SIMO converter usage. Due to the fundamental issue of sharing the inductor current, SIMO converters are not suitable for multiple heavy load uses. With every additional output, the inductor current ripple increases significantly requiring large inductance value to operate. Also, output voltage ripple of the converter increases due to the large magnitude of inductor current. Single energizing designs had
superior efficiency at light loads compared to multiple energizing cases. Therefore, single energizing SIMOs are more practical for a given application. However, the cross regulation issue from single-energizing SIMOs remains to be the bottleneck in industry-wide adoption.

2.2 Flexible Frequency SIMO Converters

Since 2007, many new SIMO designs were introduced which improved upon the OPDC SIMO converter to counter the cross regulation problem as much as possible. Researchers realized that the main issue of cross-regulation with Le’s design was the fixed time period of switching cycle. Due to the fixed time period, the trailing outputs either did not have enough current delivered, or too much current delivered. By having the converter dynamically change the switching period according to its instantaneous load conditions, the converter should theoretically experience minimal cross regulation.

In 2010, K. C. Lee et al. introduced a PLL-based multiple-output bang-bang (PMB) SIMO converter that would allow the switching period to be changed according to how much load current is needed at the outputs [15]. The converter as outlined in Figure 2.9, operates by measuring the errors between each output voltage and their respective reference voltages. The error voltages are prioritized in descending order and the inductor current is guided to the outputs one by one. Similar to the OPDC, the comparators make sure that outputs 1 through 5 are satisfied while the charge error from the last output is computed. In addition, the PLL detects the phase difference between the switching waveform versus the reference clock and calculates the phase error of the converter. The charge error from the last output and the overall phase error is summed up to define the duty cycle of high-side and low-side switches ($S_1$ and $S_2$ in the figure). The resulting switching signals satisfy the last output, as well as keep the converter in phase with the reference clock. The
The converter in this case, becomes a duty cycle controlled oscillator, where its gain $\frac{F_{sw}}{D_{in}}$, is determined by the output load condition.

By allowing the switching period to be flexible, the converter was able to reduce cross regulation dramatically in the outputs, with the exception for the last output. Therefore, the converter was able to support much large load transients compared to its predecessors. While the

Figure 2.9. PMB SIMO DC-DC Converter using PLL to fix the frequency [15].
frequency can be changed instantaneously, the PLL-based design keeps the frequency intact over a longer period of time for easier EMI isolation and constrained output voltage ripple. However, the last output was still under PID control and susceptible to cross regulation issues. In addition, the control scheme was unable to support light loads requiring DCM operation. This introduced a limitation in the magnitude of load step than can be supported. This is more apparent if the target output was charged in the falling slope of the inductor current as shown in Figure 2.10.

![Figure 2.10. Large load step system failure scenario.](image)

As illustrated in Figure 2.10, if a large light-to-heavy load step occurs at output 3 as shown, the inductor current would continue to charge the output until its reference voltage is met. However, since the inductor current is sloping downwards, it will eventually become negative. This corresponds to current flowing from the output back into the input, reducing its output voltage. The controller would become unstable in this case and eventually the converter would fail. Therefore, this design is unable to support large load transients. Lastly, this converter is rather complex and difficult to implement due to the number of required analog summers, and error amplifiers.
2.2.1 Fully Hysteretic (bang-bang) SIMO Converters

Figure 2.11. Fully hysteretic RBAOT SIMO converter by D. Lu et al, [14].

Figure 2.12. Operation principle of above RBAOT converter [14].

In 2014, D. Lu et al. introduced a ripple-based adaptive on-time (RBAOT) converter in an attempt to completely remove cross-regulation [14]. It improved upon the PMB converter design by making the controller simpler and fully hysteretic. As illustrated in Figure 2.11 and Figure 2.12, the converter operates by simply cycling through each outputs, turning on the corresponding output switch ($M_{s1}$ to $M_{s4}$) until the output voltages reach its reference voltages. During these switching
events, the duty cycle of complementary high-side and low-side switches \( S_p \) and \( S_n \) are adjusted through a PLL in order to keep the switching frequency equal to the reference clock.

The controller is very simple to design, as it only requires comparators, some control logic and a PLL. Although the control scheme only allows for peak voltage detection, the converter eliminated the cross-regulation problem for all outputs including the last by becoming fully hysteretic. In addition, it retained high efficiency for many number of outputs by minimizing the number of switching phases. However, the control scheme was unable to operate in light-load conditions similar to PMB control. This also implied a large load step is unsupported, similar to the case for PMB.

### 2.3 Summary of Designs

Table 2.1. Summary of SIMO Designs Discussed in Terms of Performance

<table>
<thead>
<tr>
<th>SIMO Design</th>
<th>Simplicity</th>
<th>Cross-regulation</th>
<th>Efficiency</th>
<th>Load Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCM</td>
<td>Good</td>
<td>Good</td>
<td>Poor</td>
<td>Poor</td>
</tr>
<tr>
<td>PCCM</td>
<td>Poor</td>
<td>Good</td>
<td>Poor</td>
<td>Good</td>
</tr>
<tr>
<td>OPDC</td>
<td>Good</td>
<td>Poor</td>
<td>Excellent</td>
<td>Excellent</td>
</tr>
<tr>
<td>PMB</td>
<td>Good</td>
<td>Good</td>
<td>Excellent</td>
<td>Poor</td>
</tr>
<tr>
<td>RBAOT</td>
<td>Excellent</td>
<td>Excellent</td>
<td>Excellent</td>
<td>Poor</td>
</tr>
<tr>
<td>SDC (Proposed)</td>
<td>Excellent</td>
<td>Excellent</td>
<td>Good</td>
<td>Excellent</td>
</tr>
</tbody>
</table>

As outlined in the previous sections, many SIMO designs were invented to support minimal cross-regulation, high efficiency, and large load range using a simple design. However, the designs always traded off one for the other as outlined in Table 2.1, unable to achieve reasonable performance in all categories. The proposed Single-Discharge (SDC) SIMO converter described in this thesis is a simple design requiring basic output stage, comparators, finite state machine (FSM) controller, and a PLL. Similar to RBAOT, the proposed SIMO converter is fully-hysteretic
and is able to operate in DCM. Therefore, the SDC SIMO converter is capable of large range of loads from completely disconnected, to potentially large loads. The efficiency of the converter is also reasonable, allowing the design to excel in many performance categories. The next Chapter provides the design of the proposed SDC SIMO converter in more detail.
3 SDC SIMO Design and Simulations

In this chapter, the design of the proposed Single-Discharge (SDC) SIMO converter is presented. Section 3.1 discusses the converter architecture and operation assuming ideal components. Sections 3.2 to 3.5 describes the practical implementation and simulation results. Section 3.6 discusses the integration of all the components and the high level design considerations for potential application cases. Section 3.7 summarizes the layout of the IC using TSMC’s 0.18μm Gen II BCD process. Lastly, in Section 3.8, the PCB testbench implementation is described.
3.1 Design Overview

3.1.1 Operating Principle

The design of SIMO converters always involves a compromise between cross-regulation reduction, design simplicity, and supported range of loads. In this thesis, a new Single-Discharge (SDC) SIMO converter design is proposed with the aim to tackle the previously mentioned criteria while maintaining reasonable efficiency. The overall architecture and the operation of the proposed converter are illustrated in Figure 3.1 and Figure 3.2, respectively.

![Diagram of Proposed SDC single-inductor 4-output converter.](image-url)
Figure 3.2. SDC SIMO converter operation in CCM (a), and DCM (b).

The SDC SIMO converter operates by first charging each output individually until their voltages reach the required reference voltage. This is done by guiding current through high-side switch (HS) via inductor, $L_I$, to output switches S1 to S4. In the next phase, recycling switch (RC) and low-side switch (LS) turn on while previous switches turn off to direct inductor current back into the input power source. Since SIMO converters are most practical in mobile applications, the reverse current would re-charge the battery and/or input decoupling capacitor of the power source, ultimately recycling the energy. The duration of this recycling phase is determined by the PLL which tries to align the overall switching signal (HS), to be in phase with the 1MHz reference clock. For the operation in DCM, when the inductor current goes below zero during the recycling
phase, the output of the comparator measuring the current through the RC switch would go high. This causes the freewheeling switch (FW) to turn on and RC to turn off. The inductor current stays zero, as the inductor is shorted. The inductor current increases again to charge outputs as soon as the cycle resets again. Using just the comparators, PLL, and some logic, the converter controller is simple to implement. Since the control is fully-hysteretic and with fixed frequency, it can minimize cross regulation and limit the output voltage ripples. In addition, the converter is able to support wide range of load currents and transients as it can operate in both DCM and CCM. Finally, a Dynamic Bulk Bias (DBB) circuitry is added to the body of the output switches to allow forward and reverse voltage blocking while ensuring low on-resistance for the transistors. Additional details on this bulk biasing can be found in Section 3.5.1

3.1.2 Ideal Simulation

Using behavioral Verilog-A model for the comparator, PLL, and a state machine, an ideal system is set up and simulated to verify the proposed operation. The simulation testbench can be found in Appendix A.

![Figure 3.3. Ideal SDC SIMO operating at CCM. From top to bottom: Inductor current, Input current, $V_{o1}$, $V_{o2}$, $V_{o3}$, and $V_{o4}$.](image-url)
To demonstrate the ability to support multiple outputs, four loads were connected to the SIMO converter. To ensure that the on-time of the switches are sufficient, a nominal switching frequency of 1 MHz is chosen. Based on this, an inductance of 4.7 μH and an output capacitance of 10 μF are chosen such that the inductor ripple current and the output ripple voltage would be within reasonable range. The nominal output loads are chosen as 1 V / 33 mA, 1.2 V / 50 mA, 1.5 V / 50 mA, and 1.8 V / 70 mA to ensure the magnitude of inductor current stays well within the current density ratings for TSMC’s 0.18 μm Gen II BCD process. The ratio of the output powers are set to create similar on-time for the output switches. An input voltage of 3.7 V is used in the simulation, as it is the typical lithium-ion battery voltage. Figure 3.3 shows the converter operating in CCM with the nominal output loads. On the rising inductor current, all outputs are charged up to their specified reference voltage one by one. On the falling inductor current, it is recycled back into the input as proposed.

![Figure 3.3](image.jpg)

Figure 3.4. Ideal SDC SIMO operating in DCM.
The converter operation in DCM is shown in Figure 3.4. The output loads are changed to 10 mA for all loads in this case. As expected, the on-time of the output switches become shorter and the voltage ripples become smaller as a result of the lighter loads. When the inductor current reaches zero, the freewheeling switch shorts the inductor and ensures no current is drawn from the input.

Cross-regulation effect is examined with the ideal SDC SIMO simulation. While keeping output 2, 3, and 4 with nominal load, the load at output 1 is changed from 0 to 100 mA. Figure 3.5 shows the output voltages and inductor current waveforms during light-to-heavy load transient. Figure 3.6 plots the waveforms during heavy-to-light load transient. As can be observed from these figures, the succeeding output voltages experience minimal changes in its magnitude. Therefore, cross-regulation effect is minimal.

![Waveform Diagram](image.jpg)

Figure 3.5. Cross-regulation effect on all outputs during light-to-heavy (0 to 100mA) load transient on $V_{o1}$. 

Figure 3.6. Cross-regulation effect on all outputs during heavy-to-light (100 to 0mA) load transient on $V_{o1}$.

<table>
<thead>
<tr>
<th>Output</th>
<th>$I_{o1}$ 0 to 100 mA step</th>
<th>$I_{o1}$ 100 to 0 mA step</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Before (V)</td>
<td>After (V)</td>
</tr>
<tr>
<td>$V_{o2}$</td>
<td>1.194</td>
<td>1.188</td>
</tr>
<tr>
<td>$V_{o3}$</td>
<td>1.492</td>
<td>1.487</td>
</tr>
<tr>
<td>$V_{o4}$</td>
<td>1.790</td>
<td>1.786</td>
</tr>
</tbody>
</table>

In order to precisely measure the cross regulation, the output voltages were averaged before and after the transient. The resulting change in voltage is divided by the amount of load change to calculate cross-regulation. As shown in Table 3.1, the largest cross-regulation is observed at $V_{o2}$ during light to heavy transient at 0.06 mV/mA. The residual amount of cross-regulation is due to the small change in voltage ripple, due to the sharing of inductor current.
In the practical implementation of the proposed converter, each circuit block is designed and tested step by step. The succeeding sections describe the reasoning behind design choices encountered, as well as simulations to show its functionality and performance.

### 3.2 Comparators

#### 3.2.1 Comparator Architecture

![Comparator Architecture Diagram](image)

Figure 3.7. Overview of the auto-zeroing comparator used.

Comparators are a key block in the proposed converter. It is used for detecting the output voltages with respect to the reference voltages, detecting when the inductor current falls below zero, and detecting when the cycle reset should occur according to PLL outputs. The comparators used for detecting cycle reset does not need to be accurate. Since it operates in a PID feedback loop, its offset errors can be neglected. The comparators used for detecting the output voltage, as well as inductor zero current, must be fast and accurate in order to provide fast transient response. As a result, an auto-zeroing latched comparator is chosen.

Compared to a conventional non-latching comparator using an open-loop opamp, the latched comparator is able to achieve much faster propagation delay, due to its positive feedback...
loop. For example, the conventional 0.18 µm non-latching CMOS comparator used by Ma et al. [6] has a propagation delay of about 50 ns. In contrast, a latched comparator design can have a propagation delay of less than 1 ns when implemented using the same process. This is because the latched comparator can utilize a positive feedback network for fast settling time.

The inclusion of a preamplifier in front of the latched comparator provide buffering of the input signal. The positive feedback of the latched comparator could produce unwanted voltage spikes in the input due to large charge injection. The preamplifier prevents the input from seeing this voltage spike, by acting as a buffer. When there is offset on the latched comparator due to poor layout and component mismatch, the preamplifier can also be used to increase the difference between the input voltages. This essentially reduces the voltage offset caused by the latched comparator. Finally, using preamplifiers with auto-zeroing scheme would provide additional offset cancellation.

![Figure 3.8. Preamplifier in the auto-zeroing phase.](image1)

![Figure 3.9. Preamplifier in amplifying phase.](image2)
As outlined in Figure 3.8, during $\phi_1$ and $\phi_{1d}$, the switches force the preamplifier to be in unity gain feedback configuration. This creates a virtual short between the positive and negative input terminals. Provided that the preamplifier open-loop gain is large enough, this ‘virtual short’ in reality is a small constant voltage due to the layout mismatch of the input differential pair. This offset voltage is sampled onto the input capacitors during this phase. $\phi_{1d}$ is slightly delayed compared to $\phi_1$ switches, such that $\phi_1$ switches turn off first in order to sample the parasitic charge injection from turning off the $\phi_1$ switch. In the next phase $\phi_2$, the input voltage is amplified through open-loop configuration of the preamplifier as shown in Figure 3.9. Because of the sampled offset voltage on the capacitor, input of the preamplifier sees no offset between the two nodes and amplifies the signal without offset. There must be some delay until $\phi_{2l}$ (as depicted in Figure 3.7) can rise in order for output of the preamplifier to settle. After the delay, $\phi_{2l}$ switches on, and causes the positive feedback of the latched comparator to decide on the output. Finally, the resulting output is fed through the SR latch in order to keep it constant throughout the clock cycle.

Since the offset cancellation capacitor acts as an AC coupling device, the input signal of the preamplifier is always set to the same common-mode voltage. Therefore, the auto-zeroing scheme also acts as a level shifter to maintain the same operating point for the preamplifier, regardless of the input common-mode voltage.

### 3.2.2 Preamplifier Design

The preamplifier is a fully-differential opamp which is used in open-loop configuration to amplify the incoming signal. Preamplifier design focuses on settling time of the signal since the latched comparator operates in high frequency setting. Therefore, the CMFB circuit is often disregarded, and diode-connected transistors are used at the output instead. However, the small-signal impedance of diode-connected transistors are small. This causes the open-loop voltage gain
to be significantly smaller even with aggressive designs. In order to increase gain without reducing settling time, positive feedback circuit can be added in parallel to the output loads. This technique originated from Bult et al. [16]. Figure 3.10 shows preamplifier design utilizing the Bult’s technique to increase its open-loop DC gain.

![Figure 3.10. Bult’s preamplifier used in the comparator. Transistor sizes are shown in µm.](image)

The preamplifier is biased with 20 µA of current. This current is mirrored and doubled in M7 through diode connected transistor M8. Therefore, the input differential pair is biased with 20 µA of current in each branch, amplifying the incoming signal through its transconductance, $g_m$:

$$g_{m1} = \frac{2I_{D1}}{V_{eff1}}$$  \hspace{1cm} (3)

where $I_{D1}$ is the drain current of M1, and $V_{eff1}$ is the overdrive voltage of M1.
The resulting small signal current is then multiplied by the active loads at the output node as illustrated by Figure 3.11. Assuming that $1/g_{m3} \ll r_{o1}, r_{o3}, r_{o5}$, the output impedance becomes:

$$Z_{out} = \left( \frac{1}{g_{m3}} \right) || \left( \frac{1}{g_{m5}} \right) = \frac{1}{g_{m3} - g_{m5}}$$ (4)

If the Bult’s technique was not used, the output impedance would have been $1/g_{m3}$, which is clearly smaller. By designing $g_{m5}$ to be close to $g_{m3}$, the output impedance can become quite large, increasing the overall open-loop gain of the preamplifier. However, it must not be bigger than $g_{m3}$ such that the output impedance is positive to maintain a negative feedback loop. The overall voltage gain becomes:

$$\frac{V_{out}}{V_{in}} = \frac{g_{m1}}{g_{m3} - g_{m5}}$$ (5)

To ensure stability of the loop through possible layout mismatches, M5 is sized to be half of M3.
The preamplifier is tested in open-loop configuration with a 1 MHz 10 mV sine wave. Figure 3.12 shows the output differential voltage of the preamplifier. The open-loop gain is measured to be 5.66 V/V.

![Figure 3.12. Preamplifier transient simulation.](image)

The preamplifier is also tested in unity gain feedback configuration. Figure 3.13 plots the loop gain of the preamplifier. The DC gain is measured to be 6.3 V/V. The unity gain bandwidth was around 100 MHz with phase margin of 98 degrees.

![Figure 3.13. Preamplifier loop gain.](image)
3.2.3 Comparator Decider Design

The decider circuit used as the main positive feedback comparator is shown in Figure 3.14. It is similar to a conventional Strong-arm flip-flop. When $\phi_{2l}$ is off, the decider resets all the differential nodes to VDD through M7 to M10. When $\phi_{2l}$ is on, the input signal drives the differential pair M1 and M2. The differential pair creates a small signal current flowing down each branch. M3 to M6 creates a positive feedback latch as back-to-back inverters. A miniscule difference in small signal current through this positive feedback latch can cause the output node to either go high or low. The resulting output is then fed to a conventional SR latch as illustrated in Figure 3.15 so that its value is maintained when $\phi_{2l}$ is off again.
Figure 3.15. Conventional SR latch used to hold outputs.

In order to make sure the latch can perform at high speeds, the sizes of the transistors for both the decider and SR latch are kept to a minimum. This also helps to reduce any charge kickback from the output nodes back into the input.

The decider and SR latch combination is tested against a 1 MHz input sine wave with 10 mV amplitude. The input common mode voltage is set to 2.76 V, which is what the preamplifier output common mode voltage settles to. The comparator clock is set to be 50 MHz so that the 0.18 µm CMOS 5 V device can operate with conservative margins. Figure 3.16 shows the decider operation with output, Q. The output switches back and forth when the inputs are close to each other. This is because of the large gain of the positive feedback latch, amplifying the noise between the input differential current. Since the comparator was used along with a preamplifier with sufficient gain, this behavior had little effect in the overall comparator performance as described in the next section.
3.2.4 Overall Comparator Functionality

Using the preamplifier and decider designed above, the full comparator is made to emulate the design previously shown in Figure 3.7. The switches used for auto-zeroing are implemented using transmission gates with W/L = 5/0.6 µm for the PMOS and 2/0.6 µm for the NMOS devices. The offset cancellation input capacitor ‘C’ shown is 160 fF. This is sufficiently larger than the parasitic capacitance of the input differential pair of the preamplifier. The capacitance size is not increased further to make sure that the settling time of each node is kept to be as small as possible for the 50 MHz clock. Figure 3.17 plots the output signal with an input of 1 MHz, 10 mV sine wave along with a 1 V reference. The offset of the comparator is not observable with comparator clocks switching at 50 MHz. The simulation also plots the input of the preamplifier which is switching at around 2.5 V common mode. As demonstrated with Figure 3.18, this common mode voltage stays constant even with 3.7 V input common mode signals.
Figure 3.17. Simulation result for the full auto-zeroing comparator. From top to bottom: input waves with 1V common mode, output (Q), positive input of preamplifier, negative input of preamplifier, and $\phi_{2l}$.

Figure 3.18. Simulation result for the full auto-zeroing comparator with input common mode of 3.7 V.
Figure 3.19. Simulation of the comparator operation with 8 mV offset added to the input of the preamplifier. From top to bottom: Input waves, output without auto-zeroing, output with auto-zeroing, and $\phi_{2i}$.

The full comparator is also tested with an 8 mV offset artificially introduced to the input of the preamplifier. Figure 3.19 plots output waves in this test case. The second waveform in the figure shows the 8 mV offset when auto-zeroing is disabled and the input is directly fed into the preamplifier. The third waveform in the figure shows the output with auto-zeroing enabled, which reduces the 8 mV offset to less than 1 mV. Since the preamplifier has finite open-loop gain, the offset does not cancel all the way to zero, leaving a small offset even with auto-zeroing.
3.3 Finite State Machine Controller

3.3.1 FSM Logic

The main component of the SDC SIMO converter that differs from the other designs is the controller. A finite state machine (FSM) is used to provide the necessary control signals for the proposed converter. Each state provides instructions to determine which output stage transistors must be turned on or off in order to direct the inductor current properly. There are 6 states in the proposed converter as outlined in Figure 3.20. The first four states relate to directing current to flow from input voltage source, through the inductor to each outputs. The states end and proceed to next whenever its output voltage is greater than its desired reference voltage. State 5 directs the inductor current back into the input voltage source with all output switches are off. Given that
input voltage source is a rechargeable battery, this ensures that the energy is recycled. The last state 6 is an optional state, which shorts the inductor when the inductor current reaches below zero. This prevents the scenario where the inductor current would become negative and eventually draw current from the outputs back into input. For both states 5 and 6, when cycle reset signal is received, the state changes back to the first state.

In order to improve the load transient performance, state skipping is introduced. When the controller is about to switch to the next state, it evaluates whether or not the next state’s ending requirement is fulfilled. If so, the controller proceeds to evaluate state ending requirement for the one after the next. The controller does this until it finds a state where the requirement has not been met, and directly goes into that state. All these events happen in one clock cycle for the controller. In order to prevent the controller from skipping through too many states in one clock cycle, state 5 is invoked at least for one clock cycle regardless of input conditions. Also, for the case where all outputs are disconnected and their voltages satisfied (greater than reference voltage) for a long time, the controller stays in state 5 and eventually to state 6 even if the cycle reset is on. As soon as one of the outputs are not satisfied, the controller goes directly to that state and starts the cycle again.

State skipping brings many advantages to the design. First, since it can skip the satisfied outputs, it improves the load transient response for other outputs that require charging. Second, the converter is able to regulate the output voltage even when no load is connected to some of the outputs. The outputs would always be satisfied when there is no load, and the controller would simply skip the state without any increase in voltage. Lastly, it improves light-load efficiency. When some outputs are handling light loads, the output voltage may overshoot during charging due to the fixed time period of the controller. For example, when the controller operates with a 50
MHz clock, the output voltage may overshoot during the 20 ns period of charging. If the load is light enough, the output voltage may not drop below the reference voltage for the next few cycles. This causes the controller to skip the output charging for a few cycles. This is equivalent to Pulse Frequency Modulation (PFM) where the light load is regulated with low frequency operation. This significantly decreases the gate driver loss as the output does not need to be turned on frequently, and therefore the overall efficiency of the converter at light loads can be increased.

3.3.2 FSM Circuit Realization

Figure 3.21. The FSM circuit realization. Each D-flip-flop holds a state value depending on its input logic.

The implementation of the FSM mentioned above is simple, requiring only small number of logic gates and D flip-flops to hold the state outputs. In order to allow state skipping, each state
blocks contain logic to evaluate whether any preceding states can hop into the corresponding state. Additional logic is also required to make sure only one state is turned on at any given clocking edge to prevent logic failure. Since state skipping increases logic propagation delay, a conservative clocking speed of 50MHz is used.

In order to simulate the functionality of the FSM controller, ideal voltage pulses were used to emulate the situation when the output voltages meet the reference voltages. They were also used to provide cycle reset every 1 µs. The resulting switch signals are plotted in Figure 3.22.

![Figure 3.22](image)

Figure 3.22. The FSM controller operation simulated with ideal voltage pulses. From top to bottom: the gate drive waveforms for HS, LS, RC, FW, and S1 to S4.

To emulate DCM operation, the inductor zero-current comparator output is also pulsed near the end of the switching cycle. The resulting signals are plotted in Figure 3.23.
Figure 3.23. FSM controller simulation under DCM operation. From top to bottom: the gate drive waveforms for HS, LS, RC, FW, and S1 to S4. The zero-current comparator output is pulsed just before FW goes high.
3.4 Phased Locked Loop

3.4.1 PLL Architecture

![Figure 3.24. A conventional PLL architecture.](image1)

The proposed SDC SIMO converter relies on the PLL to steer the switching cycle into a fixed frequency. Since the switching frequency is known, a simple EMI notch filter can be designed to protect sensitive analog circuits nearby. In addition, constant frequency allows for limitations on output voltage ripple.

A conventional PLL architecture is illustrated in Figure 3.24. It includes phase detector to measure the error in phase, a loop filter to compensate for that error, and the voltage controlled oscillator (VCO) to produce new oscillations based on that compensation. The N divider is often included such that the PLL can produce higher frequency oscillations compared to the reference clock. This conventional architecture can be modified slightly to stabilize the switching cycle of
the SIMO converter as shown in Figure 3.25. The VCO is replaced with a voltage-controlled duration (VCD) and duration-controlled oscillator (DCO), which is formed by the FSM controller and the output stage. The N divider can be bypassed such that the switching frequency of the converter is equal to the reference clock.

The single-discharge control (SDC) scheme has two phases, where the first phase is used to charge outputs, and the second phase to recycle the energy. The duration of the first phase (charging) is determined by the load. The phase ends when all the output voltages are larger than their reference voltages. The duration of second phase can be used to control the switching frequency. For example, as illustrated in Figure 3.26, suppose the output load stays constant. When the duration of the recycling phase increases, the magnitude of the inductor current is reduced. Therefore, it takes longer for outputs to charge, which increases the length of the switching cycle. The reverse is also true, where the inductor current increases to shorten the length of the switching cycle. With the proposed control scheme, the frequency of the switching is inversely proportional to the duration of the recycling phase. Therefore, the FSM controller, controlling this output stage can be considered as a duration-controlled oscillator (DCO).

![Figure 3.26. The switching cycle period is controlled by the duration of recycling phase, \( T_R \).](image)
To interface this DCO with the rest of the PLL loop, a voltage controlled duration (VCD) is required after the loop filter. This can be implemented by the comparator, comparing between the loop filter output, $V_{CNTL}$, and an inverse sawtooth waveform, $S_{TH}$. The inverse sawtooth waveform starts falling when the recycling phase begins. As illustrated in Figure 3.27, if the loop filter output is an increasing voltage, the comparator pulses high after a shorter duration of the recycling phase. If the loop filter output is lower, the comparator pulses high with longer delay. This pulsed signal, CRST, signals the end of the recycling phase, informing the FSM to proceed to the next charging phase. Therefore, the duration of the recycling phase is controlled by the magnitude of loop filter output voltage.
3.4.2 PLL Implementation

Figure 3.28. The circuit implementation of phase detector, loop filter, and VCD.

For the remaining blocks of the PLL, a conventional model can be used. The phase detector is implemented using two D flip-flops, producing charge pump current proportional to the phase difference of its inputs. The loop filter is designed using a type-III model, incorporating one resistor, and two capacitors. The loop filter output, $V_{CNTL}$, is converted into a pulsed output, by comparing with an inverse sawtooth waveform generator. A simple current source discharging a large capacitor, $C_{st}$, is used to generate inverted sawtooth waveform.

To simplify the design, the comparator used by the VCD, functions without auto-zeroing. Since the comparator utilized NMOS input differential pair, the input signal can swing from around 0.7 V to VDD. Based on this information, the inverted sawtooth waveform was designed to produce any length of the recycling phase duration at the nominal converter switching frequency of 1 MHz. Therefore, the slope of the sawtooth waveform was chosen such that it can cover at least 1 µs during the full swing of 0.7 V to VDD:
\[ \frac{dv}{dt} = VDD - 0.7 \frac{(2.7 \sim 4.2) V - 0.7}{1 \mu s} = 2 \sim 3.5 \frac{V}{\mu s} \]  

(6)

For the PLL to work for all possible VDD, a 2 V/\mu s slope was chosen for the sawtooth waveform.

Using a 10 \mu A current (I_{st}) to discharge the capacitor, its size becomes:

\[ C_{st} = \frac{I_{st}}{dv/dt} = \frac{10 \times 10^{-6}}{2 \times 10^6} = 5pF \]  

(7)

The resulting size of the capacitor is reasonable. Using MIM capacitors, the layout uses around 100 \mu m x 100 \mu m area.

3.4.3 Phase Loop Filter Design

In order to design the Type-III loop filter to stabilize the phase loop, a standard design approach is taken. However, the ‘VCO’ gain must be known before hand to calculate the filter component values. The ‘VCO’ in this case includes the VCD, which was discussed previously, along with the DCO which includes the FSM controller and the SIMO converter output stage. Theoretical derivation of this ‘VCO’ gain is complex, as it involves many parameters such as load resistances, output voltages, input voltages and parasitics. Instead, simple open-loop simulation is run to measure the switching frequency of the converter with a given loop filter output, \( V_{CNTL} \). The testbench for this test can be found in Appendix A.
Figure 3.29. The VCO open-loop test with $V_{CNTL} = 3$ V. From top to bottom: Inductor current, inverse sawtooth/$V_{CNTL}$, $V_{o1}$, $V_{o2}$, $V_{o3}$, and $V_{o4}$.

Table 3.2. Switching Frequency of the Converter for different $V_{CNTL}$

<table>
<thead>
<tr>
<th>Loop Filter Output, $V_{CNTL}$ (V)</th>
<th>Switching Frequency (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.2</td>
<td>1.33</td>
</tr>
<tr>
<td>3.1</td>
<td>1.2</td>
</tr>
<tr>
<td>3</td>
<td>1</td>
</tr>
<tr>
<td>2.9</td>
<td>0.9</td>
</tr>
<tr>
<td>2.8</td>
<td>0.8</td>
</tr>
</tbody>
</table>

Table 3.2 outlines roughly what the switching frequency will be for a given $V_{CNTL}$. Using this data, and assuming VCO gain is linear with small $V_{TH}$ variation of 2.8V to 3.2V, the VCO gain is:

$$K_{VCO} = 2\pi \frac{1.33 - 0.8}{3.2 - 2.8} \times 10^6 = \frac{8.325 \times 10^6}{3.2 \cdot 2.8} \text{ rad} / \text{s} \cdot \text{V}$$

(8)

Using the value for $K_{VCO}$ found above, the PLL loop filter design can proceed. First, the 3dB loop bandwidth of the PLL is set to be $1/5^{th}$ of the input frequency. The quality factor, Q, of
the loop was set to be 0.5 so that the peaking of the phase step response is minimized with optimal settling time. Therefore, the loop gain, \( w_{pll} \) is chosen to be:

\[
w_{pll} = \sqrt{K_{pd}K_{lp}K_{VCO}} = 0.4 \times w_{3\text{db}} = 0.4 \times \frac{1}{5} \times 2\pi \times 1\text{MHz} = 5.02 \times 10^5 \frac{\text{rad}}{\text{s}} \quad (9)
\]

where \( K_{pd} \) is the gain of the phase detector, and \( K_{lp} \) is the gain of the loop filter. The gain of the charge pump phase detector \( K_{pd} \), is simply:

\[
K_{pd} = \frac{I_{ch}}{2\pi}
\]

The loop filter comprised of \( R, C_1, \) and \( C_2 \) can also be simplified to derive \( K_{lp} \):

\[
K_{lp} \approx \frac{1}{C_1}
\]

Substituting (8) and (9) into (7), \( C_1 \) can be found by setting \( I_{ch} \) to 10 µA:

\[
C_1 = \frac{I_{ch}K_{VCO}}{2\pi w_{pll}^2} = \frac{10 \times 10^{-6} \cdot 8.325 \times 10^6}{2\pi \cdot (5.02 \times 10^5)^2} = 52\text{pF}
\]

\( R \) is then found by setting the zero frequency, \( w_z \) to be \( Qw_{pll} \):

\[
R = \frac{1}{Q w_{pll}C_1} = \frac{1}{0.5 \cdot 5.02 \times 10^5 \cdot 52 \times 10^{-12}} = 75\text{k}\Omega
\]

The resulting value of 52 pF for \( C_1 \) is too big, taking up too much area for a single capacitor. To make the layout more realizable, the capacitance for \( C_1 \) found above is halved to around 26 pF while the resistance for \( R_1 \) is doubled to 150 kΩ. This slightly increases the overall loop bandwidth of the system while keeping the zero frequency to be the same as before. Thus, some phase margin is sacrificed for a simpler layout. Finally, \( C_2 \) is found by setting it to be \(1/8^{\text{th}}\) of \( C_1 \) in order to suppress glitches:
\[ C_2 = \frac{C_1}{8} \approx 3.2pF \]  

(14)

The overall loop gain using the component values found above is plotted below in Figure 3.30.

The loop bandwidth was found to be 240 kHz, with a phase margin of around 48 degrees.

![Phase loop gain of PLL](image.png)

Figure 3.30. The phase loop gain of the PLL.
3.4.4 PLL Functionality Simulation

Figure 3.31. Simulation of the PLL functionality with ideal converter and controller. From top to bottom: Inductor current, $V_{CNTL}/S_{TH}$, and CRST.

Using the component values chosen above, simulation was carried out using an ideal converter and comparators attached to the PLL circuit. Large load step was imposed, where outputs 1, 3 and 4 were changed back and forth from 33, 50, and 70 mA to 0 mA for all outputs. The PLL was able to stabilize the converter such that the switching frequency stayed at around 1 MHz before and after load transients. The resulting plot is shown in Figure 3.31.
3.5 Output Stage

3.5.1 Output Stage Overview and Dynamic Bulk Bias (DBB)

The output stage design is illustrated in Figure 3.32. For the main switches, high-side (HS) and recycling (RC) switches are chosen to be PMOS 5 V devices. This is because of the input voltage which is limited to within 4.2 V. By using 5 V devices, the Figure of Merit (FOM) for these transistors is better than that of higher voltage devices, which allows for higher overall efficiency of the converter. Bootstrapping is out of the question as the overhead from adding bootstrapping capacitor would occupy too much area. Therefore, PMOS 5 V device is the most logical choice. Similarly, the low-side transistor (LS) and freewheeling transistor (FW) are chosen to be NMOS 5 V device as they have source nodes that are close to ground. Output switches S1 to S4 are also chosen as NMOS as the nominal reference voltages (1, 1.2, 1.5, 1.8 V) are low enough such that NMOS devices have better FOM than the PMOS devices.
The bulk of the transistors for HS, LS, and RC are connected to the source for optimal on-resistance. However, the freewheeling switch must be able to block the voltage in both forward and reverse direction. This can be done by connecting the body of the FW switch to ground. As illustrated in Figure 3.33, since ground is at a lower potential than both $V_d$ and $V_s$, the body diodes block the voltage successfully, and there is no conduction path if the transistor is off.

![Figure 3.33. Body diodes of the transistor.](image)

Similarly, the output switches (S1 to S4) need to have their body connected to the ground in order to block voltages in both directions. However, connecting the body to ground would cause the threshold voltage to increase dramatically. As a result, the transistor could suffer from having a lot smaller overdrive voltage, and ultimately increase in on-resistance. In order to overcome this issue, a simplified dynamic bulk bias circuit proposed in SIMO converter by Kuan et al. [17] is used. The schematic is illustrated in Figure 3.32. When the transistor is on, the body is connected to the source of the transistor, lowering on-resistance as much as possible. When the transistor is off, the body is shorted to ground, allowing it to block reverse voltages.
3.5.2 Output Stage Sizing

Due to the technology limitations of the 5 V 0.18 μm devices, and the area limitations of the chip, the output power of the converter for testing is set to be around 300 mW.

Table 3.3. Output Stage Transistor Characteristics

<table>
<thead>
<tr>
<th>Function</th>
<th>Model</th>
<th>Width</th>
<th>Length</th>
<th>$R_{on}$</th>
<th>$C_g$ (pF)</th>
<th>FOM (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>High-side (HS)</td>
<td>PMOS</td>
<td>160000</td>
<td>0.5</td>
<td>0.038</td>
<td>237</td>
<td>9</td>
</tr>
<tr>
<td>Low-side (LS)</td>
<td>NMOS</td>
<td>64000</td>
<td>0.6</td>
<td>0.034</td>
<td>121</td>
<td>4.1</td>
</tr>
<tr>
<td>Recycling (RC)</td>
<td>PMOS</td>
<td>160000</td>
<td>0.5</td>
<td>0.038</td>
<td>237</td>
<td>9</td>
</tr>
<tr>
<td>Freewheel (FW)</td>
<td>NMOS</td>
<td>4000</td>
<td>0.6</td>
<td>0.544</td>
<td>38</td>
<td>21</td>
</tr>
<tr>
<td>Output 1 (S1)</td>
<td>NMOS</td>
<td>48000</td>
<td>0.6</td>
<td>0.06</td>
<td>87</td>
<td>5.2</td>
</tr>
<tr>
<td>Output 2 (S2)</td>
<td>NMOS</td>
<td>48000</td>
<td>0.6</td>
<td>0.06</td>
<td>84</td>
<td>5.5</td>
</tr>
<tr>
<td>Output 3 (S3)</td>
<td>NMOS</td>
<td>64000</td>
<td>0.6</td>
<td>0.057</td>
<td>102</td>
<td>5.8</td>
</tr>
<tr>
<td>Output 4 (S4)</td>
<td>NMOS</td>
<td>64000</td>
<td>0.6</td>
<td>0.07</td>
<td>106</td>
<td>7.4</td>
</tr>
</tbody>
</table>

Keeping this in mind, the output stage transistors are sized to reduce the on-resistance, $R_{on}$, while keeping gate capacitance, $C_g$, to be as low as possible. Table 3.3 shows the sizing and simulated characteristics of the transistors under 3.7 V input voltage. The source and drain of the transistors are set to the steady state voltage when the transistor is on. Small drain-to-source voltage of 0.1 V is applied to measure the current through the transistor to estimate $R_{on}$. In order to measure $C_g$, a 1 kΩ resistance is added in series to the transistor gate. The RC time constant during turn-on is then measured on the gate of the transistor to estimate $C_g$.

Table 3.4. Gate Driver Transistor Areas for Each Output Stage

<table>
<thead>
<tr>
<th>Function</th>
<th>1st</th>
<th>2nd</th>
<th>3rd</th>
<th>4th</th>
<th>5th</th>
<th>6th</th>
<th>Transistor Area (μm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>High-side (HS)</td>
<td>3.6</td>
<td>14.4</td>
<td>57.6</td>
<td>288</td>
<td>2304</td>
<td>18432</td>
<td>80000</td>
</tr>
<tr>
<td>Low-side (LS)</td>
<td>3.6</td>
<td>14.4</td>
<td>57.6</td>
<td>230.4</td>
<td>921.6</td>
<td>7372.8</td>
<td>38400</td>
</tr>
<tr>
<td>Recycling (RC)</td>
<td>3.6</td>
<td>14.4</td>
<td>57.6</td>
<td>288</td>
<td>2304</td>
<td>18432</td>
<td>80000</td>
</tr>
<tr>
<td>Freewheel (FW)</td>
<td>3.6</td>
<td>14.4</td>
<td>57.6</td>
<td>230.4</td>
<td></td>
<td></td>
<td>2400</td>
</tr>
<tr>
<td>Output 1 (S1)</td>
<td>3.6</td>
<td>14.4</td>
<td>57.6</td>
<td>172.8</td>
<td>691.2</td>
<td>5529.6</td>
<td>28800</td>
</tr>
<tr>
<td>Output 2 (S2)</td>
<td>3.6</td>
<td>14.4</td>
<td>57.6</td>
<td>172.8</td>
<td>691.2</td>
<td>5529.6</td>
<td>28800</td>
</tr>
<tr>
<td>Output 3 (S3)</td>
<td>3.6</td>
<td>14.4</td>
<td>57.6</td>
<td>230.4</td>
<td>921.6</td>
<td>7372.8</td>
<td>38400</td>
</tr>
<tr>
<td>Output 4 (S4)</td>
<td>3.6</td>
<td>14.4</td>
<td>57.6</td>
<td>230.4</td>
<td>921.6</td>
<td>7372.8</td>
<td>38400</td>
</tr>
</tbody>
</table>
The gate driver was sized such that the area of transistor driving it is 4 to 10 times the area of the transistors inside the gate driver for fast signal propagation. Table 3.4 lists the total area of the transistors inside gate drivers which are driving the succeeding gate drivers, and eventually the output stage transistor. The first four gate drivers consistently have a fanout-of-4 to make the delay as short as possible. The remaining gate drivers are designed to have a fanout larger than 4 to make sure that the design is realizable and efficient.

### 3.5.3 Dead-Time Generator

![Dead-time generation circuit for the output stage switches: HS, LS, RC, and FW.](image)

To make sure that there is no shoot-through current during converter operation, a dead-time generator is implemented at the output of the FSM controller. Figure 3.34 illustrates how the dead-time is generated for the main power switches, high-side (HS), low-side (LS), recycling (RC), and freewheel (FW). The dead-time between HS and LS is the most crucial part, as the shoot through current may damage the transistors if it is too long.
An example of dead-time generation is as follows: when HS turns off, the signal after the HS gate driver is fed back into the input, where its inverted version is compared against the State 5 signal, equivalent to LS signal. This comparison ensures that LS before the gate driver, does not turn on until the HS fully turns off after the gate driver. The delay in gate driver with addition to the ‘dead-time delay’ buffers shown on Figure 3.34 add up as the full dead-time between LS and HS. A simulation was performed to measure this dead-time during steady state operation, and is shown in Figure 3.35.

Figure 3.35. Dead-time between HS and LS/RC.
The output switches S1 through S4 also need dead-time. This is to make sure that the outputs do not experience shoot through current between one another. The operation is similar to HS and LS as discussed previously. First, the state signal is compared with inverted HS signal to make sure that the output switch will turn on only when HS is on. Then, an AND gate is used to make sure none of the other switches after the gate driver is on. The simulated result is shown in Figure 3.37.
Figure 3.37. Dead-time between S1 and S2.

3.5.4 Efficiency Simulation

Figure 3.38. Simulated power conversion efficiency as a function of output power. The output voltages are 1, 1.2, 1.5, 1.8 V. The graph includes $R_{on}$, $R_{ind}$, and $P_{gd}$ as source of loss.
Using the output stage designed previously, the power conversion efficiency is simulated to ensure proper operation. The on-resistance $R_{on}$, and gate capacitance $C_{gd}$ at input voltages of 3, 3.3, and 3.7 V are measured and listed in Appendix B. Using these values and including inductor resistance, $R_{ind}$, the efficiency of the converter is approximated using the testbench as shown in Appendix A. Ideal switches are used including the parasitics measured previously to emulate converter operation. The output loads are set to a fixed ratio to ensure similar on-time of output switches. Then, the all loads were swept together from total output power of 0 to 1 W. As discussed previously, this fixes the on-time for output switches to be similar to each other. The testbench is ran for 150 µs, and the last 80 switching cycles are captured. The captured cycles are averaged to find the resulting output voltage values and the input current. The efficiency is then calculated and plotted in Figure 3.38.

The maximum efficiency is 90.0% at 3 V input and with an output power of 198 mW. Overall, the circuit behaves as expected. When the output power is low, gate drive losses, $P_{gd}$, dominate, allowing the lower input voltage to have higher efficiency. As the load is increased, conduction losses from $R_{on}$ and $R_{ind}$ become dominant. Therefore, the efficiency gap between 3.7 and 3 V input becomes smaller. All output paths require the inductor current to pass through at least 2 transistors and the resistance of the inductor as in most SIMO converter designs. This makes them sensitive to conduction losses and is one of the major reasons why SIMO is more suitable for lower power applications. This effect is also evident from Figure 3.38, as the peak efficiency occurs at a output power of 198 mW.
3.6 Full Integration

3.6.1 Modularity

Since the proposed converter is a first prototype, many issues may be expected. To overcome the possible needs for debugging, it is essential for the design to be both modular and configurable. For example, if the FSM controller does not work as intended, the tester should be able to bypass it through an external controller. This modularity was implemented in two ways: by having the ability to turn off each part of the system, and by creating signal paths to bypass each modules. The modules in the proposed system that included this ability were comparators, and the FSM controller.

For the comparators, a large pass transistor operating in triode mode is included in series with the preamplifier tail current source. During the normal operation, this transistor is on. Since the impedance of triode transistor is small, it does not affect the performance of the preamplifier. When it is desired to turn off the comparator, this transistor turns off and blocks all current flowing...
into the preamplifier. The rest of the comparator, which are transmission gates, strongarm flip-flop, and the SR latch are dynamic circuits. Simply turning off the clocks effectively turns off these circuits. The FSM controller is also dynamic, and the same method can be used to shut it down.

Multiplexers and digital output buffers are used to bypass the comparator and the FSM controller. This circuitry is illustrated in Figure 3.39, which depicts overall integrated system. In order to replace the internal comparators, external comparator can be used to monitor the output voltages. The outputs of these external comparators can then be fed into the multiplexer just before the FSM controller. The use of an external controller is similar, as the output of the internal comparator is buffered into the external pins. An FPGA can be used to emulate the FSM controller, and its output is fed into the multiplexer before the output stage.

Using these methods, if the comparators or FSM controller operation is faulty, they can be easily replaced with an external substitution. Since these modules are back-to-back, it is also possible to use both external comparators, and an FPGA as a fully external controller.

### 3.6.2 Configurability

![Figure 3.40. The configurable bias current generator for the comparators, and PLL.](image-url)
The proposed converter includes several analog circuits that are sensitive to process variation and mismatch. Therefore, if the converter is configurable externally, these variations can be overcome and performance may be improved.

The bias current generator is created with this in mind. The complete bias generator is illustrated in Figure 3.40. Using large transistors as switches in series with resistors, the final resistance value can be configured according to the digital inputs cb[0] to cb[3]. With the default settings, cb[0] and cb[1] are on. This causes the final resistor value to be 135 kΩ. Through the PMOS current mirrors, this resistance value generates 20 µA of current to be delivered to each preamplifiers (PA) located far away on the chip. By changing digital inputs cb[0] to cb[3], this bias current can be chosen to be anywhere between 5 to 80 µA.

Other circuit modules include configurability as well. For example, the auto-zeroing comparator included a transmission gate connected from input of the comparator to the input of the preamplifier. By turning this on, the inputs can be directly fed into the input of preamplifier, bypassing auto-zeroing circuitry. Another example is the output buffer enable. Since the digital output buffers are used only during bypassing, or debugging, it dissipates unnecessary power during the normal operation. An AND gate is included before these buffers to enable or disable propagation of signal.
3.6.3 Shift Register Programmer

With all the modularity and configurability options intact, the pin count of the integrated circuit becomes difficult to realize. Therefore, shift registers illustrated in Figure 3.41, were used to program the configuration bits. It uses a total of 4 pins: clock, data, update, and reset for unlimited number of configuration bits. For every clock edge, a data bit is shifted into the array of registers. After data is shifted into all registers, an update signal changes all the configuration bits together. A reset pin is used to keep all the default values of the configuration bits during the start-up of the converter.

If the clock delay between the flip-flops is too long, a single data bit can propagate through all flip-flops in one positive edge of the clock. This is unwanted, as the proper operation would have one data bit passing through exactly one flip-flop for every positive edge of the clock. Therefore, the clock signal is directed in the opposite direction of the data signal. In this case, regardless of the clock delay, a single data bit can only pass through one flip-flop at a time.

After reducing the number of pins through shift register programmers, the overall converter only requires a total of 60 pins.
3.6.4 Overall Converter Performance

Figure 3.42. Simulated efficiency vs output power. The output voltages are 1, 1.2, 1.5, 1.8 V. This graph includes $R_{on}, R_{ind}, P_{gd}$, and the controller loss $P_{cntl}$.

The overall converter efficiency as a function of the total output power is plotted in Figure 3.42. Compared to the previous efficiency plot in Figure 3.38, it includes the power consumption of all peripherals: the comparators, FSM controller, PLL, bias current generator, and shift registers. Similar to the previous efficiency graph, the output power is set to a fixed ratio for similar on-time of the output switches. Then, the output power is swept from 0 to 1 W. The peak efficiency of this test is found to be 86.5% at 198 mW. The graph is similar to that of Figure 3.38 except for the decrease in efficiency due to the controller loss. Since controller loss is constant throughout all output power, the efficiency decrease is most significant with lower output power.
3.7 Layout

3.7.1 Bondwire Connections

Figure 3.43. Bondwire connections for the proposed chip package.

Before the layout implementation of the proposed converter, it is a good idea to consider the chip packaging with bondwires. This will also help in the design of the floorplan by considering the lengths of the bondwires available. For example, the output stage in the proposed converter requires low impedance connection to the external inductor and capacitor to maintain high efficiency. Therefore, the output stage would be placed near the pads with short bondwires.
Since the die size was $5\text{mm} \times 5\text{mm}$, QFN package sized $7\text{mm} \times 7\text{mm}$ is chosen to minimize the length of the bondwires. The die is a multi-project chip. As a result, the SDC SIMO converter has 60 pins spread out from the bottom side of the chip. The I/O ring, which protects the pins from electro-static discharge (ESD), forced the pins to be located along the edges of the orange rectangle as shown in Figure 3.43. Because of this, half of the pins on the bottom side of the die needed to be connected to the top side of the package.

### 3.7.2 Overall Placement

![Figure 3.44. Complete layout of the SDC SIMO converter.](image)

![Figure 3.45. Die photo of the fabricated SDC SIMO converter. The area used on the die is 4 x 1.5 mm.](image)

Based on the bondwire connections described in the previous section, the top-level layout blocks were placed as shown in Figure 3.45. The output stage transistors were placed near the
lower part of the die to minimize low bondwire parasitics. The gate drivers were placed right next to these transistors to ensure low propagation delay. The comparators were also placed near these blocks as their input signals originated from these devices. The rest of the system such as the PLL and FSM controller had connections that were less sensitive to parasitics, as they use 1 MHz digital signals. Therefore, they are placed further above for simpler routing.

3.7.3 Analog Circuit Layout

![Comparator preamplifier layout](image)

Figure 3.46. Comparator preamplifier layout. The active area is 20 x 26 µm

Analog circuits that are sensitive to mismatch in the proposed converter include the auto-zeroing comparators, and the PLL. The differential nodes of the comparators were especially
sensitive as the mismatch would introduce offset. Therefore, the circuit layout is organized with extra attention to match layout parasitics connected to corresponding differential nodes. For device matching, a common centroid method is employed to ensure differential transistors have same center of mass. Mismatch can be modeled to have a horizontal and a vertical gradient. By having same center of mass for each transistor, these mismatch gradients cancel out and ensure their sizes are equal. For example, as illustrated in Figure 3.46, the differential transistor pair $M_1$ and $M_2$, are drawn with $M_1$ in the middle, and $M_2$ around it. Substrate connections are located nearby the sensitive transistors to ensure a low impedance connection to the supply. Finally, dummy transistors are placed around the edges to ensure the source and drain of the transistors are under same environment.

Figure 3.47. The layout for the PLL. The active area is 560 x 340 µm
The capacitors used for the loop filter in the PLL is also laid out using common centroid as shown on the left of Figure 3.47. The capacitor plates are divided into smaller unit sizes, and are connected together such that the capacitors have same center of mass located in the middle of the capacitor array.

### 3.7.4 Digital Circuit Layout

![Image of FSM Controller layout](image)

Figure 3.48. The layout of the FSM Controller. The total area used is 245 x 212 µm.

For the digital circuits, accuracy is not of importance. Therefore, to speed up design time, the logic cells are designed to be stackable on a 0.6 µm grid. The pin connections of each logic cells are also on this same grid, allowing large scale implementation to be simple. In addition, the power and ground lines are alternating and placed horizontally as well.
3.7.5 Output Power Stage Layout

Since the W/L of the power transistors is large, each power transistor is made up of smaller power transistor cells connected in parallel. This power transistor cell is visible in Figure 3.49, depicting the layout of high-side (HS) transistor. The power transistors require low resistance connections to its drain and source nodes for higher overall efficiency. Therefore, the metal connections to these nodes include large number of contacts and thick metal lines stacked on top of each other.

![Power transistor cell](image)

Figure 3.49. The high-side transistor layout including 40 power transistor cells, and gate drivers on the left.
3.8 Testbench Design

3.8.1 PCB Overview

To test the SDC SIMO IC, the PCB testbench requires 4 major blocks to operate as outlined by Figure 3.50:

1. Output stage components and load for the outputs.
2. LDOs for reference voltages.
3. External switches to reset/enable FSM controller.
4. FPGA to generate necessary clocks and configuration bits.

The testbench designed for SDC SIMO included the above along with necessary components to interface between them. The list of off-the-shelf components used for setting up this testbench is listed in Table 3.5.
Table 3.5. List of External Components Used for the PCB Testbench

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
<th>Model</th>
<th>Package Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inductor</td>
<td>4.7uH/55mΩ</td>
<td>NRG4026T4R7M</td>
<td>4mm x 4mm</td>
</tr>
<tr>
<td>Output Capacitors</td>
<td>10uF</td>
<td>CL10A106MQ8NNNC</td>
<td>0603</td>
</tr>
<tr>
<td>Load Step Transistors</td>
<td>140mΩ</td>
<td>BSS214N H6327</td>
<td>SOT-23-3</td>
</tr>
<tr>
<td>Potentiometers</td>
<td>250Ω/5W</td>
<td>026TB32R251B1A1</td>
<td>6mm x 6mm</td>
</tr>
<tr>
<td>LDOs</td>
<td>1V/150mA</td>
<td>TLV71310PDBVR</td>
<td>SOT-23-5</td>
</tr>
<tr>
<td></td>
<td>1.2V/150mA</td>
<td>TLV71312PDBVR</td>
<td>SOT-23-5</td>
</tr>
<tr>
<td></td>
<td>1.5V/150mA</td>
<td>TLV71315PDBVR</td>
<td>SOT-23-5</td>
</tr>
<tr>
<td></td>
<td>1.8V/150mA</td>
<td>TLV71318PDBVR</td>
<td>SOT-23-5</td>
</tr>
<tr>
<td>External Switches</td>
<td>SPDT</td>
<td>EG1218</td>
<td>11mm x 4mm</td>
</tr>
<tr>
<td>Digital Isolators</td>
<td>150Mbps</td>
<td>SI8660BA-B-IS1</td>
<td>16-SOIC</td>
</tr>
</tbody>
</table>

Taiyo Yuden’s 4.7 µH 4mm × 4mm inductor is chosen for the proposed testbench. Its low on-resistance minimizes converter conduction losses, while its 46 MHz self-resonant frequency ensures the parasitic capacitance is minimal. Output capacitors are chosen to be conventional 0603 10 µF ceramic capacitors. To allow flexible output load operating condition, potentiometers are used as a load. Maximum output current for all load testing is set to 100 mA to protect the IC circuitry. Using this information, potentiometer with 250 Ω and 5 W rating was chosen for all outputs.

The reference voltage is generated by Texas Instrument’s TLV713 series LDO. This specific LDO was chosen due to its low-noise performance at high-frequencies. This is especially important in this application as the small noise from the LDO will vary the output of the internal comparator, causing system instability. Finally, all interface with FPGA is directed through digital isolators SI8660BA. This allows digitally isolating the ground between noisy FPGA and the IC testbench. Also, regardless of the FPGA output voltage level, it is level-shifted to the testbench input voltage to ensure proper digital operation.
With the chosen components, the PCB testbench is laid out. The inductor is placed as close to the chip as possible to reduce parasitic trace resistance and inductances that may reduce converter efficiency. The output capacitors are also placed close by, to reduce ringing caused by the trace inductances. Reference LDOs are also placed close to the IC in order to provide accurate voltages. The rest of the circuit is laid out around those components and fit into a small PCB. As discussed earlier, the digital isolator are used to interface between the IC and the FPGA for
configuration and backup control purposes. It also separates the ground connections such that left-side ground plane was connected to the IC while the right side was connected to the FPGA. This ensured that noise from FPGA does not interfere with the IC.

The next chapter will discuss the experimental results for the PCB testbench discussed above. In addition, the functionality and performance results will be presented and discussed.
4 Experimental Results and Discussions

This chapter outlines the testing methodology and results of the proposed SDC SIMO converter with 4 outputs. The testing setup is described in Section 4.1 in detail. Section 4.2 presents and discusses the oscilloscope captures of various signals under steady state operation. Section 4.3 includes efficiency plots versus multiple variables and explanations for the resulting curves. Section 4.4 provides the converter response against the load step transient behavior, to characterize its cross-regulation performance. Finally, Section 4.5 summarizes the results and issues encountered.

4.1 Testing Setup

![Testing setup for the SDC SIMO converter.](image)
For testing the proposed converter, a setup as shown in Figure 4.1 is used. This setup includes the SIMO testbench, containing the PCB test board discussed in Chapter 3. The SIMO testbench also includes an FPGA, which generates the necessary clocks and data bits to configure the IC with the desired settings. This FPGA is programmed directly using a computer. Other equipment is the power supply for the FPGA and the SIMO converter test board. For debugging and measurements, a multimeter and an oscilloscope are used. The multimeter is used to measure the final input and output voltages during the efficiency measurements. Lastly, the oscilloscope is used to probe circuit nodes on the PCB for debugging and signal analysis.

Figure 4.2 presents the close-up view of the SIMO testbench. To speed up the efficiency measurements, all four outputs are connected to different potentiometers. A 10Ω resistor is
soldered in series with each potentiometer to ensure a minimum load resistance. The SIMO PCB testbench is powered by two voltage sources. One voltage source is used to power the peripheral circuits, such as the reference voltage LDOs and level shifters. A separate voltage source is used for the SIMO converter IC under test.

4.1.1 Nominal Operation

![Typical Startup Procedure](image1)

Figure 4.3. Typical startup procedure.

![System Components](image2)

Figure 4.4. System components involved with the startup operation.
The typical startup operation of the testbench involves three reset/enable switches: SRST, CNTL_RST, and EN_ICNTL as shown in Figure 4.4. In the beginning, SRST is set high to reset the shift register outputs to default values. CNTL_RST is also set high, making sure that FSM controller starts with a defined state. EN_ICNTL is kept low to direct the FPGA signals to control the output stage, resetting the switches. Next, SRST goes down, and the shift registers are programmed using SCLK, SDATA, and SUPDATE as shown in Figure 4.3. Then, the CNTL_RST signal goes down, such that the FSM controller is enabled. Lastly, EN_ICNTL goes up, allowing the FSM controller to directly control the output stage transistors, and start the operation of SDC SIMO converter.

Figure 4.5. An equivalent circuit during precharging state.
When EN_ICNTL is low, the converter is reset to a precharging state as illustrated in Figure 4.5. This charges all outputs to VDD - V_{TN} as shown in Figure 4.6, where V_{TN} is the threshold voltage of the NMOS output transistors. When EN_ICNTL goes high, the converter starts the normal operation. It initializes to the freewheeling state since all outputs are larger than its reference voltages. This keeps the inductor current at zero until the output voltages drop below 1.8 V. Then, the controller switches to charge V_{o4} and recycle energy every cycle to regulate the output. As other output voltages slowly drop, V_{o3} joins the regulation. This repeats until all outputs are regulated to their respective reference voltages. This soft-starts operation causes the inductor current to rise slowly to its final steady state value. A more conventional soft-start procedure, where the output reference voltages are increased slowly, is also possible. However, this was not tested.

When EN_ICNTL is low, pre-charging is possible as the FPGA generates the required signals to control the output stage. This can be modified to turn on/off any output stage switches as desired. For example, for the comparator test, one output switch is turned off such that the function generator output can be directly fed into that particular output for testing.
4.2 Functionality Tests

4.2.1 Comparator Functionality

Figure 4.7. Simple comparator functionality test. A function generator input (sine wave), and a comparator output (square wave) is shown.

The comparators are one of the most important circuits within the SIMO converter. Many components in the system ranging from the PLL to the FSM controller depend on its functionality. To test the comparator by itself, output switch 1 (S1) is turned off using the FPGA. Then, a 20 Hz with 300 mVpp sine wave, is connected to Output 1. Figure 4.7 displays this function generator input, and its corresponding comparator output. Since the reference voltage is 1V, the output becomes VDD when the input is larger than 1V. The reverse is true when the sine wave is smaller than 1V. With this simple test, the rough functionality of the comparator is verified.
4.2.2 Comparator offset

![Comparator offset testing methodology](image_url)

Figure 4.8. Comparator offset testing methodology.

The performance of the converter also depends on the offset of the comparator. Namely, the zero-current detector across the recycling switch (RC) needs to have a minimal offset. This is because the resistance of the recycling switch is small, making the voltage drop on the transistor small enough to be sensitive to offset. If this zero-current comparator outputs high too early, or too late, it causes a significant amount of inductor current to flow through the freewheeling transistor (FW). The freewheeling transistor is designed to be small to minimize gate drive loss while supporting zero-current conduction. Therefore, if a significant amount of current flowed through it, it would cause large conduction loss.

To measure the offset of the comparator precisely, the setup shown in Figure 4.8 is used. This setup is superior to simply directing function generator output to the input of the comparator. To measure small offsets, the function generator output must have a small amplitude. In order to measure at which amplitude the output of comparator toggles, accurate measurement using the oscilloscope is required. This is often not possible due to the accuracy limitation of the oscilloscope. Therefore, the function generator output is directed to the input resistor divider as shown in Figure 4.8. The function generator output can now be larger, and the voltage when the
comparator output toggles can be deduced more easily. The measured voltage can be calculated from the resistor divider ratio to determine the actual voltage offset of the comparator. Sample output of this test result is shown below in Figure 4.9, where the resistor divider ratio is set to be 21:1.

![Figure 4.9. The comparator offset measurement for the zero-current comparator.](image)

Using this technique, the bias current of the zero-current comparator’s pre-amplifier is varied. Then, the voltage offset is measured with and without auto-zeroing at $V_{in} = 3.3$ V. This data is plotted in Figure 4.10. The experimental data shows that with auto-zeroing disabled, the comparator performs better with less offset. The offset measured at default bias setting is 41.9 mV with auto-zeroing, and 10.7 mV without auto-zeroing. This is in contrast to the simulated
comparator result in the previous chapter, where the auto-zeroing reduced the offset of the comparator.

![Voltage Offset vs Bias Current (V_{vin} = 3.3V)](image)

Figure 4.10. The voltage offset of zero-current comparator vs. bias current.

The main cause of this increase in voltage offset with auto-zeroing, was due to the layout parasitics. The comparator layout block was extracted to determine the parasitic capacitance of the differential nodes. It was found that the differential nodes used for auto-zeroing had significant mismatch in capacitance. The extracted layout was modeled in HSPICE and was simulated with a default bias current of 40 µA, and with a 2 V_{pp} 20 kHz input signal. The simulation used the same comparator testbench as Figure 4.8 where the same resistor divider is used. The resulting waveforms are displayed in Figure 4.11. The offset of the comparator with auto-zeroing was
around 39.5 mV, while without auto-zeroing it was 16.9 mV. The resulting offsets are relatively close to the experimentally measured offsets.

![Graph showing input waves, output with auto-zeroing, and output without auto-zeroing.](image)

Figure 4.11. Extracted simulation of the final comparator, with and without auto-zeroing. From top to bottom: Input waves, output with auto-zeroing, output without auto-zeroing.

Since a large offset in zero-current comparator would introduce premature turn on of the freewheeling switch during CCM, auto-zeroing was disabled throughout the remaining experiments.
4.2.3 State Machine

Figure 4.12. Steady state waveform for the SIMO converter at $V_{in} = 3V$. Top to bottom: Switching node (LXN), $V_{o1}$, $V_{o2}$, and $V_{o4}$.

After the comparator tests, the internal controller was enabled to start the operation of SDC SIMO converter at nominal load ($R_{load1,2,3,4} = 30 \Omega, 24 \Omega, 30 \Omega, 25.5 \Omega$). With a controller clock speed of 50 MHz for the controller, the state machine halted operation after few seconds due to metastability issues. Therefore, the controller frequency is reduced to 25 MHz. The comparator clock frequency is also changed to 25 MHz to ensure no metastability issues. The resulting steady state waveforms are shown in Figure 4.12. As discussed in the previous chapter, the switching node, LXN, should follow the FSM state machine output. Since the converter should be operating in CCM at this loading condition, LXN should be a steadily rising staircase of output voltages 1,
1.2, 1.5, 1.8 V and \( V_{DD} \) at the end of the recycling state. This is clearly the case in Figure 4.12, and the general functionality of the state machine is verified.

![Steady state waveform with \( V_{in} = 3.7 \) V. Top to bottom: Switching node (LXN), \( V_{o1}, V_{o2}, \) and \( V_{o4} \).](image)

Figure 4.13. Steady state waveform with \( V_{in} = 3.7 \) V. Top to bottom: Switching node (LXN), \( V_{o1}, V_{o2}, \) and \( V_{o4} \).

When the input voltage is increased to 3.7 V, the converter operation became highly irregular as shown in Figure 4.13. Compared to the 3 V case, the output voltage ripples are larger and inconsistent. For example, the voltage ripple at output 4 is more than 60 mV. Also, the switching node drops to ground from time to time, implying that the freewheeling switch turns on. With a total output power of 295 mW, the inductor current should never reach the zero current based on the simulations. Therefore, it is evident that the switching cycle is unstable.
The problem was identified to be mainly from the parasitic bond wire inductances connected to the output stage pins. During the design, the bond wire resistances and inductances were calculated. Since the layout was planned with the output stage pins connected with the shortest bond wires, these parasitics were of small value. Due to this reason, they were neglected during final simulations. The worst case bond wire length for the output stage was 0.6 mm. The parasitic resistance becomes:

$$R_{bw} = \frac{\rho l}{A} = \frac{2.44 \times 10^{-8} \times 0.6 \times 10^{-3}}{\pi (12.5 \times 10^{-6})^2} \cong 0.03\Omega$$ (15)

Since 1-mil gold wire bonds are used, the parasitic inductance was estimated to be 0.6 nH. Including these parasitics in the full simulation yields the following result in Figure 4.14.

Figure 4.14. Full simulation including bond wire inductance. From top to bottom: Inductor current, output switch 2 signal (S2), the internal output voltage 2 (\(V_{o2}\)), comparator output for output 2, and comparator clock.
The simulation shows that due to the parasitic inductance, the internal output voltage nodes experience ringing during the switching events. Figure 14 shows that the comparator for output 2 provides a high output even though the internal voltage is smaller than the reference voltage (1.2V). This is because the comparator decision occurs during the ringing of internal nodes.

As observed from Figure 4.15, the comparator compares between Output 2 and the reference voltage during the ringing event. This causes the comparator to sometimes produce a high output erroneously during the ringing event. The converter becomes unstable through these inconsistent comparator outputs as shown in Figure 4.16.
Figure 4.16. Overall view of the converter with ringing instability. From top to bottom: Output switch 2 (S2), internal $V_{o2}$ ($V_{o2,i}$), and switching node (LXN).

This ringing of the internal output voltage is caused by a variety of sources interacting with the bond wire inductance. Figure 4.17 illustrates the occurrence of ringing in different phases. The ringing is separated into four phases and are shown in Figure 4.18 as equivalent circuits.

Figure 4.17. Phases of ringing in the internal output voltage. From top to bottom: Output switches 1 and 2, switching node, internal $V_{o2}$ ($V_{o2,i}$), and parasitic current.
Figure 4.18. Equivalent circuits in different phases of ringing.
The first phase is during the deadtime between output switch 1 and output switch 2. During this time, all output switches are off, causing the inductor current to charge the parasitic capacitance at Lxn. This parasitic capacitance comes from the gate capacitances of output stage transistors. When the output switch 2 turns on in phase 2, the gate driver forces the gate of the output switch transistor to become \( V_{DD} \). During this time, \( V_{o2,i} \) is forced to be equal to Lxn due to the turning on of the transistor. With a strong gate driver, this sudden change causes charges to be added to nodes Lxn and \( V_{o2,i} \). Because of these effects, the voltage at \( V_{o2,i} \) is significantly higher than \( V_{o2} \) at the end of phase 2. The voltage difference between \( V_{o2,i} \) and \( V_{o2} \) causes the parasitic inductance \( L_{bw} \) to source current from \( C_p \). Since \( L_{bw} \) is very small, the parasitic current \( I_p \) rises much faster than \( I_L \) when the transistor is still turning on. This causes a drop in voltage at Lxn and \( V_{o2,i} \) during phase 3. The voltages eventually drop below \( V_{o2} \), and causes \( L_{bw} \) to sink current into \( C_p \). This increases the voltage levels at Lxn and \( V_{o2,i} \) during phase 4. The process repeats between phase 3 and 4 until the parasitic resistance dissipates the ringing while \( I_L \) takes over as the main current source.

Figure 4.19. Close-up of ringing. From top to bottom: S1 and S2, current through bond wire, current through gate capacitance, \( V_{o2,i} \), and Lxn.
Therefore, the ringing is caused by a combination of bond wire inductance, gate driver strength, parasitic gate capacitance, gate driver voltage, and deadtime. Reducing gate driver strength and voltage or reducing gate capacitances are not a good solution as it significantly affects the overall efficiency. Reducing deadtime can reduce the amplitude of ringing, but clock-feedthrough during phase 2 described previously, still results in ringing. Reducing the bond wire inductance is one of the possible solutions to this problem as it increases the frequency of ringing, and therefore reduces its duration. Another solution is to increase the delay for the comparator decision, such that it compares after the ringing has died down. With the current design, this requires reducing the switching frequency of the comparator and the controller greatly. This reduces the resolution of the controller significantly, and therefore was not tested.

In some steady state settings, the comparator latched more often, when the internal output voltage from ringing was below the reference voltage. This allowed some steady states to operate with less instability. This case is true for the input voltage of 3 V with nominal operating conditions as shown in Figure 4.12. Therefore, the remaining tests were done with an input voltage of 3 V set as the nominal case. Also, with larger input voltages, the ringing amplitude exceeded the absolute maximum rating of the 0.18 µm 5 V transistors. The operation of the chip with more than 3.9 V input caused permanent damage to the transistors. Therefore, the data gathered focuses on the operation at lower input voltages.

4.2.4 Phased Locked Loop

Another important part of the system is the PLL. As described in the previous chapter, PLL is necessary to stabilize the output stage switching signals into a constant frequency. This allows easier EMI isolation, and well-defined output ripple voltage. To ensure the frequency stabilization
is taking place correctly, the switching node (LXN) waveform is displayed with FFT. The FFT shows the largest tone at 1 MHz, demonstrating that the converter is indeed operating at 1 MHz.

Figure 4.20. FFT of the switching node (LXN).
4.3 Efficiency

After the functionality tests to verify that the design is operational, efficiency is measured under different operating conditions.

4.3.1 Efficiency versus Total Load

![Efficiency vs All Load (F_{sw} = 1MHz)](image)

Figure 4.21. Efficiency versus total load. The voltage outputs are 1, 1.2, 1.5, and 1.8V. All loads are kept with the same ratio and swept together.

Similar to simulation tests done in the previous chapter, all loads are kept to the same ratio to maintain similar on-time for the output switches. All of the loads were swept together, and the efficiency of the converter was measured as a function of the total output power in Figure 4.21. The peak efficiency of the converter was 72.4 % at an output power of 195 mW with $V_{in} = 3V$. The efficiency was smaller at $V_{in} = 3.3V$ as expected due to increased gate drive loss at light loads.
In contrast to the experimental measurements, the peak efficiency from simulation was observed to be 86.5%. The peak efficiency during experimental measurement is significantly lower than expected due to two reasons: unaccounted parasitic resistances, and converter instability due to ringing. The first reason for efficiency loss was due to the unaccounted parasitic resistance of layout interconnects and bond wires.

Figure 4.22. Current density distribution across Metal 5 for the high-side transistor (HS). 0.1 V is applied between the drain and the source.
To gain more insight into the layout parasitics, output stage was simulated using R3D to calculate the parasitic resistance values. To do this, 0.1 V was applied across the source and drain nodes of each output stage transistors. The distribution of current density on metal 5 layer of the high-side transistor (HS) is illustrated in Figure 4.22 above. As seen from the figure, a $V_{ds} = 0.1$ V was applied to the right side of the layout, where the wire bond pad resides. Due to the fact that the I/O pads are on the right side, most of the current travels through the right side of the transistor. Due to this, the interconnect resistance seen from the bond wires are significant. The interconnect resistances for each output stage transistor is measured with R3D and is listed below.

**Table 4.1. List of Interconnect Resistances for Output Stage Transistors**

<table>
<thead>
<tr>
<th>Output Transistor</th>
<th>Channel (mΩ)</th>
<th>Interconnect (mΩ)</th>
<th>Total (mΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>High-side (HS)</td>
<td>38.4</td>
<td>86.1</td>
<td>124.4</td>
</tr>
<tr>
<td>Low-side (LS)</td>
<td>34.7</td>
<td>80.0</td>
<td>114.7</td>
</tr>
<tr>
<td>Recycling (RC)</td>
<td>38.2</td>
<td>84.7</td>
<td>122.9</td>
</tr>
<tr>
<td>Freewheeling (FW)</td>
<td>544.8</td>
<td>1479</td>
<td>2024</td>
</tr>
<tr>
<td>Output 1 (S1)</td>
<td>64.8</td>
<td>156.7</td>
<td>221.4</td>
</tr>
<tr>
<td>Output 2 (S2)</td>
<td>70.4</td>
<td>170.9</td>
<td>241.3</td>
</tr>
<tr>
<td>Output 3 (S3)</td>
<td>60.0</td>
<td>143.8</td>
<td>203.8</td>
</tr>
<tr>
<td>Output 4 (S4)</td>
<td>72.9</td>
<td>128.9</td>
<td>201.8</td>
</tr>
</tbody>
</table>

As listed in Table 4.1, the interconnect resistances lead to an increase in the parasitic resistance by 3 to 4 times. With the resistance of bond wires being taken into account, an additional 30 mΩ (based on Equation 1) is added to each bond wire in the current path. Figure 4.23 illustrates all the parasitic resistances and inductances discussed so far during inductor current charging, delivering charge to the outputs. Figure 4.24 demonstrates the parasitic components during recycling of inductor current.
Figure 4.23. All parasitic resistances and inductances during charging.

Figure 4.24. All parasitic resistances and inductances during recycling.
Figure 4.25. Efficiency vs. all load at 3 V input. Output voltages are 1, 1.2, 1.5, and 1.8 V. Comparison between including and excluding layout/bondwire parasitic.

Accounting for all these parasitics, a simulation testbench used in the previous chapter was modified. The total output power was swept while the efficiency of the converter was measured. Figure 4.25 plots the efficiency at an input voltage of 3 V, before and after adding the interconnect/bond wire resistances. Due to the additional parasitic resistances, the peak efficiency of the converter drops to 81.4% at an output power of 191 mW. The drop is most significant when the output power is large as the conduction loss becomes dominant.

Table 4.2. Comparison of Efficiency Measured and Simulated at $V_{in} = 3V$, with Nominal Loads

<table>
<thead>
<tr>
<th>Case</th>
<th>$R_{on}$, $P_{gd}$, $P_{cntf}$</th>
<th>$R_{int}$, $R_{bw}$</th>
<th>$L_{bw}$</th>
<th>Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simulated</td>
<td>Included</td>
<td>Excluded</td>
<td>Excluded</td>
<td>86.3%</td>
</tr>
<tr>
<td>Simulated</td>
<td>Included</td>
<td>Included</td>
<td>Excluded</td>
<td>79.1%</td>
</tr>
<tr>
<td>Simulated</td>
<td>Included</td>
<td>Included</td>
<td>Included</td>
<td>74.7%</td>
</tr>
<tr>
<td>Experimental</td>
<td></td>
<td></td>
<td></td>
<td>71.8%</td>
</tr>
</tbody>
</table>
The second reason for the efficiency drop is due to the ringing issue described in the previous sections. Table 4.2 listed above shows the decrease in efficiency from including bond wire inductance at $V_{in} = 3$ V with nominal loads. Although the operation at $V_{in} = 3$ V produced significantly less unstable waveforms than when $V_{in}$ is larger, the ringing still existed. This caused the converter to switch more often than required. Gate drive losses fluctuated from this, causing efficiency to decrease overall. Also, the freewheeling switch turned on prematurely every few cycles due to ringing. This caused large conduction loss due to the large on-resistance of the freewheeling switch.

### 4.3.2 Efficiency versus Single Load

![Efficiency vs Single Load Sweep](image)

Figure 4.26. Efficiency vs. single load sweeps. The output voltages are 1, 1.2, 1.5, and 1.8 V.

To characterize the converter performance further, each load was swept one by one, and efficiency curves are plotted based on the total output power. First, all the outputs are disconnected,
and efficiency is measured once the converter started regulating. Although all the outputs are disconnected, the output power is measured to be 3.3 mW due to the parasitic resistances connected to the outputs. Output 4 is swept from no load to 100 mA as plotted in Figure 4.26 as ‘Vo4 sweep’. Then, output 4 is reset to the nominal load (70 mA), and Output 3 is swept from no load to 100 mA. This is repeated for the rest of the outputs.

As shown in Figure 4.26, the peak efficiency is 81.4% at 171 mW with only output 4 connected to a load. During the Vo4 sweep, the converter operates similar to a single-output SMPS with hysteretic control. Gate drive losses are significantly reduced, causing the efficiency to be much better than other output sweeps. As more outputs are added, the efficiency slowly degrades due to the added gate drive losses and conduction losses.

### 4.3.3 Efficiency versus Switching Frequency

![Efficiency vs Switching Frequency](image)

Figure 4.27. Efficiency vs. switching frequency. The output voltages are 1, 1.2, 1.5, and 1.8 V.
Fixing the output load to nominal, the switching frequency of the converter is varied. This is done by changing the frequency of the reference clock entering the PLL. Because of the limitations imposed from the sawtooth wave generator inside the PLL, the switching frequency is varied only from 500 kHz to 2 MHz, where the PLL was capable of operating. The peak efficiency of the converter was measured to be 73.2% at 757.6 kHz with $V_{in} = 3$ V. As the switching frequency is swept, only the gate drive loss is increased with increased frequency. The conduction loss stays the same, which causes the efficiency to drop with increasing frequency. A slight efficiency drop at 500 kHz is found due to the ringing effect from changing the operating condition.

4.3.4 Efficiency versus Input Voltage

![Efficiency vs Input Voltage (F\text{\scriptsize{sw}} = 1\text{MHz}, P_{\text{load}} = 260\text{mW})](image.png)

Figure 4.28. Efficiency vs. input voltage. The output voltages are 1, 1.2, 1.5, and 1.8 V.

Finally, efficiency versus input voltage was plotted while keeping a 1 MHz nominal frequency, with nominal loads. The peak efficiency in this measurement was 71.7% with $V_{in} = 3$ V. In general, efficiency drops with increasing input voltage due to the increase in gate drive loss.
The nominal load is at a point where the gate drive loss is more significant than the conduction loss. Therefore, although the conduction loss decreased with increased voltage from reduced $R_{on}$, the overall efficiency is worse. With voltages below 3 V, the conduction loss increased dramatically as the output 4 transistor (S4) would experience gate-source voltage below 1.2 V, which is close to its threshold voltage.

### 4.4 Load Regulation

#### 4.4.1 Cross-regulation with Single Load Step

Cross-regulation suppression is one of the most important features in the proposed SDC SIMO converter. To characterize this, Output 1 was put under a load step switching between 0 and

![Figure 4.29. Load step response. From top to bottom: $V_{o1}$, $V_{o2}$, $V_{o3}$, and load step.](image)
100 mA, switching between every 200 µs. The output voltages 1, 2 and 3 along with the load step signal is plotted in Figure 4.29. The cross-regulation is measured to be 0.24 mV/mA on output 2 compared to 0.06 mV/mA measured from ideal simulation in the previous chapter. The close-up of this is plotted in Figure 4.30. The settling time to the new steady-state is found to be around 10 µs. The load transient on output 1 is calculated to be 0.33 mV/mA.

![Figure 4.30. Close-up of cross regulation on V_{o1}, V_{o2}, V_{o3}, during output 1 light-to-heavy load transient.](image-url)
Figure 4.31. An example of parasitic resistance affecting the output voltage.

The increase in cross regulation is mostly due to the parasitic resistance in the circuit as discussed previously. This can be illustrated with the simplified circuit in Figure 4.31. The output comparator compares the internal output voltage and the reference voltage. The internal output voltage connection is very close to the output stage transistor. Therefore, the interconnect resistance is divided up into two components to realistically represent where the comparator is connected to. Because of the significant inductor current flowing through interconnect resistance, \( R_{int} \), and bond wire resistance, \( R_{bw} \), there exists a significant voltage drop across \( V_{o,i} \) and \( V_o \). This forces the output switch to turn off prematurely when the external output voltage, \( V_o \), has not yet reached the reference voltage. Therefore, a voltage offset is observed at the output proportional to the amount of current flowing through the output. This is shown in Figure 4.32, where the output voltage offsets were measured during all load sweep.
Figure 4.32. Output offset voltage vs. all load.

During load step, the outputs experience a sudden change in output load. Therefore, the output voltages experience changes in the offset voltage due to this effect. This causes the output voltage to be different, before and after the load step. This voltage change is used for calculating the cross regulation, which is the reason why the experimental performance is worse than simulated performance.
4.4.2 Cross-regulation with Multi-Load Step

Figure 4.33. Load step response with two output load step.

Transient response with multiple load steps occurring together is plotted in Figure 4.33. In this experiment, Output 1 experiences load step from 0 to 100 mA, as well as output 2 from 0 to 50 mA. Since Output 3 and 4 are regulated with nominal load currents of 50 mA, and 70 mA, the load step current change is larger than the existing load currents. Even with this relatively large load step, the converter is capable of reaching steady state within 20 µs. The cross regulation performance in this case is measured to be 0.147 mV/mA on Output 3.

4.5 Summary of Results and Issues

The proposed SDC SIMO converter is tested under a variety of operating conditions, and its performance is characterized. The performance of the design deviated from the simulation results. Different reasons and possible improvements are discussed in the previous sections. Aside from
the parasitics introduced from the layout and wire bonding, the converter is capable of operating as proposed. It is capable of supporting no loads for all outputs, while having smooth transition between large load changes. Efficiency and cross-regulation performance are reduced due to parasitics, but are consistent throughout large ranges. The following table summarizes the resulting design, and its performance characteristic.

Table 4.3. List of Performance Characteristics Measured on Proposed SDC SIMO Converter

<table>
<thead>
<tr>
<th>Process</th>
<th>TSMC 0.18 µm BCD Gen II</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control Method</td>
<td>Fully Hysteretic Comparator-Based (SDC)</td>
</tr>
<tr>
<td>Topology</td>
<td>4 Buck Outputs</td>
</tr>
<tr>
<td>Input Voltage</td>
<td>2.7 ~ 3.7 V</td>
</tr>
<tr>
<td>Frequency</td>
<td>1 MHz</td>
</tr>
<tr>
<td>Inductor</td>
<td>4.7 µH</td>
</tr>
<tr>
<td>Output Capacitors</td>
<td>10 µF</td>
</tr>
<tr>
<td>Output Voltage Ripple (nominal)</td>
<td>&lt;30 mV</td>
</tr>
<tr>
<td>Load Transient</td>
<td>0.33 mV/mA</td>
</tr>
<tr>
<td>Cross Regulation</td>
<td>0.147 mV/mA</td>
</tr>
<tr>
<td>Max Efficiency</td>
<td>73.2%</td>
</tr>
<tr>
<td>Minimum Load</td>
<td>No Limit</td>
</tr>
</tbody>
</table>

The next chapter concludes the thesis with a summary of design and results. Future improvements are also discussed.
5 Conclusion

5.1 Summary of Results

The SDC SIMO converter is proposed and designed using a simple set of circuit blocks. The converter is made up of a latched comparator, FSM controller, PLL, gate drivers, and an output stage. The design is discussed step-by-step with simulations to verify its functionality in Chapter 3. The final proposed SDC SIMO converter regulates 4 outputs with output voltages of 1, 1.2, 1.5, and 1.8 V. Each output support nominal load of 33, 50, 50, and 70 mA respectively.

The proposed converter was fabricated using TSMC 0.18 µm BCD Gen II technology. The die was packaged into a 60-pin QFN and was tested through multiple operating conditions. The converter is able to achieve 73.2% peak efficiency with 0.147 mV/ mA cross regulation. The Table 5.1 below, compares the performance of the SDC SIMO converter against recent designs from International Solid State Circuits Conference (ISSCC). The cross regulation and efficiency performance is worse than previous designs mostly due to the aforementioned issues regarding layout and bond wire parasitics. However, the overall functionality of the prototype is as proposed. Unlike many of the previous designs, it can regulate outputs with no loads, as well as operating in DCM for light loads. The load transient response across this wide range is consistent. With performance optimizations, the proposed SDC control scheme has potential to be the next step towards industrial adaptation of the SIMO converters.
Table 5.1. A Comparison between Previous Designs and This Work

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>0.35 µm</td>
<td>0.35 µm</td>
<td>0.35 µm</td>
<td>0.18 µm</td>
</tr>
<tr>
<td>Control method</td>
<td>PMB</td>
<td>RBAOT</td>
<td>Error-based</td>
<td>SDC</td>
</tr>
<tr>
<td>Topology</td>
<td>6 buck outputs</td>
<td>4 buck outputs</td>
<td>10 buck outputs</td>
<td>4 buck outputs</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>5.0 V</td>
<td>2.7 ~ 5.0 V</td>
<td>5.0 V</td>
<td>2.7 ~ 3.7 V</td>
</tr>
<tr>
<td>Frequency</td>
<td>2 MHz</td>
<td>1 MHz</td>
<td>0.7 MHz</td>
<td>1 MHz</td>
</tr>
<tr>
<td>Inductor &amp; capacitor</td>
<td>4.7 µH &amp; 10µF</td>
<td>4.7 µH &amp; 10µF</td>
<td>10 µH &amp; 10µF</td>
<td>4.7 µH &amp; 10µF</td>
</tr>
<tr>
<td>Output voltage ripple</td>
<td>&lt; 25 mV</td>
<td>&lt; 30 mV</td>
<td>&lt; 40 mV</td>
<td>&lt; 30 mV</td>
</tr>
<tr>
<td>Load transient</td>
<td>0.93 mV/mA</td>
<td>0.16 mV/mA</td>
<td>0.17 mV/mA</td>
<td>0.33 mV/mA</td>
</tr>
<tr>
<td>Cross regulation</td>
<td>0.31 mV/mA</td>
<td>0.04 mV/mA</td>
<td>0.10 mV/mA</td>
<td>0.15 mV/mA</td>
</tr>
<tr>
<td>Max Efficiency</td>
<td>N/A</td>
<td>87 %</td>
<td>89 %</td>
<td>73 %</td>
</tr>
<tr>
<td>DCM operation</td>
<td>Unsupported</td>
<td>Unsupported</td>
<td>Supported</td>
<td>Supported</td>
</tr>
<tr>
<td>No load operation</td>
<td>Unsupported</td>
<td>Unsupported</td>
<td>Unsupported</td>
<td>Supported</td>
</tr>
</tbody>
</table>

5.2 Future Works

There are multiple improvements that can be made to the design to improve its performance, as well as its reliability.

5.2.1 Layout Optimization

As discussed in Section 4.2.2, the comparator layout was found to have imbalance in parasitic capacitance in its differential nodes, causing the comparator to have significant offset when auto-zeroing is enabled. With optimized layout with better differential node matching, auto-zeroing comparator should have less offset. The resulting comparator should reduce offset of the output voltages. In addition, the freewheeling switch would not turn on prematurely due to an offset, allowing the efficiency of the converter to improve.

Additionally, the sub-optimal placement of output stage transistors forced most of the current to flow on small part of the transistors as discussed in Section 4.3.1. With better placement,
the current flow can be evenly distributed, reducing the interconnect resistance from the layout. This would decrease the overall conduction loss of the system, and allow the converter to be more viable with larger loads. In addition, this would decrease the voltage drop between internal output voltage inside the IC compared to the external output voltage. Therefore, the voltage offset would be reduced with higher loads. The cross regulation performance would also improve due to the smaller amount of voltage offset change.

5.2.2 Ringing Reduction

As found in Section 4.2.3, the main issue with the current design is the instability of the system due to ringing in the internal nodes. These originate mainly from bond wire inductance, and comparator latch timing. Bond wire inductance can be reduced by having multiple pads connected to the same node. This allows multiple bond wires to be in parallel, reducing its equivalent resistance and its inductance. Additionally, this increases reliability of the design.

Increasing the delay for comparator latch was an issue that was not possible. This was mainly due to the long period of time required for the propagation delay of the FSM controller logic. The controller logic can be optimized to reduce this propagation delay, allowing the comparator to gain more delay. In addition, the PLL can be redesigned with slower converter frequency in mind. This would allow slower comparator/controller clock without affecting the controller resolution. By having more delay and/or slower clock frequency, the comparator can operate without error as the ringing dies down.

5.2.3 Over-current protection circuit

An over-current protection circuit would be a great addition to this converter. The FSM controller for the proposed system either charges or discharges the inductor current in every state excluding the freewheeling state. If the comparator fails in any time, or if the logic fails to resolve,
the converter may stay in one state too long. This would cause the inductor current to increase or
decrease to a significant amount of current, possibly damaging the output stage transistors. An
over-current protection circuit would detect the magnitude of inductor current when it reaches a
threshold, and seize operation of the converter to prevent permanent damage.
References


Appendix A  Simulation Testbenches

The following figures show the schematic of the testbenches used.

Figure A.1 Ideal SDC SIMO testbench with ideal comparator, and ideal FSM controller.
Figure A.2. Preamplifier functionality testbench.

Figure A.3. Loop gain AC testbench for the preamplifier.
Figure A.4. Decider functionality testbench.

Figure A.5. Full auto-zeroing comparator functionality testbench.
Figure A.6. FSM Controller functionality testbench.

Figure A.7. Measuring VCO gain of the SDC SIMO using ideal components.
Figure A.8. Functionality test of the PLL using ideal converter.

Figure A.9. Output stage functionality testbench.
Figure A.10. Simulation testbench for approximation of efficiency. This includes $R_{on}$, $R_{ind}$, and $C_{gd}$. 
Appendix B  Transistor Characteristics

The following tables are measured on-resistance and gate capacitance of the transistors used in the output stage.

Table B.1. On-resistance of the Transistors under Different $V_{in}$

<table>
<thead>
<tr>
<th>Switch</th>
<th>$V_{in} = 3$V</th>
<th>$V_{in} = 3.3$V</th>
<th>$V_{in} = 3.7$V</th>
</tr>
</thead>
<tbody>
<tr>
<td>High-side (HS)</td>
<td>44</td>
<td>41</td>
<td>38</td>
</tr>
<tr>
<td>Low-side (LS)</td>
<td>40</td>
<td>37</td>
<td>34</td>
</tr>
<tr>
<td>Recycling (RC)</td>
<td>44</td>
<td>41</td>
<td>38</td>
</tr>
<tr>
<td>Freewheeling (FW)</td>
<td>647</td>
<td>595</td>
<td>544</td>
</tr>
<tr>
<td>Output 1 (S1)</td>
<td>85</td>
<td>71</td>
<td>60</td>
</tr>
<tr>
<td>Output 2 (S2)</td>
<td>99</td>
<td>79</td>
<td>66</td>
</tr>
<tr>
<td>Output 3 (S3)</td>
<td>104</td>
<td>74</td>
<td>57</td>
</tr>
<tr>
<td>Output 4 (S4)</td>
<td>186</td>
<td>103</td>
<td>70</td>
</tr>
</tbody>
</table>

Table B.2. Gate Capacitance of Transistors under Different $V_{in}$

<table>
<thead>
<tr>
<th>Switch</th>
<th>$V_{in} = 3$V</th>
<th>$V_{in} = 3.3$V</th>
<th>$V_{in} = 3.7$V</th>
</tr>
</thead>
<tbody>
<tr>
<td>High-side (HS)</td>
<td>224</td>
<td>239</td>
<td>237</td>
</tr>
<tr>
<td>Low-side (LS)</td>
<td>109</td>
<td>99</td>
<td>121</td>
</tr>
<tr>
<td>Recycling (RC)</td>
<td>224</td>
<td>239</td>
<td>237</td>
</tr>
<tr>
<td>Freewheeling (FW)</td>
<td>32</td>
<td>12</td>
<td>38</td>
</tr>
<tr>
<td>Output 1 (S1)</td>
<td>72</td>
<td>63</td>
<td>87</td>
</tr>
<tr>
<td>Output 2 (S2)</td>
<td>72</td>
<td>61</td>
<td>84</td>
</tr>
<tr>
<td>Output 3 (S3)</td>
<td>91</td>
<td>80</td>
<td>102</td>
</tr>
<tr>
<td>Output 4 (S4)</td>
<td>95</td>
<td>84</td>
<td>106</td>
</tr>
</tbody>
</table>