WIDE-RANGE 7-SWITCH FLYING CAPACITOR BASED DC-DC CONVERTER FOR POINT-OF-LOAD APPLICATIONS

By

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In this thesis a dc-dc converter referred to as the 7-switch flying capacitor (7SFC) based multi-level buck converter intended for point-of-load applications is presented. The 7SFC operates with the principle of “transformability” which allows it to run in several switching modes when paired with a digital controller. The mode is selected based on input and output conditions by estimating the highest efficiency mode. The 7SFC converter utilizes a flying capacitor, which for certain modes allows for a large reduction in switching losses, especially when the converter is operated with high-input voltages. Compared to the conventional 2-phase interleaved buck converter, the 7SFC is able to reduce the size of the output inductors and capacitor by 33%. The 7SFC discrete prototype is able to achieve efficiencies greater than 90% over the majority of the operating range.
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CHAPTER 1:

1. INTRODUCTION

In almost all electronics today, point-of-load (PoL) dc-dc converters are needed to provide regulated dc voltages to various functional blocks in a system. Generally, these functional blocks require different voltage and power levels and, therefore, dedicated PoL converters are used for each block. For these systems, custom designs of the buck converter are almost exclusively used as the PoL of choice. The use of custom PoL designs allows the designer to maximize efficiency and minimize volume for each converter, and optimize the full system performance. However, this increases system-level design complexity, could influence reliability, and increases manufacturing cost [1]. For example, to design, verify and implement up to 10 dedicated PoLs would heavily burden the designer and increase the time-to-market significantly. For these reasons, it is beneficial to have a stand-alone wide-range “universal” converter that can provide a large range of voltages and power levels suitable for all applications, rather than specific ones.

For many applications the success of a PoL is determined by its ability to provide a regulated voltage and power with high power processing efficiency, low volume, and good dynamic performance. The main objective of this thesis is to propose a topology that will act as the aforementioned “universal” converter and meet the necessary requirements for wide-range PoL applications.

1.1 Point-of-Load Converters

Point-of-load converters are used expansively in electronic systems to efficiently distribute power to all of the necessary loads, from communications and computer applications to medical and military areas. PoLs are dc-dc converters that are placed close to the loads they are supplying power to, and provide conversion, regulation and in some cases isolation [2]. A diagram of the intermediate bus power architecture is presented in Figure 1-1. In this system, an ac-dc front-end converter is utilized to provide basic isolation and conversion to a high-voltage bus (generally 48V to 380V). Following this, an isolated dc-dc converter is used to supply an intermediate bus at a lower voltage (typically 3.3V to 48V) from which the PoLs operate. This power architecture
has gained popularity over the last fifteen years and is the main architecture for point-of-load systems [3].

Intermediate bus voltages are heavily tied to particular applications: 8V or 12V for the communications segment, 12V and 24V for computer systems, 3.3V, 5V, 12V and 48V for medical, and voltages even higher for military and aerospace applications [4]. Since isolation is already provided by the previous conversion stages, the PoLs can be non-isolated.

![Diagram of intermediate bus power architecture for point-of-load applications](image)

Figure 1-1: Intermediate bus power architecture for point-of-load applications

According to market research performed by Darnell [4,5], the total market revenue for dc-dc converter modules in 2016 is expected to be $4.3 billion and, for dc-dc converter IC solutions, the market sales are expected to be 32 billion units; both being rapidly growing markets. Particular attention in the studies is given to the non-isolated PoL application segment where the intermediate bus power architecture has gained popularity due to increased system performance. The growth of this market segment relies on the improvements of PoL converters compared to the conventional buck solution. By increasing power processing efficiency, lowering cost, reducing size, and improving configurability, the use of the PoL can be expanded.

In a conventional PoL system each non-isolated PoL block in Figure 1-1 would be a custom buck converter designed based on the intermediate bus voltage and required output voltage and power. In a large system, the design complexity increases directly with the number of required PoLs.
Another drawback of the conventional buck solution is the dependence of system performance on the input and output operating conditions. For high intermediate bus voltages, the power processing efficiency of the buck converter significantly degrades.

Due to these limitations, the focus of this thesis will be on the design of a novel non-isolated PoL converter that can operate for a wide range of operating conditions with high power processing efficiency and low volume compared to the conventional buck converter.

1.2 Thesis Objective

The objective of this thesis is to analyze the limitations of existing PoL solutions and to propose a new solution that can improve on them. The specific limitations that are being addressed are wide-range conversion, overall volume and power processing efficiency. This is done by introducing a novel non-isolated topology that utilizes specific advantages of several pre-existing topologies and combining them into a single low-volume high-efficiency converter. Compared to the conventionally used 2-phase interleaved buck converter, this new topology improves in the following ways:

- Taking advantage of multi-level dc-dc conversion
- Multi-mode converter operation for efficiency optimization
- Significant reduction in reactive component volume
- Reducing silicon area needed for implementation

1.3 Thesis Outline

The material of this thesis is presented in the following sequence:

In Chapter 2 pre-existing topologies for non-isolated PoL applications are presented. These topologies include the conventional 2-phase interleaved buck converter, as well as previously proposed alternatives, the double step-down buck [6] and the 3-level buck converter [7]. The topology limitations are discussed, clearly stating specific areas of improvement, which are addressed in Chapter 3 with the introduction of the new topology. Following this discussion, prior art for control is presented including digital control techniques for dc-dc converters.
Chapter 3 begins by outlining the design strategy used to come up with the novel 7-switch flying capacitor (7SFC) based multi-level buck converter. Then, the principle of operation and full analyses of converter losses and volume estimations are presented. Control techniques are discussed for the 7SFC converter and the controller complexity is analyzed.

In Chapter 4 an experimental prototype that was designed, built and tested is introduced with the following specifications: $3V < V_{in} < 48V$, $1V < V_{out} < 12V$, $I_{load} < 6A$. Power loss breakdowns for the 7SFC converter and the conventional interleaved buck converter are compared over this operating range. Efficiency results for the 7SFC multi-level buck are presented for many operating points. The volume comparison for reactive components is verified through inductor current ripple and transient comparisons.

The thesis conclusion as well as possible future work with regards to the 7SFC multi-level buck converter is presented in Chapter 5.
CHAPTER 2:

2. PRIOR ART IN NON-ISOLATED POINT-OF-LOAD CONVERSION

This section is a review of the conventional and previously proposed technologies for non-isolated point-of-load conversion in terms of both topologies and complementary control methods. Single-stage topologies are preferred for this application due to the design simplicity, and the efficiency improvements by neglecting a front-end conversion stage. First, three topologies will be examined as background in non-isolated PoL topologies, the 2-phase interleaved buck converter, the double step-down buck converter [6], and the 2-phase 3-level buck converter [7]. In the second part of this section digital control methods are discussed as a means of controlling PoLs.

2.1 Non-Isolated Point-of-Load Converter Topologies

The buck converter topology is the most widely used topology for non-isolated PoLs due to the extensive research with regards to its design and control [8]. Also, to improve on the buck converter’s performance, many topologies and control methods have been derived to optimize efficiency for particular applications of PoLs [9-13]. In these topologies, the trade-off for design simplicity over flexibility for a wide range of conversion ratios is made. Multi-level converters have also been adopted for high-power converters [7], and recently proposed for low-power applications as well [14]. Multi-level topologies have gained attention over recent years due to their improvements in efficiency and volume over conventional buck topologies at the cost of added design complexity. Three topologies will be discussed in this section as a review of prior art in non-isolated PoL conversion, 1) the 2-phase interleaved buck, 2) the double step-down buck proposed by Nishijima [6] and 3) the 2-phase 3-level buck converter, whose single-phase counterpart was proposed by Meynard [7]. The three topologies are shown in Figure 2-1.
Along with its single-phase counterpart, the 2-phase interleaved buck converter of Figure 2-1a) is a popular choice for power modules and wide-range step-down conversion. The buck converter is very well understood, and a plethora of research has been done modeling its losses and control [8]. This makes it an attractive, simple solution for many designers. However, it has significant drawbacks when it comes to high step-down conversions, which is required in a large number of applications. For the sake of convenience the switching sequence and inductor waveforms for the 2-phase interleaved buck converter operating with a duty ratio of $D < 0.5$ is shown in Figure 2-2. The conversion ratio for this converter is $M(D)=D$, and it can operate from $0 < D < 1$. 

Figure 2-1: Prior art in non-isolated point-of-load conversion. a) Interleaved buck converter, b) Double step-down buck converter, c) 2-phase 3-level buck converter

2.1.1 2-Phase Interleaved Buck Converter
The first limitation of the buck converter for high step-down conversion ratios is in the range of duty ratio values. Since the conversion ratio is directly related to the duty ratio, the highest possible step-down conversion depends on the lowest duty ratio possible in the converter. In high-frequency converters, which are common for low-volume applications, low duty ratio values become more difficult to produce.

Other disadvantages of the buck converter relate to the power density and volume limitations of the topology. The buck converter switches must all be rated to block the full input voltage of the converter which impacts the silicon area taken up by the switches. Along with this, the switching losses of the converter are directly related to the voltage across the switches. For high input voltages the switching losses dominate the total losses of the converter, thus reducing the efficiency and power density. For dc-dc converters with switching frequencies in the hundreds of
kilohertz, as targeted in this thesis, the reactive components take up the majority of the volume. Generally, the inductor is chosen to achieve a particular current ripple specification, as shown in Eq. (2-1) for the 2-phase interleaved buck converter where $V_{in}$ is the input voltage, $V_{out}$ is the output voltage, $I_{load,\text{max}}$ is the maximum load current of the converter, $\Delta i_L$ is the desired peak-peak current ripple, and $f_s$ is the switching frequency.

$$L = \frac{(1-V_{out}/V_{in})V_{out}I_{load,\text{max}}}{f_s \Delta i_L I_{load,\text{max}}}.$$  

(2-1)

The volume of the inductor is related to the energy storage requirement [15] based on Eq. (2-2),

$$\text{Inductor Volume} \propto L \cdot (i)^2,$$  

(2-2)

where $L$ is the chosen inductance value from (1) and $i$ is the maximum current in the inductor. For high input voltages, and conversion ratios close to $M(D)=0.5$, the required inductance value will be large, thus presenting a major contribution to the overall converter volume.

2.1.2 Double Step-Down Buck Converter

The double step-down buck converter of Figure 2-1,b) was proposed by Nishijima et al. [6] as an alternative to the 2-phase interleaved buck converter intended for high step-down ratios. Since it incorporates a flying capacitor, $C_{fly}$, it is able to reduce the switching losses and voltage ratings of the switches without increasing the number of switches. This converter has been analyzed in detail in previous work [16] and has been shown to achieve higher efficiencies than the 2-phase interleaved buck converter over its operating range. The conversion ratio for this topology is $M(D)=D/2$ and it operates over the range of duty ratios of $0<D<0.5$. For completeness, the switching sequence and relevant inductor waveforms for the double step-down buck are provided in Figure 2-3. When operating in steady-state, the flying capacitor has approximately half of the input voltage across it.
Figure 2-3: Switching sequence and inductor waveforms for the double step-down buck converter.

As can be seen from Figure 2-3, three out of four of the switches, all except for SW3, are only required to block half of the full input voltage. This will significantly reduce the silicon area requirement for this topology compared to the 2-phase interleaved buck. In terms of power density, all four of the switches experience switching losses proportional to half of the input voltage, as opposed to the full input voltage in the conventional buck converter. This explains the efficiency and power density improvements of the double step-down buck. Furthermore, the output inductors can be reduced in size compared to the interleaved buck converter for the same current ripple requirement. The equation for the selection of inductance for the double step-down buck converter is shown in Eq. (2-3),

$$L = \frac{\left(1 - \frac{2V_{out}}{V_{in}}\right)V_{out}I_{load,max}}{2f_s\left(\frac{\Delta i_L}{I_{load,max}}\right)}, \quad (2-3)$$

where $V_{in}$ is the input voltage, $V_{out}$ is the output voltage, $I_{load,max}$ is the maximum load current, $\Delta i_L$ is the desired peak-peak current ripple, and $f_s$ is the switching frequency.
The main limitation of the topology is a much reduced operating range compared to the 2-phase interleaved buck converter. Given the duty ratio range of $0<D<0.5$, the converter can only provide conversion ratios up to $\frac{1}{4}$. Thus, for a wide-range converter which requires voltage conversion above $\frac{1}{4}$, the double step-down buck is not suitable as a full solution.

The double step-down buck converter also has the advantage of inherent inductor current balancing. Observing the dc equivalent circuit of the converter shown in Figure 2-4, it can be seen that the inductor currents, $I_{L_1}$ and $I_{L_2}$, are forced equal if the duty ratios for State 1 and State 3 are the same. Also, if we assume the equivalent phase resistances for $L_1$ and $L_2$, $R_{eq1}$ and $R_{eq2}$, are close, then the flying capacitor, $C_{fly}$, will also be approximately half of the input voltage without the need for additional control.

Figure 2-4: DC equivalent circuit for the double step-down buck converter

2.1.3 2-Phase 3-Level Buck

The 2-phase 3-level buck converter shown in Figure 2-1c) and its single-phase counterpart are less conventional topologies for low to medium power levels of PoL conversion. The original research on the 3-level buck converter was performed by Meynard and Foch [7] where they model several variations of the multilevel converter. The 3-level buck was originally proposed as a high voltage inverter since the high voltage across the power switches in this application was a serious reliability issue [17]. As shown in [7], with the addition of a single flying capacitor the conventional buck converter becomes a 3-level converter that can be used for step-down dc-dc conversion. As a result, the blocking voltage requirement for all of the switches is reduced by
half, and thus reduces switching losses for each switch as well. The 3-level buck can be operated with two distinct switching sequences to achieve conversion for all step-down cases. The first sequence achieves a conversion ratio of $M(D)=D$ with a duty ratio range of $0<D<0.5$ and the second sequence achieves a conversion ratio of $M(D)=\frac{1}{2}+D$ with the same duty ratio range. In this thesis we are interested in 2-phase converters so the switching sequence and relevant inductor waveforms for the 2-phase 3-level buck is provided in Figure 2-5 for $M<0.5$. The switching sequence and inductor waveforms for the $M>0.5$ case has been referred to Appendix A. The 2-phase 3-level buck converter has two flying capacitors, $C_{fly1}$ and $C_{fly2}$, which have approximately half of the input voltage across them in steady-state.

The main advantage of the 2-phase 3-level buck is the reduction in output inductor volume based on the current ripple requirement. The inductor selection for the 2-phase 3-level buck based on the current ripple requirement is shown in Eq. (2-4),

$$L = \frac{\left(\frac{1}{2} - \frac{V_{in}}{V_{out}}\right)V_{out}I_{load,max}}{f_s\left(\frac{\Delta i}{I_{load,max}}\right)}.$$  \hspace{1cm} (2-4)

where $V_{in}$ is the input voltage, $V_{out}$ is the output voltage, $I_{load,max}$ is the maximum load current, $\Delta i_L$ is the desired peak-peak current ripple, and $f_s$ is the switching frequency. Compared to the 2-phase interleaved buck converter the output inductors can be reduced by more than half, and compared to the double step-down buck converter the inductors are halved, using Eq. (2-2) for inductor energy storage capacity. Since the reactive components are the major contributors for volume in dc-dc converters operating in the hundreds of kilohertz, this reduction is a significant benefit of the 2-phase 3-level buck converter. At the same time, however, core losses for each inductor are doubled due to the increased apparent frequency in the inductor.

The drawbacks for the 2-phase 3-level buck converter appear mainly due to the increased number of switches it requires to operate. The switching losses for each switch is reduced, however, the fact that eight switches are operated in every switching cycle, as opposed to four in the interleaved buck converter, diminishes this advantage significantly. The result is an overall efficiency that is comparable to the interleaved buck converter, with the clear advantage of significantly reduced volume as mentioned earlier. Along with the additional switches, the 2-
phase 3-level buck requires two flying capacitors, increasing volume further. Unlike the double step-down buck converter, the 2-phase 3-level buck does not have inherent current balancing.

Figure 2-5: Switching sequence and inductor waveforms for the 2-phase 3-level buck converter operating in the $M<0.5$ mode
This implies that the flying capacitors are not guaranteed to be balanced at half of the input voltage. Some previous work has been done that suggests the flying capacitors can be monitored, and controlled to achieve the desired voltage [18,19], however, this increases the controller complexity for this topology.

2.2 Digital Control

Digital control has gained increasing attention over the last ten years for low-cost volume-sensitive applications. In most cases a digital controller can be fully integrated on-chip and consume a fraction of the volume and power of the converter itself [20-21]. Compared to its analog alternative, a digital controller does not require large capacitors and resistors to make up the control feedback network. Another advantage of digital control is the increase in flexibility for the controller compared to an analog controller. In a digital controller, since the compensator is implemented using digital arithmetic, with the change of a single number the compensator design can be adjusted. In an analog implementation, this degree of flexibility would require a large bank of capacitor and resistor values, and additional circuitry to select desired values, which would increase the controller volume. This makes digital control an attractive solution for a wide-range converter that has varying input voltage, output voltage and load current.

To deal with sudden changes in the load current, a frequent occurrence for PoLs, several digital control methods exist. The most conventional method is by tuning the PID coefficients in the digital compensator to achieve a good transient response. This, however, has limitations when dealing with a wide range of input voltages, output voltages and load currents since the PID can only be optimized for a certain range. Time-optimal control [22] is a non-linear solution to the issue of transients that can function for any variation of input voltage, output voltage and load current. In a time-optimal controller, when a load transient occurs, the PID is bypassed and the inductor current is either ramped up or ramped down until the charge in the output capacitor is recovered and has settled to the desired output voltage. Once this has completed, the PID is re-initialized and resumes operation. The advantages of a time-optimal control other than flexibility for converter parameters are a fast dynamic response, in one switching cycle, and reduced output voltage deviation compared to a tuned PID controller. This allows for a reduction in the output
capacitance, one of the most spacious elements of the converter. This method is used as the benchmark for transient control in Chapter 3 for output capacitor sizing.
3. **A Novel Flying Capacitor Based DC-DC Topology**

This section proposes a novel dc-dc converter as a solution to the wide-range “universal” dc-dc converter issue. To address the design issue of a novel dc-dc converter for a wide-range application the operating range was divided into four categories: 1) high voltage, low current, 2) high voltage, high current, 3) low voltage, low current, and 4) low voltage high current, as shown in Figure 3-1, where the voltage is the input voltage $V_{in}$ and the output current is $I_{load}$. For high input voltages switching loss should be avoided, and for high output currents switch conduction loss is mitigated. For low voltage and low output current conditions, gate drive losses are avoided and specialized control techniques such as phase shedding can be used.

- **High Input Voltage, Low Output Current**
  - Trade-off switching loss with conduction loss
- **High Input Voltage, High Output Current**
  - Low switching loss and low conduction loss
- **Low Input Voltage, Low Output Current**
  - Low gate drive losses
  - Control techniques
- **Low Input Voltage, High Output Current**
  - Low conduction loss where there can be switching loss

**Figure 3-1:** Four quadrants of the operating range

By looking at the problem in this way, different topologies, such as the ones in Chapter 2, could be categorized to achieve high efficiency in one category but not the others. For example, the interleaved buck converter has good efficiency for low input voltages where switching losses are less dominant, and the double step-down buck converter has high efficiency for high step-down cases. A summary of the prior art of Chapter 2 categorized into the four quadrants of the operating range is shown in Figure 3-2.
The new topology, referred to as the 7-switch flying capacitor multi-level buck converter, or 7SFC, is shown in Figure 3-3. As the name suggests, it has an increased number of switches compared to the conventional interleaved buck converter and double step-down converter. Paired with a digital controller, the added benefits of the 7SFC converter are manifold in terms of efficiency, volume, and flexibility.

**Figure 3-2:** Prior art categorized into the four quadrants of the operating range

<table>
<thead>
<tr>
<th>High Input Voltage, Low Output Current</th>
<th>High Input Voltage, High Output Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>- 2-phase, 3-level buck</td>
<td>- Double step-down buck</td>
</tr>
<tr>
<td>- 2-phase, 3-level buck</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Low Input Voltage, Low Output Current</th>
<th>Low Input Voltage, High Output Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>- Single-phase buck</td>
<td>- Interleaved buck</td>
</tr>
<tr>
<td>- Single-phase, 3-level buck</td>
<td></td>
</tr>
</tbody>
</table>

It utilizes specific advantages from the prior art, such as the wide conversion range of the interleaved buck converter, the high step-down advantages of the double step-down buck, and the reduced switch ratings and switching voltages of the 3-level converter, to form a complete solution that can provide high efficiency and high power density for a wide range of conversion ratios. The principle of operation is discussed next, followed by a complete loss breakdown for each mode, converter volume estimation and some implementation details. The controller is then discussed and general control issues are summarized.
3.1 Principle of Operation

The 7-switch flying capacitor (7SFC) multi-level buck converter operates on the principle of “transformability”, which refers to its ability to choose its mode of operation based on operating conditions. This mode changing characteristic is facilitated by a complementary digital controller. The three modes of operation being presented here are: 1) interleaved buck mode, 2) high step-down mode, and 3) 3-level buck mode. The interleaved buck mode is derived from the 2-phase interleaved buck converter, the high step-down mode from the double step-down buck converter and the 3-level buck mode from the 3-level buck. To maintain the reduced switch ratings of half of the maximum input voltage across all of the switches, an advantage of the double step-down buck and 3-level buck, the modes must be operated accordingly. The mode with the highest efficiency is selected by the digital controller based on a look-up table.

The following sub-sections present the switch operation and particular details of each of the modes of the 7SFC based multi-level buck converter followed by a description of the digital controller implementation.

3.1.1 7SFC: 2-Phase Interleaved Buck Mode Operation

In the 7SFC based multi-level buck converter the interleaved buck mode can only be used for a reduced input voltage range. This is due to the fact that we require that all of the switches are rated for a maximum blocking voltage of \( V_{in,max}/2 \), where \( V_{in,max} \) is the highest input voltage of the operating range. In the interleaved buck mode of operation all of the switches are exposed to the full input voltage so the maximum input voltage to operate this mode would be \( V_{in,max}/2 \). The interleaved buck mode is mainly used for conversion ratios close to and greater than 0.5, and it is the only mode that can provide a conversion ratio greater than 0.5. The conversion ratio for the interleaved buck mode is shown in Eq. (3-1),

\[
M(D) = D ,
\]  

(3-1)

where \( M(D) \) is the conversion ratio and \( D \) is the duty ratio for the mode.
The switching sequence for the 7SFC interleaved buck mode with $D > 0.5$ is shown in Figure 3-4. $SW_1$, $SW_2$ and $SW_4$ remain ‘ON’ which holds the intermediate capacitor voltage, $V_{Cfly}$, at the input voltage. This mode operates the same as a conventional interleaved buck converter, where $SW_7$ and $SW_5$ act as the main switches, and $SW_3$ and $SW_6$ act as the synchronous rectifiers, for the $L_1$ and $L_2$ phases respectively. One difference incurred from utilizing the interleaved buck converter mode in the 7SFC which is not present in the conventional interleaved buck converter is the increased current in $SW_1$, and $SW_4$ during State 1. In this state the switches must conduct the full load current, which increases conduction losses in these transistors.

Figure 3-4: Switching sequence and inductor waveforms for the interleaved buck mode of the 7SFC converter operating with $D<0.5$
The switching sequence for $D < 0.5$ is shown in Figure 3-5 where the switches have the same functions as for the $D > 0.5$ case, however, $SW_1$ and $SW_4$ do not conduct increased current at any point during the switching cycle.

Figure 3-5: Switching sequence and inductor waveforms for the interleaved buck mode of the 7SFC converter operating with $D>0.5$

The inductor current ripple for the interleaved buck mode is represented by $\Delta i_{L-AB}$, and shown in Eq. (3-2),

$$\Delta i_{L-AB} = \frac{(V_{in}-V_{out}) \cdot \frac{V_{out}}{V_{in}} \cdot T_s}{L},$$

(3-2)

where $V_{in}$ is the input voltage, $V_{out}$ is the output voltage, $T_s$ is the switching period and $L$ is the inductance value.

3.1.2 7SFC: High Step-Down Mode Operation
The high step-down mode of the 7SFC is derived from the double step-down buck converter presented in Chapter 2, and provides the highest efficiency for high step-down cases, as the name suggests. Like the double step-down buck, this mode of operation has a limited range of operation of 0<\(D<0.5\) and conversion ratio shown in (3-3),

\[
M(D) = \frac{D}{2},
\]  

(3-3)

where \(M(D)\) is the conversion ratio, and \(D\) is the duty ratio. The main advantage of the high step-down mode of the 7SFC from the double step-down buck converter is that with the addition of two switches, \(SW_7\) and \(SW_5\), all 7 of the switches in the 7SFC can be rated at half of the full input voltage. The benefit of a lower voltage rating for a switch is a reduced volume and figure of merit compared to a higher voltage switch [23]. Figure of merit is a measure of the quality of a specific semiconductor device, used to compare different devices. The switching sequence for the 7SFC operating in the high step-down mode is shown in Figure 3-6.

Figure 3-6: Switching sequence and inductor waveforms for the high step-down mode of the 7SFC converter
Observing the switching sequence it can be seen that another difference from the double step-down converter of Chapter 2 is the current division during State 2 and 4. In these synchronous rectification states the inductor currents are divided amongst $SW_2$, $SW_3$, $SW_5$, $SW_6$, and $SW_7$ based on their on-resistances. This distributes the current amongst the switches to achieve lowest power losses naturally compared to if $SW_5$ and $SW_7$ were not present.

The inductor current ripple for the high step-down mode is represented by $\Delta i_{L-HSD}$, and shown in Eq. (3-4),

$$\Delta i_{L-HSD} = \frac{(V_{in} - V_{out})}{(2V_{out}/V_{in})} T_s,$$

where $V_{in}$ is the input voltage, $V_{out}$ is the output voltage, $T_s$ is the switching period and $L$ is the inductance value.

### 3.1.3 7SFC: 3-Level Buck Mode Operation

The 3-level buck mode of the 7SFC converter is a simplified version of the two-phase 3-level buck introduced in Chapter 2. This mode is operated with both inductors in parallel by keeping $SW_5$ and $SW_7$ on over the full switching cycle. This allows the load current to be split between the two inductors, reducing the volume requirement and losses of the inductors, as would be seen in any 2-phase topology. This mode operates with a duty ratio range of $0 < D < 0.5$ and a conversion ratio of $M(D) = D$, where $M(D)$ is the conversion ratio, and $D$ is the duty ratio. Similar to the high step-down mode the switches are switched at half of the input voltage, reducing switching losses as well. The 3-level buck mode has many potential savings in terms of efficiency however there are also several control issues, such as intermediate capacitor balancing and inductor current balancing, which make it more difficult to use.

The switching sequence and inductor voltage and current waveforms for the 3-level buck mode are shown in Figure 3-7. The current division during synchronous rectification is similar to that of the high step-down mode as well since several switches are present in the conduction path.
Figure 3-7: Switching sequence and inductor waveforms for the 3-level buck mode of the 7SFC converter

For this mode of operation, since the inductors are in parallel, the advantages of interleaved operation from the 2-phase 3-level buck of Chapter 2 are lost. The consequence of this is an increased output capacitor value for the same output voltage ripple compared to that topology. Also, some of the switches, such as $SW_1$, $SW_2$, $SW_3$ and $SW_4$, are exposed to the full load current during certain periods of the switching cycle, thus increasing conduction losses compared to the 2-phase 3-level buck converter.

The inductor current ripple for the 3-level buck mode is represented by $\Delta i_{L-3LB}$, and shown in Eq. (3-5),

$$\Delta i_{L-3LB} = \frac{(V_{in} - V_{out})}{L} \left( \frac{V_{out}}{V_{in}} \right) T_s,$$

where $V_{in}$ is the input voltage, $V_{out}$ is the output voltage, $T_s$ is the switching period and $L$ is the inductance value.

3.1.4 Digital Controller for the 7SFC Converter
A digital controller was chosen for the 7SFC based multi-level buck converter since it easily allows for the control of multiple modes of operation, where the switches are operated differently for each mode. Compared to conventional controllers the control system for the 7SFC converter requires additional features. The full control system for a voltage mode controller is shown in Figure 3-8. The output voltage regulation control loop consists of an output voltage sensor, whose gain is represented by $H(s)$, followed by an analog-to-digital converter (ADC) to translate the output voltage into the digital domain. In the digital voltage controller the sensed output voltage, $V_{out}[n]$, is compared to a desired output voltage, or reference, $V_{ref}[n]$, to produce an error signal, $error[n]$, which is sent to the digital compensator. The digital voltage compensator produces a duty ratio command, $D[n]$, based on current and previous error values and previous duty ratios, to be modulated by the digital pulse width modulator (DPWM) to control the switches of the dc-dc converter. This is a typical voltage mode control loop for dc-dc converters.

![Figure 3-8: Voltage mode controller for the 7SFC converter](image)

The important blocks of the digital controller, designed for the 7SFC converter, are the DPWM and the Mode Select blocks. The Mode Select block takes the input voltage $V_{in}$, desired output voltage $V_{ref}$, and information about the required output current $I_{ref}$, to determine the operating mode. In a final product for a power module the user should be able to select the operating conditions, so this information is assumed to be available to the controller. The Mode Select
block contains a look-up table that stores which modes have the highest efficiency for specific operating conditions, and therefore the highest efficiency mode can always be selected. The *Mode Select* block sends the required mode of operation, *Mode*, to the *DPWM* which contains switching sequences for each mode. Using the duty ratio, $D[n]$, from the compensator, and the *Mode* input from the *Mode Select* block, the *DPWM* modulates the switches accordingly.

3.2 Loss Breakdown

A loss breakdown for all of the modes of the 7SFC based multi-level buck converter is provided in the following sections. Once the losses have all been modeled, numerical comparisons can be made to the alternative topologies presented in Chapter 2.

3.1.1 Conduction Losses

The conduction losses in the converter are governed by the resistive losses in the MOSFETs and the inductors. The equivalent series resistance (ESR) of the output capacitor and the flying capacitor is considered negligible and ignored in this analysis. The equation for conduction loss, represented by $P_{\text{cond}}$, is well understood [8] and shown in Eq. (3-6),

$$P_{\text{cond}} = i_{\text{RMS}}^2 \cdot R,$$

where $i_{\text{RMS}}$ is the RMS current through a resistor, and $R$ is the resistor value.

This method applies for all of the resistive elements of the converter, and since the analysis is repetitive, the full conduction loss breakdown for each mode of the 7SFC converter is referred to Appendix B. Details with regards to adding RMS currents is provided in Appendix C.

3.1.2 Switching Losses

The switching losses are caused by the current-voltage overlap during the switching transitions of the MOSFETs. For a turn-on transition, as the input capacitance of the MOSFET is charged, the drain current will rise and the voltage across the MOSFET will fall. Similarly, for a turn-off transition, the input capacitance is discharged and the current reduces as the drain-source voltage rises. This is known as a hard switching transition. A soft transition, which does not cause switching losses, utilizes the body-diode of the MOSFET to conduct prior to a switching
transition. This causes the voltage to be equal to the diode forward voltage drop, which is considered negligible here, as the current rises or falls in the MOSFET.

For the interleaved buck mode of operation the only two switches experiencing hard switching transitions are $SW_7$ and $SW_5$. The remaining switches do not demonstrate this category of loss because $SW_1$, $SW_2$ and $SW_4$ are always on, and $SW_3$ and $SW_6$ have soft-switching transitions. The equations for turn-on switching losses for $SW_7$ and $SW_5$, i.e. $P_{SW7,ON-IB}$ and $P_{SW5,ON-IB}$, are shown in Eq. (3-7),

$$P_{SW5,ON-IB} = P_{SW7,ON-IB} = \frac{1}{2} \cdot V_{in} \cdot \left(\frac{I_{load}}{2} - \frac{\Delta i_{L,IB}}{2}\right) \cdot f_s \cdot t_{on}, \quad (3-7)$$

where $V_{in}$ is the input voltage, $I_{load}$ is the load current, $\Delta i_{L,IB}$ is the inductor current ripple for the interleaved buck mode, $f_s$ is the switching frequency, and $t_{on}$ is the overlap time of the voltage and current during the turn-on transition. The turn-off switching losses, $P_{SW7,OFF-IB}$ and $P_{SW5,OFF-IB}$ are shown in Eq. (3-8),

$$P_{SW5,OFF-IB} = P_{SW7,OFF-IB} = \frac{1}{2} \cdot V_{in} \cdot \left(\frac{I_{load}}{2} + \frac{\Delta i_{L,IB}}{2}\right) \cdot f_s \cdot t_{off}, \quad (3-8)$$

where $t_{off}$ is the overlap time of the voltage and current in the MOSFET during the turn-off transition.

The switching loss analysis for the high step-down mode of operation is more involved than the interleaved buck mode, considering six out of seven of the switches are operated in one switching cycle. As expected $SW_3$ will not experience any switching losses since it remains on through the whole cycle. The analysis is performed by observing the transition between each state, starting with $State$ 1 to $State$ 2. For this transition $SW_1$ experiences a hard turn-off and to maintain the continuous current in the inductor the body diodes of $SW_2$ and $SW_5$ are forced to conduct. Therefore the turn-on transition for $SW_2$ and $SW_5$ is soft, and will not incur switching losses. The transition between $State$ 2 and $State$ 3 begins with the turn-off of $SW_6$ and $SW_7$. Once again, to maintain the continuous current in each inductor their body diodes will begin conducting producing soft turn-off transitions. Then, $SW_4$ is turned on with a hard transition to start ramping up the inductor current, producing turn-on switching losses. The transition to $State$ 4 has the opposite effect, with $SW_4$ turning off with a hard transition, followed by the soft turn-on
of $SW_7$ and $SW_6$. The final transition back to State 1 consists of the soft turn-off transition of $SW_2$ and $SW_5$ followed by the hard turn-on of $SW_1$. The relevant switching losses for $SW_1$ and $SW_4$, the only hard-switched switches, i.e. $P_{SW_1,ON-HSD}$, $P_{SW_4,ON-HSD}$ and $P_{SW_1,OFF-HSD}$, $P_{SW_4,OFF-HSD}$, are shown in Eqs. (3-9,3-10),

$$P_{SW_1,ON-HSD} = P_{SW_4,ON-HSD} = \frac{1}{2} \cdot \left( \frac{V_{in}}{2} \right) \cdot \left( \frac{l_{load}}{2} - \frac{\Delta i_{L-HSD}}{2} \right) \cdot f_s \cdot t_{on},$$  

$$P_{SW_1,OFF-HSD} = P_{SW_4,OFF-HSD} = \frac{1}{2} \cdot \left( \frac{V_{in}}{2} \right) \cdot \left( \frac{l_{load}}{2} + \frac{\Delta i_{L-HSD}}{2} \right) \cdot f_s \cdot t_{off},$$

where $\Delta i_{L-HSD}$ is the inductor current ripple for the high step-down mode.

The switching loss breakdown for the 3-level buck mode of operation follows that of the high step-down buck closely, however, there are fewer switching elements. $SW_5$ and $SW_7$ remain on through the whole switching cycle connecting both inductors in parallel. The only switches experiencing hard switching transitions are $SW_1$ and $SW_4$ once again, where the remaining switches have soft-switching characteristics for both turn-on and turn-off. The switching losses for $SW_1$ and $SW_4$, i.e. $P_{SW_1,ON-3LB}$, $P_{SW_4,ON-3LB}$ and $P_{SW_1,OFF-3LB}$, $P_{SW_4,OFF-3LB}$, are shown in Eqs. (3-11,3-12),

$$P_{SW_1,ON-3LB} = P_{SW_4,ON-3LB} = \frac{1}{2} \cdot \left( \frac{V_{in}}{2} \right) \cdot \left( \frac{l_{load}}{2} - \frac{\Delta i_{L-3LB}}{2} \right) \cdot f_s \cdot t_{on},$$  

$$P_{SW_1,OFF-3LB} = P_{SW_4,OFF-3LB} = \frac{1}{2} \cdot \left( \frac{V_{in}}{2} \right) \cdot \left( \frac{l_{load}}{2} + \frac{\Delta i_{L-3LB}}{2} \right) \cdot f_s \cdot t_{off},$$

where $\Delta i_{L-3LB}$ is the inductor current ripple for the 3-level buck mode.

3.1.3 MOSFET Output Capacitor Losses

The MOSFET output capacitor losses are incurred from the charging and discharging of the output capacitor of the MOSFET, $C_{oss}$, during switching transitions. The output capacitor losses for each mode are derived based on the assumption that the inductor current remains positive over the switching period.

For the interleaved buck mode of operation, all four switches that are operated, i.e. $SW_7$, $SW_3$, $SW_5$, and $SW_6$, experience output capacitor losses, $P_{Coss-IB}$, as shown in Eq. (3-13),
\[ P_{\text{Coss-1B}} = \frac{1}{2} \cdot C_{\text{oss}} \cdot V_{\text{in}}^2 \cdot f_s , \]  

(3-13)

where \( V_{\text{in}} \) is the input voltage and \( f_s \) is the switching frequency.

For the high step-down mode the output capacitor losses are much lower due to the lower blocking voltages of the switches. Since \( SW_3 \) remains on it does not experience these losses. The output capacitance loss in each of the remaining six switches, \( P_{\text{Coss-HSD}} \), is represented by Eq. (3-14),

\[ P_{\text{Coss-HSD}} = \frac{1}{2} \cdot C_{\text{oss}} \cdot \left( \frac{V_{\text{in}}}{2} \right)^2 \cdot f_s . \]  

(3-14)

The output capacitor losses for the 3-level buck mode of operation are expected to be higher than that of the high step-down mode but lower than the interleaved buck mode. Even though \( SW_5 \) and \( SW_7 \) do not experience any losses of this type, the output capacitors of \( SW_3 \) and \( SW_6 \) are charged and discharged to \( V_{\text{in}}/2 \) at twice the frequency of the other switches, thus doubling their respective output capacitor loss. The remaining switches, however, experience loss at the switching frequency according to the high step-down mode equation given in Eq. (3-14). The equation for the output capacitor loss for \( SW_3 \) and \( SW_6 \), \( P_{\text{Coss-3LB}} \), is shown in Eq. (3-15),

\[ P_{\text{Coss-3LB}} = \frac{1}{2} \cdot C_{\text{oss}} \cdot \left( \frac{V_{\text{in}}}{2} \right)^2 \cdot (2 \cdot f_s) . \]  

(3-15)

3.1.4 Gate Drive Losses

The gate drive losses for the switches come from charging and discharging the input capacitance of a switch to turn it on. The gate drive loss of a switch, \( P_{\text{gate}} \), can be calculated utilizing the gate charge, \( Q_g \), gate drive voltage, \( V_{\text{drive}} \), and switching frequency, \( f_s \), as shown in Eq. (3-16),

\[ P_{\text{gate}} = Q_g \cdot V_{\text{drive}} \cdot f_s . \]  

(3-16)

It is assumed that these parameters are consistent for all three modes, so the losses are compared based on the number of switches being operated. It is clear that the interleaved buck mode would have the lowest gate drive losses, since only four switches are operated. The high step-down mode has a higher gate drive loss since there are six operating switches.
The 3-level buck mode can be operated in two ways depending on the efficiency trade-off due to the double switching of $SW_6$. At low currents, where gate drive losses become more dominant, we can choose to gate $SW_6$ either once during the switching cycle or to not gate it at all, to save on gate drive losses. The result would be higher current flowing in $SW_5$ and $SW_7$ but at low currents this effect should not be a large factor. Therefore, if we choose to gate $SW_6$ twice during the switching period then the gate drive losses would be equivalent to that of the high step-down mode, and if we were to not gate $SW_6$ at all the losses would be equivalent to the interleaved buck mode.

3.1.5 Reverse Recovery Losses

Reverse recovery losses are caused during the turn-off switching transition of a conducting body diode when another switch begins conducting the inductor current [8]. These losses come from the removal of charge from the body diode, where the recovered charge is represented by $Q_{rr}$. Reverse recovery loss information is highly influenced by the test conditions and for different conditions this information can vary significantly. Knowing this, we can assume the reverse recovery loss calculation is simply a basic estimation that we can use to compare topologies on a basic level.

The reverse recovery losses in the interleaved buck mode come from the main-switch turn-on, $SW_7$ or $SW_5$, while the body diode of the low-side switch, $SW_3$ or $SW_6$ respectively, is conducting. The resulting reverse recovery loss corresponding to $SW_3$ and $SW_6$, i.e. $P_{rr-IB}$, is shown in Eq. (3-17),

$$P_{rr-IB} = Q_{rr} \cdot V_{in} \cdot f_s,$$  \hspace{1cm} (3-17)

Where $V_{in}$ is the input voltage and $f_s$ is the switching frequency.

The reverse recovery losses for the high step-down mode are higher than the other modes of operation. This is due to the fact that there are more switches whose body diodes conduct in one switching cycle. When the $SW_1$ turn-on transition occurs, both $SW_2$ and $SW_5$ experience reverse recovery losses. Similarly, when $SW_4$ turns on, both $SW_6$ and $SW_7$ experience reverse recovery loss. The equation for reverse recovery loss in the high step-down mode, $P_{rr-HSD}$ is given in Eq. (3-18),
\[ P_{rr-HSD} = Q_{rr} \cdot \left(\frac{V_{in}}{2}\right) \cdot f_s. \]  \hspace{1cm} (3-18)

For the 3-level buck mode of operation we will look at the case where SW\(_6\) is operated twice in one switching cycle. Therefore, for the turn-on transition of SW\(_1\), SW\(_2\) and SW\(_6\) experience reverse recovery losses, and for the turn-on transition of SW\(_4\), SW\(_3\) and SW\(_6\) experience reverse recovery losses. The equation for reverse recovery loss in the 3-level buck mode, \( P_{rr-3LB} \), is the same as the high step-down mode, and shown in Eq. (3-19),

\[ P_{rr-3LB} = Q_{rr} \cdot \left(\frac{V_{in}}{2}\right) \cdot f_s. \]  \hspace{1cm} (3-19)

The specific reverse recovery loss for SW\(_6\) is equal to \( 2 \cdot P_{rr-3LB} \).

3.1.6 Inductor Core Loss

Inductor core losses are based on magnetic losses dependent on the frequency and magnitude of the inductor current ripple. The equation that defines the core loss, \( P_{core} \), in an inductor is shown in Eq. (3-20),

\[ P_{core} = K \cdot (f_{ind})^\alpha \cdot (\Delta i)^\beta, \]  \hspace{1cm} (3-20)

where \( f_{ind} \) is the effective frequency of the current in the inductor, \( \Delta i \) is the current ripple magnitude, and \( K, \alpha, \) and \( \beta \) are inductor design constants specific to each inductor.

For the interleaved buck mode the inductor current frequency is equal to the switching frequency, and the current ripple has a magnitude previously defined in Eq. (3-2). Thus the equation for core loss, \( P_{core-IB} \), becomes that of Eq. (3-21),

\[ P_{core-IB} = K \cdot (f_s)^\alpha \cdot \left(\frac{(V_{in}-V_{out})}{V_{in}}\frac{V_{out}}{V_{in}}T_s\right)^\beta, \]  \hspace{1cm} (3-21)

where \( V_{in} \) is the input voltage, \( V_{out} \) is the output voltage, \( T_s \) is the switching period, \( f_s \) is the switching frequency and \( L \) is the inductance value.
In the high step-down mode the inductor frequency is also equal to the switching frequency, and by substituting the equation for inductor current ripple from Eq. (3-4), the core loss equation, $P_{\text{core-HSD}}$, becomes that of Eq. (3-22),

$$P_{\text{core-HSD}} = K \cdot (f_s)^{\alpha} \left( \frac{\left(\frac{V_{\text{in}}}{2} - V_{\text{out}}\right)}{L} \cdot \left(\frac{2V_{\text{out}}}{V_{\text{in}}}\right) T_s \right)^{\beta}.$$  \hspace{1cm} (3-22)

The core losses for the 3-level buck mode are higher than the other modes due to the higher effective frequency of the current in each inductor. Given the current ripple of Eq. (3-5), the core loss for this mode, $P_{\text{core-3LB}}$, is shown in Eq. (3-23),

$$P_{\text{core,3LB}} = K \cdot (2 \cdot f_s)^{\alpha} \cdot \left( \frac{\left(\frac{V_{\text{in}}}{2} - V_{\text{out}}\right)}{L} \cdot \left(\frac{V_{\text{out}}}{V_{\text{in}}}\right) T_s \right)^{\beta}.$$  \hspace{1cm} (3-23)

3.3 Volume Estimation

The volume estimation for the 7SFC based multi-level buck converter is done by observing the worst case inductor current ripple, the blocking voltages of the switches, and the worst case output capacitor voltage ripple and voltage deviation in response to a transient. Inductor volume is governed by the relation shown in Eq. (3-24),

$$\text{Inductor Volume} \propto L \cdot i_{\text{rated}}^2$$  \hspace{1cm} (3-24)

where $L$ is the inductance value, and $i_{\text{rated}}$ is the inductor rated current. It is clear that the inductor volume is proportional to the inductance value directly and the current rating with a squared relation [15]. Since all of the topologies have the same inductor current ratings we can use the inductance value to compare the volumes.

Similar to the inductor volume equation, the output capacitor volume is governed by the relation of Eq. (3-25),

$$\text{Capacitor Volume} \propto C \cdot v_{\text{rated}}^2$$  \hspace{1cm} (3-25)
where $C$ is the capacitor value, and $v_{\text{rated}}$ is the voltage rating for the capacitor [15]. Here we notice the volume is proportional to the capacitor value directly, and the voltage rating with a squared relation.

The worst case inductor current ripple analysis is done by observing the worst case current ripple for each mode, given the specific operating range of the mode. Depending on the specifications of the power module being designed, the analysis can help determine how the inductor should be sized.

For the interleaved buck converter the inductor current ripple is proportional to the input and output voltages according to Eq. (3-26),

$$IB \text{ current ripple } \propto (V_{in} - V_{out}) \cdot \left(\frac{V_{out}}{V_{in}}\right)$$  \hspace{1cm} (3-26)

where $V_{in}$ is the input voltage and $V_{out}$ is the output voltage. Thus the worst case inductor current ripple for the interleaved buck mode is for the highest input voltage, $V_{in}=V_{in,max}/2$ and for a conversion ratio of $V_{out}/V_{in}=0.5$, where $V_{in,max}$ is the highest input voltage in the operating range.

For the high step-down mode of operation the inductor current ripple depends on the input and output voltages through the equation of Eq. (3-27),

$$HSD \text{ current ripple } \propto \left(\frac{V_{in}}{2} - V_{out}\right) \cdot \left(\frac{2V_{out}}{V_{in}}\right).$$  \hspace{1cm} (3-27)

For this mode the highest current ripple occurs for the highest input voltage, which in this case is $V_{in}=V_{in,max}$, and for a conversion ratio of $V_{out}/V_{in}=0.25$ since this is the conversion ratio limit.

For the 3-level buck mode the inductor ripple is defined by Eq. (3-28),

$$3LB \text{ current ripple } \propto \left(\frac{V_{in}}{2} - V_{out}\right) \cdot \left(\frac{V_{out}}{V_{in}}\right).$$  \hspace{1cm} (3-28)

The worst case current ripple occurs for the highest input voltage, $V_{in}=V_{in,max}$ and conversion ratio $V_{out}/V_{in}=0.5$. 
For the analysis of MOSFET silicon area usage we will simply look at the maximum blocking voltage for each switch and total number of switches. In [23] it is stated that the on-resistance for a MOSFET per unit silicon area, \( R_{on}/(\text{unit silicon area}) \), is defined by Eq. (3-29),

\[
\frac{R_{on}}{\text{unit silicon area}} = \gamma \cdot (V_B)^2,
\]

where \( R_{on} \) is the on-resistance of the MOSFET, \( \gamma \) is a technology dependent factor, and \( V_B \) is the MOSFET breakdown voltage. Using this principle, the MOSFET on-resistance increases with a squared relation to the blocking voltage, for a fixed silicon area specification. From this relation it can be inferred that, by increasing the silicon area, the on-resistance can be normalized, allowing for a silicon area evaluation of multiple converters. For example, by increasing the silicon area in a squared proportion to the blocking voltage, the on-resistance is held constant. To determine the total silicon area used by the MOSFETs in the 7SFC converter we observe the necessary blocking voltages for all of the switches. Since the switches are all rated for \( V_{in,max}/2 \), the total silicon area for the 7SFC can be approximated by Eq. (3-30),

\[
\text{Total Silicon Area (7SFC)} \propto \frac{7}{4} \cdot (V_{in,max})^2.
\]

This is equivalent to the double step-down buck converter and less than the interleaved buck converter and 2-phase 3-level buck converter from Chapter 2.

The output capacitor selection was performed by observing the two specifications below and selecting the larger capacitance value requirement, satisfying both conditions:

1) Maximum output voltage ripple, \( \Delta v_{out} \), as a fraction of the dc output voltage, \( V_{out} \)

2) Maximum output voltage deviation, \( V_{out,dev} \), to a maximum load transient of \( I_{tran,max} \)

This method was proposed in [24] assuming time-optimal control was used to control transients. For the output voltage ripple specification the positive current of the capacitor is integrated to find the added charge, \( \Delta Q_C \), in the output capacitor in one switching cycle, shown in Figure 3-9.
The output capacitor value, $C$, based on this specification, is found using Eq. (3-31),

$$C \geq \frac{\Delta Q_C}{V_{out} \left( \frac{\Delta V_{out}}{V_{out}} \right)}.$$  \hspace{1cm} (3-31)

To find the output capacitor value according to output voltage deviation specification we observe the output voltage deviation in response to step-up and step-down transients. The required output capacitor, $C$, for a step-down transient is found using Eq. (3-32),

$$C \geq \frac{L \left( I_{trans, max} \cdot \left( \frac{\Delta i}{2} \right)^2 \right)}{2V_{out} V_{out, dev}}, \hspace{1cm} (3-32)$$

where $L$ is the inductance value and $\Delta i$ is the inductor current ripple.

For a step-up transient the capacitor value is selected using Eq. (3-33),

$$C \geq \frac{L \left( I_{trans, max} \cdot \left( \frac{\Delta i}{2} \right)^2 \right)}{2V_{out} V_{out, dev}} \cdot \frac{M}{1-M}, \hspace{1cm} (3-33)$$

where $M$ is the conversion ratio.

In Chapter 4 a volume comparison is performed between the interleaved buck converter of Chapter 2 and the 7SFC converter for a real prototype. Here we are able to compare real component values and computationally verify the worst case conditions given a specific converter operating range.

### 3.4 Phase Shedding
Similar to the interleaved buck converter and the 2-phase 3-level buck converter of Chapter 2, the 7SFC converter has the ability to perform phase shedding to further increase efficiency at low currents. This can be done for the interleaved buck mode and the 3-level buck mode of the 7SFC. The switching sequence and corresponding inductor waveforms for the single phase buck mode is provided in Figure 3-10.

Figure 3-10: Switching sequence and inductor waveforms for the single-phase interleaved buck operation of the 7SFC converter

The same for the single-phase 3-level buck mode is provided in Figure 3-11.
The gate driving strategy for the 7SFC based multi-level buck converter follows two schemes that have been previously proposed. The first is the conventional bootstrapping scheme for high-side switches, mainly used for the buck converter [25], and the second is a gate driving scheme proposed for the double step-down buck converter by Nishijima [26]. These two methods are used accordingly to drive the MOSFETs in all of the modes of operation in the 7SFC converter.

The full gate drive setup is as follows. SW2 and SW6 are driven with low-side gate drivers supplied by the gate drive voltage, V_{drive}. SW3 and SW7 utilize the conventional bootstrapping technique from the drain node of SW2 with high-side gate drivers, and SW5 has the same gate driving technique bootstrapped off of the drain node of SW6. Lastly SW4 and SW1 utilize the second gate driving technique where there bootstrap capacitors are charged from the bootstrap capacitor of SW3 when their source nodes are connected. The two gate driving techniques will be described by example by analyzing the high step-down mode of operation of the 7SFC converter.

As described in Section 3.1.2, in State 1 of the high step-down buck mode inductor L1 is charging with \( V_{in} - V_{Cfly} - V_{out} \) and L2 is discharging with \( -V_{out} \). The gate driving analysis for State 1...
is shown in Figure 3-12a). In this state the bootstrap capacitor of \( SW_5, C_{bt5} \), is able to charge since the source node of \( SW_5 \) is grounded by the \( SW_6 \) turn-on. The bootstrap capacitors of \( SW_4 \) and \( SW_1 \) are not charged during this state. The next portion of the gate driving scheme occurs during State 3, shown in Figure 3-12b). In this state when \( SW_5 \) is turned on the source nodes of \( SW_4 \) and \( SW_5 \) are connected. This allows the bootstrap capacitor \( C_{bt4} \) to be charged off of the \( C_{bt5} \) bootstrap capacitor. Then \( SW_4 \) is able to turn-on, thus connecting the source nodes of \( SW_4 \) and \( SW_1 \) allowing the bootstrap capacitor of \( SW_1, C_{bt1} \), to be charged as well. This shows that all of the switches are able to be driven given this gate driving scheme.
Figure 3-12: Gate driving implementation of the 7SFC converter, a) charging of $SW_5$ bootstrap circuit, b) charging of $SW_1$ and $SW_4$ bootstrap circuits
CHAPTER 4:

4. EXPERIMENTAL RESULTS AND COMPARISON

This section of the thesis details the experimental prototype that was built to verify the novel 7SFC based multi-level buck converter as well as compare to conventional and alternative topologies. Using the same prototype, the conventional interleaved buck converter of Chapter 2 was also built to compare results. A wide range of operating conditions was tested to fully characterize the 7SFC converter’s advantages. The prototype was built to operate with input voltages of $3V < V_{in} < 48V$ and output voltages of $1V < V_{out} < 12V$, with only step-down operation. The load current range the prototype was designed for is $I_{load} < 6A$. The prototype was designed and tested for a switching frequency of $f_s = 800kHz$.

Figure 4-1: Image of the top view of the experimental prototype. The top PCB consists of the power stage and the bottom PCB is the control board with sensing, ADCs and DACs.
The components used in the power stage of the 7SFC converter as well as the conventional interleaved buck converter are provided in Table 1. The prototype was built on a 4-layer PCB board and separated into a power stage board (top) and control board (bottom). An image of the prototype is provided in Figure 4-1.

Table 1. Experimental Prototype Components

<table>
<thead>
<tr>
<th>Part</th>
<th>Role</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSD88539 MOSFET</td>
<td>7SFC: $SW_1, SW_4, SW_5, SW_7$</td>
</tr>
<tr>
<td></td>
<td>Interleaved Buck: $SW_1, SW_3$</td>
</tr>
<tr>
<td>AO4264 MOSFET</td>
<td>7SFC: $SW_2, SW_3, SW_6$</td>
</tr>
<tr>
<td></td>
<td>Interleaved Buck: $SW_2, SW_4$</td>
</tr>
<tr>
<td>MCP1407 low-side gate driver</td>
<td>7SFC: $SW_2, SW_6$</td>
</tr>
<tr>
<td></td>
<td>Interleaved Buck: $SW_2, SW_4$</td>
</tr>
<tr>
<td>LTC4440 high-side gate driver</td>
<td>7SFC: $SW_1, SW_3, SW_4, SW_5, SW_7$</td>
</tr>
<tr>
<td></td>
<td>Interleaved Buck: $SW_1, SW_2$</td>
</tr>
<tr>
<td>Wurth 1uH inductor: 744 373 490 10</td>
<td>7SFC inductors</td>
</tr>
<tr>
<td>Wurth 1.5uH inductor: 744 373 490 15</td>
<td>Interleaved buck inductors</td>
</tr>
<tr>
<td>2x10uF ceramic capacitor</td>
<td>$C_fy$ for 7SFC</td>
</tr>
<tr>
<td>2x100uF ceramic capacitor</td>
<td>$C$ for both converters (output capacitor)</td>
</tr>
<tr>
<td>Current sense wire for $L_1$ phase: 15m$\Omega$</td>
<td></td>
</tr>
<tr>
<td>Current sense wire for $L_2$ phase: 14m$\Omega$</td>
<td></td>
</tr>
</tbody>
</table>
The following subsections discuss the experimental verification of the 7SFC based multi-level converter and its comparisons to conventional topologies. The double step-down buck converter is neglected here since it cannot function as a full solution given the operating range. First the inductor and capacitor selection for the 7SFC is performed given the operating conditions. From this we can compare the volume of the 7SFC with the interleaved buck converter and 2-phase 3-level buck converter. Next, a power loss breakdown is shown for the conventional interleaved buck converter and compared to the power loss of the 7SFC converter for several operating points. In the final sections experimental waveforms are shown for the prototype and efficiency results are discussed.

4.1 Reactive Component Selection and Volume Comparison

Based on the operating range of the prototype we are able to choose and compare the inductors and capacitors for the 7SFC based multi-level buck, the conventional 2-phase interleaved buck and the 2-phase 3-level buck topologies. Along with this, the total silicon area of the switches is considered for each topology. Using this information, a total converter volume comparison is made for the three topologies.

4.1.1 Inductor Selection

Since this thesis targets low-volume PoL applications, the 7SFC converter inductors were chosen to have values of 1uH each. This value is chosen because with current inductor technology, inductors in this range start to be considered for integrated applications. Given the 1uH inductor selection we can solve for the worst case current ripple for the 7SFC converter, which is equal for the high step-down mode and the interleaved buck mode. The equation for worst case inductor ripple of the 7SFC is shown in Eq. (4-1),

$$\Delta i_{7\text{SFC},\text{worst}} = \frac{(48V - 12V)(2\cdot12V)}{2\cdot12V} \cdot \frac{1uH\cdot800kHz}{48V} = 7.5A,$$

(4-1)

by substituting the parameters for the worst case, i.e. input voltage of $V_{in}=48V$, output voltage of $V_{out}=12V$ as well as converter parameters, inductance of $L=1uH$ and switching frequency of $f_s=800kHz$, into Eq. (3-4) for the high step-down mode.
Using the 1uH inductance of the 7SFC as a benchmark we can solve for the necessary inductance value for the conventional interleaved buck converter and 2-phase 3-level buck converter to achieve the same worst case inductor current ripple. For the conventional interleaved buck converter we can solve for the inductance value by substituting the benchmark current ripple of 7.5A and switching frequency of $f_s=800kHz$, as well as the worst case current ripple conditions of $V_{in}=48V$ and $V_{out}=12V$ into Eq. (3-2), to get the inductance value $L_{IB}$ of Eq. (4-2):

$$L_{IB} = \frac{(48V-12V)\left(\frac{12V}{48V}\right)}{7.5A\cdot800kHz} = 1.5uH .$$  \hspace{1cm} (4-2)

It is clearly shown that for this operating range the interleaved buck converter requires 1.5 times larger inductors to achieve the same worst case current ripple as the 7SFC converter.

For the 2-phase 3-level buck converter, the chosen inductor is represented by $L_{2Ph-3LB}$ and shown in Eq. (4-3),

$$L_{2Ph-3LB} = \frac{(48V-12V)\left(\frac{12V}{48V}\right)}{7.5A\cdot800kHz} = 0.5uH .$$  \hspace{1cm} (4-3)

where the worst case current ripple is 7.5A, the switching frequency is $f_s=800kHz$, and the worst case operating conditions are $V_{in}=48V$ and $V_{out}=12V$. As expected, the 2-phase 3-level buck converter only requires half of the inductance of the 7SFC converter to achieve the same current ripple specification as the 7SFC converter.

4.1.2 Output Capacitor Selection

The practical output capacitor selection for each converter was found using the two specifications below and selecting the larger capacitance value requirement:

1) Output voltage ripple of 1\% of the output voltage, i.e. $\frac{\Delta V_{out}}{V_{out}} = 0.01$

2) Output voltage deviation of $V_{out,dev}=50mV$ to a maximum load transient of $I_{tran,max}=3A$

To find the worst case conditions for each specification for the three topologies, a MATLAB script was written. In the analyses the inductor values derived in the previous section were utilized for the corresponding topologies.
The output capacitor value, $C$, based on the first specification, is found using Eq. (4-4),

$$C \geq \frac{\Delta Q_C}{V_{out} \cdot 0.01}, \quad (4-4)$$

where the 0.01 factor appears from the 1% output voltage ripple requirement. Table 2 outlines the results for the conventional interleaved buck converter, 2-phase 3-level buck converter and the 7SFC converter based on the output voltage ripple specification. Clearly shown in the results, the 7SFC converter requires a larger output capacitor value by approximately 43% compared to the conventional interleaved buck topology for the worst case conditions. Compared to the 2-phase 3-level buck converter the required output capacitor is twice as large to maintain the same output voltage ripple.

Table 2. Output capacitor selection based on output voltage ripple

<table>
<thead>
<tr>
<th>Topology</th>
<th>Operating Conditions</th>
<th>Capacitor Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional Interleaved Buck Converter</td>
<td>$V_{in} = 48V, V_{out} = 1V$</td>
<td>6.239uF</td>
</tr>
<tr>
<td>2-Phase 3-Level Buck Converter</td>
<td>$V_{in} = 48V, V_{out} = 1V$</td>
<td>4.476uF</td>
</tr>
<tr>
<td>7SFC based Multi-level Buck Converter</td>
<td>High Step-Down Mode</td>
<td>8.952uF</td>
</tr>
</tbody>
</table>

For the output voltage deviation specification, the results are outlined in Table 3, for step-down and step-up transients, utilizing Eq. (4-5) and Eq. (4-6) respectively,

$$C \geq \frac{L \left( \frac{3A+\Delta i}{2} \right)^2}{2V_{out} \cdot 50mV}, \quad (4-5)$$

$$C \geq \frac{L \left( \frac{3A+\Delta i}{2} \right)^2}{2V_{out} \cdot 50mV} \cdot \frac{M}{1-M}, \quad (4-6)$$
where $L$ is the inductance value and $\Delta i$ is the inductor current ripple depending on the converter being analyzed. For the step-up transients, we assume the maximum steady-state conversion ratio is 96% or else the inductor slope would be zero and the transient would not be possible. We can see for the transient specification the requirements for output capacitor value are much larger to achieve a 50mV voltage deviation with a maximum load transient of 3A. Therefore, for a PoL application this specification will be the dominant one. The 7SFC converter is able to achieve a 33% reduction in output capacitance compared to the conventional interleaved buck, further improving on the volume. Compared to the 2-phase 3-level buck, however, the 7SFC converter will require an output capacitor of twice the value, thus having a larger volume.

Table 3. Output capacitor selection based on output voltage deviation

<table>
<thead>
<tr>
<th>Topology</th>
<th>Transient Type</th>
<th>Operating Conditions</th>
<th>Capacitor Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional Interleaved Buck</td>
<td>Step-Down</td>
<td>$V_{in} = 48V, V_{out} = 1V$</td>
<td>71.81uF</td>
</tr>
<tr>
<td>Buck Converter</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Step-Up</td>
<td>$V_{in} = 3V, V_{out} = 2.875V$</td>
<td>544uF</td>
</tr>
<tr>
<td>2-Phase 3-Level Buck Converter</td>
<td>Step-Down</td>
<td>$V_{in} = 48V, V_{out} = 1V$</td>
<td>24.57uF</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Step-Up</td>
<td>$V_{in} = 3V, V_{out} = 2.875V$</td>
<td>182uF</td>
</tr>
<tr>
<td>7SFC based Multi-level Buck</td>
<td>Step-Down</td>
<td>High Step-Down Mode</td>
<td>49.15uF</td>
</tr>
<tr>
<td>Converter</td>
<td></td>
<td>$V_{in} = 48V, V_{out} = 1V$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Step-Up</td>
<td>Interleaved Buck Mode</td>
<td>364uF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{in} = 3V, V_{out} = 2.875V$</td>
<td></td>
</tr>
</tbody>
</table>

4.1.3 Volume Comparison

Using the inductor and capacitor values from the previous section as well as the MOSFET silicon area analyses from Chapter 3, the volume of the various topologies can be compared. Referring back to Eq. (3-24), it is clear the 7SFC converter will have a 33% smaller inductor volume than the interleaved buck converter but at the same time double the inductor volume of
the 2-phase 3-level buck converter. Similar to the inductor volume results, observing Eq. (3-25) shows that the 7SFC converter can have a 33% reduction in output capacitor volume as well compared to the interleaved buck converter but requires twice the volume of output capacitor when compared to the 2-phase 3-level buck converter.

Utilizing the silicon area analysis of Chapter 3 for the 7SFC converter on the interleaved buck converter and the 2-phase 3-level buck converter, the total silicon area for the three topologies can be compared, as shown in Table 4. The results show that the 7SFC converter utilizes less than half of the silicon area of the interleaved buck converter and has a 1/8 reduction of silicon area compared to the 2-phase 3-level buck converter.

Table 4. Total silicon area comparison based on maximum input voltage, $V_{in,max}$

<table>
<thead>
<tr>
<th>Topology</th>
<th>Total Silicon Area Representation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional Interleaved Buck Converter</td>
<td>$\propto 4 \cdot (V_{in,max})^2$</td>
</tr>
<tr>
<td>2-Phase 3-Level Buck Converter</td>
<td>$\propto 2 \cdot (V_{in,max})^2$</td>
</tr>
<tr>
<td>7SFC based Multi-level Buck Converter</td>
<td>$\propto \frac{7}{4} \cdot (V_{in,max})^2$</td>
</tr>
</tbody>
</table>

Thus, in general, the total volume savings of the 7SFC based multi-level converter make it an attractive solution compared to alternative ones as long as the efficiency results agree.

4.2 Power Loss Breakdown

In this section power loss break downs are provided for specific operating points for the interleaved buck converter and the 7SFC converter. The loss breakdown for the 7SFC converter was presented in Chapter 3, and the loss breakdown for the conventional 2-phase interleaved buck converter is provided in Appendix D. By doing this it is easy to observe where the 7SFC converter provides savings in terms of specific loss elements. The operating points that will be
analyzed are a high step-down conversion with input voltage, $V_{in} = 24\text{V}$, and output voltage, $V_{out} = 1\text{V}$, a medium step-down conversion with lower input voltage of $V_{in} = 7\text{V}$ to $V_{out} = 1\text{V}$ and a step-down ratio close to 0.5 of $V_{in} = 12\text{V}$ to $V_{out} = 5\text{V}$. We will not show a comparison of step-down ratios of $M > 0.5$ because the 7SFC converter always operates in the interleaved buck mode in this operating range, thus having similar losses and performance.

4.2.1 High Step-Down Ratio Loss Breakdown

The power loss breakdown for the interleaved buck converter and the 7SFC converter for $V_{in} = 24\text{V}$ and $V_{out} = 1\text{V}$ is provided in Figure 4-2a) and b). A major difference that is clearly noticeable for this operating point is the large difference in switching losses for the two converters. The interleaved buck converter has approximately double the switching losses over the entire load current range due to the switching transitions with the full input voltage, $V_{in}$, which in this case is very high (24V). At this operating point the conduction losses are lower because of the low inductor current ripple. Another difference between the two converters is the slightly larger switch conduction losses for the 7SFC converter. This is due to the increased number of switches, which also explains the increased gate drive losses. The inductor core loss is negligible for both converters.
4.2.2 Medium Step-Down Ratio Loss Breakdown

The power loss breakdown for a medium step-down ratio with $V_{in}=7V$ and $V_{out}=1V$ for the interleaved buck converter and the 7SFC converter is provided in Figure 4-3a) and b). For the interleaved buck converter we can see that even for this operating point the switching losses are dominant, along with the gate drive losses. For the 7SFC converter, however, since the switching losses are basically halved, they are comparable to the conduction losses of the switches and inductors. The gate drive losses for the 7SFC converter remain high at the operating point. Core losses are negligible for both topologies once again. We can once again see the main advantage of introducing the high step-down mode of operation for the 7SFC converter, the large reduction in switching losses and its effectiveness for conversion ratios less than 0.25.
4.2.3 Loss Breakdown for Step Down Ratio Close to 0.5

The loss breakdown for the interleaved buck converter and the 7SFC converter for the operating point of $V_{in}=12\text{V}$ and $V_{out}=5\text{V}$ is shown in Figure 4-4a), b) and c). At this operating point the 7SFC converter can operate in the interleaved buck mode and 3-level buck mode, so loss breakdowns for both modes are shown. At this operating point the interleaved buck converter and the 7SFC converter operating in the 3-level buck mode have different dominant losses altogether. For the interleaved buck converter, it is not surprising to see that the switching loss is the largest component. For the 7SFC converter operating in the 3-level buck mode the switch conduction losses become very substantial at high currents. This is also expected, since certain switches in the 3-level buck mode are exposed to the full load current, and the number of switches has increased. Along with the reduction in switching losses for the 3-level buck mode, inductor conduction losses are significantly reduced compared to the interleaved buck converter due to the decrease in inductor current ripple. For the 7SFC converter operating in the interleaved buck mode we notice most of the losses are very similar to the interleaved buck converter, except for the switch conduction losses. This is again due to the increased number of switches from 4 in the interleaved buck converter to 7 in the 7SFC converter.

Figure 4-3: Power loss breakdown for $V_{in}=7\text{V}$ & $V_{out}=1\text{V}$, a) interleaved buck converter, b) 7SFC converter
4.3 7SFC Steady-State Operation

In this section operating waveforms of the 7SFC converter are provided to demonstrate its functionality for several operating points on the experimental prototype. For each mode, one operating point is selected that the specific mode is designed for. Since the conventional interleaved buck converter was also tested using the same prototype, operating waveforms for this topology are also shown. Waveforms for several other operating points for both the 7SFC converter and the conventional interleaved buck converter are provided in Appendix E.

4.3.1 7SFC: High Step-Down Mode Waveforms
The waveforms shown in Figure 4-5a) and b) are for the switching nodes, $v_{x1}$ and $v_{x2}$, inductor currents, $i_{L1}$ and $i_{L2}$, and the output voltage, $v_{out}$, for the operating point of input voltage, $V_{in}$=12V, output voltage, $V_{out}$=1V and load current, $I_{load}$=1A. Figure 4-5a) shows that the voltage at the switching nodes, $v_{x1}$ and $v_{x2}$, are alternating between 6V and 0V, as expected for the high step-down mode. We also notice that the inductor currents are balanced and since the voltages at the $v_{x1}$ and $v_{x2}$ nodes are close, it means the flying capacitor $C_{fly}$ is approximately equal to $V_{in}/2$. The output voltage shown in Figure 4-5b) confirms that we are operating with a conversion ratio of 12V-to-1V.

![Waveforms](image)

Figure 4-5: Experimental waveforms for the 7SFC converter operating in the high step-down mode with $V_{in}$=12V & $V_{out}$=1V, a) displaying switching nodes $v_{x1}$ and $v_{x2}$, b) displaying switching node $v_{x1}$ and output voltage $v_{out}$

4.3.2 7SFC: Interleaved Buck Mode Waveforms

Waveforms for the interleaved buck mode of the 7SFC converter are shown in Figure 4-6a) and b). for the operating point of input voltage, $V_{in}$=24V, output voltage, $V_{out}$=12V and load current, $I_{load}$=1A. We notice that the switching nodes $v_{x1}$ and $v_{x2}$ switch at 24V, or the full input voltage. We can also expect the proper conversion ratio by observing the duty ratio of approximately 0.5 in Fig. 36.a. Fig. 36.b. confirms the output voltage of $V_{out}$=12V is achieved.
Figure 4-6: Experimental waveforms for the 7SFC converter operating in the interleaved buck mode with $V_{in}=24V$ & $V_{out}=12V$, a) displaying switching nodes $v_{x1}$ and $v_{x2}$; b) displaying switching node $v_{x1}$ and output voltage $v_{out}$.

4.3.3 7SFC: 3-Level Buck Mode Waveforms

Waveforms for the 7SFC converter operating in the 3-level buck mode are shown in Figure 4-7 for input voltage, $V_{in}=36V$, output voltage, $V_{out}=12V$ and load current, $I_{load}=1A$. Since the inductors are connected in parallel only one switching node is displayed, which is referred to as $v_x$ for this mode. The $v_x$ node switches between approximately 18V and 0V which implies the flying capacitor $C_{fly}$ voltage is balanced at $V_{in}/2$. There is a slight current imbalance for the current waveforms, $i_{L1}$ and $i_{L2}$. Unlike the high step-down mode there is no inherent loop maintaining balance between the inductor currents for the 3-level buck mode of the 7SFC converter. The output voltage signal, $v_{out}$, at the top of the Figure confirms that the 7SFC is operating with $V_{out}=12V$. 
Figure 4-7: Experimental waveforms for the 7SFC converter operating in the 3-level buck mode with \( V_{in}=36V \) & \( V_{out}=12V \), displaying switching node \( v_x \) and output voltage \( v_{out} \)

4.3.4 Conventional Interleaved Buck Converter Waveforms

Two operating points are selected to demonstrate the interleaved buck converter operation, 1) input voltage, \( V_{in}=12V \), output voltage, \( V_{out}=1V \) and load current, \( I_{load}=1A \) and 2) \( V_{in}=36V \), \( V_{out}=12V \) and \( I_{load}=1A \). The conventional interleaved buck converter was operated with an increased inductor value of 1.5uH according to the inductor selection of Section 4.1. Figures for the two operating points described are shown in Figure 4-8 and Figure 4-9.

For the 12V-to-1V operating point the required duty ratio for the conventional interleaved buck converter is half of that of the 7SFC high step-down mode. The result is increased voltage spiking. The fact that the switching node is between the full input voltage of 12V and 0V confirms the interleaved buck converter operation. The output voltage in Figure 4-8b) confirms the operating point of \( V_{out}=1V \).

![Figure 4-8: Experimental waveforms for the conventional interleaved buck converter with \( V_{in}=12V \) & \( V_{out}=1V \), a) displaying switching nodes \( v_{x1} \) and \( v_{x2} \), b) displaying switching node \( v_{x1} \) and output voltage \( v_{out} \)](image)

For the second operating point the switching nodes, \( v_{x1} \) and \( v_{x2} \), are switching between approximately 36V and 0V. The currents are slightly imbalanced since there is no inherent current balancing with a voltage mode controller. Comparing the inductor current ripple to the 3-level buck mode of the 7SFC converter of the previous section shows that the inductor current ripple is approximately three times the magnitude, which is a major loss contribution of the
interleaved buck converter at this operating point. Finally, the output voltage can be confirmed in Figure 4-9b) as $V_{\text{out}}=12\text{V}$.

![Waveform Diagram]

Figure 4-9: Experimental waveforms for the conventional interleaved buck converter with $V_{\text{in}}=36\text{V}$ & $V_{\text{out}}=12\text{V}$, a) displaying switching nodes $v_{x1}$ and $v_{x2}$, b) displaying switching node $v_{x1}$ and output voltage $v_{\text{out}}$

4.4 Efficiency Results and Comparison

To verify the expected efficiency improvements of the 7SFC based multi-level converter over the conventional interleaved buck converter, efficiency measurements were taken for both converters at various operating points. In this section, efficiency results for three operating points are presented and compared between the two converters, 1) input voltage, $V_{\text{in}}=12\text{V}$, output voltage, $V_{\text{out}}=1\text{V}$, 2) $V_{\text{in}}=12\text{V}$, $V_{\text{out}}=5\text{V}$ and 3) $V_{\text{in}}=15\text{V}$, $V_{\text{out}}=12\text{V}$. Additional efficiency curves are provided in Appendix F.

In the first operating point the benefit of the high-step down mode of the 7SFC converter, whose purpose is to achieve highest efficiency for high step-down ratios, is demonstrated. Efficiency curves for the conventional interleaved buck converter and the 7SFC converter operating in the high step-down mode are presented in Figure 4-10 for this operating point. At this operating point the 7SFC converter improves on the efficiency of the interleaved buck converter for the entire range of load currents. The previously shown loss breakdown clearly demonstrated that switching losses are the major component that is reduced by moving to the high step-down mode of the 7SFC converter. Thus, for this operating point, the 7SFC converter is a very attractive option.
Figure 4-10: Efficiency curves for $V_{in}=12\,V$ & $V_{out}=1\,V$ for, a) conventional interleaved buck converter, b) 7SFC converter

Efficiency curves for the second operating point are presented in Figure 4-11. For this operating point we can see how the highest efficiency mode of the 7SFC converter depends on load current.

Figure 4-11: Efficiency curves for $V_{in}=12\,V$ & $V_{out}=5\,V$ for, a) interleaved buck converter, b) 7SFC converter

At the low end of currents, up to approximately 3A, the 3-level buck mode has significantly higher efficiency. Even when compared to the conventional interleaved buck converter the
efficiency is much improved. As the load current is increased past 3A the interleaved buck mode becomes the highest efficiency mode. For this segment of the efficiency curve the 7SFC converter achieves almost equivalent efficiency compared to the conventional interleaved buck. The higher conduction losses of the interleaved buck mode of the 7SFC compared to the interleaved buck converter are what cause the efficiency to be slightly reduced.

The third operating point is a direct comparison between the interleaved buck converter and the interleaved buck mode of the 7SFC converter as shown in Figure 4-12. Here, over the full operating range, the interleaved buck converter has slightly higher efficiency, peaking at 97% where the interleaved buck mode of the 7SFC only reaches 96.5% with a higher efficiency drop-off at high currents. However, the benefits gained by introducing the other modes of the converter for other operating points make the tradeoff very worthwhile.

Figure 4-12: Efficiency curves for $V_{in}=15V$ & $V_{out}=12V$ for, a) interleaved buck converter, b) 7SFC converter
CHAPTER 5:

5. CONCLUSIONS AND FUTURE WORK

This thesis presented a novel solution for a wide-range dc-dc converter, the 7-switch flying capacitor (7SFC) based multi-level buck converter, that improves on the conventional solution, the 2-phase interleaved buck converter, in several ways. The merits of the 7SFC converter were evaluated in terms of efficiency, volume, and controller complexity. The major accomplishments of this work and future research are provided in the following sections.

5.1 Major Accomplishments

This work was able to show that the 7SFC based multi-level converter is a suitable alternative to the conventional 2-phase interleaved buck converter in terms of efficiency and volume over the majority of the operating range for a wide-range converter. The increased number of switches in the converter, for the cost of no additional volume, and paired with a digital controller, provides flexibility that is not present in conventional topologies. The following list summarizes the advantages of the 7SFC converter:

- Multi-mode switch operation facilitated by a digital controller
- Operating point based efficiency optimization
- High-step down ratio efficiency significantly improved over the conventional interleaved buck by significantly reducing switching losses
- Reduced volume inductor volume requirement by 33%
- Reduced output capacitor requirement by 33%
- Less than 50% of the silicon area for the MOSFETs compared to the interleaved buck

The modes of operation of the 7SFC converter are categorized into operating range based on Figure 5-1.
5.2 Future Work

The future work for the 7SFC based multi-level buck converter relates mainly with putting all of the control features together. This thesis has shown that the switch configuration can be used to operate in many modes, but selecting modes and changing modes during the converter operation can present a new set of design challenges. For example, in response to a load transient, it becomes complicated to move between the interleaved buck mode and the 3-level buck mode while maintaining balanced inductor currents and not allowing a large output voltage deviation. Specialized control with regards to the flying capacitor should be addressed to make the mode changing possible. In general, load transients should be tested for this converter to confirm the theoretical claims made here with regards to the output capacitor selection.

Furthermore, some control issues pertaining to the specific operating modes haven’t been solved in previous research. For example, for the 3-level buck mode, the capacitor balancing issue remains a challenge for a wide range converter.


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APPENDICES
APPENDIX A:

A. 2-PHASE 3-LEVEL BUCK CONVERTER OPERATION FOR $M > 0.5$

The switching sequence and inductor voltage and current waveforms for the 2-phase 3-level buck converter for conversion ratio, $M > 0.5$, is shown in Figure A-1.
Figure A-1: Switching sequence and inductor waveforms for the 2-phase 3-level buck converter operating in the $M>0.5$ mode

**APPENDIX B:**
B. 7SFC Converter Conduction Losses

This Appendix details the conduction losses for each mode of the 7SFC based multi-level buck converter.

B.1 Interleaved Buck Mode

The inductor and switch currents for the interleaved buck mode for both $D < 0.5$ and $D > 0.5$ are shown in Fig. 22.a. and b. respectively. For the $D < 0.5$ case of Fig. 22.a. the RMS currents for both inductors, $i_{L1,RMS}$ and $i_{L2,RMS}$ as well as all of the switches $i_{SW1,RMS}$, $i_{SW4,RMS}$, $i_{SW2,RMS}$, $i_{SW3,RMS}$, $i_{SW6,RMS}$, $i_{SW5,RMS}$ and $i_{SW7,RMS}$ are shown in Eqs. (B-1 to B-4),

$$i_{L1,RMS} = i_{L2,RMS} = \frac{l_{load}}{2} \cdot \sqrt{1 + \frac{1}{12} \cdot \left(\frac{\Delta i_{L-IB}}{l_{load}}\right)^2},$$

(B-1)

$$i_{SW1,RMS} = i_{SW4,RMS} = \frac{l_{load}}{2} \cdot \sqrt{2} \cdot D \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{\Delta i_{L-IB}}{l_{load}}\right)^2},$$

(B-2)

$$i_{SW2,RMS} = i_{SW3,RMS} = i_{SW6,RMS} = \frac{l_{load}}{2} \cdot \sqrt{(1 - D) \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{\Delta i_{L-IB}}{l_{load}}\right)^2}},$$

(B-3)

$$i_{SW5,RMS} = i_{SW7,RMS} = \frac{l_{load}}{2} \cdot \sqrt{D} \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{\Delta i_{L-IB}}{l_{load}}\right)^2},$$

(B-4)

where $l_{load}$ is the load current, $\Delta i_{L-IB}$ is the inductor current ripple from Eq. (3-2), and $D$ is the duty ratio.

In the $D > 0.5$ case the RMS current value for $SW_1$ is found by looking at two portions of the switching cycle, for State 1 (or State 3) and State 2 (or State 4). For this mode of operation $SW_4$ and $SW_1$ have the same current, so to simplify we will look at the current through $SW_1$. 
Figure B-1: Switching sequence and inductor waveforms for the interleaved buck mode of the 7SFC converter for a) $D<0.5$ and b) $D>0.5$

In State 1 the average current through $SW_1$ is $I_{load}$ and with a current ripple of $\Delta i_{SW1a}$. The value of $\Delta i_{SW1a}$ is shown in Eq. (B-5),

$$\Delta i_{SW1a} = \Delta i_{SW4a} = \frac{2(V_{in} - V_{out})(1 - D)}{L} T_s,$$

(B-5)

In State 2 the average current through $SW_3$ is $I_{load}$ and with a current ripple of $\Delta i_{SW3a}$. The value of $\Delta i_{SW3a}$ is shown in Eq. (B-6),

$$\Delta i_{SW3a} = \Delta i_{SW5a} = \frac{2(V_{in} - V_{out})(1 - D)}{L} T_s,$$

(B-6)
where $V_{in}$ is the input voltage, $V_{out}$ is the output voltage, $T_s$ is the switching period and $L$ is the inductance value.

In State 2 the average current through $SW_1$ and $SW_4$ is $I_{load}/2$ with a current ripple of $\Delta i_{SW1b}$ shown in Eq. (B-6),

$$\Delta i_{SW1b} = \Delta i_{SW4b} = \frac{(V_{in}-V_{out})\cdot(1-D)\cdot T_s}{L}.$$  \hspace{1cm} (B-6)

The total RMS current of $SW_1$ and $SW_4$, i.e. $i_{SW1,RMS}$ and $i_{SW4,RMS}$, is provided in Eq. (B-7),

$$i_{SW1,RMS} = i_{SW4,RMS} = \sqrt{2 \cdot \left[ \left( D - \frac{1}{2} \right)^2 \cdot I_{load}^2 \cdot \left( 1 + \frac{1}{3} \cdot \left( \frac{\Delta i_{SW1a}}{2 \cdot I_{load}} \right)^2 \right) + \cdots \right]} \cdot \sqrt{\left( 1 - D \right)^2 \cdot \left( \frac{I_{load}}{2} \right)^2 \cdot \left( 1 + \frac{1}{3} \cdot \left( \frac{\Delta i_{SW1b}}{I_{load}} \right)^2 \right)}}.$$

For a more detailed explanation of adding RMS values proceed to Appendix C.

The RMS currents for the remaining switches for the interleaved buck mode operating with $D > 0.5$ are the same as for the $D < 0.5$ case and have been provided in Eqs. (B-1, B-3, B-4) previously.

B.2 High Step-Down Mode

The inductor and switch currents for the 7SFC converter operating in the high step-down mode of operation are shown in Fig. 23. The RMS current values for the inductors, i.e. $i_{L1,RMS}$ and $i_{L2,RMS}$, are shown in Eq. (B-8),

$$i_{L1,RMS} = i_{L2,RMS} = \frac{I_{load}}{2} \cdot \sqrt{1 + \frac{1}{12} \cdot \left( \frac{\Delta i_{L-HSD}}{I_{load}} \right)^2},$$

where $I_{load}$ is the load current and $\Delta i_{L-HSD}$ is the inductor current ripple from Eq. (3-4). The RMS currents for $SW_1$ and $SW_4$, i.e. $i_{SW1,RMS}$ and $i_{SW4,RMS}$, where the effect of current division is not a contributing factor, are provided in Eq. (B-9),

$$i_{SW1,RMS} = i_{SW4,RMS} = \frac{I_{load}}{2} \cdot \sqrt{D} \cdot \sqrt{1 + \frac{1}{3} \cdot \left( \frac{\Delta i}{I_{load}} \right)^2},$$

where $\Delta i$ is the current ripple.
where $D$ is the duty ratio. The RMS currents for the rest of the switches are found using the method in Appendix C. The current ripple for the switches where only one phase is in synchronous rectification, i.e. $SW_2$ and $SW_3$ during State 3, and $SW_6$ during State 1, is given in Eq. (B-10) and denoted by $\Delta i_{sr,j}$:

$$\Delta i_{sr,j} = \frac{(V_{out})D \cdot T_s}{L},$$

(B-10)

Where $V_{out}$ is the output voltage, $T_s$ is the switching period and $L$ is the inductance value.
Figure B-2: Switching sequence and inductor waveforms for the high step-down mode of the 7SFC converter
To complete the RMS current calculations the current division during the synchronous rectification states, State 2 and State 4, are analyzed. The simplified current division circuit considering the on-resistances of the switches that are involved is shown in Fig. 24. It should be noted that the averages of the inductor currents \(i_{L1}(t)\) and \(i_{L2}(t)\) during each synchronous rectification state are different.

![Current Division Circuit](image)

Figure B-3: Current division during synchronous rectification for the high step-down mode of the 7SFC converter

The average currents during the first synchronous rectification state, State 2, are denoted with the subscript \(sr\alpha\) and for the second one, State 4, with the subscript \(sr\beta\). These average currents and their respective current ripples over the state are shown in Eqs. (B-11 to B-23):

\[
\begin{align*}
I_{L1,sr\alpha} &= \frac{I_{load}}{2} + \frac{1}{4} \cdot \left(\frac{V_{out} T_s}{L}\right), \\
I_{L2,sr\alpha} &= \frac{I_{load}}{2} - \frac{1}{4} \cdot \left(\frac{V_{out} T_s}{L}\right), \\
I_{SW2,sr\alpha} &= I_{SW3,sr\alpha} = \frac{I_{L1,sr\alpha}(R_{on2}+R_{on5})+I_{load}R_{on6}}{R_{on2}+R_{on3}+R_{on5}+R_{on6}+R_{on7}}, \\
I_{SW5,sr\alpha} &= I_{SW7,sr\alpha} = \frac{I_{load}R_{on6} - I_{L1,sr\alpha}(R_{on2}+R_{on3}+R_{on6})}{R_{on2}+R_{on3}+R_{on5}+R_{on6}+R_{on7}}, \\
I_{SW6,sr\alpha} &= \frac{I_{load}(R_{on2}+R_{on3}+R_{on5}+R_{on7}) - I_{L1,sr\alpha}(R_{on5}+R_{on7})}{R_{on2}+R_{on3}+R_{on5}+R_{on6}+R_{on7}}, \\
I_{L1,sr\beta} &= \frac{I_{load}}{2} - \frac{1}{4} \cdot \left(\frac{V_{out} T_s}{L}\right),
\end{align*}
\]
\[ I_{L2,\text{sr\beta}} = \frac{l_{\text{load}}}{2} + \frac{1}{4} \cdot \left( \frac{V_{\text{out}} \cdot T_s}{L} \right), \quad (B-17) \]

\[ I_{SW2,\text{sr\beta}} = I_{SW3,\text{sr\beta}} = \frac{l_{\text{load}} R_{\text{on}6} - I_{\text{L1, sr\beta}} (R_{\text{on}3} + R_{\text{on}6})}{R_{\text{on}2} + R_{\text{on}3} + R_{\text{on}5} + R_{\text{on}6} + R_{\text{on}7}}, \quad (B-18) \]

\[ I_{SW5,\text{sr\beta}} = I_{SW7,\text{sr\beta}} = \frac{l_{\text{load}} R_{\text{on}6} - I_{\text{L1, sr\beta}} (R_{\text{on}3} + R_{\text{on}6})}{R_{\text{on}2} + R_{\text{on}3} + R_{\text{on}5} + R_{\text{on}6} + R_{\text{on}7}}, \quad (B-19) \]

\[ I_{SW6,\text{sr\beta}} = \frac{l_{\text{load}} (R_{\text{on}2} + R_{\text{on}3} + R_{\text{on}5} + R_{\text{on}7}) - I_{\text{L1, sr\beta}} (R_{\text{on}5} + R_{\text{on}7})}{R_{\text{on}2} + R_{\text{on}3} + R_{\text{on}5} + R_{\text{on}6} + R_{\text{on}7}}, \quad (B-20) \]

\[ \Delta i_{SW2,\text{sr}} = \Delta i_{SW3,\text{sr}} = \frac{(V_{\text{out}}) \left( \frac{1}{2} - D \right) T_s}{L} \cdot \left( \frac{R_{\text{on}5} + 2 \cdot R_{\text{on}6} + R_{\text{on}7}}{R_{\text{on}2} + R_{\text{on}3} + R_{\text{on}5} + R_{\text{on}6} + R_{\text{on}7}} \right), \quad (B-21) \]

\[ \Delta i_{SW5,\text{sr}} = \Delta i_{SW7,\text{sr}} = \frac{(V_{\text{out}}) \left( \frac{1}{2} - D \right) T_s}{L} \cdot \left( \frac{R_{\text{on}2} + R_{\text{on}3} - R_{\text{on}6}}{R_{\text{on}2} + R_{\text{on}3} + R_{\text{on}5} + R_{\text{on}6} + R_{\text{on}7}} \right), \quad (B-22) \]

\[ \Delta i_{SW6,\text{sr}} = \frac{(V_{\text{out}}) \left( \frac{1}{2} - D \right) T_s}{L} \cdot \left( \frac{2 \cdot (R_{\text{on}2} + R_{\text{on}3} + R_{\text{on}5} + R_{\text{on}7})}{R_{\text{on}2} + R_{\text{on}3} + R_{\text{on}5} + R_{\text{on}6} + R_{\text{on}7}} \right), \quad (B-23) \]

with the labelling corresponding to Figure B-3. The current ripples for both synchronous rectification states are equal. The RMS currents for the remaining switches, i.e. \( i_{SW2,\text{RMS}}, i_{SW3,\text{RMS}}, i_{SW5,\text{RMS}}, i_{SW6,\text{RMS}}, i_{SW7,\text{RMS}}, \) are then calculated and given in Eqs. (B-24 to B-28),

\[
i_{SW2,\text{RMS}} = \sqrt{\left( \frac{1}{2} - D \right)^2 \cdot i_{SW2,\text{sr\alpha}}^2 \cdot \left( 1 + \frac{1}{3} \cdot \left( \frac{\Delta i_{SW2,\text{sr}}}{2 \cdot i_{SW2,\text{sr\alpha}}} \right)^2 \right) + \left( \frac{1}{2} - D \right)^2 \cdot i_{SW2,\text{sr\beta}}^2 \cdot ...} 
\]

\[
i_{SW3,\text{RMS}} = \sqrt{\left( \frac{1}{2} - D \right)^2 \cdot i_{SW3,\text{sr\alpha}}^2 \cdot \left( 1 + \frac{1}{3} \cdot \left( \frac{\Delta i_{SW3,\text{sr}}}{2 \cdot i_{SW3,\text{sr\alpha}}} \right)^2 \right) + \left( \frac{1}{2} - D \right)^2 \cdot i_{SW3,\text{sr\beta}}^2 \cdot ...} 
\]
\[
i_{SW5,RMS} = \sqrt{\frac{1}{2} - D} \cdot I_{SW5,SR}^2 \cdot \left(1 + \frac{1}{3} \cdot \frac{\Delta i_{SW5,SR}}{2 \cdot I_{SW5,SR}} \right)^2 + \left(\frac{1}{2} - D\right) \cdot I_{SW5,SR}^2 \cdot \ldots
\]
\[
\ldots \left(1 + \frac{1}{3} \cdot \frac{\Delta i_{SW5,SR}}{2 \cdot I_{SW5,SR}} \right)^2 + D^2 \cdot \left(\frac{I_{load}}{2}\right)^2 \cdot \left(1 + \frac{1}{3} \cdot \frac{\Delta i_{load}}{I_{load}} \right)^2
\], \quad (B-26)

\[
i_{SW6,RMS} = \sqrt{\frac{1}{2} - D} \cdot I_{SW6,SR}^2 \cdot \left(1 + \frac{1}{3} \cdot \frac{\Delta i_{SW6,SR}}{2 \cdot I_{SW6,SR}} \right)^2 + \left(\frac{1}{2} - D\right) \cdot I_{SW6,SR}^2 \cdot \ldots
\]
\[
\ldots \left(1 + \frac{1}{3} \cdot \frac{\Delta i_{SW6,SR}}{2 \cdot I_{SW6,SR}} \right)^2 + D^2 \cdot \left(\frac{I_{load}}{2}\right)^2 \cdot \left(1 + \frac{1}{3} \cdot \frac{\Delta i_{load}}{I_{load}} \right)^2
\], \quad (B-27)

\[
i_{SW7,RMS} = \sqrt{\frac{1}{2} - D} \cdot I_{SW7,SR}^2 \cdot \left(1 + \frac{1}{3} \cdot \frac{\Delta i_{SW7,SR}}{2 \cdot I_{SW7,SR}} \right)^2 + \left(\frac{1}{2} - D\right) \cdot I_{SW7,SR}^2 \cdot \ldots
\]
\[
\ldots \left(1 + \frac{1}{3} \cdot \frac{\Delta i_{SW7,SR}}{2 \cdot I_{SW7,SR}} \right)^2 + D^2 \cdot \left(\frac{I_{load}}{2}\right)^2 \cdot \left(1 + \frac{1}{3} \cdot \frac{\Delta i_{load}}{I_{load}} \right)^2
\]. \quad (B-28)

B.3 3-Level Buck Mode

The 3-level buck mode of operation of the 7SFC converter demonstrates higher conduction losses than the other modes of operation due to the fact that some of the switches experience the full load current over a portion of the switching cycle. The waveforms for the currents of the inductors and switches are shown in Fig. 25. The RMS currents for each inductor, \(i_{L1,RMS}\) and \(i_{L2,RMS}\), as well as \(SW_1\) and \(SW_4\), \(i_{SW1,RMS}\) and \(i_{SW2,RMS}\), are simply calculated in Eq. (B-29) and (B-30),

\[
i_{L1,RMS} = i_{L2,RMS} = \frac{I_{load}}{2} \cdot \sqrt{1 + \frac{1}{12} \cdot \frac{\Delta i_{L3LB}}{I_{load}}}^2
\], \quad (B-29)

\[
i_{SW1,RMS} = i_{SW4,RMS} = \frac{I_{load}}{2} \cdot \sqrt{D} \cdot \sqrt{1 + \frac{1}{3} \cdot \frac{\Delta i_{L3LB}}{I_{load}}}^2
\], \quad (B-30)

where \(I_{load}\) is the load current, \(\Delta i_{L3LB}\) is the inductor current ripple for the 3-level buck mode from Eq. (3-5), and \(D\) is the duty ratio. The RMS current calculations for the other switches are more cumbersome. For these switches the current is divided during the synchronous rectification states, \(State 2\) and \(State 4\). The current division circuit is the same as that of the high step-down case shown previously in Figure B-4, but the inductor currents when entering synchronous
rectification have changed. Assuming the flying capacitor, $C_{fly}$, is balanced at half of the input voltage, we can assume the average currents and current ripple for each individual switch is equal between both synchronous rectification states. These currents are denoted with the subscript $sr\sigma$ and are shown in Eqs. (B-31 to B-37):
Figure B-4: Inductor and switch currents for the 3-level buck mode of the 7SFC converter

\[ I_{L_{1,SR}} = I_{L_{2,SR}} = \frac{I_{\text{load}}}{2}, \]  \hspace{1cm} (B-31)
\[ I_{SW2,sr} = I_{SW3,sr} = I_{load} \cdot \frac{(R_{on3} + R_{on6})_{2}}{R_{on2} + R_{on3} + R_{on5} + R_{on6} + R_{on7}}. \] (B-32)

\[ I_{SW5,sr} = I_{SW7,sr} = I_{load} \cdot \frac{(R_{on2} + R_{on3} - R_{on6})_{2}}{R_{on2} + R_{on3} + R_{on5} + R_{on6} + R_{on7}}, \] (B-33)

\[ I_{SW6,sr} = I_{load} \cdot \frac{R_{on2} + R_{on3} + (R_{on5} + R_{on7})_{2}}{R_{on2} + R_{on3} + R_{on5} + R_{on6} + R_{on7}}, \] (B-34)

\[ \Delta i_{SW2,sr} = \Delta i_{SW3,sr} = \frac{(V_{out})(\frac{1}{2} - D)T_s}{L} \cdot \left( \frac{R_{on5} + 2R_{on6} + R_{on7}}{R_{on2} + R_{on3} + R_{on5} + R_{on6} + R_{on7}} \right), \] (B-35)

\[ \Delta i_{SW5,sr} = \Delta i_{SW7,sr} = \frac{(V_{out})(\frac{1}{2} - D)T_s}{L} \cdot \left( \frac{R_{on2} + R_{on3} - R_{on6}}{R_{on2} + R_{on3} + R_{on5} + R_{on6} + R_{on7}} \right), \] (B-36)

\[ \Delta i_{SW6,sr} = \frac{(V_{out})(\frac{1}{2} - D)T_s}{L} \cdot \left( \frac{2(R_{on2} + R_{on3}) + R_{on5} + R_{on7}}{R_{on2} + R_{on3} + R_{on5} + R_{on6} + R_{on7}} \right), \] (B-37)

where the current and on-resistance labels are present in Fig. X and X, respectively. Using the RMS current adding method of Appendix C, the RMS currents for the remaining switches, \( i_{SW2,RMS}, i_{SW3,RMS}, i_{SW5,RMS}, i_{SW7,RMS}, i_{SW6,RMS} \), are calculated with Eqs. (B-38 to B-40):

\[ i_{SW2,RMS} = i_{SW3,RMS} = \sqrt{D^2 \cdot I_{load}^2 \cdot \left( 1 + \frac{1}{3} \cdot \left( \frac{\Delta i}{I_{load}} \right)^2 \right) + 2 \cdot \left( \frac{1}{2} - D \right)^2 \cdot I_{SW2,sr}^2 \cdot \ldots \cdot \left( 1 + \frac{1}{3} \cdot \left( \frac{\Delta i_{SW2,sr}}{2I_{SW2,sr}} \right)^2 \right)} \] (B-38)

\[ i_{SW5,RMS} = i_{SW7,RMS} = \sqrt{2 \cdot D^2 \cdot \left( \frac{I_{load}}{2} \right)^2 \cdot \left( 1 + \frac{1}{3} \cdot \left( \frac{\Delta i}{I_{load}} \right)^2 \right) + 2 \cdot \left( \frac{1}{2} - D \right)^2 \cdot I_{SW5,sr}^2 \cdot \ldots \cdot \left( 1 + \frac{1}{3} \cdot \left( \frac{\Delta i_{SW5,sr}}{2I_{SW5,sr}} \right)^2 \right)} \] (B-39)

\[ i_{SW6,RMS} = \sqrt{2 \cdot \left( \frac{1}{2} - D \right)^2 \cdot I_{SW6,sr}^2 \cdot \left( 1 + \frac{1}{3} \cdot \left( \frac{\Delta i_{SW6,sr}}{2I_{SW6,sr}} \right)^2 \right)}. \] (B-40)

**APPENDIX C:**
C. ADDING RMS CURRENTS

This Appendix outlines the general technique for adding RMS currents. A typical inductor current waveform is provided in Fig. 45. To find the total RMS current of \( i(t) \) the period is separated into three portions: 1) \( 0 < t < DT_s \), 2) \( DT_s < t < T_s / 2 \), and 3) \( (1/2 + D)T_s < t < T_s \), where \( D \) is the duty ratio, and \( T_s \) is the switching period. The total RMS current can be found by performing a weighted sum of the squared RMS currents of each portion, followed by a square root operation as in Eq. (C-1).

\[
I_{\text{RMS, total}} = \sqrt{D \cdot I_{\text{RMS,1}}^2 + \left(\frac{1}{2} - D\right) \cdot I_{\text{RMS,2}}^2 + \left(\frac{1}{2} + D\right) \cdot I_{\text{RMS,3}}^2} \tag{C-1}
\]

It is simple to find the RMS values of each individual portion, \( I_{\text{RMS,1}} \), \( I_{\text{RMS,2}} \), and \( I_{\text{RMS,3}} \), as shown in Eqs. (C-2 to C-3):

\[
I_{\text{RMS,1}} = I_{\text{ave}} \cdot \sqrt{D} \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{\Delta i}{2 \cdot I_{\text{ave}}}\right)^2} \tag{C-2}
\]

\[
I_{\text{RMS,2}} = I_{\text{RMS,3}} = I_{\text{ave}} \cdot \sqrt{\left(\frac{1}{2} - D\right)} \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{\Delta i}{2 \cdot I_{\text{ave}}}\right)^2} \tag{C-3}
\]

Thus, the total RMS current, \( I_{\text{RMS, total}} \) is calculated with Eq. (C-4),

\[
I_{\text{RMS, total}} = \sqrt{D^2 \cdot I_{\text{ave}}^2 \cdot \left(1 + \frac{1}{3} \cdot \left(\frac{\Delta i}{2 \cdot I_{\text{ave}}}\right)^2\right) + 2 \cdot \left(\frac{1}{2} - D\right)^2 \cdot I_{\text{ave}}^2 \cdot \left(1 + \frac{1}{3} \cdot \left(\frac{\Delta i}{2 \cdot I_{\text{ave}}}\right)^2\right)} \tag{C-4}
\]

APPENDIX D:
D. 2-PHASE INTERLEAVED BUCK CONVERTER LOSS BREAKDOWN

This Appendix presents a breakdown of the major loss contributions for the conventional 2-phase interleaved buck converter.

D.1 Conduction Losses

The inductor current ripple for the interleaved buck, $\Delta i_L$, is shown in Eq. (D-1),

$$
\Delta i_L = \frac{(V_{in} - V_{out}) \cdot D \cdot T_s}{L},
$$

where $V_{in}$ is the input voltage, $V_{out}$ is the output voltage, $D$ is the duty ratio, $T_s$ is the switching period, and $L$ is the inductance value. The RMS current values for each inductor, $i_{L1,RMS}$ and $i_{L2,RMS}$, are found using Eq. (D-2),

$$
i_{L1,RMS} = i_{L2,RMS} = \frac{I_{load}}{2} \cdot \sqrt{1 + \frac{1}{12} \cdot \left( \frac{\Delta i_L}{I_{load}} \right)^2},
$$

where $I_{load}$ is the load current. The RMS current values for the switches, $i_{SW1,RMS}$, $i_{SW3,RMS}$, $i_{SW2,RMS}$, and $i_{SW4,RMS}$, are provided in Eqs. (D-3,D-4),

$$
i_{SW1,RMS} = i_{SW3,RMS} = \frac{I_{load}}{2} \cdot \sqrt{D} \cdot \sqrt{1 + \frac{1}{3} \cdot \left( \frac{\Delta i}{I_{load}} \right)^2},
$$

$$
i_{SW2,RMS} = i_{SW4,RMS} = \frac{I_{load}}{2} \cdot \sqrt{(1 - D)} \cdot \sqrt{1 + \frac{1}{3} \cdot \left( \frac{\Delta i}{I_{load}} \right)^2}.
$$

D.2 Switching Losses
In the interleaved buck topology, only the two high-side switches, i.e. $SW_1$ and $SW_3$, experience hard-switching transitions. The low-side switches, $SW_2$ and $SW_4$, have soft transitions due to the body diode conduction which results in no losses in this category.

Figure D-1: Inductor and switch currents for the interleaved buck converter.
The equations for turn-on and turn-off switching losses for \( SW_1 \) and \( SW_3 \), i.e. \( P_{SW1,ON} \), \( P_{SW3,ON} \), \( P_{SW1,OFF} \) and \( P_{SW3,OFF} \), are shown in Eq. (D-5) and (D-6),

\[
P_{SW1,ON} = P_{SW3,ON} = \frac{1}{2} \cdot V_{in} \cdot \left( \frac{I_{load}}{2} - \frac{\Delta i_L}{2} \right) \cdot f_s \cdot t_{on},
\]

\[
P_{SW1,OFF} = P_{SW3,OFF} = \frac{1}{2} \cdot V_{in} \cdot \left( \frac{I_{load}}{2} + \frac{\Delta i_L}{2} \right) \cdot f_s \cdot t_{off},
\]

where \( V_{in} \) is the input voltage, \( I_{load} \) is the load current, \( \Delta i_L \) is the inductor current ripple for the conventional interleaved buck converter, \( f_s \) is the switching frequency, \( t_{on} \) is the current and voltage overlap during a turn-on transition, and \( t_{off} \) is the overlap during a turn-off transition.

Equations (D-5) and (D-6) show that switching losses present a significant drawback for the interleaved buck converter. This converter has the full input voltage, \( V_{in} \), frequently appearing across the MOSFETs, and at high input voltages, as will be seen in Chapter 4, the majority of the losses of this converter come from switching losses.

D.3 MOSFET Output Capacitor Losses

Assuming a positive inductor current over the full switching period, each of the four switches of the interleaved buck converter will experience output capacitor losses. The equation for output capacitor loss, \( P_{Coss} \), is shown in Eq. (D-7),

\[
P_{Coss} = \frac{1}{2} \cdot C_{oss} \cdot V_{in}^2 \cdot f_s,
\]

where \( C_{oss} \) is the output capacitance, \( V_{in} \) is the input voltage and \( f_s \) is the switching frequency. Once again, for the interleaved buck converter, the output capacitor losses will be very significant at high input voltages due to the \( V_{in}^2 \) factor.

D.4 Gate Drive Losses
The gate drive losses, $P_{\text{gate}}$, are found utilizing the gate charge, $Q_g$, gate drive voltage, $V_{\text{drive}}$, and switching frequency, $f_s$, as shown in Eq. (D-8).

$$P_{\text{gate}} = Q_g \cdot V_{\text{drive}} \cdot f_s$$  \hspace{1cm} (D-8)

With four switches, the gate drive losses are fairly low in the interleaved buck for a two-phase topology.

D.5  Reverse Recovery Losses

The reverse recovery losses in the interleaved buck come from the main-switch turn-on ($SW_1$ or $SW_3$) while the body diode of the low-side switch ($SW_2$ or $SW_4$) is conducting. The reverse recovery losses, $P_{rr}$, are calculated using Eq. (D-9),

$$P_{rr} = Q_{rr} \cdot V_{\text{in}} \cdot f_s,$$ \hspace{1cm} (D-9)

where $Q_{rr}$ is the recovered charge from the low-side diode, $V_{\text{in}}$ is the input voltage, and $f_s$ is the switching frequency.

D.6  Inductor Core Loss

For the interleaved buck converter the inductor current frequency is equal to the switching frequency, and the current ripple has a magnitude previously defined in Eq. (D-1). By substituting the switching frequency, $f_s$, as the inductor frequency, and current ripple, $\Delta i_L$, into Eq. (3-20), the core loss equation becomes Eq. (D-10),

$$P_{\text{core}} = K \cdot (f_s)^\alpha \cdot \left(\frac{(V_{\text{in}}-V_{\text{out}}) \cdot D \cdot T_s}{L}\right)^\beta.$$ \hspace{1cm} (D-10)

**APPENDIX E:**
E. ADDITIONAL EXPERIMENTAL STEADY-STATE WAVEFORMS

This Appendix simply contains additional steady-state operation waveforms for both the 7SFC based multi-level buck converter and the conventional interleaved buck converter.

E.1 7SFC: High Step-Down Mode Waveforms

Figure E-1: Experimental waveforms for the high step-down mode of the 7SFC converter with $V_{in}=48\text{V}$ & $V_{out}=3.3\text{V}$

Figure E-2: Experimental waveforms for the high step-down mode of the 7SFC converter with $V_{in}=48\text{V}$ & $V_{out}=11\text{V}$
E.2 7SFC: Interleaved Buck Mode

Figure E-3: Experimental waveforms for the interleaved buck mode of the 7SFC converter with $V_{in}=15V$ & $V_{out}=12V$

Figure E-4: Experimental waveforms for the interleaved buck mode of the 7SFC converter with $V_{in}=6V$ & $V_{out}=5V$
E.3 7SFC 3-level buck mode

Figure E-5: Experimental waveforms for the 3-level buck mode of the 7SFC converter with $V_{in}=48\text{V}$ & $V_{out}=12\text{V}$

Figure E-6: Experimental waveforms for the 3-level buck mode of the 7SFC converter with $V_{in}=5\text{V}$ & $V_{out}=3.3\text{V}$
E.4 Conventional Interleaved Buck Converter

Figure E-7: Experimental waveforms for the conventional interleaved buck converter with $V_{in}=48\,\text{V} \& V_{out}=3.3\,\text{V}$

Figure E-8: Experimental waveforms for the conventional interleaved buck converter with $V_{in}=48\,\text{V} \& V_{out}=12\,\text{V}$

Figure E-9: Experimental waveforms for the conventional interleaved buck converter with $V_{in}=24\,\text{V} \& V_{out}=12\,\text{V}$
Figure E-10: Experimental waveforms for the conventional interleaved buck converter with $V_{in}=15\,\text{V}$ & $V_{out}=12\,\text{V}$

Figure E-11: Experimental waveforms for the conventional interleaved buck converter with $V_{in}=6\,\text{V}$ & $V_{out}=5\,\text{V}$

Figure E-12: Experimental waveforms for the conventional interleaved buck converter with $V_{in}=15\,\text{V}$ & $V_{out}=3.3\,\text{V}$
APPENDIX F:

F. ADDITIONAL EXPERIMENTAL EFFICIENCY RESULTS

This Appendix simply contains additional efficiency curves for the 7SFC based multi-level buck converter for the remainder of the operating range.

Figure F-1: Efficiency curves for the 7SFC converter with $V_{out}=1V$
Figure F-2: Efficiency curves for the 7SFC converter with $V_{out}=3.3V$
Figure F-3: Efficiency curves for the 7SFC converter with $V_{\text{out}}=5\text{V}$

Figure F-4: Efficiency curves for the 7SFC converter with $V_{\text{out}}=12\text{V}$