ADAPTIVE BLOCKER CANCELLATION FOR WIRELESS RECEIVERS

by

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Abstract

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This thesis targets cancellation of unwanted signals (blockers), one of the most difficult requirements for a wireless receiver. Current state-of-the-art analog filtering ADCs are analyzed and compared in detail. Recognizing that the analog circuitry requires accurate calibration and PVT correction, a digital filtering ADC in the baseband is proposed that has a digitally defined transfer function that is highly reconfigurable and insensitive to PVT variations. A blocker adaptation algorithm is also presented that tracks the blocker in real time and takes approximately 26µs to converge. The proposed architecture is demonstrated in a wireless receiver prototype implemented in 28nm CMOS technology. The measured programmable digital filter provides 34.9dB attenuation of TX leakage and variable attenuation of an additional blocker anywhere in the frequency range 17.5MHz–107.5MHz. The receiver front-end operates at 1.8GHz with a noise figure of 3.9dB, IIP3 of -5dBm, and consumes only 20.4–37.5mW, the lowest among state-of-the-art designs.
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Chapter 1

Introduction

1.1 Motivation

Mobile communication technology is undergoing an explosion. In 2016, 76% of Canadians own a smartphone, up from 55% just two years ago [1]. Thanks to the rapid rise in the adoption of smartphones, the global mobile data traffic grew 63% in 2016, and it has grown 18-fold over the past 5 years. Cisco predicts that the global mobile data traffic will increase almost 7 times between 2016 and 2021 [2]. The increasing demand for faster data connections requires the design of high bandwidth and low power wireless receivers for the mobile device.

One of the most difficult requirements for a wireless receiver is to reject signals in adjacent bands (blockers) whose amplitude is much larger than the inband signal. In addition, the blocker amplitude can change, and move to different frequencies very quickly, especially as mobile devices move around. Traditionally, a wireless receiver is designed for a set of worst case blocker masks, leading to over design and worse power efficiency. Hence, the focus in this work is for adaptive solutions that automatically reconfigures receiver performance as the environment changes.

Moreover, there is a desire to move towards software defined wireless receivers. This is motivated partly by CMOS technology trends, along with the desire to integrate analog / RF front-ends together with DSP and digital processors inside compact and low-cost mobile devices. It also allows for a receiver to potentially accommodate multiple different standards. The challenge here is that the blocker requirements are very different between different standards. This work is trying to solve this problem by moving towards more flexibility in the receiver, while being in scaled CMOS.
1.2 Thesis Organization

This thesis is organized as follows:

Chapter 2. Background Background information on blocker challenges in wireless receivers is presented. Blocker specifications in the LTE standard are reviewed in detail. Different types of baseband designs are analyzed and compared.

Chapter 3. Baseband Digital Filtering ADC The architecture and design challenges for a digital filtering ADC in the receiver baseband is presented.

Chapter 4. Blocker Adaptation Algorithm A blocker adaptation algorithm that tracks the blocker location in real time is proposed allowing the receiver to adapt to changing channel conditions.

Chapter 5. Circuit Implementations Detailed circuit schematic and simulations are presented for important blocks inside the receiver.

Chapter 6. Experimental Results The prototype fabricated in 28nm CMOS is measured and the results are summarized and compared with state-of-the-art designs.

Chapter 7. Conclusion This thesis is summarized and future work is discussed.

1.3 Contributions

This thesis has 3 main contributions. First, a digital filtering ADC architecture is proposed and digital filter design methods are discussed. The architecture uses a high pass filter to improve the dynamic range of the feedback DAC. To the best of the author’s knowledge, this is the first time a high pass filter is used at the output of the feedback DAC for an ADC. Second, a blocker adaptation algorithm that tracks the blocker amplitude and frequency in real time is proposed. This algorithm complements the easily reconfigurable digital filtering ADC to dynamically save power consumption in certain situations. Finally, a wireless receiver with the blocker adaptive digital filtering ADC is implemented and demonstrated. The receiver targets LTE standard, and has minimum analog circuitry and lowest power consumption compared to state-of-the-art designs [3, 4]. The author believes that the adaptive and easily reconfigurable wireless receiver presented in this thesis is a major step toward a software defined radio.
Chapter 2

Background

2.1 Blocker Filtering in Wireless Receivers

Low supply voltages and analog gain in nanoscale CMOS make the design of a wireless receiver (RX) very challenging. One of the most difficult requirements is to reject signals in adjacent bands (blockers) whose amplitude is much larger than the inband signal. Typically, the biggest blocker comes from a local transmitter (TX leakage). For example, in the LTE standard TX leakage can be as high as -30dBm at the receiver front-end assuming a TX-RX isolation of 57dB and TX-antenna insertion loss of 2dB [5].

The block diagram of a typical mobile wireless receiver is shown in Fig. 2.1. A direct-conversion or zero-IF receiver architecture is assumed, as in for example [6]. In the baseband, an analog low pass filter (LPF) is used before the ADC to filter the blockers. A typical received spectrum highlighting the location of key blocker specifications is shown in Fig. 2.2(a). Usually, the desired signal (SIG) is very small. The closest blocker defines the adjacent channel

![Figure 2.1: The front-end block diagram of a typical wireless receiver, with TX and duplexer to illustrate the blocker profile.](image-url)
selectivity (ACS), and is in a neighbouring channel, right beside the signal band edge. In-band blockers (IBB) are other user channels governed by the same standard as the inband SIG while out-of-band blockers (OBB) are not governed by the same standard. The maximum stable amplitude (MSA) can be defined loosely as the maximum input amplitude such that the ADC in-band noise (IBN) rises by 1dB. An example MSA for a second order LPF followed by an ADC is shown in Fig.2.2(b). In order for the wireless receiver to pass the blocker mask, the MSA should be above the maximum blocker power at all possible frequencies.

The ideal MSA should go up at a slope of 40dB/dec for a second order filter, since the small signal attenuation for a second order filter is 40dB/dec. However, nonlinearity, jitter and gain compressions in the signal chain will cause the actual MSA of the receiver to be worse. Typically, the ADC’s DR is defined by ACS blocker because filtering it would require an unrealistically sharp filter. The filter’s corner frequency is placed such that the attenuation at the signal band edge is small. Depending upon the frequency offset and amplitude of other blockers, one may completely dominate the MSA requirement, and thus determine the filter order. Normally, because of the high loss wireless channel, the transmitter output power is very high. Even with a 56dB transmitter to receiver isolation from the duplexer, the TX leakage will likely dominate the filter order as illustrated in the example (Fig.2.2(b)). However depending on the wireless standard, it is also possible for another blocker (IBB for example) to decide the filter order.
The specification of a wireless receiver based on TX leakage and blocker power is shown in Fig. 2.3. The sensitivity test and blocking test are worst case scenarios for a wireless receiver, where the desired signal is very small and the TX leakage and blocker power are high. However, a more common scenario is in the bottom left corner, where the TX leakage and blocker power are moderate. Designing a wireless receiver working in this region is trivial. A typical wireless receiver is designed to work in the worst case scenarios. In this work, we are targeting a highly reconfigurable receiver that works in the worst case scenarios, but can also take advantage of the common scenario to save power.
The detailed LTE blocker specifications [5] are shown in Table 2.1. A Triquint LTEB20 duplexer is assumed; the in-band and out-of-band attenuation is 3dB and 40dB respectively, and the TX-RX isolation is 56dB. The smallest TX leakage frequency offset from the channel of interest is 41MHz in Band 20. The first test is the sensitivity test, where the signal power is at -93dBm at the receiver input, and transmit power is at +23dBm. For the blocking test, the transmitter power is allowed to be 4dB smaller and the signal power is at least 9dB larger. The blockers are defined either as continuous wave (CW) or modulated with 5MHz bandwidth.

Assuming a direct-conversion architecture, the blocker power before duplexer is plotted in Fig. 2.4 and after duplexer in Fig. 2.5. The CW blockers are indicated using black arrows and modulated blockers are represented with grey boxes. After the duplexer, the TX leakage is at -30.5dBm which is much larger than other blockers.

Table 2.1: Detailed LTE blocker specifications, before and after duplexer.

<table>
<thead>
<tr>
<th>Blocker</th>
<th>Power(dBm) before dup</th>
<th>Power(dBm) after dup</th>
<th>BW (MHz)</th>
<th>$F_{offset}(MHz)$</th>
<th>TX Power (dBm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Refsens</td>
<td>-90 (B20)</td>
<td>-93 (B20)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$F_{signal_{max}}$</td>
<td>-25</td>
<td>-28</td>
<td></td>
<td></td>
<td>19</td>
</tr>
<tr>
<td>ACS1</td>
<td>Refsens + 14</td>
<td>-79</td>
<td>-50.5</td>
<td>-53.5</td>
<td>19</td>
</tr>
<tr>
<td>ACS2</td>
<td>-50.5</td>
<td>-53.5</td>
<td>-25</td>
<td>-28</td>
<td>1</td>
</tr>
<tr>
<td>IBB1</td>
<td>Refsens + 9</td>
<td>-84</td>
<td>-56</td>
<td>-59</td>
<td>19</td>
</tr>
<tr>
<td>IBB2</td>
<td>Refsens + 9</td>
<td>-84</td>
<td>-44</td>
<td>-47</td>
<td>19</td>
</tr>
<tr>
<td>OBB1</td>
<td>Refsens + 9</td>
<td>-84</td>
<td>-44</td>
<td>-47</td>
<td>19</td>
</tr>
<tr>
<td>OBB2</td>
<td>Refsens + 9</td>
<td>-84</td>
<td>-30</td>
<td>-70</td>
<td>19</td>
</tr>
<tr>
<td>OBB3</td>
<td>Refsens + 9</td>
<td>-84</td>
<td>-15</td>
<td>-55</td>
<td>19</td>
</tr>
<tr>
<td>NBB</td>
<td>Refsens + 16</td>
<td>-77</td>
<td>-55</td>
<td>-58</td>
<td>19</td>
</tr>
<tr>
<td>IMD</td>
<td>Refsens + 9</td>
<td>-84</td>
<td>-46</td>
<td>-49</td>
<td>19</td>
</tr>
</tbody>
</table>
Figure 2.4: LTE Band 20 blocker powers before the duplexer.

Figure 2.5: LTE Band 20 blocker powers after the duplexer.
The cumulative distribution function of TX leakage power after duplexer in WCDMA standard under different real life scenarios is extracted from [7] and shown in Fig. 2.6. The cumulative distribution function shows the probability that the TX leakage is below a certain power level. For example, outdoor public will have TX leakage after duplexer lower than -80dBm 40% of the time and -70dBm 70% of the time. For all scenarios, the TX leakage after duplexer is below -52dBm (20dB lower than the peak value of -32dBm) in at least 70% of the time. Therefore, designing a reconfigurable receiver that takes advantage of the lower TX leakage will translate to significant power consumption reduction.

![Figure 2.6: The cumulative distribution function of TX leakage after duplexer in WCDMA standard under different scenarios.](image)

**2.2 State-of-the-Art Baseband Architecture**

**2.2.1 Conventional Approach**

Conventionally, the filter and the ADC in the baseband is designed separately. Blockers are first filtered by a passive capacitor at the baseband input, then go through analog low pass filters followed by high resolution ADCs [8–10]. Traditionally, discrete-time delta sigma modulators are used in wireless receivers. Recently, continuous-time delta sigma modulators (CTDSM) have become popular due to higher sampling rate, inherent anti-aliasing, and more power efficient amplifier structure [11]. The most power efficient modulator architectures are the cascade of integrators in feedforward (CIFF) and the cascade of integrators in feedforward-feedback (CIFF-B) [12–15]. The feedforward path allows a larger gain in the first integrator of the modulator, therefore reducing the input referred noise of subsequent stages. This can be best
explained by the example block diagram of a third order CIFF-B modulator shown in Fig 2.7. The modulator consists of 3 parts: the first integrator with transfer function $\omega_{ADC}/s$, subsequent stages with transfer function $L_{ADC}(s)$, and the quantizer. Because of the feedforward path with gain $b_1$, there is no feedback path to the input of the second integrator. As a result, when a very low frequency signal is present at input X, there can not be any signal content at the output of the first integrator $V_1$, otherwise the second integrator will saturate. Therefore, only quantization noise is present at $V_1$ which means the gain of the first integrator $\omega_{ADC}/s$ can be maximized. Even though CIFF and CIFF-B architectures are more power efficient, they exhibit signal transfer function (STF) peaking which is not ideal for wireless receivers. The peaking in the STF will translate to a higher filter order in the preceding LPF because blockers in some frequencies are amplified.

![Block Diagram of Third Order CIFF-B Modulator](image)

Figure 2.7: The block diagram a third order CIFF-B architecture illustrating the output of the first integrator contains only quantization noise.

A vast amount of research has also been devoted to better controlling the STF of feedforward modulators [16–21], and although they may provide some filtering of blockers with large frequency offset from the desired channel, they provide no filtering of adjacent channels. Cascade of integrators in feedback (CIFB) modulators are also used because of their steeper STF rolloff, however they generally require more power consumption than CIFF architectures because their smaller gain in the first integrator would otherwise increase their input referred noise [22, 23].

### 2.2.2 Analog Filtering ADC

To improve power efficiency, the LPF and ADC can be combined within a shared global feedback loop thus creating an analog filtering ADC [24]. There are two approaches to designing an analog filtering ADC. The first embeds the filter inside the feedback loop of the ADC, thus relaxing the filter’s noise and distortion requirements [25–27]. The second approach moves the
Figure 2.8: The block diagrams of (a) the cascade of a filter and ADC, and (b) an ADC with embedded filter. The integrator gains $\omega_{ADC}/s$ in (a) and (b) after dynamic range scaling are not necessarily the same.

ADC inside the feedback loop of the filter, relaxing the ADC thermal and quantization noise requirements [6, 28–32].

**ADC with Embedded Filter**

The conventional baseband implementation shown in Fig. 2.8(a), takes the mixer output $X$, which could be either voltage or current depending on the mixer architecture, goes into a LPF with a transfer function $H_{LPF}(s)$, followed by a continuous-time delta-sigma modulator (CTDSM). The first integrator of the modulator has a gain of $\omega_{ADC}/s$. The subsequent stages are combined inside the block $L_{ADC}(s)$ such that the transfer function from $V_1$ to the quantizer input is $L_{ADC}(s)$. The feedback signal $Y$ is injected into zero, one, or multiple integrators inside the block $L_{ADC}(s)$ depending on the ADC architecture, and its transfer function to the quantizer input is not $L_{ADC}(s)$.

The filter can be moved into the $\Delta\Sigma$ loop of the ADC, after the first integrator. A compensation path is introduced as shown in Fig. 2.8(b) to restore the noise transfer function (NTF) and ensure loop stability [25]. With the assumption that $H_{LPF}(s)$ has a DC gain of unity, the compensation path consists of an integrator with the same gain $\omega_{ADC}/s$ and a highpass filter with transfer function $1-H_{LPF}(s)$. It is easy to see that the transfer function from $X$ to $Y$ as well
as NTF are the same for Fig. 2.8(a) and (b). Specifically, the voltage $V_1$ at the input of $L_{ADC}(s)$ are the same in both cases.

By embedding the filter inside of the ADC, the filter’s input-referred noise is divided by the gain of the first integrator when referred to the input, $X$. To maximize the benefit of this technique, the gain of the first integrator $\omega_{ADC}/s$ should be as high as possible, without saturation at the integrator output. If the modulator uses a feedforward architecture, the DC component at $V_1$ in Fig. 2.8(a) is zero, since it directly connects to subsequent integrators [33]. With the first integrator only processing shaped quantization noise, its gain can be very high after proper dynamic range scaling.

When the filter is embedded into the $\Delta\Sigma$ loop (Fig. 2.8(b)) however, the gain of the first integrator needs to be lower compared to the the cascade of filter and ADC (Fig. 2.8(a)) for two reasons. First, the signal at the output node $Y$ goes through the compensation path and appears at the summing node in front of the node $V_1$. Since $V_1$ contains only quantization noise, the same signal must come from the output of $H_{LPF}(s)$, and thus the output of the first integrator will have a signal component. Second, if a strong out of band blocker appears at the input $X$, almost all the blocker power goes through the first integrator because the feedback $Y$ already has the blocker attenuated by the filter. Therefore the output swing of the first integrator would be dominated either by the signal or out of band blockers, not quantization noise. As a result, even though by embedding the filter inside the $\Delta\Sigma$ loop, the filter noise is reduced, the subsequent integrators in the modulator ($L_{ADC}(s)$) will contribute more noise due to the reduction in the gain of the first integrator.

The first analog filtering ADC with embedded filter is proposed in [25] where a single bit fourth order CTDSM is used in a cascade of integrators with feedforward (CIFF) topology and no feedback path to $L_{ADC}(s)$, as shown in Fig. 2.9(a). The low pass filter $H_{LPF}(s)$ is realized with a first order passive RC filter. Since the DC gain of $H_{LPF}(s)$ is unity, $1-H_{LPF}(s)$ has a zero at DC, which cancels the integrator pole; therefore only one opamp is required in the compensation path. The first order filter combined with a CIFF architecture which has peaking and slow roll-off in the signal transfer function (STF), offers very limited blocker filtering. Also due to the single-bit DAC, the modulator is sensitive to clock jitter and the first integrator needs to consume extra power to achieve the required linearity.
An improved filtering ADC has a second order Butterworth low pass filter embedded into a single bit fourth order CTDSM [27], as shown in Fig. 2.9(b). The filter has a transfer function \(1/[1+(s/\omega_Q)+(s^2/\omega_0^2)]\) and is implemented with two integrators. Similar to [25], the zero in \(1-H_{LPF}(s)\) cancels the integrator pole. As a result, the response of the compensation path and the filter have identical polynomials in the denominator, and can be realized with the same network with appropriate choice of feedback factor \(a_f\). In this design, the gain of the first integrator \(\omega_{ADC}/s\) attenuates the total in-band filter noise power by 8.3dB. To compromise between power efficiency and STF roll-off, the cascade of integrators with feedforward-feedback (CIFF-B) modulator topology is used. The jitter sensitivity and linearity requirements of the first integrator are relaxed by the use of 4 bit FIR feedback DAC.

**Filter with Embedded ADC**

The conventional cascade of filter and ADC is again used as a starting point as shown in Fig. 2.10(a), where the filter is expressed as a feedback loop comprising a first integrator with gain \(\omega_{LPF}/s\) and subsequent stages with transfer function \(L_{LPF}(s)\). The ADC is modeled by
the transfer function $\text{STF}_{\text{ADC}}(s)$. The modulator can be embedded into the filter, as shown in Fig. 2.10(b). The transfer function from X to Y remains the same as the case in Fig. 2.10(a) if $\text{STF}_{\text{ADC}}(s)$ is unity within the frequency range of interest. By embedding the ADC inside the filter, the thermal and quantization noise of the ADC is reduced compared with the cascade of filter and ADC, because the filter open loop gain $\omega_{\text{LPF}}L_{\text{LPF}}(s)/s$ is larger than the closed-loop filter response $H_{\text{LPF}}(s)$ in the signal band.

Figure 2.10: The block diagram of (a) the cascade of filter and ADC, and (b) filter with embedded ADC.

The first filter with embedded ADC is proposed in [28, 29] as shown in Fig. 2.11(a). The design takes a current input, and a second order modulator is embedded in a second order Rauch biquad. The noise advantage compared to a filter-ADC cascade for this work is 7.5dB for the integrated quantization noise and 2dB for the total integrated analog noise. The extra phase shift contributed by the ADC STF and the DAC delay do not alter the filter closed loop transfer function significantly because of the high oversampling ratio and low filter order.
The filter with embedded ADC was further developed in [31] where a second order CTDSM is embedded in a third order Chebyshev filter (Fig. 2.11(b)). A large open loop gain is developed by the three integrators inside the filter, thus attenuating the ADC in-band quantization and thermal noise by 19.8dB compared with the conventional filter-ADC cascade. The extra phase shift contributed by the ADC STF and the DAC delay is compensated by adjusting the filter coefficients $a_1$-$a_3$ with techniques presented in the same work [31]. The same research group published a wireless receiver with a first order modulator embedded in a fourth order Butterworth filter [6]. The ADC quantization noise is improved by 23.6dB compared with the cascade of a filter and ADC.

Comparison of Analog Filtering ADCs

The block diagram of the two types of analog filtering ADCs is shown in Fig. 2.12, with all stages in the filter and the ADC shown. In the presence of large blockers, the gain of the first integrators for the two implementations will have the same maximum gain to prevent saturation at the integrator output. Therefore the second integrator $\omega_{\text{LPF}}/s$ and $L_{\text{LPF}}(s)$ in Fig. 2.12(a) will have similar noise requirements as $L_{\text{LPF}}(s)$ and $\omega_{\text{ADC}}/s$ in Fig. 2.12(b). The main difference between the two approaches is the gain seen by $L_{\text{ADC}}(s)$ and the quantizer. In the case of Fig. 2.12(a), $L_{\text{ADC}}(s)$ and the quantizer are preceded by $H_{\text{LPF}}(s)$ which is unity inside the signal band and the first integrator. In the case of Fig. 2.12(b), $L_{\text{ADC}}(s)$ and the quantizer are preceded...
by $L_{LPF}(s)$ and $\omega_{ADC}/s$ in addition to the first integrator, therefore the design requirements of $L_{ADC}(s)$ and the quantizer will be relaxed by the extra gain compared to Fig. 2.12(a).

Both types of analog filtering ADCs show an improvement compared to the filter and ADC cascade. However the filter transfer function is still determined by the poles of the analog circuitry hence limiting selectivity and requiring accurate calibration and PVT correction. The next section will present a digital filtering ADC which has a digitally defined transfer function that is highly reconfigurable and completely insensitive to PVT variations.

### 2.2.3 Digital Filtering ADCs

The first digital filtering ADC was proposed in [34, 35], which was developed in parallel with work outlined in this thesis [3, 4]. The main objective is to find an easily reconfigurable baseband architecture that scales well in newer CMOS technologies. Therefore the starting point is to have as much digital circuits as possible, as shown in Fig. 2.13(a), where a digital low pass filter is placed after the ADC to attenuate the blockers. However, the ADC needs to have a high dynamic range because it needs to handle the large blocker without saturating. A digital
high pass filter (HPF) in feedback, in combination with a DAC can be used to reconstruct the blocker and cancel it at the summing node in front of the ADC (Fig. 2.13(b)). As a result, the ADC’s dynamic range requirement is reduced. However in this case, at high frequency, the digital filter gain never rolls off, and the phase shift contributed by the ADC and the digital filter becomes significant; hence, the feedback loop becomes unstable. To make the loop stable, high frequency loop gain can be reduced by replacing the digital highpass filter with a digital bandpass filter (Fig. 2.13(c)). Blockers are still canceled within the bandwidth of the digital bandpass filter. In the case where more than one blocker is present, multiple bandpass filters can be placed in parallel (Fig. 2.13(d)), each responsible for one blocker. The proposed digital filtering ADC is easily reconfigurable, and the digital filters can be turned off when there are no blockers to save power.
Figure 2.13: Block diagram of a digital filtering ADC with (a) low pass filter after the ADC, (b) high pass filter in feedback, (c) band pass filter in feedback, and (d) multiple band pass filters in feedback.
Chapter 3

Baseband Digital Filtering ADC

This chapter covers implementation details of designing a digital filtering ADC. A systematic method for designing the digital filter transfer function is introduced. The biggest challenge of the proposed architecture (high DAC dynamic range requirement) will be addressed. And the proposed architecture is compared with previous state-of-the-art filtering ADCs.

3.1 Filter Design

A second order digital bandpass filter is used in the feedback path of the filtering ADC which makes the closed loop response a second order notch filter. The resulting closed-loop magnitude responses for notch filters with different centre frequencies are plotted in Fig. 3.1(a). They all have the same Q factor of 24, and the peak attenuation is adjusted such that the gain at the signal band edge, B, is -1dB. Assuming that there is only one blocker present, and the centre frequency of the notch can be placed exactly at the blocker frequency, the effective attenuation of the 2nd order notch filter is plotted for continuous wave (CW) blockers and modulated blockers in Fig. 3.1(b). The attenuation of the modulated blocker is calculated based on the average attenuation over a bandwidth of B/2. It can be seen that the 2nd order notch filter provides much more attenuation of nearby narrowband CW blockers than a fourth order Butterworth filter, and an attenuation of modulated blockers similar to a third order Butterworth filter.

The simplified block diagram of the digital filtering ADC is shown in Fig 3.2. The objective is to design the digital filter $H_d(z)$ such that the desired closed-loop transfer function $Y/X = H_{CL}(s)$ is obtained. The digital filter $H_d(z)$ can be obtained in three steps:

1. Design the desired closed-loop continuous time transfer function $H_{CL}(s)$.

2. Convert $H_{CL}(s)$ to discrete time equivalent $H_{CL}(z)$.
3. Derive $H_d(z)$ from $H_{CL}(z)$ based on some assumptions.

It is possible to swap the order of step 2 and 3 which designs the digital filter in $s$-domain first then converts it to the $z$-domain. However, due to difficulties in modelling group delays in continuous time, it is much easier to design the digital filter using the three steps outlined above.

First, the desired notch filter transfer function $H_{CL}(s)$ is

$$ H_{CL}(s) = \frac{s^2 + \omega_s s/Q + \omega_0^2}{s^2 + \omega_s s/(Q \cdot \alpha) + \omega_0^2} \quad (3.1) $$
where $\omega_o$ is the notch frequency, $Q$ is the notch Q factor, and $\alpha$ is the gain at $\omega_o$. The discrete time equivalent $H_{CL}(z)$ can be obtained in the form

$$H_{CL}(z) = \frac{b_0 + b_1z^{-1} + b_2z^{-2}}{1 + a_1z^{-1} + a_2z^{-2}}$$ (3.2)

There are different methods of performing continuous time to discrete time conversion, each suitable for different applications [36]. In this work, the filter’s magnitude response is the most important aspect, and the simulated magnitude responses are compared between different conversion methods in Fig 3.3. The system sampling frequency is 720MHz, and the transfer function is designed to cancel the TX leakage at 41MHz. Matched pole zero conversion method relates poles and zeros in the discrete time to continuous time by the transformation $z_i = e^{s_i T}$, where $z_i$ is the ith pole or zero in the discrete time system, $s_i$ is the ith pole or zero in the continuous-time system, and $T$ is the sampling period. Zero order hold method assumes inputs are piecewise constant over the sampling period $T$. Bilinear transformation uses first order approximation and substitutes $s$ in the continuous time transfer function by $\frac{2z-1}{Tz+1}$. Matched pole zero transformation offers the best matching and is thus used in this work to obtain $H_{CL}(z)$. 

Figure 3.2: The simplified block diagram of the digital filtering ADC, illustrating continuous time and discrete time.
Figure 3.3: (a) Simulated magnitude response of 2nd order notch filter with different continuous to discrete time conversion method, and (b) the zoomed-in plot at the notch frequency, and half of the sampling frequency. The simulation is performed in Matlab.

If the ADC and the DAC in Fig 3.2 are assumed to have unity gain and no delay, the digital filter can be related to the closed-loop transfer function by

\[
H_{\text{CL}}(z) = \frac{1}{1 + H_d(z)} \tag{3.3}
\]

and

\[
H_d(z) = \frac{1 - H_{\text{CL}}(z)}{H_{\text{CL}}(z)} \tag{3.4}
\]

substituting \(H_{\text{CL}}(z)\) with equation 3.2,
\[ H_d(z) = \frac{d_0 + d_1 z^{-1} + d_2 z^{-2}}{1 + c_1 z^{-1} + c_2 z^{-2}} = \frac{1 - (b_0 + b_1 z^{-1} + b_2 z^{-2})/(1 + a_1 z^{-1} + a_2 z^{-2})}{(b_0 + b_1 z^{-1} + b_2 z^{-2})/(1 + a_1 z^{-1} + a_2 z^{-2})} = \frac{1 + a_1 z^{-1} + a_2 z^{-2} - (b_0 + b_1 z^{-1} + b_2 z^{-2})}{b_0 + b_1 z^{-1} + b_2 z^{-2}} = \frac{1 - b_0 + (a_1 - b_1) z^{-1} + (a_2 - b_2) z^{-2}}{b_0 + b_1 z^{-1} + b_2 z^{-2}} = \frac{1 - b_0}{b_0} + \frac{a_1 - b_1}{b_0} z^{-1} + \frac{a_2 - b_2}{b_0} z^{-2} \]

\[ (3.5) \]

Matching the coefficients, we have

\[ d_0 = \frac{1 - b_0}{b_0} \]  
\[ d_1 = \frac{a_1 - b_1}{b_0} \]  
\[ d_2 = \frac{a_2 - b_2}{b_0} \]  
\[ c_1 = \frac{b_1}{b_0} \]  
\[ c_2 = \frac{b_2}{b_0} \]  
\[ (3.6) \]
\[ (3.7) \]
\[ (3.8) \]
\[ (3.9) \]
\[ (3.10) \]

The analysis so far assumed zero delay in the ADC, DAC, and the digital filter. If a total delay of one period is present as shown in Fig 3.4, the new closed-loop magnitude response will deviate from the ideal case and exhibit peaking (Fig 3.5).

![Figure 3.4: The simplified block diagram of the digital filtering ADC, with one period delay.](image)

Delay compensation can be performed by designing the new digital filter under the presence of one period delay \( H_{d1}(z) \) by relating it to the old digital filter transfer function \( H_d(z) \) by
\[ H_{d1}(z) \cdot z^{-1} = H_d(z) \]  \hspace{1cm} (3.11)

and,

\[
H_{d1}(z) = H_d(z) \cdot z \\
= \frac{d_0 + d_1 z^{-1} + d_2 z^{-2}}{1 + c_1 z^{-1} + c_2 z^{-2}} \cdot z \\
= \frac{d_0 z + d_1 + d_2 z^{-1}}{1 + c_1 z^{-1} + c_2 z^{-2}} \]  \hspace{1cm} (3.12)

The term \(d_0 z\) translates to a negative delay which is impossible to realize. Luckily, the coefficient \(d_0\) is small and can be omitted without significant impact upon the closed-loop transfer function. Therefore, the delay compensated digital filter is,

\[ H_{d1}(z) \approx \frac{d_1 + d_2 z^{-1}}{1 + c_1 z^{-1} + c_2 z^{-2}} \]  \hspace{1cm} (3.13)

Fig 3.5 shows that with delay compensation, there is minimal peaking compared to the case without delay compensation. The open loop transfer function is shown in Fig 3.6. The phase margin is improved from 60 degrees without delay compensation to 85 degrees with delay compensation. Phase margin might not be the best measure of stability for a bandpass open loop response, however it is difficult to look at other measures of loop stability because the system involves both discrete time and continuous time transfer functions.
Figure 3.6: The Matlab simulated open loop transfer function of the system in Fig 3.4 with or without delay compensation.

### 3.2 DAC Challenges

The DAC in Fig 3.7 needs a much larger full scale than the ADC because it needs to reproduce the blocker. At the same time, any of DAC’s noise and distortion directly appears at the ADC input through the summing node. Therefore, the DAC needs a very high dynamic range in the signal band.

Figure 3.7: Simplified block diagram illustrating the DAC’s noise and distortion effects.

The quantization noise produced from truncating 18 bits at the digital filter output to 5 bits in the DAC can be shaped by a 1st order digital $\Delta\Sigma$ modulator that is delay-less as shown in Fig 3.8. Moreover, recognizing that the DAC is used to replicate blockers and does not have
any signal content in the band of interest, a 1st order passive high pass filter (HPF) is placed at the DAC output to reduce in-band quantization noise, thermal noise, and mismatch distortion from the DAC.

The simulated DAC quantization noise spectrum is plotted in Fig 3.9. The signal bandwidth is 9MHz, with an oversampling ratio (OSR) of 40, which results in a sampling rate of 720MHz. The HPF corner frequency is 20MHz. Without any quantization noise shaping, the in-band noise (IBN) is -29dBFS which is too high. The 1st order digital $ΔΣ$ modulator improves the IBN to -56dBFS, and the 1st order passive HPF further improves the IBN to -66dBFS.
Fig. 3.10 shows the simulated DAC in-band noise and distortion suppression as a function of HPF corner frequency. The corner frequency is presented as a function of the signal bandwidth $B$. The worst case distortion tone attenuation is calculated at the signal band edge where the HPF introduces the least attenuation. The thermal noise, quantization noise and worst case distortion suppression with a corner frequency of $2.2B$ are 12.1dB, 9.7dB, and 7.7dB respectively.

The 1st order passive HPF with transfer function $H_{HPF}(s)$ modifies the open loop gain of the system, and thus introduces 4dB peaking and 4dB less blocker attenuation as shown in Fig. 3.11. A 1st order digital IIR LPF ($H_{LPF}(z)$) with 26dB DC gain and a zero at 20MHz is added to compensate the HPF. It is designed such that the magnitude of $H_{HPF}(s)H_{LPF}(z)$ is approximately unity from 1MHz to 360MHz, where the system sampling frequency is 720MHz.

### 3.3 Detailed Architecture

The detailed baseband architecture is shown in Fig 3.13(a). A first order CTDSM with OSR of 40 is chosen as the ADC topology. More quantization noise shaping is possible by using a higher order modulator, however it also translates to more delays in the ADC’s STF. The simulated baseband closed-loop magnitude responses with a 1st order or a 2nd order modulator are compared in Fig 3.14. The use of the 2nd order modulator increases peaking by 4dB compared with the 1st order modulator. It is possible to reduce peaking by sacrificing blocker attenuation by 3dB. In this work, since majority of the blocker power is absorbed by the digital
Figure 3.11: The simulated closed-loop magnitude response $|D_{OUT}/X|$ with the LPF used to compensate the HPF in Matlab.

Figure 3.12: The block diagram of the LPF introduced to cancel the peaking caused by the HPF.

filter and the DAC, a 1st order modulator provides sufficient dynamic range with the 1st order quantization noise shaping.
Figure 3.13: Detailed system block diagram highlighting (a) ADC topology, 1st order passive LPF, digital filter, and (b) transfer function of each block.
There are two digital band pass filters used. A digital band pass filter extracts the TX leakage at its known frequency offset, while a programmable digital band pass filter can be used to track another blocker. The programmable filter can be set to reject blockers at any frequency offset in the range 17.5MHz–107.5MHz under the control of a blocker adaptation algorithm that will be explained in detail in Chapter 4.

Since the digital filter is in discrete time, the maximum centre frequency of the bandpass filter is limited to 360MHz, half of the sampling frequency. The actual limit in this design is 107.5MHz to ensure a reasonable phase margin and peaking in the closed-loop magnitude response. A 1st order passive LPF is added in front of the summing node to provide attenuation to out of band blockers (larger than 107.5MHz) as well as to reduce the peaking in the closed-loop magnitude response. The LPF does not consume any power, and the corner frequency is 20MHz which is the same as the HPF at the DAC output.

The transfer function for each block is labeled in Fig 3.13(b). The ADC’s STF is modelled as the product of the continuous time loop filter Fs/s and the NTF (1-z\(^{-1}\)). A delay of 0.5 clock period is assumed from the ADC output to the DAC input, and it is modelled in the block z\(^{-0.5}\). A non-return-to-zero (NRZ) DAC is used which has a transfer function \(\frac{1-e^{-st}}{sT}\), where T is the system sampling time. Fig. 3.15(a) shows the simulated transfer function of the implemented digital band pass filters programmed to cancel a blocker at 22.5MHz and the TX leakage at 41MHz. The coefficients for the two digital filters are obtained separately using the methods outlined in Section 3.2. The closed loop transfer function is shown in Fig. 3.15(b).
Figure 3.15: Simulated transfer function in Matlab of (a) the digital bandpass filters for TX leakage and additional blocker, and (b) the closed loop transfer function.

### 3.4 Comparison with other Filtering ADCs

Compared with the analog filtering ADCs reviewed in Section 2.2, the proposed digital filtering ADC has three advantages. First, the proposed architecture has a digitally defined transfer function that is highly configurable and insensitive to PVT variations. The transfer function defined by the digital filters only relies on digital coefficients and clock frequency which are very accurate. Even though an analog 1st order LPF is used in this work, it does not require tuning because most of the filtering is performed by the digital filter. Fig. 3.16 compared the simulated variations in baseband gain for the proposed digital filtering ADC and a 4th order analog Butterworth LPF. If the analog filter corner frequency varies $\pm 40\%$, the gain at signal bandwidth $B$ only changes by 2dB for this work compared with 16dB if a 4th order analog Butterworth LPF is used for blocker rejection (Fig. 3.16(a)). The gain at a blocker...
Figure 3.16: Simulated gain variations in Matlab at (a) the signal bandwidth B, and (b) the blocker frequency 3B.

frequency of 3B changes by 5dB for this work compared with 30dB for the 4th order analog Butterworth LPF (Fig. 3.16(b)). Analog circuit tuning to $\pm 5\%$ might be easy, however there is still large area overhead associated with programmable R and C. The mosfet switches also cause nonlinearity. It is possible to only tune R to have a constant RC, but this might cause noise or stability problems across process variations.

Second, when there are no strong blockers present, the digital band pass filters in this work can be turned off to save power. This is not possible in the case of analog filtering ADCs because the analog filters are in the feed forward path. Moreover, the digital filtering ADC provides much more attenuation to nearby CW blockers than the analog filtering ADCs as shown previously in Fig 3.1. This will lead to an easier ADC design if nearby blockers are limiting the ADC’s dynamic range.

An architecture similar to Fig. 2.13(c) was first proposed in [34, 35], with two differences. First, the digital bandpass filter in [35] was used to assist the STF rolloff of a third order
CTDSM and increased blocker suppression by 6dB. Since the filter transfer function still relies on the poles of the analog path, accurate calibration and PVT correction is needed. In this work, the filter transfer function depends entirely on the digital bandpass filter which is very accurate. Second, without a first order passive HPF at the DAC output, the dynamic range required of the DAC in [35] was very high. In addition to the consequently low thermal noise and distortion requirements on the DAC, in the presence of strong blockers DAC clock jitter in [35] will contribute significant noise in the signal band. Moreover, to mitigate the quantization noise from the DAC, an off-chip reconstruction filter that accurately matches the transfer function of the analog path was needed in [35].

The other filtering ADCs have a low pass transfer function which does not need to be reconfigured for different blocker scenarios. The drawback for this work is that the digital filtering ADC needs to know the location of blockers at all times to be able to cancel them effectively with digital bandpass filters. Therefore, a blocker adaptation algorithm with only limited hardware and power consumption can be used and will be discussed in detail in the next Chapter.
Chapter 4

Blocker Adaptation Algorithm

4.1 Algorithm Overview

In this section, a blocker detection algorithm that tracks the blocker location in real time is proposed allowing the receiver to adapt to changing channel conditions. There are two requirements for the blocker detection algorithm. First, the time required for blocker detection must be much smaller than the rate of change in the channel conditions. Second, the blocker frequency needs to be accurately detected as any uncertainty in the blocker frequency will lower the effective blocker attenuation due to the filter’s high Q factor.

To see how quickly blockers must be tracked, it is useful to consider the mechanisms used to compensate for variations in the channel conditions. For example, the LTE standard provides for an automatic repeat request (ARQ) [37]. In an ARQ scheme, for every block of data 1ms in length, the receiver relies on error detection to detect uncorrectable errors. If uncorrectable errors exist, the receiver can ask for the transmitter to retransmit the same information. The block with errors is preserved and combined with the retransmitted block to increase the effective SNR. Hence in this work, the block length of 1ms is assumed to be the maximum time allowable for the blocker detection algorithm.

Blocker detection can be considered a spectrum sensing problem, where the spectrum at the ADC output needs to be sensed and the frequency of the largest blockers need to be detected. A popular narrowband spectrum sensing algorithm in cognitive radio networks is energy detection [38] as shown in Fig. 4.1(a). A bandpass filter followed by a square and integrate block are used to calculate the total power in the narrowband that is defined by the bandpass filter. It has the advantage of lower implementation and computational complexity compared to other narrowband spectrum sensing techniques [38]. If the centre frequency of the bandpass filter is swept, wideband spectrum sensing is achieved. The block diagram for blocker detection mode is shown in Fig. 4.1(b) where the programmable digital bandpass filter is disconnected from the
Figure 4.1: Block diagram of (a) narrowband spectrum sensing (b) implemented blocker detection with programmable digital filter reused.

main loop and reused for energy detection. Therefore the only extra hardware is the square and integrate block and the finite state machine (FSM) which are implemented off-chip in Matlab for this prototype. If implemented on-chip, this additional digital logic will increase the total digital circuit area by 15%.

The programmable digital bandpass filter is swept over the frequency range from 17.5MHz to 107.5MHz and the simulated magnitude responses are shown in Fig 4.2. The Q factor of the filter is 24. For each frequency setting, the digital filter starts in the reset state, and runs for 400 samples to obtain an accurate power estimate.
The state diagram of the blocker detection algorithm is shown in Fig 4.3. The baseband starts in the initial state, where the bandpass filter responsible for the TX leakage is turned on. Note that for LTE, the TX leakage appears at a known frequency offset, and no blocker detection is needed for the TX leakage. The next state is the power save state, where the programmable filter is turned off and the ADC output is continuously monitored to detect saturation from a new blocker. In the case where the ADC saturates, it means that a blocker is present and the blocker detection algorithm starts. First the baseband fullscale is maximized to bring the ADC out of saturation, with a small noise penalty. The centre frequency of the bandpass filter is swept in 1MHz increments from 17.5MHz to 107.5MHz, taking a total of 36400 samples which takes a total of 50.6\(\mu\)s with an ADC sampling frequency of 720MHz. The algorithm time can be cut in half to 25.6\(\mu\)s by using both the I and Q channel of the baseband, since they see the same channel condition. The frequency setting with the most power is the blocker frequency and the programmable digital filter is programmed to that setting and connected to the main feedback loop to cancel the blocker. The total blocker detection algorithm takes approximately 26\(\mu\)s and it is dominated by the filter frequency sweep time. Note that this time is much less than the transport block size of 1ms in LTE. After the blocker is detected and cancelled, the baseband goes into normal operation, where the ADC output is continuously monitored in case the blocker frequency changes. The blocker power is also monitored at the output of the programmable filter to ensure that the baseband goes into power save mode when the blocker disappears.
4.2 Blocker Detection

The total time used for the blocker detection algorithm should be minimized to reduce the power consumption overhead of the detection circuitry. Each time the centre frequency of the digital filter is incremented, register resets within the filter to erase all memory from the previous frequency setting. Since the digital bandpass filter has a high quality factor, many samples are needed for the filter output to settle when the filter input has large frequency content near the bandpass filter’s centre frequency.

Fig 4.4(a) shows the simulated filter output for filter centre frequency at 32.5MHz. At the filter input, there is a -12dBFS signal at 2MHz, a -5dBFS blocker at 22.5MHz and a -15dBFS TX leakage at 41MHz, all of them are CW signals. The filter goes out of reset at sample 10, and takes around 200 samples to reach steady state. When the filter centre frequency is...
22.5MHz (exactly at where the blocker is), the transient response takes much longer to settle just as expected (Fig 4.4(b)). There is quantization noise at the filter input from the first order delta sigma modulator, however minimum quantization noise appears at the filter output in Fig 4.4(b) because of the filter’s narrowband magnitude response.

The filter output power is obtained for each centre frequency of the digital bandpass filter by calculating the average power of the filter output for a certain number of samples. Fig 4.5(a) shows the simulated result for 4000, 400, and 100 samples per each frequency setting. The filter output power curve when only taking 100 samples is very poor because the transient time at the filter output is much larger than 100 samples. When 4000 samples are used for each frequency point, the filter output power curve accurately detects the location of the blocker at
22.5MHz and TX leakage at 41MHz. When 400 samples are used per frequency point, there is a 4dB error in detecting the blocker power at 22.5MHz. However it still shows clearly the location of the blocker and is a good compromise between number of samples and blocker detection accuracy.

Since the early samples after resetting the filter are far away from the steady state filter output, they can be discarded when calculating the average power of the filter output. Fig 4.5(b) shows the filter output power zoomed in around 22.5MHz when discarding different number of samples. It can be seen that discarding 240 samples and using 160 samples (240+160 samples) is the optimum choice when only 400 samples are used.

![Figure 4.5](image_url)

Figure 4.5: The simulated filter output power versus filter centre frequency in Matlab for (a) different number of samples for each frequency point, and (b) different number of samples discarded for each frequency point.
4.3 ADC Saturation Detection

In the case where a large blocker appears, the ADC will saturate, and the IBN will increase. It is very hardware intensive to directly monitor the IBN because it requires performing a FFT. Here, an alternative method is proposed that looks at the quantizer output histogram.

In this work, the quantizer has 17-levels, and its output code centres around 0 and ranges from -8 to 8. Fig 4.6(a) shows the simulated quantizer output histogram for 32k samples, when a CW blocker at -6dBFS is applied. In this case, the quantizer output is spread out with more content in the centre. When the blocker power is at 0dBFS (Fig 4.6(b)), the ADC saturates and the maximum and minimum codes are now much more likely than before.

![Quantizer Output Histogram](image)

Figure 4.6: The simulated quantizer output histogram in Matlab for 32k samples when the blocker power is at (a) -6dBFS, and (b) 0dBFS.

First, the simulated maximum and minimum code occurrence probability and IBN are plotted versus blocker power at the quantizer output in Fig 4.7. There exists a strong correlation, and both of them increase near the ADC full scale. In this work, when the IBN increases by more than 2dB due to a large blocker, the ADC will be defined as saturated. The corresponding maximum and minimum code probability is 0.2.
When a maximum code occurs, the comparator with the maximum reference voltage will output high. When the minimum code occurs, the comparator with the minimum reference voltage will output low. Therefore, the total number of maximum and minimum code can be easily obtained by counting the number of 1s in the top comparator and the number of 0s in the bottom comparator using a counter. This counter resets every 400 samples, and the ADC saturation will be detected if the counter output exceeds 80.

### 4.4 Power Save Mode Detection

One advantage of the digital filtering ADC is that when the blocker disappears, the baseband can enter into power save mode which turns off the programmable digital filter to save power. The programmable digital filter should only be turned off if the ADC IBN will not be affected. Fig 4.8(a) shows the IBN versus input blocker power with programmable filter on and off. With the programmable filter on, the ADC achieves good IBN up to +12dBFS blocker power, compared with -5dBFS with the programmable filter off. When the blocker power is lower than -10dBFS, the programmable filter does not have an impact on the IBN, and it can be turned off.
Figure 4.8: The simulated (a) IBN versus input blocker power, and (b) filter output power versus input blocker power in Matlab.

It is difficult to know the blocker power at a specific frequency. Here, recognizing that when the programmable digital bandpass filter is on, the filter output power is representative of the blocker power because of filter’s high quality factor, the filter’s output power can be continuously monitored. Fig 4.8(b) shows the output power of the programmable filter as a function of the blocker power. In this work, the programmable filter is turned off when the filter output power is less than 11dB, which corresponds to an input blocker power of -10dBFS.
Chapter 5

Circuit Implementations

In order to demonstrate that the blocker cancellation architecture can provide performance suitable for a real application with a power consumption competitive with state-of-the-art in modern CMOS technologies, a prototype was developed in 28nm CMOS targeting the LTE20 standard. This chapter presents implementation details and important design choices of the prototype, supported by simulation results in adice (an in-house simulator developed by Analog Devices) and spectreRF.

5.1 System Overview

The top level block diagram of the proposed wireless receiver prototype is shown in Fig. 5.1. A RF front-end is designed and included to test the blocker cancellation of the baseband in a realistic scenario.

Figure 5.1: The top level block diagram of the proposed wireless receiver, with TX and duplexer to illustrate the blocker profile.
A detailed block diagram of the proposed wireless receiver is shown in Fig 5.2. Typical amplitude is illustrated assuming a moderate input at 1MHz offset from carrier frequency, and a TX leakage tone at 41MHz offset. Differential voltage and current amplitude are shown after the balun, and the equivalent impedance is also shown differentially. A lossless balun is assumed for convenience; in the measurement section, loss of the real balun will be de-embedded. The LNA has a differential input impedance of 50Ω. The output impedance of the LNA is limited by parasitic capacitance (single-ended capacitance is 140fF). A decoupling capacitor $C_C$ is used to make sure no DC current will go into the mixer. The signal and noise output impedance of the passive current mixer is different [39]. Analyzing the mixers in charge domain, [39] showed that the equivalent signal differential output impedance

$$Z_{EQS} = \frac{1 + j}{2C_{LNA}f_0}$$  \hspace{1cm} (5.1)

and the equivalent noise differential output impedance is

$$Z_{BB} = \frac{1}{C_{LNA}f_0}$$  \hspace{1cm} (5.2)

The transconductance gain of the RF front-end is 11.4mS, and it is calculated as a ratio of the differential input current in the I path $I_{BB}$ and the differential voltage at the LNA input. The first order passive filter created by $R_0$ and $C_0$ attenuates the TX leakage. Since a current passive mixer is used, the resistor $R_0$ contributes minimum noise because ideally, a device in series with a current source does not alter the current passing through it [40]. The ADC quantizer has a range from -170mV to 170mV. According to simulation, a -60dBm signal at the input translate to -10.8dBFS at the ADC output. Note that dBm is a unit of power, and is referenced to 50Ω in RF design. When circuits are not matched to 50Ω (after the LNA), signal amplitude are specified in voltage or current. In the context of ADC, it is convenient to reference the signal amplitude to the ADC fullscale, such that 0dBFS refers to a signal amplitude at the ADC fullscale.

It is possible to put more gain before the filtering ADC to reduce the analog power consumption of the first integrator, the benefit will be minimal however, as the amplifier in the first integrator consumes a small fraction of the total baseband power. Also the linearity requirement of the filtering ADC will be greatly increased as the blockers are amplified as well.

5.2 Baseband Architecture

Fig. 5.3 shows the detailed baseband circuit design. Since the mixer outputs a current mode signal, a first order passive lowpass filter with 20MHz cutoff frequency is realized simply by
Figure 5.2: Detailed block diagram of the proposed wireless receiver. Voltage and current amplitude are shown differentially after the balun.
R₀ and C₀. The passive lowpass filter acts as an anti-aliasing filter and also provides some attenuation of out-of-band blockers. Without the passive filter, the voltage swing at the current mixer output is minimal as it is connected to the virtual ground of the integrator. The inclusion of the passive filter increases the voltage swing at the mixer output, and thus increases distortion from the mixer. A small R₀ (100Ω) is chosen to improve the mixer linearity, however this requires C₀ to be 80pF which occupies a large area. This may be a challenge in adapting this approach to very narrowband applications because for the same R₀ required by mixer linearity, C₀ is inverse proportional to the filter corner frequency. The small series impedance formed by R₀ and C₀ also increases the noise contribution of the first amplifier. The first operational amplifier is the integrator while the second operational amplifier acts as a variable gain amplifier (VGA) and allows for excess loop delay compensation with DAC₂ [41]. A zero is added by introducing C₂ to extend the bandwidth of the VGA. Otherwise, the phase shift of the VGA will cause peaking in the noise transfer function (NTF).

Figure 5.3: Baseband circuit design with first order CTDSM, digital circuit and HPF highlighted.
DAC$_1$ is clocked with the same clock as the quantizer and uses [1, 2] timing. Meaning that the signal sampled at time 0 by the quantizer is fed back by DAC$_1$ between time T and 2T, where T is the clock period. The excess loop delay added by DAC$_1$ is compensated by the direct feedback DAC$_2$ which is not clocked. DAC$_{DIG}$ is clocked by CLK$_{DIG}$, which is delayed from CLK by 0.7 period. This delay is controlled by a programmable delay line to allow sufficient time margin for the quantizer and the digital filter. The baseband has an input bandwidth of 9MHz (LTE20) with a 17-level quantizer clocked at 720MHz yielding an oversampling ratio (OSR) of 40. The output noise and distortion from DAC$_{DIG}$ is shaped furthermore by the 1st order passive highpass filter created by R$_{DAC}$ and C$_{DAC}$. The value of R$_{DAC}$ is chosen to be much larger than R$_0$ to minimize the effects of the HPF on the feedback factor of the first amplifier.

The baseband transfer function is very accurate as it is determined completely by the digital filter coefficients and clock frequency. On the other hand, an analog filter (for example, the 4th order Butterworth filter in [6]) requires accurate tuning of R and C. With process and temperature variations, the metal-oxide-metal (MOM) capacitor value in 28nm CMOS can vary by ± 20%, and poly resistors vary by ± 15%. Even excluding the switches, making R and C tunable presents at least 15-20% area overhead, as well as increasing complexity for calibration. A digital filter is also much easier to port into newer CMOS technologies and will benefit from scaling.
The thermal noise of the entire baseband is simulated and input referred to the antenna. The noise spectral density (NSD) in the signal band is -179.3dBm/Hz, which is 5.5dB lower than the noise in the antenna impedance. The equivalent input-referred thermal noise at the baseband input is -59dBFS. The integrator including $R_0$ dominates the baseband thermal noise, and the increasing noise versus frequency is due to the decreasing impedance in $C_0$.

The low baseband noise is mainly due to the high output impedance of the current mode passive mixer. To better understand the effects of impedance on noise, a single-ended inverting amplifier feedback configuration with a voltage input is shown in Fig 5.5(a). The voltage noise from resistor $R_0$ and amplifier are represented by $V_{NR0}$ and $V_{NA}$ respectively. Assuming the negative feedback provides a virtual ground at the amplifier input terminals, the output voltage can be easily solved by superposition:

$$V_{OUT1} = V_{IN}(-\frac{Z_1}{R_0}) + V_{NR0}(-\frac{Z_1}{R_0}) + V_{NA}(\frac{Z_1 + R_0}{R_0})$$  \hspace{1cm} (5.3)
Fig 5.5(b) changes the voltage input to a current input with an equivalent output impedance of $Z_{EQ}$. The input current is chosen such that the voltage on the left of $R_0$ is $V_{IN}$. The output voltage is

$$V_{OUT2} = V_{IN}(-\frac{Z_1}{R_0}) + V_{NR0}(-\frac{Z_1}{R_0 + Z_{EQ}}) + V_{NA}(-\frac{Z_1 + R_0 + Z_{EQ}}{R_0 + Z_{EQ}})$$ (5.4)

which can be rewritten as

$$V_{OUT2} = V_{IN}(-\frac{Z_1}{R_0}) + V_{NR0}(-\frac{Z_1}{R_0 + Z_{EQ}})(\frac{R_0}{R_0 + Z_{EQ}}) + V_{NA}(-\frac{Z_1 + R_0}{R_0})(1 + \frac{Z_{EQ}}{Z_{1} + R_0})$$ (5.5)

Compare equation 5.5 with equation 5.3, both configurations have the same signal amplitude at the output, however the noise contribution from $V_{NR0}$ in the current input configuration is $R_0/(R_0 + Z_{EQ})$ times that of the voltage input configuration. Similarly, the noise contribution from $V_{NA}$ in the current input configuration is also greatly reduced.

The capacitor from the first order passive filter at the baseband input reduces the effective impedance in parallel with the input current, and results in increased noise versus frequency as was observed in Fig 5.4. A circuit diagram with the capacitor and only noise sources is shown in Fig 5.6. The output noise voltage is

$$V_{OUT3} = V_{NR0d}(-\frac{Z_{ld}}{R_{0d} + 1/sC_{0d} \parallel Z_{EQBB}}) + V_{NAd}(-\frac{Z_{ld} + R_{0d} + 1/sC_{0d} \parallel Z_{EQBB}}{R_{0d} + 1/sC_{0d} \parallel Z_{EQBB}})$$ (5.6)

The baseband noise can be referred back to the antenna simply by calculating the noise current $I_{BB,N}$, and dividing by the RF front-end transconductance. The simplified analysis above provides an intuitive understanding of the baseband circuit noise with a current mode mixer. A more rigorous analysis is provided in [39].

### 5.3 Detailed Circuit Implementations and Simulations

This section covers the circuit implementations of individual blocks in detail. All simulations are performed with RC extracted netlist including coupling capacitance and with a nominal VDD of 0.9V at 55°C and corner TT unless otherwise specified. RF front-end simulations are performed by spectreRF and baseband is simulated with adice, an in-house simulator in Analog Devices specialized in ADC simulations.
5.3.1 RF Front-end

The low input-referred noise of the baseband permits a simplified and low-power low-noise amplifier (LNA) design. A common-gate LNA with a differential input impedance of 50 Ω is used, shown in Fig. 5.7(a). To improve its transconductance, the NMOS input pair is capacitively cross-coupled [42], and the differential input is also fed into the gate of the PMOS input pair. The LNA output impedance is improved with cascode NMOS and PMOS devices. The off-chip balun which provides the single-ended to differential conversion is also used to provide the DC bias current to the LNA input. The output common mode is sensed by two resistors and used to bias the NMOS input differential pair. The LNA consumes a total of 4mA.
Chapter 5. Circuit Implementations

Figure 5.7: RF front-end building blocks (a) LNA schematic with $L = 80\text{nm}$ for all transistors, and (b) 25% duty cycle divider with $L = 30\text{nm}$ for all transistors.

The I and Q current-mode passive mixers schematic is shown in Fig 5.8. All NMOS switches have a size of 6um/30nm. The mixer is driven by a 25% duty cycle divider that consists of two latches [43] (Fig. 5.7(b)). The divider outputs 75% duty cycle clock phases which are converted to 25% duty cycle with an inverter afterward. The latch output regenerates when clock is high, and resets to $V_{\text{DD}}$ when clock is low. A 50% duty cycle clock at twice the LO frequency is provided to the divider from off-chip.
Figure 5.8: Current-mode passive mixer schematic, all NMOS switches have a size of 6um/30nm.

The simulated S11, transconductance gain ($g_m$), and noise figure (NF) of the LNA are shown in Fig 5.9. In the frequency range 800MHz to 2GHz, S11 is smaller than -20dB, $g_m$ is larger than 26mS, and noise figure is better than 3.3dB. The simulated LNA input third-order intercept point (IIP3) at 1.8GHz is -0.1dBm. At 1.8GHz, the entire RF front-end has a NF of 3.6dB, IIP3 of -3.8dBm and a transconductance gain of 11.4mS at 1MHz offset from carrier frequency.

5.3.2 Amplifier Design for the Integrator

A 3rd order feed-forward amplifier is used for the 1st operational amplifier (Fig. 5.10(a)). The 1st stage consumes 53% of the opamp power to reduce the input referred noise, whereas the output stage consumes only 20% of the opamp power since the blocker power is mostly cancelled by the digital path. The 2nd order and 1st order path are formed by injecting the differential input signal to the PMOS transistors in the 2nd and 3rd stage. A compensation capacitance $C_C$ is placed at the output of the 1st stage to reduce the bandwidth of the 3rd order path. Three low speed common mode feedback (CMFB) circuits are used to produce bias voltages $V_{CM1}$, $V_{CM2}$, and $V_{CM3}$ for the 3 stages. To protect the amplifier from high frequency common mode noise, mainly from the supply voltage ripples amplified by the PMOS pseudo differential pair, a high speed CMFB circuit is added for the second stage that has a bandwidth of approximately 360MHz (Fig. 5.10(b)). The differential output of the second stage $V_{O2+}$ and $V_{O2-}$ are averaged using a source follower, and common mode current is injected back into
Figure 5.9: The simulated S11, $g_m$, and NF for the LNA in spectreRF. Everything is RC extracted with coupling capacitance, and the simulation is performed with a VDD of 0.9V at 55°C.

$V_{O2+}$ and $V_{O2-}$ with a differential pair similar to the one used in the 2nd stage. The high speed CMFB circuit slightly reduces the differential gain of the second stage.

The open loop response of the first amplifier is simulated with the feedback network and all the loading as shown in Fig 5.11(a). The unity gain frequency is 560MHz with a phase margin of 56 degrees. The overall open loop gain follows the 3rd order path at low frequency, and 2nd order path near the unity gain frequency. Because of the small feedback factor, the gain of the first order path does not have a big impact on the overall open loop gain. Closed loop transfer function of the integrator with the first amplifier is compared with the ideal integrator response (Fig 5.11(b)). The simulated integrator has a phase of -95 degrees at 360MHz, half of the ADC sampling frequency, which translates to -5 degrees compared to the ideal integrator response.

It is important to evaluate the stability and effectiveness of the CMFB circuit. First, the local CMFB loops are broken one at a time and the open loop transfer function is shown in (Fig 5.12(a)). The phase margins for CMFB1, CMFB2, CMFB2HS and CMFB3 are 61, 100, 64, and 72 degrees respectively. Second, with the local CMFB loops closed, the overall loop is broken at the input of the amplifier, and the common mode open loop response is plotted in (Fig 5.12(b)). The open loop gain is below -18dB for all frequencies, indicating that the local
Figure 5.10: Schematic of (a) the third order feedforward amplifier, and (b) the high speed common mode feedback circuit for the second stage. $L = 200\, \text{nm}$ for all transistors.

CMFB circuit are very effective at suppressing the common mode disturbances, and the loop is stable because the open loop gain is always below 0dB.

### 5.3.3 Amplifier Design for the VGA

A 2nd order feed-forward amplifier is used for the VGA (Fig. 5.13). The second stage of the amplifier consumes 66% of the power because it needs to drive additional capacitance at the quantizer input. The noise of the first stage is not important because of the large gain the preceding integrator. Two low speed CMFB circuits are used to produce bias voltage $V_{CM1}$ and $V_{CM2}$. The PMOS tail current source in the second stage is initially added to lower the common mode gain of the 1st order path, however after extracted RC simulation, it was found that a high speed CMFB circuit similar to Fig. 5.10(b) still needs to be added to the differential output $V_{OUT+}$ and $V_{OUT-}$ ensure good common mode rejection at high frequency.
The open loop response of the amplifier is simulated with the feedback network and all the loading as shown in Fig 5.14(a). The unity gain frequency is 630MHz with a phase margin of 65 degrees. Because of the small feedback factor, the gain of the first order path does not have a big impact on the overall open loop gain. Closed loop transfer function of the vga is compared with the ideal vga response (Fig 5.14(b)). The simulated vga has a phase of +3 degrees at 360MHz.

Figure 5.11: The simulated integrator (a) open loop response, and (b) closed loop response. The simulation is performed in adice with a nominal VDD of 0.9V at 55°C. Everything is RC extracted with coupling capacitance included.
The local CMFB loops are broken one at a time and the open loop transfer function is shown in (Fig 5.15(a)). The phase margins for CMFB1, CMFB2, and CMFB2HS are 70, 48, and 126 degrees respectively. Second, with the local CMFB loops closed, the overall loop is broken at the input of the amplifier, and the common mode open loop response is plotted in (Fig 5.12(b)). The open loop gain is below -20dB for all frequencies, indicating that the local CMFB circuit are very effective at suppressing the common mode disturbances, and the loop is stable because the open loop gain is always below 0dB.
5.3.4 Comparator

The comparator consists of a pre-amplifier and a double-tail latch [44] and is shown in Fig. 5.16. The pre-amplifier draws 140 $\mu$A and it has a DC gain of 6.2 dB and bandwidth of 3.8 GHz. The phase shift is -5.7 degrees at 360MHz, half of the ADC sampling frequency. There are several advantages of using pre-amplification. First, the pre-amplifier reduces the input referred offset and thermal noise of the comparator. Second, it provides some common mode rejection of the input signal. Moreover, kickback noise of the latch is attenuated by the pre-amplifier.

The double-tail latch [44] uses the bottom tail for the input stage and the top tail for regenerative latching. This latch is ideal for low supply voltage because only three transistors are stacked compared to four in the conventional strongarm latch. In the reset phase, CK is low and $\overline{CK}$ is high, therefore output voltage of the bottom tail is pulled high, which resets the latch output $V_{OUT-}$ and $V_{OUT+}$ to ground. In the latch phase, the voltage imbalance between $V_{OUT1-}$ and $V_{OUT1+}$ will tilt the cross-coupled inverters in the top tail, and positive regeneration begins. A SR latch is used at the output of the double-tail latch (not shown in Fig. 5.16) that consists of a pair of cross-coupled NOR gates.

The input referred thermal noise of the comparator is 3.2mV$_{\text{rms}}$. The comparator offset has a mean of 1.3mV and standard deviation of 20.6mV. Comparator offset compensation is performed by two 5-bit current DACs with programmable current $I_{\text{CAL,P}}$ and $I_{\text{CAL,N}}$ from VDD to the pre-amplifier differential output $V_{OUT1-}$ and $V_{OUT1+}$. The two most significant bits (MSB) are thermometer coded to reduce DNL and the three LSBs are binary coded to reduce DAC complexity. The unit current $I_U$ is 1uA and the input code to $I_{\text{CAL,N}}$ is inverted from $I_{\text{CAL,P}}$ such that the sum of the two current DACs is always equal to 31$I_U$. The programmable input referred offset versus digital code is shown in Fig 5.17. 0mV offset occurs at digital code
Figure 5.14: The simulated VGA (a) open loop response, and (b) closed loop response. The simulation is performed in adice with a nominal VDD of 0.9V at 55°C. Everything is RC extracted with coupling capacitance included.

18 probably because of an imbalance in the layout. Since the current $2I_U$, $4I_U$ and $8I_U$ are not created from exact replica of unit $I_U$, there is noticeable nonlinearity from bit 7-8, 15-16, and 23-24.

The comparator delay including the SR latch and buffers after the double-tail latch is plotted versus input voltage in Fig 5.18. The delay is measured as the time difference between the clock crosses 50% of the supply voltage and the differential output crosses 50%. The comparator
Figure 5.15: The simulated VGA common mode open loop response of (a) the local CMFB loops, and (b) the overall loop. The simulation is performed in adice with a nominal VDD of 0.9V at 55°C. Everything is RC extracted with coupling capacitance included.

time constant is 2.7ps with a fixed delay of 42.8ps. This fixed delay mainly comes from the SR latch and buffers.

5.3.5 DAC

DAC₁, DAC₂, and DACDIG are designed using a high-speed current-steering architecture [45] and an unit current DAC is shown in Fig 5.19. The unit current for DAC₁, DAC₂ and DACDIG
are 1.6\(\mu\)A, 1.4\(\mu\)A, and 7\(\mu\)A respectively. The top and bottom current sources are implemented using cascode devices to improve the output impedance. The static accuracy and noise of the cascode current source are dominated by M1 and M8. Therefore the transistor length is chosen to have the standard deviation of static mismatch error to be 1\% of \(I_{\text{LSB}}\), and current noise is minimized by choosing the transistor width to have \(V_{\text{eff}} = 300\text{mV}\). The length of cascode devices M2 and M7 are small to minimize the parasitic capacitances on the source node of the switching differential pairs \(V_{\text{SP}}\) and \(V_{\text{SN}}\).
Figure 5.18: Simulated comparator delay versus input voltage in adice, with a nominal VDD of 0.9V at 55°C, with RC extracted netlist with coupling capacitance included.

\[ \text{Delay} = -2.7 \text{ps} \times \ln(V_{\text{in}}) + 42.8 \text{ps} \]

Figure 5.19: Schematic of DAC core.

Voltage supplies +1.8V and -1.0V are used to provide sufficient voltage headroom for the six stacked transistors. Since the DAC output \( I_{\text{OUT-}} \) and \( I_{\text{OUT+}} \) connect directly to the virtual ground of the amplifiers, and Fig 5.4 shows that the thermal noise contribution from the DACs are minimal compared to other components, \( V_{\text{eff}} \) of M1 and M8 can be decreased to accommodate a nominal supply voltage of 0.9V and ground in future designs.

In addition to the static current mismatch error, there are two dynamic errors; specifically switching error and timing error [46]. Fig 5.20 shows the ideal current waveform \( I_{\text{IDEAL}} \) and the
actual current waveform due to dynamic mismatch errors \( I_{\text{ACTUAL}} \). The error charges \( Q_1 \) and \( Q_2 \) can be separated into switching error \( Q_{\text{SW}} \) where the same error appears at each transition, and timing error \( Q_{\text{TIMING}} \) where the error has the same magnitude but different sign in rising and falling edges. The timing error is mainly caused by the threshold mismatch of the switching differential pair \( M3 \) and \( M4 \), and \( M5 \) and \( M6 \) [46]. The voltages at node \( V_{SP} \) and \( V_{SN} \) will be different for 1 and 0, and the voltage difference in combination with the parasitic capacitance will translate to a charge error \( Q_{\text{SW}} \). The timing error comes from delay mismatch in the DAC latch, and it affects both the rising edge and falling edge equally.

A hundred monte carlo simulations are performed on a RC extracted unit DAC element, and the error standard deviations as a percentage of \( I_{\text{LSB}} \) are documented in Table 5.1. To understand the impact of these errors on the overall performance, system simulation in simulink is performed. For each DAC unit element in DAC_1, DAC_2 and DAC_DIG, a random error is assigned based on the extracted standard deviation and the system error in terms of IBN is recorded. For example, when evaluating the effects of static errors from DAC_1, each of the 16 unit DAC elements in DAC_1 is assigned a random static error based on a standard deviation of 0.9% \( I_{\text{LSB}} \), and the system error in IBN is recorded. For each type of error in a DAC, 100 system simulations in simulink are performed, and the mean and standard deviation of system errors are shown in Table 5.1. The IBN from the DAC errors are much lower than the thermal noise of the baseband (-59dBFS) which means they do not limit the baseband performance.

5.3.6 Digital

The detailed digital feedback filter implementation running at 720MHz is shown in Fig. 5.21. The filter is designed in verilog and mixed signal simulations were performed to verify functionality. The 16 bit thermometer coded quantizer output is first converted to 5 bit binary code.
Table 5.1: Summary of simulated DAC unit element errors and their effects on system performance. Unit element errors are simulated in adice with monte carlo enabled. The unit DAC cell is RC extracted with a nominal VDD of 1.8V and 55°C. The system errors are simulated in Simulink using the unit element errors obtained in adice.

<table>
<thead>
<tr>
<th></th>
<th>Unit Element Error (% of I&lt;sub&gt;LSB&lt;/sub&gt;)</th>
<th>System Errors (IBN(dBFS))</th>
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<tr>
<td></td>
<td>Static</td>
<td>Switching</td>
</tr>
<tr>
<td>DAC&lt;sub&gt;1&lt;/sub&gt;</td>
<td>0.9</td>
<td>0.8</td>
</tr>
<tr>
<td>DAC&lt;sub&gt;2&lt;/sub&gt;</td>
<td>0.6</td>
<td>-</td>
</tr>
<tr>
<td>DAC&lt;sub&gt;DIG&lt;/sub&gt;</td>
<td>1.1</td>
<td>0.3</td>
</tr>
</tbody>
</table>

with a thermometer to binary decoder (T2B) which is implemented using Wallace tree adders. Two digital 2nd order infinite impulse response (IIR) filters with 9-bit coefficient resolution detect and cancel TX leakage and one additional blocker. Note that in an intermodulation test, where TX leakage plus two additional blockers are present, cancelling the TX leakage and the blocker at lower offset frequency is sufficient to reduce the intermodulation product significantly. The fully programmable coefficients allow accurate adjustment of the filter centre frequency, gain, and Q factor to effectively cancel blockers with different frequency, power level, and modulated bandwidth. The output of both IIR filters are truncated to 18 bits to achieve a balance between hardware complexity and rounding error. The multipliers and adders in the IIR filters use two’s complement representation where the MSB denotes the sign. The outputs of all multipliers and adders are truncated to 18 bits. A 1st order lowpass IIR filter is added to cancel the effect of the passive highpass filter at the output of DAC<sub>DIG</sub>. The quantization noise produced from truncation at the input of the binary to thermometer encoder (B2T) is shaped by a 1st order delay-less digital ΔΣ modulator.
Figure 5.21: Detailed digital circuit implementation.
Chapter 6

Experimental Results

The proposed RF receiver front-end with digital filtering ADC was implemented in TSMC 28nm CMOS technology. This chapter covers the test setup and measurement results of the prototype.

6.1 Test Setup

This section presents the detailed test setup of the prototype. The test setup consists of the prototype, the printed circuit board (PCB), external equipment used to supply input and clock signals, and a computer that retrieves the ADC digital output through serial interfaces and performs the fast Fourier transform (FFT).

The proposed RF receiver front-end occupies $1.07 \times 1.38 \text{ mm}^2$ with an active area of $0.64 \text{ mm}^2$ (Fig. 6.1). A 6 layer flip chip ball grid array is used for die packaging. An 8 layer PCB was designed and fabricated to test the prototype as shown in Fig 6.2.

The block diagram of the entire test setup is shown in Fig 6.3. The RF clock, RF input, and the baseband clock are provided by three signal generators. For testing with modulated RF inputs, an advanced vector signal generator (SMW200A) is used instead. One external balun and two on-board baluns are used to perform single-ended to differential conversion of the input and two clocks.

There is an on-chip first in, first out (FIFO) memory that captures 32k samples of the full rate ADC data output. A data capture board is used to read the entire FIFO content through the slower serial peripheral interface bus (SPI) on-chip. The FIFO and SPI digital circuits were IP blocks provided by collaborators. The data capture board also provides a 3.3V supply voltage for the on board regulators. The ADC output data is post processed in a computer running Matlab. All component and equipment details are tabulated in Table 6.1.
CHAPTER 6. EXPERIMENTAL RESULTS

Figure 6.1: Die photo

Figure 6.2: PCB
### Table 6.1: List of components and equipments used

<table>
<thead>
<tr>
<th>Item</th>
<th>Part number</th>
<th>Part description</th>
</tr>
</thead>
<tbody>
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<td>R&amp;S SMA100A</td>
<td>R&amp;S SMA100A</td>
<td>9kHz - 6GHz CW signal generator</td>
</tr>
<tr>
<td>R&amp;S SMW200A</td>
<td>R&amp;S SMW200A</td>
<td>100kHz - 6GHz vector signal generator</td>
</tr>
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<td>BAL-1850</td>
<td>1850BL15B050</td>
<td>surface mount 1850MHz 1:1 Balun</td>
</tr>
<tr>
<td>BAL-0009</td>
<td>BAL-0009SMG</td>
<td>surface mount 500kHz to 9GHz 1:2 Balun</td>
</tr>
<tr>
<td>BALH-0006</td>
<td>BALH-0006</td>
<td>external 200kHz to 6GHz 1:1 or 1:2 Balun</td>
</tr>
<tr>
<td>Regulator</td>
<td>ADP1741ACPZ</td>
<td>2A low dropout linear regulator</td>
</tr>
<tr>
<td>Data capture board</td>
<td>ADS7-V2EBZ</td>
<td>FPGA based data capture kit</td>
</tr>
</tbody>
</table>

### 6.2 Measurement Results

The RF receiver front-end prototype was fabricated in 28nm CMOS technology. It occupies $1.07\text{mm} \times 1.38\text{mm}$ with an active area of $0.64\text{mm}^2$ (Fig. 6.1). In this prototype, part of the blocker detection digital circuitry was implemented off-chip in Matlab as shown previously in Fig. 4.1(b). If implemented on-chip, the total digital area will increase by 15% and the power...
Table 6.2: Measurement summary and comparison table with other DSM-based receivers.

<table>
<thead>
<tr>
<th></th>
<th>[6]</th>
<th>[47]</th>
<th>[48]</th>
<th>[49]</th>
<th>This work</th>
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<tbody>
<tr>
<td>Architecture</td>
<td>RX with ΔΣ-CSF</td>
<td>RX with filtering ADC</td>
<td>Direct ΔΣ RX</td>
<td>Direct ΔΣ RX</td>
<td>RX with ΔΣ-fb digital filter</td>
</tr>
<tr>
<td>CMOS Technology (nm)</td>
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<td>80</td>
<td>65</td>
<td>40</td>
<td>28</td>
</tr>
<tr>
<td>RF Frequency (GHz)</td>
<td>0.6-3</td>
<td>0.04-1</td>
<td>0.4-4</td>
<td>0.7-2.7</td>
<td>0.9</td>
</tr>
<tr>
<td>NF (dB)</td>
<td>2.4-3.5</td>
<td>2.7-3.5</td>
<td>5.9-8.8</td>
<td>3.8</td>
<td>3.9</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>35.5-53</td>
<td>221.4</td>
<td>17-70.5</td>
<td>90</td>
<td>19.5-36.6</td>
</tr>
<tr>
<td>Power Breakdown (mW)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RF</td>
<td>23.5-36.7</td>
<td>113.4</td>
<td>-</td>
<td>48</td>
<td>4.4</td>
</tr>
<tr>
<td>BB Analog</td>
<td>12-16.3</td>
<td>108</td>
<td>-</td>
<td>42</td>
<td>14.6</td>
</tr>
<tr>
<td>BB Digital</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>0.5-17.6</td>
</tr>
<tr>
<td>Supply (V)</td>
<td>1.2</td>
<td>1.8/1</td>
<td>1.5/1.2</td>
<td>1.1</td>
<td>0.9</td>
</tr>
<tr>
<td>IIP3 (dBm)</td>
<td>-6</td>
<td>-13</td>
<td>13.5</td>
<td>-2</td>
<td>-7</td>
</tr>
<tr>
<td>SNDR (dB)</td>
<td>45-52</td>
<td>52-68</td>
<td>40-43</td>
<td>48</td>
<td>18</td>
</tr>
<tr>
<td>RF Carrier BW (MHz)</td>
<td>10,20,40</td>
<td>5,6,7,8</td>
<td>4,10</td>
<td>1.4,15</td>
<td>1</td>
</tr>
<tr>
<td>Area (mm$^2$)</td>
<td>0.7</td>
<td>5.6$^4$</td>
<td>0.56</td>
<td>1</td>
<td>0.64</td>
</tr>
</tbody>
</table>

1. LTE20 mode  2. Estimated  3. RF power includes LNA, mixer, divider and LO distribution  
4. Incl. PLL and DSP

consumption of these digital logic will be minimal as the blocker detection algorithm is only active for a maximum of 26µs every 1ms.

The measurement result is summarized and compared with other DSM-based RX designs [6, 47–49] in Table 6.2. All measurements are performed with a maximum gain setting (44dB) from the LNA input to the quantizer input, controlled by the VGA unless otherwise specified. The receiver front-end operates at 0.9GHz and 1.8GHz with a noise figure (NF) of 3.8dB and 3.9dB respectively. The NF is measured by integrating the baseband output noise from 45kHz to 9MHz with the on-chip digital feedback filter turned on. The RF front-end (LNA + mixer) accounts for 82% of the total receiver noise, and the baseband adds 18% which is dominated by the integrator. This work has a higher NF than [6] because of the lower power consumption in the RF front-end.

The setup for NF measurement is shown in Fig 6.4. A -60dBm signal at 1MHz offset from 1.8GHz is applied from the signal generator, and the total integrated noise from a 50Ω source impedance in a 18MHz bandwidth is -101.3dBm, hence the SNR at the signal generator output is 41.3dB. The total loss (L) of the cable and balun, is 2.3dB at 1.8GHz. The measured SNDR
at the I channel ADC output is 35.1 dB. The NF, including the loss from cable and balun is calculated based on the equation [40]

\[ \text{NF} = \frac{\text{SNR}_{\text{in}}}{\text{SNR}_I} \]  

(6.1)

Which could also be expressed as

\[ \text{NF}_{\text{dB}} = \text{SNR}_{\text{in}, \text{dB}} - \text{SNR}_{I, \text{dB}} = 41.3 \text{dB} - 35.1 \text{dB} = 6.2 \text{dB} \]  

(6.2)

The NF of the receiver can be obtained by de-embedding the loss from cable and balun [40]

\[ \text{NF}_{\text{RX, dB}} = \text{NF}_{\text{dB}} - L_{\text{dB}} = 6.2 \text{dB} - 2.3 \text{dB} = 3.9 \text{dB} \]  

(6.3)

The above method for NF measurement is called the gain method [50]. The output SNR measurement in this method is often performed upon an analog output with the aid of a spectrum analyzer, and is then typically reserved for RF receivers with very high gain or very high NF because the spectrum analyzer noise floor otherwise impacts the accuracy of the measurement [50]. However, since this prototype includes the baseband ADC which has a digital output, no spectrum analyzer is needed. Thus this method provides a very accurate NF measurement for this prototype. The only source of uncertainty that remains is in identifying the setup losses, L. The cable loss is measured with a spectrum analyzer, and the balun loss is extracted from its data sheet. Y factor method is another popular way to measure NF but it requires an Excess Noise Ratio source. Moreover, like the gain method used here, it also required accurate de-embedding of setup loss.

The baseband digital circuitry consumes as little as 0.5mW with no blockers present, 11.7mW with only TX leakage cancellation on and 17.6mW with both TX leakage and blocker
cancellation enabled, hence the total power consumption for 1.8GHz input can vary between 20.4mW and 37.5mW. The IIP3 is measured with two blockers at 17.5MHz and 35MHz, in accordance with the LTE20 standard [5]. The programmable notch was placed at 17.5MHz, thus canceling most of the intermodulation product. IIP3 is -5dBm at 1.8GHz. The baseband is very linear in the presence of blockers due to the digital blocker cancellation path, therefore IIP3 is dominated by the RF front-end.

Fig. 6.5 shows the measured output spectrum of channel I in three different scenarios for band 20 of the LTE20 standard. Note that the thermal noise is dominated by the RF front-end. With the maximum gain setting, -48dBm at the receiver input translates to 0dBFS at the ADC input. First, in Fig. 6.5(a), the desired signal (SIG) is at -3dBFS. Since there are no blockers present, the digital filter can be turned off to provide a 45% power savings. Second, a +15dBFS CW TX leakage is present at 41MHz frequency offset from the input and the desired signal is -20dBFS. The digital bandpass filter is turned on and placed exactly at 41MHz to provide an attenuation of 34.9dB (Fig. 6.5(b)). With the digital filter off, the ADC saturates as expected. Furthermore, in addition to the TX leakage, a +5dBFS blocker is introduced at 22.5MHz and is attenuated by 24.7dB by the programmable filter as shown in Fig. 6.5(c). Note that in Fig. 6.5(b) and Fig. 6.5(c), it seems that with the digital filter on, the TX leakage is only attenuated by 20dB. This is because the FFT spectrum taken at the saturated quantizer output can only have a maximum amplitude around 0dBFS, even though the TX leakage is at +15dBFS.

Fig. 6.6(a) shows the ADC output spectrum with a -30.5dBm modulated TX leakage at 41MHz as required by the LTE20 standard [5]. The modulated TX leakage is produced by PRBS9 data patterns modulated with 16QAM at a bandwidth of 5MHz. The resulting input to the receiver has a peak envelope power (PEP) of -24dBm. The modulated TX leakage is attenuated by 31.5dB on average. Fig. 6.6(b) shows the ADC output spectrum with a -47dBm modulated blocker at 22.5MHz and a modulated TX leakage that is 4dB lower than Fig. 6.6(a) as required by the LTE20 standard [5]. Both blockers are produced by PRBS9 data patterns modulated with 16QAM at a bandwidth of 5MHz. The resulting input to the receiver has a peak envelope power (PEP) of -26dBm. The additional blocker is attenuated by an average of 17.3dB.
Figure 6.5: Measured FFT spectrum for (a) no blocker, (b) CW TX leakage at +15dBFS, and (c) CW TX leakage at +15dBFS and additional blocker at +5dBFS
Figure 6.6: Measured FFT spectrum for (a) modulated TX leakage at -30.5dBm, and (b) modulated TX leakage at -34.5dBm and additional blocker at -47dBm.

Fig. 6.7 shows the measured baseband frequency response with different settings for the programmable notch. It can be moved to any frequency in the range of 17.5MHz–107.5MHz as shown in Fig. 6.7(a). The minimum frequency step size is 1MHz. The amount of attenuation can be decreased in 6dB steps to increase the loop phase margin (Fig. 6.7(b)). The Q factor of the notch can be adjusted depending on the modulated blocker bandwidth as shown in Fig. 6.7(c). A low Q notch is undesirable near the signal band to prevent signal attenuation, however that’s not a problem as blockers close to the signal band have a maximum bandwidth of 5MHz [5].
Figure 6.7: Measured baseband frequency response for programmable notch at different (a) frequency, (b) attenuation, and (c) Q factor settings
Signal to noise and distortion ratio (SNDR) is measured with a signal input offset 1MHz from the carrier, and the interference-to-noise and distortion ratio (INDR) is measured at 41MHz offset, as shown in Fig. 6.8(a). The INDR is defined as the power ratio between the interferer at the input and the inband noise. It can be seen that the receiver front-end can handle a TX leakage 24dB larger than the ADC fullscale, while maintaining the same in-band noise. It is possible for the baseband to handle a blocker even larger than 24dBFS by increasing the fullscale current of DAC\textsubscript{DIG}, however the in-band noise and distortion from DAC\textsubscript{DIG} will increase as well, which increases the receiver overall NF. The SNDR is plotted with different gain settings in Fig. 6.8(b). The receiver gain is digitally programmable in 1dB steps via the VGA from 32dB to 44dB. The receiver has a larger dynamic range at low gain settings, at the expense of higher NF.

![Graph of SNDR and INDR vs. RF input power](image)

Figure 6.8: Measured (a) SNDR and INDR at maximum gain setting versus RF input power, and (b) SNDR at different gain settings versus RF input power.
For CW and modulated blockers with 5MHz bandwidth, $P_{NF,1dB}$ is measured as the input blocker power when the NF increases by 1dB (Fig. 6.9). The modulated blocker used in this test has a peak-to-average power ratio (PAPR) of 9.5dB, which is 6.5dB higher than the CW blocker. The receiver has great rejection for nearby blockers, just as expected. It can tolerate a -31dBm (+18dBFS) CW blocker at 17.5MHz, which is less than twice the signal bandwidth.

Figure 6.9: Measured $P_{NF,1dB}$ versus frequency for CW blocker and modulated blocker with 5MHz bandwidth.

Figure 6.10: Measured blocker detection algorithm with 400 samples per iteration. The 22.5MHz blocker is increased from -12dBFS to +7dBFS to saturate the ADC and the blocker adaptation algorithm correctly detects and cancels the blocker.
Table 6.3: Comparison with other filtering ADCs.

<table>
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<th>[25]</th>
<th>[27]</th>
<th>[28]</th>
<th>[31]</th>
<th>[6]</th>
<th>[35]</th>
<th>This work</th>
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<tr>
<td>Architecture</td>
<td>Analog fADC</td>
<td>Analog fADC</td>
<td>Analog fADC</td>
<td>Analog fADC</td>
<td>Analog fADC</td>
<td>Digital fADC</td>
<td>Digital fADC</td>
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<td>CMOS Technology (nm)</td>
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<td>90</td>
<td>65</td>
<td>65</td>
<td>90</td>
<td>28</td>
</tr>
<tr>
<td>BW (MHz)</td>
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<td>6</td>
<td>9</td>
<td>9</td>
<td>10</td>
<td>9</td>
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<td>OSR</td>
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<td>34</td>
<td>16</td>
<td>16</td>
<td>24</td>
<td>40</td>
</tr>
<tr>
<td>Power (mW)</td>
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<td>54</td>
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<td>5.6</td>
<td>14.3</td>
<td>16.1</td>
</tr>
<tr>
<td>SNDR (dB)</td>
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<td>74.4</td>
<td>74.6</td>
<td>58.1</td>
<td>48*</td>
<td>70.3</td>
<td>48*</td>
</tr>
<tr>
<td>Blocker Frequency (F_{blocker}/BW)</td>
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<td>4.6</td>
<td>5</td>
<td>4.6</td>
<td>4.6</td>
<td>4</td>
<td>4.6</td>
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<tr>
<td>Blocker Attenuation (dB)</td>
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<td>12</td>
<td>12</td>
<td>12</td>
<td>35</td>
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<td>Maximum Blocker Power (dBFS)</td>
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<td>14</td>
<td>16</td>
<td>20</td>
<td>9.5**</td>
<td>24</td>
</tr>
</tbody>
</table>

* Includes RF front-end   **Limited by equipment

Measured operation of the blocker detection algorithm is shown in Fig. 6.10. In the beginning, 22.5MHz blocker is at -12dBFS and the receiver is healthy with a SNDR of 30dB at a signal amplitude of -20dBFS. At iteration 7, a large blocker (+7dBFS) appeared and the SNDR is reduced to 10dB due to receiver saturation. The algorithm first increases the ADC fullscale and then initiates the blocker detection algorithm that sweeps the programmable filter centre frequency from 17.5MHz to 107.5MHz in 1MHz steps. The detection finishes at iteration 54. With the blocker frequency known, it is cancelled and the ADC fullscale is restored. It can be seen that around iteration 58, the SNDR rises to 30dB again. At iteration 60, the blocker disappeared and low power mode is activated, which turns off the digital filter to save power. Overall, it takes 46 iterations from the time blocker appears to the time is cancelled, with each iteration being 400 samples at 720MHz. This translates into 26µs if the detection circuitry were integrated on-chip. This is much less than the 1ms block length identified in Chapter 4 as a target for LTE. Therefore, this approach is suitable for tracking blockers in a real application in real-time without loss of data.

This work is compared with other filtering ADCs in Table 6.3. The SNDR measured in this work and [6] includes the RF front-end as well. The blocker attenuation and maximum allowed blocker power are calculated at the same blocker frequency relative to the signal bandwidth. This work can handle the largest blocker (24dBFS) among all filtering ADCs.
Chapter 7

Conclusion

7.1 Summary

Low supply voltages and analog gain in nanoscale CMOS make the design of a RF receiver very challenging. One of the most difficult requirements is to reject blockers in frequency bands adjacent to the channel of interest whose amplitude is much larger than the inband signal. Traditionally, an analog LPF is used before the ADC in the baseband to provide blocker filtering. This thesis proposed a digital filtering ADC which has a digitally defined transfer function that is highly reconfigurable and completely insensitive to PVT variations. The programmable digital filter provides 34.9dB attenuation of TX leakage and variable attenuation of an additional blocker anywhere in the frequency range 17.5MHz – 107.5MHz. A blocker detection algorithm for this receiver is presented and takes approximately 26µs to converge.

Noise and distortion introduced in the blocker cancellation feedback DAC is highpass filtered with a trivial uncalibrated 1st-order passive network. As a result, the analog baseband circuitry consists only of a 1st-order CTDSM, a feedback DAC with relaxed specifications, plus a few passive components that do not require tuning. The resulting receiver is low-power and well-suited to implementation in CMOS technologies at 28nm and beyond.

7.2 Future Work

The RF front-end is included in this work to test the blocker cancellation of the baseband in a realistic scenario. For a typical receiver, the linearity is usually limited by the backend because of the increasing amplitude in the signal chain. In this case, since the blocker is cancelled by a DAC assisted by a HPF, the overall receiver IIP3 was limited by the RF front-end instead. In
future designs if lower noise figure is required, it would be ideal to have a better RF front-end to take advantage of the linear baseband.

Second, similar to an oversampled modulator, the proposed digital filtering ADC has a tradeoff between blocker attenuation (STF in ADC design) and modulator order (NTF). As previously shown in Fig. 3.14, if a second order modulator is used in the digital filtering ADC instead of a first order, blocker attenuation needs to be sacrificed by 4dB. In future work, it would be beneficial to derive a relationship between the maximum blocker attenuation and the modulator order for easier analysis of design trade-offs. Since the baseband dynamic range depends on the difference between the biggest blocker tolerable and the ADC quantization noise level, understanding the trade-offs will help to obtain the system parameters for achieving the best overall dynamic range.

Even though the first order passive filter used at the baseband input does not consume any power, the two single-ended 80pF capacitors occupy a large area. This makes adapting the proposed solution to lower bandwidth applications difficult, as capacitance is inversely proportional to bandwidth, assuming the same voltage swing at the mixer output (thus the resistance does not change). A differential capacitor could be used to reduce the total capacitor size by a factor of 4, at the expense of reduced common mode rejection.

Moreover, the blocker adaptation algorithm introduced in Section 4 was implemented in Matlab in this work. As a result, the digital logic power and area overhead as well as the convergence time for the algorithm are all estimated. Integration of the algorithm on-chip would allow for confirmation of these estimates.

Finally, even though adaptive blocker cancellation is demonstrated in LTE only, the technique is applicable to other standards such as the upcoming cellular standard 5G, and the newest WiFi standard 802.11ac. The proposed architecture is also a step towards software-defined radio, where instead of digitizing huge bandwidth of data including the blockers, this work digitally differentiates between wanted signal and blockers, and thus reduces the front-end requirement.
Bibliography


