Active Mitigation of Transformer Saturation in Dual-Active-Bridge Converter for Electric Vehicle Chargers

by

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A thesis submitted in conformity with the requirements for the degree of Master of Applied Science Graduate Department of Electrical and Computer Engineering University of Toronto

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Abstract

Active Mitigation of Transformer Saturation in Dual-Active-Bridge Converter for Electric Vehicle Chargers

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University of Toronto
2019

This thesis presents a non-linear active transformer saturation-mitigation-technique suitable for Dual-Active-Bridge(DAB) dc-dc converters, used in bi-directional on-board Electric Vehicle(EV) battery chargers. Bi-directional on-board EV chargers enable features such as vehicle-to-grid, and vehicle-to-vehicle capabilities.

The proposed technique detects the variation in current slope near the saturation boundary. This controller operates with minimal saturation safety-margin and over-design. Compared to protection methods that regulate average current, the proposed control provides a fast and simple way to detect saturation and take corrective action with fewer sensors. The detection and reaction time of the proposed controller reduces the required operating safety-margin, increasing transformer power and converter density.

Validation is done on a 450V, 6.6kW DAB with 96.8% efficiency and 80cm³ transformer. Compared to similar DAB converters, the proposed controller halves the transformer volume with a higher efficiency. The proposed transformer is only 20% larger than those used in resonant converters with four times the frequency.
Acknowledgements

It was always a dream of mine to work on projects that would have an impact greater than their scientific contribution. While my work on this graduate thesis is only a small step towards realizing that dream, it has been an incredible opportunity and learning experience. Professor Olivier Trescases, it has been a privilege to have a mentor who embodies dedication, professionalism, innovation, work ethic and excellence early in my professional career. Your guidance, support and vision throughout this journey have been most valuable and I am entirely grateful for it all.

I learned how to be a critical thinker and problem solver from Professor Peter Lehn who showed me as an undergraduate student that power electronics can be applied to a much broader field. Together with Professor Trescases, you have been my inspiration for going to graduate school. For this and your continued support, thank you.

Miad Nasr, Mazhar Moshirvaziri, and Professor Hirokazu Matsumoto, your help from the very beginning has been fundamental in this project. From your practical experience to your vast knowledge of magnetics, you were always there to guide me and answer my questions. Without the experience of Kishtij and Carlos I would never have been able to meet the mechanical challenges of this project. Shawkat, Sepehr and Violet, I would like to thank you for the helping hand and consultation at crucial points in this thesis.

I would be remiss to not acknowledge Tony and Theo, without whom this project would not have been possible. Your drive in developing clean vehicles is inspirational.

Bjorn, Carl, Moiz, Mojtaba, Nameer, Nick, Venkata, Samantha, Shuze, Yongshi, and Zhe, you are incredible friends. I have, not only enjoyed working with you the past few years, but also, am grateful for your help, our discussions and debates, and the problems we've solved together. You have made graduate school memorable and fun.

Finally, to my family, words cannot express how grateful I am for all your unconditional love and support not just the past couple years, but at every turn. Mom, Dad, you have been my rock, motivation, inspiration, and so much more. I am entirely grateful for everything you have done for me and I would like to dedicate this thesis to you as a token of my gratitude.
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Chapter 1

Introduction

The adoption of Electric Vehicles (EVs) is increasing both in industry as well as commercially due to the versatility, modularity and reliability of electrically driven systems. Range anxiety and initial costs are two limiting factors that hold back their widespread adoption. There are 11.9 million cars registered in Ontario, Canada’s most populated province [1]. The average commute time in Toronto, Ontario’s largest city, is 32.4 minutes one-way for a maximum average travel distance of 10 km [2, 3]. Based on the New European Driving Cycle, an EV with a 24 kWh battery pack can drive for 160 km [4]. Considering the average Toronto commute, an EV with a 24 kWh battery only depletes 10%. Depending on the power level, the charge depleted in a one-way commute to work can thus be replenished within 1 hr using an on-board ac-input charger. There are 3 levels of ac-input charging. Level 1 is rated to charge below 2 kW, level 2 is rated to charge below 20 kW and level 3 is rated for above 20 kW. Level 2 is the most common, with typical on-board EV chargers rated for 3.3 kW, 6.6 kW or 7.2 kW. A higher power rating can reduce this daily charge time further and ultimately decrease the need for a large battery pack.

The battery of an EV constitutes a minimum of 68% of the total power-train cost, while the onboard charger constitutes at most 4% of the power train cost [4]. Given the large impact that low-cost high-power on-board chargers can have on the battery size and vehicle usability, they are an ideal area of innovation to both reduce range anxiety and decrease the initial cost of EVs.

Another means of increasing EV adoption is by unlocking vehicle-to-grid, vehicle-to-home and vehicle-to-vehicle capabilities through a bi-directional Power-Hub in place of the predominately used uni-directional, on-board chargers [5]. Not only does this provide consumers with a local emergency energy storage, but it also provides utilities with a potential grid stabilizing element to aide with the integration of renewable power
generation.

1.1 EV Charger Design

The conventional architecture for an on-board charger is a two-stage structure consisting of an inverter and a dc-dc converter, as shown in Fig. 1.1.

![Conventional two-stage charger](image)

Figure 1.1: Conventional two-stage charger. The focus of this thesis is the isolated dc-dc converter.

Modern EV chargers require:

1. Power factor correction to prevent high harmonic current draw from the grid [6].

2. Galvanic isolation to prevent the injection of dc current into the grid and to provide safety from fault conditions [7].

3. A battery interface to implement a charging algorithm to control the state-of-charge and prevent damage to the battery cells.

Power factor correction is performed by the first stage ac-dc converter, while galvanic isolation and the battery interface are often implemented in the second stage, dc-dc converter. By implementing galvanic isolation using a high frequency transformer in the second stage, the system power density is higher than designs employing a 60 Hz transformer in the first stage. Furthermore, isolation that is implemented as a high frequency transformer is often cheaper than isolation implemented as a 60 Hz transformer. To reduce the initial cost associated with a complex thermal system, and the subsequent operating losses incurred as wasted energy, both stages must have high efficiency. The location of the losses has a large impact over the thermal design complexity. The focus of this thesis is the volume and efficiency optimization of a Dual-Active-Bridge (DAB), dc-dc stage of a bi-directional on-board EV Power-Hub.
1.1.1 DC-DC Converter

Three common bi-directional converters are used for the second stage of bi-directional on-board EV chargers, the DAB, the resonant LLC, and the resonant CLLC converter. The resonant converters have dc-blocking capacitors that are placed in series with the transformer to prevent the flow of dc current. Due to the operating frequency and the magnitude of current, these capacitors are often large. Unlike resonant converters, the DAB only has partial soft switching, (only soft turn-on switching). Unlike the thermal management system of resonant converters, the DAB may need extra volume to regulate the additional losses. The characteristics of each converter are listed in Table 1.1.

Table 1.1: Comparison of Bi-Directional dc-dc Converters for Two-Stage On-Board Chargers

<table>
<thead>
<tr>
<th>Feature</th>
<th>LLC [8] Fig. 1.2</th>
<th>CLLC [9] Fig. 1.3</th>
<th>DAB Fig. 1.4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Soft Switching</td>
<td>full</td>
<td>full</td>
<td>partial</td>
</tr>
<tr>
<td>Bi-directional</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Transformer dc current blocking</td>
<td>one transformer</td>
<td>both transformer</td>
<td>no</td>
</tr>
<tr>
<td></td>
<td>terminal</td>
<td>terminals</td>
<td></td>
</tr>
<tr>
<td>Relative size</td>
<td>one large resonant capacitor</td>
<td>two large resonant capacitors</td>
<td>no resonant capacitors</td>
</tr>
</tbody>
</table>

Figure 1.2: LLC converter.

Figure 1.3: CLLC converter.
The LLC and CLLC converters, both incorporate galvanic isolation in a resonating ac link. The LLC is commonly used as a uni-directional converter in commercial on-board EV chargers. Given the high-level comparison, the DAB was chosen for the second stage of the proposed Power-Hub due to its simple control and high power density. Similar to the resonant LLC and CLLC, the DAB is a bi-directional converter. Unlike the resonant LLC and CLLC, the DAB lacks resonant capacitors, which under the same efficiency, potentially makes it more dense. Through the optimal choice of transformer, DAB inductance, switching frequency, and semiconductor devices, the DAB efficiency can be optimized.

### 1.1.2 Dual-Active-Bridge Topology and Operation

The two bi-directional ports of a DAB converter are ideally connected to an ac link through full-bridges (FBs), as shown in Fig. 1.5. Each FB generates an ac square voltage waveform, \( v_1 \) and \( v_2 \), as shown in Fig. 1.5. A phase-shift between \( v_1 \) and \( v_2 \) dictates the power flow of the converter from the leading to lagging FB. In the Power-Hub application, one of the bi-directional ports of the DAB is connected to the bus and the other is connected to the battery, as shown in Fig. 1.5. In a two stage on-board charger, the bus voltage is set and varied with a command sent to the first stage ac-dc converter. In this thesis, the ports are referred to as the “bus” and “battery” for consistency.

![Figure 1.4: DAB converter.](image)

![Figure 1.5: DAB converter topology. The value of \( v_{2,reflected} \) varies with the value of \( L_{leakage} \) and change in core permeability. \( n \) is assumed to be equal to 1 in this thesis.](image)
The rate of change of the current in the ac link is given by,

$$\frac{d}{dt}i_{DAB} = \frac{v_{DAB}}{L_{DAB} + L_{\text{leakage}}},$$  \hspace{1cm} (1.1)

where $L_{\text{leakage}}$ is the leakage inductance of the transformer, $L_{DAB}$ is an inductor placed in series with the transformer, and

$$v_{DAB} = v_1 - v_2.$$  \hspace{1cm} (1.2)

The difference in time between the leading and lagging FB, $t_{ps}$ is given in terms of the phase-shift, $\varphi$, by,

$$t_{ps} = T_s \frac{\varphi}{2\pi},$$  \hspace{1cm} (1.3)

where $T_s$ is the switching period, and $\varphi$ has the unit of radians. The resulting $v_{DAB}$ waveform can be seen in Fig. 1.6.

During $t_{ps}$, the magnitude of the voltage across the inductances, $L_{DAB}$ and $L_{\text{leakage}}$ have a value equal to the sum of the DAB terminal voltages. During the plateau periods, the magnitude of the voltage, $v_{DAB}$, across the inductances, $L_{DAB}$ and $L_{\text{leakage}}$ is equal to...
the difference of the DAB terminal voltages, as labeled in Fig. 1.7. The resulting current through the ac link, $i_{DAB}$, is shown in Fig. 1.7.

![Diagram of DAB waveforms](image)

Figure 1.7: $i_{DAB}$ and $v_{DAB}$ waveforms.

The two plateaus of $i_{DAB}$ that occur every switch cycle are denoted as the positive and negative plateau in this thesis. To ensure minimal conduction loss, the $i_{DAB}$ plateaus are kept flat by varying the bus voltage to match the changing battery voltage (depending on state-of-charge). Dead-time is also implemented within each FB to take advantage of soft turn-on switching. The required dead-time is chosen based on the turn-on and turn-off times of the chosen semiconductor devices during worst-case converter operation. Several strategies have been studied in literature to expand the range of load operating conditions and bus-battery voltage ratios where soft turn-on switching can be achieved in the DAB converter. These strategies involve active frequency modulation, and active $L_{DAB}$ variation [10]. The value of $L_{DAB}$, switching frequency, $f_s$, transformer size and turns ratio, $n$, can all be varied to optimize the overall converter efficiency.

The largest passive component of an on-board EV charger DAB is typically the transformer due to the high power rating. In [11] a 3.3kW DAB converter with a transformer volume of 170 cm$^3$, and a peak efficiency of 96.3% is designed for use in an on-board charger. In [12] a bi-directional 6.6kW CLLC resonant converter for an on-board charger application with a transformer volume of 60 cm$^3$ and a peak converter efficiency of 97.8% is presented. In industry, examples of 6kW planar transformers with a volume of 80 cm$^3$ can be found from companies such as [13].
Due to full soft-switching, and inherent dc-current blocking, resonant converters can operate at high switching frequencies for a desired range of load operating conditions with low impact on efficiency. Thus, transformer minimization becomes generally independant from the switch operation. The DAB converter offers similar transformer minimization through high-frequency operation, without full soft-switching or inherent dc-current blocking. The comparatively smaller volume of the DAB in addition to the low part count make it an ideal candidate for the dc-dc stage of an on-board charger. To maximize the net benefit of the DAB, the smallest possible transformer must be used while operating at the lowest required switching frequency. To decrease the transformer size without operating at excessively high switching frequency and subsequent losses, the transformer core must operate with high magnetic flux density, $B$. High $B$ reduces the safety margin required in DAB converters to prevent transformer saturation. This safety margin is especially important in DAB converters which lack dc-blocking capacitors and thus are susceptible to saturation caused by non-ideal ac current flowing in the ac link. [14–17] have proposed active methods to mitigate transformer saturation, but require additional circuitry or non-standard core designs for implementation. Passive methods involve air gap integration and over-sizing transformers which lead to lower density and higher loss.

1.2 Thesis Motivation and Objectives

This thesis is focused on the optimization of transformer volume and converter efficiency through the transformer $B$ amplitude, $\Delta B$, and converter switching frequency, $f_s$. This requires a saturation prevention algorithm, SPA, to enable the operation of the transformer at high $\Delta B$ by reducing the required safety margin. The objectives of this thesis are to:

1. Design a transformer with the smallest volume for a given target converter loss budget.

2. Experimentally validate the mathematical model describing the cause of saturation and its effect on $i_{DAB}$ and $v_{2,\text{reflected}}$.

3. Design a SPA, to enable transformer operation at high $\Delta B$, particularly at the edge of saturation, while minimizing cost. This objective can be accomplished with the following criteria:

   (a) Ensure that the controller capability is independent of, $L_{DAB}$, and converter power level.
(b) Derive a low complexity, digital implementation of the proposed controller to minimize FPGA demand.

(c) Merge the proposed controller with the existing DAB power regulation controller.

(d) Minimize the additional number of sensors and sample rate required by the proposed algorithm. Ideally, sample rate should be proportional to switching frequency.

4. Experimentally validate the proposed controller, transformer and converter functionality.

5. Achieve similar efficiency to state-of-the-art converters while using a transformer with the smallest possible volume.

The designed transformer and the implemented SPA are targeted for a 6.6kW DAB converter for use in a Power-Hub. The primary research contribution of this thesis is a high bandwidth SPA that enables the operation of the transformer at the core saturation bounds. This is accomplished through the analysis of the effects of saturation on the DAB current waveform and the use of on-line slope measurements to infer the core $B$ and thus saturation.

This thesis is organized in six chapters. The design decisions leading to the proposed DAB, particularly those made to optimize efficiency and volume are described in Chapter 2. The challenges associated with the desired transformer minimization, particularly saturation are described in the Chapter 3. A proposed algorithm to resolve the challenges associated with saturation is proposed in Chapter 4. Experimental verification of the proposed algorithm and the overall converter operation is shown in Chapter 5. Finally, conclusions as well as suggestions for future work are provided in Chapter 6.
References


Chapter 2

Dual-Active-Bridge Converter Design

This chapter describes the volume and efficiency optimization of the DAB converter switching frequency and transformer design. The practical considerations required to implement these optimized designs from both thermal and electrical perspectives, including PCB designs and choice of semiconductor devices are analyzed in this chapter.

2.1 Transformer

The conventional transformer design methodology utilises a fixed converter parameter, such as switching frequency as the starting point for optimization [1]. This fixed frequency is often chosen based on the power-electronic capabilities. This approach is accurate if transformer and non-magnetic losses can be significantly decoupled. Furthermore, the interdependence of core and switching losses allows for the distribution of losses among electrical components with more favorable heat dissipation properties. With the use of Gallium Nitride (GaN), and Silicon Carbide (SiC) devices, converters can be operated at a high switching frequency, with low gate-drive and switching losses due to their more favourable $R_{on}Q_g$ Figure of Merit compared to available silicon devices. In isolated converters, high frequency operation is greatly limited by the associated magnetic losses. To characterize this limitation, the energy transfer mechanism of transformers and their loss characteristic with respect to magnetic flux density, $B$, and operating frequency are analyzed.
2.1.1 Operating Principles

The magnetic flux density, $B$, in a transformer is given by

$$B = \frac{1}{n A_e} \int_{t_1}^{t_2} V dt,$$  \hspace{1cm} (2.1)

where $n$ is the number of transformer winding turns, $A_e$ is the core cross section area, and $V$ is the voltage applied across the transformer terminal. With the application of a 50% duty cycle square wave voltage of amplitude $V_{peak}$, the $B$ amplitude in the transformer, $\Delta B$, is given by

$$\Delta B = \frac{1}{n A_e} \int_{t + \frac{T}{4}}^{t} V_{peak} dt,$$  \hspace{1cm} (2.2)

where $T$ is the switching period.

The effects of four possible transformer design decisions on the relation expressed in (2.2) are explored in Table 2.1. For example, reducing the core size in a converter while maintaining the switching frequency, voltage, and current limited wire gauge, the $\Delta B$ increases.

<table>
<thead>
<tr>
<th>Transformer design change</th>
<th>$V_{peak}$</th>
<th>$n$</th>
<th>$A_e$</th>
<th>$T$</th>
<th>$\Delta B$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency increase</td>
<td>constant</td>
<td>constant</td>
<td>constant</td>
<td>decrease</td>
<td>decrease</td>
</tr>
<tr>
<td>Applied voltage increase</td>
<td>increase</td>
<td>constant</td>
<td>constant</td>
<td>constant</td>
<td>increase</td>
</tr>
<tr>
<td>Core size increase</td>
<td>constant</td>
<td>constant</td>
<td>increase</td>
<td>constant</td>
<td>decrease</td>
</tr>
<tr>
<td>(A_e increase)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Core size decrease</td>
<td>constant</td>
<td>decrease</td>
<td>decrease</td>
<td>constant</td>
<td>increase</td>
</tr>
<tr>
<td>(A_e decrease, n decrease)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

2.1.2 Material Characteristics

The relationship between the magnetic flux density, $B$, and magnetic field, $H$, of ferromagnetic and ferrimagnetic materials is defined by a particular $BH$ curve, as seen in Fig. 2.1. Key features of the $BH$ curve are the:

1. transitions between the linear and non-linear regions, (denoted $+B_{sat}$ and $-B_{sat}$),
2. inverse relationship between the slope of the linear region and the core reluctance,

3. dependence of a magnetic material hysteresis on the width of its $BH$ curve. The larger the remanence flux density, $B_r$, and coercive force $H_c$ of a curve, the more energy is lost every $B$ polarity reversal. This occurs synchronously with every DAB switch cycle,

4. Curie temperature, $T_c$, of a material is the temperature at which the core loses magnetization (permeability decreases rapidly). Increasing temperature until $T_c$, the magnetic permeability increases while core loss varies with a local minimum.

![Figure 2.1: Ferromagnetic material $BH$ curve.](image)

The Curie temperature, $T_c$, ±$B_{sat}$, and $H_c$ are compared for different materials in [2] and are summarized in Table 2.2.

<table>
<thead>
<tr>
<th>Material</th>
<th>$T_c$ (°C)</th>
<th>$B_{sat}$ (T)</th>
<th>$H_c$ (A/m)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon-Iron (Iron)</td>
<td>750</td>
<td>1.5-1.8</td>
<td>31.8-47.7</td>
</tr>
<tr>
<td>Vitroperm (Amorphous)</td>
<td>460</td>
<td>1.0-1.2</td>
<td>1.6-3.2</td>
</tr>
<tr>
<td>Manganese Zinc (Ferrite)</td>
<td>100-300</td>
<td>0.3-0.5</td>
<td>3.2-19.9</td>
</tr>
<tr>
<td>Nickel Zinc (Ferrite)</td>
<td>150-450</td>
<td>0.3-0.5</td>
<td>23.9-39.8</td>
</tr>
</tbody>
</table>

Comparing core materials, iron has a higher $B_{sat}$ and $H_c$ than ferrite. Furthermore, compared to iron and amorphous materials, ferrite properties are more dependent on tem-
Temperature. The loss characteristics of different ferrite varieties are analyzed Section 2.1.3.

### 2.1.3 Temperature Considerations

Temperature affects the magnetic properties of ferrite, particularly the core loss and saturation boundaries. It can also affect the ferrite reliability due to thermal shock if the core experiences an excessive rate of temperature rise. Furthermore, the temperature rating of wire insulation must be considered. These effects are explained in further detail below:

Figure 2.2: Core loss as a function of temperature for N97 ferrite material. After a temperature of 94°C, the losses increase with temperature [3].

1. **Core loss** reaches a minimum at a specific temperature based on the particular ferrite formulation. This temperature corresponds to the ferrite “Second Maximum of Permeability”. This temperature results in the minimum magnetostriction for the particular ferrite [4]. As magnetostriction decreases, the core loss decreases due to the easier motion of magnetic domains [5]. As temperature exceeds the point towards the Curie temperature, $T_c$, thermal runaway may occur and the core loss increases with rising temperature [3], as seen in Fig. 2.2. The DAB transformer was designed with a target operating temperature at the local loss minimum.

2. **The saturation magnetic flux density**, $B_{sat}$ decreases as temperature increases to $T_c$ due to the reduction in the core saturation magnetization. In N97 material, $B_{sat}$
decreases from 510 mT to 410 mT, as temperature increases from 25 °C to 100 °C [3].

3. Ferrite cracking (thermal shock), occurs due to a sharp rise in core temperature. Companies such as [6] recommend a maximum temperature rise of 2 °C to 3 °C per minute to prevent thermal shock. In this thesis, the temperature rate is managed through a soft-start algorithm.

4. The polyurethane strand isolation coating and the nylon bundle cover on the chosen Litz wire have different breakdown temperatures, the lowest is 130 °C, which limits the maximum transformer operating temperature.

2.1.4 Loss Considerations

Winding, core and eddy-current losses in transformers are summarized below in the context of the DAB topology:

1. Winding loss is impacted by, the proximity effect, skin-depth effect and dc resistance.

   (a) Skin-depth associated loss occurs when an ac current produces a time varying magnetic field that produces opposing eddy-currents in the winding wires. The opposing eddy-currents force the main current to flow at the conductor surface, and thus increase the effective resistance, \( R_{ac} \). Skin-depth, \( \varepsilon \) is the depth away from the surface of the conductor where the current density is approximately 37% of the current density at the surface [2, 7]. It is given in centimeters by,

\[
\varepsilon = \frac{7.5}{\sqrt{f}}
\]

where \( f \) is the frequency of the current (equal to switching frequency, \( f_s \) in DAB converters). For a \( f_s \) of 50 kHz to 250 kHz, \( \varepsilon \) is between, 335.41 µm to 150 µm, which requires a minimum 29 AWG conductor. Following [1], a wire gauge between 38 AWG to 42 AWG was chosen to ensure the gauge diameter was one third of the skin depth. 40 AWG wire strands were ultimately chosen for this design.

   (b) DC winding loss is based on the wire, DC resistance. Assuming a maximum steady-state temperature of 60 °C, the wire insulation, and the expected cur-
rent carrying capacity, a 10-12 AWG wire was needed [8]. 10 AWG wire was ultimately chosen.

(c) Proximity loss occurs when two closely spaced parallel wires carry current in the same direction. The magnetic fields produced by the current in one wire creates eddy-currents in the surrounding copper wires, impeding current from flowing through the complete wire cross section. This results in an increase in $R_{ac}$, that can be calculated using the equation,

\[
\frac{R_{ac}}{R_{dc}} = F_r = 1 + \frac{\pi^2 \omega^2 \mu_0^2 N^2 n^2 d_c^6 k}{768 \rho_c^2 b_c^2}, \quad (2.4)
\]

where

- $\omega$ is the frequency of the current through the transformer, (in radians),
- $n$ is the number of wire strands,
- $N$ is the number of turns,
- $d_c$ is the wire diameter,
- $\rho_c$ is the resistivity of copper,
- $b_c$ is the breadth of core window-area usage,
- $k$ is the factor accounting for field distribution, (usually = 1).

For example, if the breadth of window usage is 33%, $b_c = 0.33$, $N=26$, $n=1100$ strands, $d_c=78.74$ um, $\rho_c=0.0001678 \ \Omega m$, $\mu_0=4\pi \times 10^{-7}$, $\omega = 150000(2\pi)$, $F_r = 1.000000002$ and therefore not a large factor.

2. Core loss originates from material hysteresis, as seen in Fig. 2.1. Materials with a large hysteresis are avoided in switch-mode-power supplies (SMPS), as they are often magnetized and demagnetized repeatedly. Therefore, higher switching frequency results in higher core losses over a constant operation time. Additionally, larger ferrite volume or a higher ferrite $\Delta B$, store and lose more energy every switch cycle. Compared to iron cores, ferrites have less core loss per volume in addition to having a smaller $B_{sat}$.

3. Eddy-Current loss originates from the formation of eddy-currents in the core material due to a changing magnetic field. In iron cores, the electrical resistance of the core material is low and thus, lamination is required to prevent large eddy-currents from forming. As ferrites are the homogeneous mixture of oxides, they have a high electrical resistance and thus low eddy-current formation.
2.1.5 Measuring Core and Eddy-Current Losses

Available manufacturer data does not provide detailed loss characterization for a wide range of operating frequencies. To do a comprehensive optimization, eddy-current and core losses are measured as a lump sum, $P_{\text{ferrite}}$, for the core material of interest. These losses are measured together due to their interdependence. To measure these losses, the resonant circuit proposed in [9] is used, as seen in Fig. 2.3.

![Core Material Under Test](image)

**Figure 2.3**: Test circuitry for measuring the sum of core loss and eddy-current loss at different frequencies and different $\Delta B$ in a core material of interest.

The test circuit applies an ac current, $I_{\text{resonant}}$, through windings around the core material under test. The magnitude of the ac current and related core $\Delta B$, are varied by control voltage $V_{\text{test}}$. The circuit resonates at every frequency of interest by varying the capacitor size and full-bridge $f_s$. With a precision resistance, the total loss absorbed by the circuit was given by

$$P_{\text{in}} = I_{\text{resonant,RMS}}^2 R_{\text{precision}} + P_{\text{ferrite}},$$

where $R_{\text{precision}}$, $I_{\text{resonant,RMS}}$ and $P_{\text{in}}$ are known and $P_{\text{ferrite}}$ is unknown. The purpose of the precision resistance is to limit the current drawn under resonance.

As described in Section 2.1.3, $P_{\text{ferrite}}$ is affected by temperature. It is challenging to cool the transformer in the closed environment of the Power-Hub. Prior to thermal runaway in the core, the hottest permissible temperature is approximately 94 °C. Therefore, the core under test was kept constant at that temperature using a thermal chamber [3]. The results of the test are shown in, Fig. 2.4.
Two trends are present in the results shown in Fig. 2.4.

1. For a fixed frequency, the relationship between the per volume core loss of ferrite and \( \Delta B \) is given by

\[ P_{\text{ferrite}} \propto \Delta B^2. \]  

(2.6)

2. An increase in frequency, increases the rate at which \( P_{\text{ferrite}} \) increases with B.

The temperature dependence of \( P_{\text{ferrite}} \) was also measured at 150 kHz switching frequency. With a temperature decrease of 34 °C from 94 °C, the core loss increased by 150%, as presented in Fig. 2.5.
Figure 2.5: Measured core and eddy-current loss at 60 °C and 94 °C for N97 ferrite under 150 kHz excitation.

2.1.6 Cooling Considerations

Ferrites are challenging to cool for two major reasons:

1. Ferrites have a high thermal resistance that increases with decreasing ferrite size. For the same loss, smaller cores operate at a higher temperature than larger, similar shaped cores. Different shapes have slightly different size to thermal resistance trends based on their surface-area to volume ratio. For example, under a constant core loss of 10 W, and ambient temperature of 25°C, an EE core and an ETD core operate at a different temperature if air cooled, as shown in Fig. 2.6. The high temperatures show that stagnant air cooling is not a viable solution as the core operates above the optimal core loss temperature for the majority of core sizes.
2. Fringing fields prevent cooling plates from being placed close to the ferrite as the plates experience eddy-current losses. Fringing fields occur around air gaps and other sharp discontinuities in ferrite material, as seen in Fig. 2.7. As such, for the same $\Delta B$, an increase in gap results in higher fringing fields.

The further placement of a cooling plate not only increases the effective volume of the core, but also decreases the thermal system efficiency. As such, no air gap was used in the transformer design. As cores decrease in size, and cooling demands increase, conductive heat removal through multiple liquid cooling plates (referred to as, a chill-pot in this thesis) and potting compound were considered. Electromagnetic simulation of eddy current losses were used to determine the minimum distance between the pot walls and core.

Figure 2.6: For 10 W of core loss, the temperature for different sizes of two core families, (ETD and EE), are shown [3]. Stagnant air cooling has been assumed. The loss per volume in units of kW/m$^3$ is labeled for each point.
Figure 2.7: (a) Electromagnetic simulation of the $B$ in a 6.6kW DAB transformer using an ETD49 core, with a chill-pot placed over half of the transformer. Fringing fields can also be seen around the transformer. (b) The fringing fields around the air gaps between the two ferrite half-cores cause eddy-current losses in the surrounding metal.
2.1.7 Leakage Inductance Considerations

Leakage inductance has three implications in the DAB converter.

1. If large enough, it can replace the need for a separate DAB inductor. The consistency required of this parameter requires a precise manufacturing process especially for windings using Litz wire. This problem can be alleviated with the use of PCB transformers [10].

2. A large leakage inductance decreases the efficacy of any separate DAB inductor used in the circuit.

3. Larger fringing fields contribute to the converter EMI and require a more complex PCB design to protect against it. Additionally, fringing fields make cooling more challenging, as described in Section 2.1.6.

A separate DAB inductor is chosen for the proposed design to increase the implementation precision. An interleaved winding is used in the transformer to reduce the transformer leakage inductance [2].

2.2 Semiconductor Device

The C3M0065090J, Silicon Carbide MOSFET was chosen as it provided the necessary breakdown voltage with low on resistance, \( R_{on} \) and low switching losses due to the fast turn-on and turn-off times of the device. Furthermore, to enable high frequency switching operation, surface mount components were chosen for their low lead inductance and size in comparison with their TO-247 counterparts (10% of the TO-247). Gate drive paths and power paths with low parasitic inductance were also designed to prevent excessive ringing and MOSFET damage. The thermal design of these packages were analyzed in detail due to the small available heat conduction area. The thermal operating condition was calculated in Appendix A to ensure device capability.

2.3 Dual-Active-Bridge Transformer and Converter Optimization

In literature, a large amount of research has been done in the development of novel computerized algorithms for transformer optimization. Variations to algorithms include variable phase [11], thermal and insulation considerations [12], algorithm methodology [13],
and variable temperature rise [14]. These studies however, do not incorporate the converter operation into the optimization process. Specifically, optimization processes that do not target resonant converters, often treat converter frequency as a predetermined specification that has been optimized for the converter operation. In non-resonant converters, frequency has a large impact on the total converter efficiency due to both transformer and the semiconductor losses. The availability of liquid cooling in EV applications provides further opportunities for high-density transformer designs. An optimization including the turn-off switching losses is performed on the proposed Power-Hub DAB.

The first step in optimizing a transformer is choosing a material. The material Performance Factor ($PF$), given by,

$$PF = f \cdot \Delta B$$  \hspace{1cm} (2.7)

allows for prospective materials to be compared in terms of maximum flux density and operating frequency (Where $\Delta B$ is the transformer flux density amplitude, and $f$ is the operating frequency) [15]. In the DAB, $f = f_s$. The $PF$ of various ferrite formulations were obtained from the manufacturer TDK, as shown in Fig. 2.8,

For a given core loss density and core temperature, the material with the highest $PF$ can also produce the smallest transformer. In frequencies below 300 kHz, N97 material yields the highest $PF$ at 90°C whether with a core loss density of 300 kW/m$^3$ (typical value used for $PF$) or 550 kW/m$^3$ (largest value characterized by TDK). Subsequently, N97 material is chosen as the DAB transformer ferrite material. The second step in transformer optimization is determining the allowable copper loss, $P_{cu}$ and associated winding design. Given a target $P_{ferrite}$, it is shown in [1] that the optimal total transformer loss,

$$P_{\text{total}} = P_{\text{ferrite}} + P_{\text{cu}}$$  \hspace{1cm} (2.8)

occurs when,

$$P_{\text{ferrite}} \approx P_{\text{cu}}.$$  \hspace{1cm} (2.9)

This is due to the opposite trends in $P_{\text{cu}}$ and $P_{\text{ferrite}}$ with respect to the transformer $f$ and $\Delta B$ as given by

$$P_{\text{cu}} \propto \frac{1}{f \cdot \Delta B},$$  \hspace{1cm} (2.10)
Figure 2.8: Datasheet derived $PF$ for N97, N87, N49, N27 ferrites from TDK, at 90 °C with a per volume core loss of, 2.8(a) 300 kW/m$^3$ and 2.8(b) 550 kW/m$^3$. 
and

\[ P_{\text{ferrite}} \propto f \cdot \Delta B. \]  

(2.11)

[1] shows that the optimal \( P_{\text{total}} \) at a particular \( \Delta B \), results in

\[ P_{\text{ferrite}} = \frac{2}{\beta} P_{\text{cu}}, \]  

(2.12)

where \( \beta \) is a physical parameter (typically close to 2) derived from the stienmetz equation for core loss.

Conventional Methodology

Existing methodologies for optimal transformer design perform the following steps.

1. An optimal converter frequency is chosen based on topology optimizations [1].

2. Optimal material and \( \Delta B \) are chosen based on material \( PF \) defined for a particular core loss density (typically 300 kW/m\(^3\)) and optimal converter frequency.

3. The smallest core size that achieves the desired \( \Delta B \) is chosen with a safety margin. For example, in [12] a margin of 20% is used to avoid saturation.

4. The target \( P_{\text{cu}} \) is calculated approximately equal to the \( P_{\text{ferrite}} \).

5. A winding is chosen that fits the core and meets the target copper loss.

This standard methodology separates the optimization of the transformer from the converter, and is inadequate for converters that are not fully soft-switching.

Proposed Methodology

Based on the discussion in Section 2.3, switching loss must also be considered in the optimization of DAB converters. To perform this optimization, the design space of \( \Delta B \) and \( f_s \) operating conditions for the converter and transformer are analyzed in terms of the total converter loss (including switching, conduction, core and eddy-current losses). The smallest transformer that can accommodate the \( \Delta B \) and \( f_s \) operating conditions is found for each possible design point, ensuring the lowest core loss. As the DAB is intended for use in an on-board charger, it is expected to operate at rated power for a prolonged period of time and thus, the transformer optimization was done at rated power. For the same total loss, an operating point with a smaller transformer is beneficial for both the
converter volume and cost. The assumptions and parameters used for this analysis are as follows:

1. Based on $PF$, N97 ferrite was chosen.

2. The ETD core family was considered due to the low leakage and high granularity of standard core sizes.

3. A turns ratio of 1:1.08 (Secondary:Primary as shown in Fig. 1.5) was chosen to ensure a flat $i_{DAB}$ plateau and therefore, no excessive conduction losses.

4. The target efficiency for the dc-dc stage of the two stage converter is 97% and thus, 198 W of loss is budgeted for the entire converter.

5. Switching loss is modeled as defined in Appendix. A.

6. Conduction loss is assumed constant as the trapezoidal $i_{DAB}$ waveform with a flat plateau is similar to a bi-polar square wave, and thus its RMS value is approximately equal to its plateau value. As such, it is not significantly dependent on phase shift or frequency.

7. Rated power is achieved when $V_{batt} = 450$ V and $V_{bus} = 480$ V.

8. The wire chosen in Section 2.1.4, is used for every design point when determining transformer size. As the rated power and terminal voltages of the DAB remain constant, the effect of different wire gauges on the number of possible transformer turns is neglected.

Based on the above assumptions, the bounds of the design space are defined in Table 2.3.

<table>
<thead>
<tr>
<th>Design Variable</th>
<th>Minimum</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_s$</td>
<td>$40 \text{ kHz}$ is the minimum frequency that the converter can operate the largest ETD core</td>
<td>$300 \text{ kHz}$ is the maximum frequency the ceramic decoupling capacitors of the converter can be operated [16]</td>
</tr>
<tr>
<td>$\Delta B$</td>
<td>$0 \text{ T}$ (not inclusive)</td>
<td>$B_{sat}=0.41 \text{ T}$ as defined in [17]</td>
</tr>
</tbody>
</table>
Result of Proposed Methodology

The switching loss was modeled to linearly increase with switching frequency, with no dependence on ΔB for the entire design space.

The eddy-current and core loss of the transformer were also modeled as seen in Fig. 2.9. The smallest feasible transformer in the ETD family at each ΔB and $f_s$ was found. A transformer is feasible if it can fit the necessary winding cross-section to operate at a particular design point (the wire gauge is defined in Section 2.1.4). When a smaller core is used in place of a larger one, a discontinuity occurs in the transformer core loss as shown by the discontinuities in Fig 2.9.

![Graph showing calculated core and eddy-current loss versus ΔB and converter $f_s$. The different colors represent the smallest feasible core (in terms of available cross-sectional area for the needed number of turns) in the ETD family. Discontinuities occur when a smaller feasible core can be used in place of a larger core to produce less loss.](image)

Two trends are analyzed in Fig. 2.9.

1. For each core size there is a frequency, $f_{optimal}$, that optimizes core and eddy-current loss, as seen in Fig. 2.10. Approaching $f_{optimal}$ from 40 kHz, a smaller ΔB is attained and a lower area of the $BH$ curve is traversed, resulting in a lower core loss. However, increasing past $f_{optimal}$, the core loss increases as the $B$ polarity is inverted more frequently.

2. Changing from one core size to the next larger size results in an efficiency improvement, as shown by the black arrows in Fig. 2.11. As a trend, the use of smaller cores require the converter and transformer to operate in conditions that lead to higher losses.
Figure 2.10: Calculated core and eddy-current loss for ETD59 versus transformer $\Delta B$ and converter $f_s$.

Figure 2.11: Calculated core and eddy-current loss for ETD54, ETD49, ETD44 versus transformer $\Delta B$ and converter $f_s$.

The total converter loss at rated power over the design space is shown in Fig. 2.12.
Figure 2.12: Calculated total converter loss versus transformer $\Delta B$ and converter $f_s$.

A slice of Fig. 2.12 is taken at the target converter loss, of 198 W to find the smallest feasible transformer core, as shown in Fig. 2.13.

Figure 2.13: Calculated feasible converter and transformer operating points for a target total converter loss of 198 W. The operating points that can sustain the smallest feasible core are outlined in red.

The smallest feasible transformer core in Fig. 2.13 is the ETD49 core. To use the ETD49 core, a switching frequency higher than 75 kHz and a $\Delta B$ from 0.2 T to 0.38 T is required, as shown in Fig. 2.13. Many designs are possible with the use of an ETD49 core, including a $\Delta B$ of 0.325 T and $f_s$ of 115 kHz. Component availability, noise, and PCB design can factor into choosing a particular design. The chosen transformer specifications,
in addition to modifications made in Section 2.4 are summarized in Table 2.4. The small margin between the $\triangle B$ and $B_{sat}$ poses a greater risk of saturation due to inherent non-idealities associated with the DAB full-bridges as explained in Section 2.4 and Section 3.2. A solution to this problem is proposed in Chapter 4.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Converter Switching Frequency</td>
<td>125</td>
<td>kHz</td>
</tr>
<tr>
<td>Power</td>
<td>6.6</td>
<td>kW</td>
</tr>
<tr>
<td>Turns ratio</td>
<td>1:1.08 $\approx$ 11.5:12.5</td>
<td></td>
</tr>
<tr>
<td>$\triangle B$</td>
<td>0.37</td>
<td>T</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Transformer physical parameters</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Core height</td>
<td>49.8</td>
<td>mm</td>
</tr>
<tr>
<td>Core width</td>
<td>48.5</td>
<td>mm</td>
</tr>
<tr>
<td>Core depth</td>
<td>16.7</td>
<td>mm</td>
</tr>
<tr>
<td>Volume (including windings)</td>
<td>80</td>
<td>cm$^3$</td>
</tr>
<tr>
<td>Effective volume (including chill-pot)</td>
<td>95</td>
<td>cm$^3$</td>
</tr>
<tr>
<td>Weight</td>
<td>124</td>
<td>g</td>
</tr>
<tr>
<td>Shape</td>
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</tr>
<tr>
<td>Material</td>
<td>N97</td>
<td></td>
</tr>
</tbody>
</table>

### 2.4 Obstacles to Optimization

An increase in DAB $f_s$ results in smaller magnetic elements. Unlike resonant converters, a high switching frequency leads to substantially higher switching losses due to the hard turn-off of the switches. Furthermore, isolated converters without series capacitors such as the DAB, cannot prevent the flow of dc current through transformer terminals. A net dc current introduces an offset in the transformer $B$, $B_{dc}$, as shown in Fig. 2.14(b).

Safety margin is defined as the difference between a core $\triangle B$ and saturation flux density, $B_{sat}$, as shown in Fig. 2.14(a).
Figure 2.14: The $BH$ curve of a typical ferrite (a) without $B_{dc}$ offset, and (b) with $B_{dc}$ offset. The figures include the $\Delta B$ traversed by the converter operation.

This $B_{dc}$ pushes the transformer into saturation under a large enough $\Delta B$, which is dependent on the transformer size, DAB terminal voltages, and converter frequency. High density designs, that incorporate a transformer operating with a high $\Delta B$, thus have a low safety margin. Saturation could either cause large losses or irreversible damage, due to large current spikes that occur from the change in the transformer core properties. To operate with the desired core size, these problems must be addressed. A closer look at the causes and effects of $B_{dc}$ in the transformer are addressed in Chapter 3. along with an analysis of the existing and proposed saturation mitigation solutions. To validate the proposed solution defined in Chapter 4, the transformer was intentionally designed with $\Delta B = 0.37$ T at $f_s = 125$ kHz. This design has a higher risk of saturation because of the low safety margin.

2.5 Chapter Summary

A power loss analysis has been performed on the proposed Power-Hub. Design decisions were made about the choice of Litz wire and core material for the transformer design, in addition to semiconductor device for the power stage design. For a given loss budget, the possible range of operating conditions, including the operating magnetic flux density, $\Delta B$, converter frequency, $f_s$, and core size have been identified. The smallest feasible transformer for 198 W of total converter loss has been selected for the design. The volume and efficiency optimized transformer specifications are presented in Table 2.4. The specified flux density requires the use of a protection algorithm for the transformer
to operate with a small safety margin between $\Delta B$ and $B_{sat}$. The required algorithm is described in Chapter 4.
References


Chapter 3

Transformer Saturation In Dual-Active-Bridge

This chapter models the cause of saturation, and its effects on the $i_{DAB}$ and $v_{2,\text{reflected}}$ waveforms. Additionally, state-of-the-art methods that mitigate saturation are described. An experimental measurement of the $B_{dc}$ in a Power-Hub DAB is performed and the respective safety margins are calculated. The circuit asymmetry caused by the placement of the DAB inductor on one side of the transformer (as shown in Fig. 3.1) is taken into account in the modeling by differentiating the effects of each DAB full-bridge. In this chapter, the full-bridge connected to the battery is denoted, $FB_{batt}$, and the bus connected full-bridge is denoted, $FB_{bus}$. In the Power-Hub DAB converter, the DAB inductor is connected between the transformer and $FB_{bus}$.

![Figure 3.1: DAB converter topology, with the two full-bridges, $FB_{bus}$ and $FB_{batt}$ labeled. $i_{DAB}$ referred to $FB_{bus}$ is labeled $i_{DAB,bus}$ (similar for $i_{DAB,batt}$).](image_url)
3.1 Effects of $B$ Saturation on $i_{DAB}$ and $v_{2,reflected}$

Due to the placement of the DAB inductor between FBbus and the transformer, any voltage difference between the bus and battery falls across the DAB inductor and causes a rise in current. As such, the $B$ waveform of the transformer is defined by FBbatt. Transformer saturation occurs when the core material operates with $|B| > |B_{sat}|$, characterized by a sharp drop in relative magnetic permeability, $\mu_r$, as seen in Fig. 3.2 for $|B_{sat}| = 0.41$ T [1].

![Figure 3.2: Calculated $\mu_r$ from measured $B$ and $H$.](image)

The decrease in voltage reflected across the winding, $v_{2,reflected}$, due to a drop in $\mu_r$ is modeled by

$$v_{2,reflected} = \frac{nA_c\mu_r\mu_0}{l} \frac{d}{dt} \bar{\delta},$$

(3.1)

where

- $A_c$ is the core cross-section area,
- $n$ is the number of winding turns,
- $l$ is the magnetic path length,
- $\bar{\delta}$ is the magneto-motive force contributed by the currents in the windings.

The waveforms of the secondary voltage, $v_2$, its reflection, $v_{2,reflected}$, and the transformer $B$ when the core is not saturated are shown in Fig. 3.3(a). As the $B$ waveform is triangular, the peaks are the first instants where the core may experience saturation. For a transformer designed with $|\Delta B| < |B_{sat}|$, and a non ideal $B$ offset, $\pm B_{dc}$, if $B + B_{dc} > +B_{sat}$, the core is said to saturate positively, while if $B - B_{dc} < -B_{sat}$, the core is said to saturate negatively. During the time intervals when $|B| > |B_{sat}|$, after the saturation thresholds have been reached, the permeability $\mu_r$ drops sharply, and the transformer behaves in an essentially linear manner. The core then returns to normal operation after the $B$ waveforms have been reduced to a level below $|B_{sat}|$. The primary winding current, $i_{DAB}$, responds quickly to the changing transformer $B$ waveform, allowing the current to no longer reflect the $B$ waveform.
the magnitude of $v_{2,\text{reflected}}$ decreases, as shown in Fig. 3.3(b) and Fig. 3.3(c). With $L_{\text{DAB}} \gg L_{\text{leakage}}$, the slope of the $i_{\text{DAB}}$ waveform is given by,

$$\frac{d}{dt} i_{\text{DAB}} = \frac{v_1 - v_{2,\text{reflected}}}{L_{\text{DAB}}}, \quad (3.2)$$

where $m_1 = \frac{d}{dt} i_{\text{DAB}}$ at the end of the positive plateau of $i_{\text{DAB}}$ and $m_2 = -\frac{d}{dt} i_{\text{DAB}}$ at the end of the negative plateau. The change in $v_{2,\text{reflected}}$ given by (3.1) subsequently changes either $m_1$ or $m_2$, as shown in Fig. 3.3 and Fig. 3.4.

Figure 3.3: The $B$ waveform with respect to $v_1$, $v_2$, $v_{2,\text{reflected}}$ and $i_{\text{DAB,batt}}$ when the core is (a) not saturating, (b) saturating positively and (c) saturating negatively. The slope at the end of the positive plateau, and the negative plateau have been labeled $m_1$ and $m_2$ respectively.

Under positive saturation, a change in $m_1$ occurs at the end of the positive $i_{\text{DAB,batt}}$ plateau, coinciding with the positive peak of the $B$ waveform. Under negative saturation, a change in $m_2$ occurs at the end of the negative $i_{\text{DAB,batt}}$ plateau. Analyzing the difference between $m_1$ and $m_2$ given by

$$\Delta m = m_1 - m_2, \quad (3.3)$$

the polarity of saturation can be deduced. The magnitude of $\Delta m$ is approximated by

$$|\Delta m| \approx \frac{1}{R_c} i_M \frac{d}{dt} R_c, \quad (3.4)$$
where

\[ i_M = \frac{R_c}{n^2} \int_{t+\frac{T}{4}}^{t} V_{\text{peak}} dt, \quad (3.5) \]

with \( R_c \) approximately equal to the unsaturated core reluctance. The derivation of (3.4) is given in Appendix C. In Appendix B, \( |\Delta m| \) is approximated to be 3.523 A/\( \mu \)s for the Power-Hub transformer with a peak \( B \) of 0.4 T (Approximations of the \( BH \) curve shape will result in slightly different experimental results). Similarly \( |\Delta m| \approx 0.813 \) A/\( \mu \)s with a peak \( B \) of 0.38 T.

The circuit asymmetry also affects the \( i_{DAB} \) waveform under saturation. The DAB inductor resists the sharp changes in \( i_{DAB} \) that occurs due to saturation. As a result, \( i_{DAB,bus} \) does not have the current spikes seen in \( i_{DAB,batt} \) under saturation, as seen in Fig. 3.4.

### 3.2 Causes of Saturation

In the Dual-Active-Bridge, volt-seconds are applied directly across the transformer and inductor from the two DAB FBs. Due to the lack of dc-blocking capacitors, any net-volt seconds applied by the FBs in one switch cycle are transferred to the magnetic components, particularly the transformer. The application of any non-zero volt-seconds to the transformer results in a dc current, \( I_{dc} \), in the ideally ac link. The net \( I_{dc} \) from each transformer winding results in a \( B \) offset, \( B_{dc} \), in the transformer. Sufficiently large \( B_{dc} \) pushes the transformer into saturation. \( B_{dc} \) and \( I_{dc} \) are related by

\[ B_{dc} = \frac{nI_{dc}}{R_c A_e}, \quad (3.6) \]

where

- \( A_e \) is the core cross-section area,
- and \( n \) is the number of turns in the transformer.

The misapplication of non-zero net volt-seconds within one switching cycle is caused by a duty-cycle offset, \( \Delta D \), applied by a FB. The relation between \( \Delta D \) and \( I_{dc} \) for one FB is given by

\[ I_{dc} = \frac{\Delta D \cdot 2 \cdot V_{\text{in}}}{R_{dc}} \], \quad (3.7)
where the resistance in the FB power-path is given by

$$R_{dc} = R_{trace} + 2 \cdot R_{on} + R_{sense} + R_{L,dab} + R_{winding}, \quad (3.8)$$

as shown in Fig. 3.5. The resistor values from (3.8) are given in Table. 3.1 for the Power-Hub DAB converter,
Table 3.1: Power-Hub DAB Full-Bridge Power-Path Resistances

<table>
<thead>
<tr>
<th>Resistance</th>
<th>Description</th>
<th>Value</th>
<th>Method of Measurement</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{\text{trace}}$</td>
<td>trace resistance of one DAB FB power-path</td>
<td>5 mΩ</td>
<td>PCB modeled in electromagnetic simulation software</td>
</tr>
<tr>
<td>$R_{\text{on}}$</td>
<td>MOSFET on-resistance at the thermal steady-state</td>
<td>90 mΩ</td>
<td>Datasheet [2]</td>
</tr>
<tr>
<td>$R_{\text{L}_{\text{dab}}}$</td>
<td>DAB inductor dc resistance</td>
<td>3.5 mΩ</td>
<td>Measured</td>
</tr>
<tr>
<td>$R_{\text{winding}}$</td>
<td>transformer dc winding resistance</td>
<td>9.77 mΩ</td>
<td>Measured</td>
</tr>
<tr>
<td>$R_{\text{sense}}$</td>
<td>sense resistor</td>
<td>15 mΩ</td>
<td>Datasheet</td>
</tr>
</tbody>
</table>

Figure 3.5: DAB FB showing power-path resistances and inductances.

There are several practical implications to (3.6) and (3.7).

1. As the interface between a high voltage bus and battery, a small $\Delta D$ can result in a large net volt-second applied to the transformer.

2. As none of the DAB transformer terminals have a dc-blocking capacitor, a non-zero $I_{\text{dc}}$ can flow from both non-ideal DAB FBs. The sum of $I_{\text{dc}}$ flowing through both terminals can subsequently be larger than that in each individual terminal.

3. A decrease in $R_{\text{dc}}$ causes an increase in $I_{\text{dc}}$. Therefore, MOSFETs with lower $R_{\text{on}}$ pose a greater risk for transformer saturation.

In order to reduce the net $I_{\text{dc}}$, and subsequent risk of saturation in the DAB transformer, the measures listed in Table 3.2 were considered.
Table 3.2: Parts Selection and PCB Design Measures to Reduce $I_{dc}$ in DAB Transformer

<table>
<thead>
<tr>
<th>Measure</th>
<th>Benefit</th>
<th>Drawback</th>
<th>Action Taken</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Choose MOSFET with high $R_{on}$</strong></td>
<td>Decrease $I_{dc}$</td>
<td>Increase loss</td>
<td>Not taken</td>
</tr>
<tr>
<td><strong>Strategic IC choices</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reduce number of individual ICs</td>
<td>Decrease IC variations due to tolerance and thus decreases $\Delta D$</td>
<td>Difficult procurement</td>
<td>Used isolated dual-gate-driver, and multi-channel digital-isolators</td>
</tr>
<tr>
<td>Dual-Gate-Driver, with low pulse-width-distortion (PWD)</td>
<td>Decrease $\Delta D$ due to greater flexibility to do symmetrical gate drive layouts and low distortion between driving channels.</td>
<td>Increases cost</td>
<td>Used best-in-class, UCC21520 ($PWD_{max}=5$ ns).</td>
</tr>
<tr>
<td><strong>PCB design</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ensure symmetry between all MOSFET driving paths</td>
<td>Decreases PCB asymmetry, and $\Delta D$</td>
<td>Complex PCB design</td>
<td>Symmetric driving layout was used for all MOSFETs</td>
</tr>
<tr>
<td>Design PCB with symmetric heat transfer from MOSFETs to cooling-plate</td>
<td>Decreases MOSFET parameter variation due to temperature differences</td>
<td>Complex PCB design</td>
<td>The power-stage layouts were made exactly symmetrical as seen in Fig. 3.6</td>
</tr>
</tbody>
</table>
3.3 Experimental Measurement of Safety Margin for Power-Hub DAB

An experimental value for $\Delta D$ was calculated from measurements of the implemented Power-Hub DAB. Operating the DAB with a 380 V battery and 410 V bus, the current flowing through both transformer terminals was measured, as shown in Fig. 3.7.

The net $I_{dc}$ in the DAB transformer was measured to be 0.4 A referred to the FB $batt$ connected transformer terminal. The resulting $B_{dc}$ was calculated to be 83.8 mT. The net $\Delta D$ was calculated to be 0.01% which is equivalent to a 0.8 ns offset in the 125 kHz DAB $T_s$. Though 0.8 ns is much less than the maximum PWD of the gate-drivers in the Power-Hub DAB, this offset still results in a large $B_{dc}$ which requires a large safety margin, or a saturation mitigation controller. To implement this safety margin passively, the transformer must either operate at a higher frequency or with a larger core. These solutions operate the converter away from the optimal operating point determined in Section 2.3, or increase the converter volume.
3.4 State-of-the-Art Saturation Prevention and Protection Methods

Both passive and active solutions have been proposed to prevent transformer saturation in the DAB topology.

**Existing Passive Solutions:**

1. In [3] capacitors are used to block dc current from flowing in the transformer windings. These capacitors are large, expensive, and decrease operating life if employed in a 6.6 kW converter.

2. The transformer can also be over designed by using a large enough core or including air gaps to accommodate any net volt-seconds applied by the FBs in a switch cycle without saturating.

**Existing Active Solutions:**

1. In [4] an expensive custom core that redirects flux to a particular winding off the main flux path when the core is saturated is used to detect saturation and take subsequent corrective action.

2. In [5] and [6] the average current entering and leaving each full-bridge of the DAB is measured and $B_{dc}$ along with them are reduced to zero, either through duty-cycle control or current-mode control. The former has a low bandwidth, while both methods require complex and costly sensing circuitry on both full-bridges.
3. In [4] the $B_{dc}$ in the core is measured through the connection and perturbation of an external ferrite loop. This method is complex and costly for mass production, as it requires a reliable and reproducible coupling between the external ferrite and the transformer core.

4. In [7] flux is measured using Hall Effect sensors placed in core air-gaps. The measured $B_{dc}$ is then corrected through the application of appropriate volt-seconds. This method requires the existence of air-gaps in the core which are not ideal in transformer design due to the reduction in magnetizing inductance.

5. In [8] a $B_{dc}$ of zero in the DAB inductor and a low $B_{dc}$ in the DAB transformer is achieved given the presence of zero-voltage-switching (ZVS). This method however, does not eliminate the transformer $B_{dc}$ and requires precise sensing to implement dead-time for ZVS.

3.5 Chapter Summary

The causes of saturation have been investigated and related to a change in slope in the DAB $i_{DAB}$ waveform. $B_{dc}$ has been identified as the uncertain parameter in circuit design that could lead to saturation. A model of the expected $B_{dc}$ for a converter has been presented, in addition to a practical DAB implementation showing its impact. Active and passive methods of reducing the impact of $B_{dc}$ have been presented and analyzed. The Saturation Prevention Algorithm is proposed in Chapter 4 along with its practical implementation and limits.
References


Chapter 4

Saturation Prevention Algorithm

This chapter introduces the Saturation Prevention Algorithm, SPA, and describes its implementation. The sensing, sampling and corrective portions of the SPA are described in separate sections with their individual benefits and drawbacks related to the algorithm as a whole. Cadence simulations of the SPA detection technique using a model of the Power-Hub DAB transformer from Table 2.4 are presented and analyzed.

4.1 SPA Methodology

In Section 3.1 it was shown that the slopes at the end of the positive and negative plateau of the $i_{DAB}$ waveform ($m_1$ and $-m_2$ respectively) indicate transformer saturation, polarity of saturation, and $B$ magnitude. $\Delta m$ represents the converter state of saturation, both in sign and magnitude. The proposed SPA uses $\Delta m$ to detect and mitigate saturation. When $\Delta m$ rises above a predefined threshold of 0.813 $A/\mu s$ (corresponds to $B = 0.38$ T, which is a tuneable factor greater than the transformer $\Delta B$), corrective action is required to prevent saturation. The sign of $\Delta m$ implies the saturating $B$ polarity and the required corrective action. When saturation is detected, the necessary volt-second offset is applied through a $\Delta D$ variation in one full-bridge to mitigate the saturation. Though the effect of saturation on $m_1$ and $m_2$ can be seen on either side of the transformer, the asymmetry of the DAB inductor placement makes the saturation effect less pronounced on the side of the transformer it is on (as described in Section 3.1).

The control is implemented digitally in the Power-Hub control FPGA. As such, the sensed signals must be quantized through a sensing and sampling circuit. Subsequently the control threshold of $|\Delta m| = 0.813$ $A/\mu s$ is represented in the FPGA as $|\Delta m_{FPGA}| =$
20 by the relation,

\[ \Delta m_{FPGA} = 24.2036 \times \Delta m. \] (4.1)

A block diagram of the digital control is given in Fig. 4.1. The sampling and sensing circuitry generates four samples every two switch cycles. These four samples are demultiplexed and paired to generate the two slopes. A filter removes high frequency noise from the two slope measurements by comparing the differences between values in a window. Values with a large difference are omitted and replaced with the adjacent value in the window. The difference in slopes is calculated and used in the hysteretic controller.

Figure 4.1: DAB circuitry and controller logical blocks.

As this algorithm senses the change in core properties due to saturation, it can tolerate a smaller safety margin than passive saturation mitigation techniques. Section 4.4 compares the tolerable safety margin for the SPA against the method of measuring and controlling both transformer terminal currents.
4.2 SPA Slope Measurement and Sampling Circuitry

An ideal slope measurement is approximated digitally through the subtraction of two samples separated by a known, fixed time, $\Delta t$. Two sample pairs of the $i_{DAB}$ waveform are used to generate $m_1$ and $m_2$. $i_{DAB,batt}$ is sensed due to the less pronounced effects of saturation on $i_{DAB,bus}$. The Power-Hub DAB uses one FPGA to control both FBs. This provides an opportunity to sample synchronous to the $i_{DAB}$ waveform. Synchronous sampling provides the following benefits:

1. The slopes $m_1$ and $m_2$ are measured at the same position in every switching cycle. This reduces the need for extensive averaging, increases the control bandwidth and reduces the required transformer saturation flux density safety margin.

2. $\Delta t$ is kept constant from switching cycle to cycle.

The benefits of synchronous sampling and the relative stability of $i_{DAB}$ from cycle to cycle enable the SPA to spread the four necessary measurements for $m_1$ and $m_2$ over two sequential switching cycles. This spread sampling technique requires an analog to digital converter, ADC, with a sample rate inversely proportional to the switching period, and not $\Delta t$, to take the four necessary measurements. Without the proposed sampling technique, an accurate instantaneous slope measurement requires the two sampling points to be taken close to each other with a high-speed ADC. For example, two samples within 100 ns ($\Delta t = 100$ ns) require a costly 10 Ms/s ADC. Furthermore, the use of a FPGA permits $\Delta t$ to be kept constant every cycle. The spread sampling technique is shown in Fig. 4.2, where the two sequential switching cycles are denoted cycle $a$ and cycle $b$.

Cycle $a$ provides the first measurement of each pair, while cycle $b$ provides the second measurement of each pair. The values for $m_1$ and $m_2$ are approximately given by

$$m_1 \approx \frac{i_{DAB,a,1} - i_{DAB,b,1}}{\Delta t}, \quad (4.2)$$

and

$$m_2 \approx \frac{i_{DAB,b,2} - i_{DAB,a,2}}{\Delta t}, \quad (4.3)$$

where the $a, b$ subscript denotes the switching cycle, and the $1, 2$ subscript denotes the sample pair. Under steady-state, (4.2) and (4.3) are equal to $m_1$ and $m_2$, while they are approximations during transient conditions. It is also important to note that $i_{DAB,a,1}$ and $i_{DAB,b,1}$ are separated by $T_s + \Delta t$, and $i_{DAB,a,2}$ and $i_{DAB,b,2}$ are also separated by $T_s + \Delta t$, where $T_s$ denotes the switching period. The SPA sampling technique uses the
Figure 4.2: The samples over the two switching cycles, a and b, are marked in red, along (a) the positive plateau, and (b) the negative plateau of the $i_{DAB}$ waveform. $\Delta i_{DAB}$ represents the change in current induced by a change in phase-shift. With the proposed scheme, $m_1$ is calculated using $i_{DAB,a,1}$ and $i_{DAB,b,1}$, while $m_2$ is calculated using $i_{DAB,a,2}$ and $i_{DAB,b,2}$.

$i_{DAB,b,1}$ and $i_{DAB,b,2}$ rather than taking measurements $\Delta t$ after the $i_{DAB,a,1}$ and $i_{DAB,a,2}$, as shown in Fig. 4.2.

Despite changes in $t_{ps}$, between switching cycles (which results in a change of $\Delta i_{DAB}$, as seen in Fig. 4.2), the effect of $\Delta i_{DAB}$ on $m_1$ and $m_2$ can be eliminated in the calculation of $\Delta m$ as shown by,

$$\Delta m = m_1 - m_2 = \frac{i_{DAB,a,1} - (i_{DAB,b,1} + \Delta i_{DAB})}{\Delta t} - \frac{(i_{DAB,b,2} - \Delta i_{DAB}) - i_{DAB,a,2}}{\Delta t} = \frac{i_{DAB,a,1} - i_{DAB,b,1}}{\Delta t} - \frac{i_{DAB,b,2} - i_{DAB,a,2}}{\Delta t}$$ (4.4)

Furthermore, with $L_{DAB}$ as an external inductor and thus fixed, equation. 3.2 shows that $\frac{d}{dt}i_{DAB}$ only fluctuates under a change in either $v_1$ or $v_2$, reflected. As these voltages have a low magnitude of change over two switching cycles, the slopes, $m_1$ and $m_2$, remain
equal when the transformer is not in saturation. The implementation of the sensing and sampling circuitry at the base of the battery full-bridge requires the negation of one of the approximated slopes for the controller to operate with the rectified signal.

### 4.3 SPA Sensing Circuitry

Hall-effect sensors are not used due to the high bandwidth requirement of slope measurement. Alternatively, two sense-resistor-based options are considered:

1. A differential amplifier and ADC that sense and sample the voltage across a sense resistor placed in the ac-link.

2. A differential amplifier, and ADC that sense and sample the voltage across a sense resistor placed on the return path of FB\textsubscript{batt}.

![Figure 4.3: \(v\text{\_sense}\) seen across the sense resistor placed on return path of FB\textsubscript{batt} is shown in relation to \(i\text{\_batt}\) (as defined in Fig. 1.5) and \(i\text{\_DAB}\). Commutation instances have been labeled. Voltage oscillation due to the high \(\frac{d}{dt} i\) across the power-path inductance is encircled.](image)

Both options are less costly than the use of a hall-effect sensor. The sense resistor was placed on the return path of the FB due to the high common-mode voltage required from
the differential amplifier if the former option was implemented. The low common-mode voltage of the latter option enables the use of a high-bandwidth differential amplifier, as shown in Fig. 4.1. The sensed voltage of the latter option is proportional to a commutated $i_{DAB}$ waveform, as shown in Fig. 4.3.

High voltage oscillations are experienced at the commutation points due to the sharp change in current across the power-path parasitic inductance. The use of low inductance sense resistors and optimal power-path layout, ensure the commutation oscillations subside before the start of the next commutation period. With the oscillations decaying prior to the start of the next commutation, true samples are taken at the end of each positive and negative plateau.

4.4 SPA Safety Margin Tolerance

In the averaged transformer winding current method described in Section 3.4, the controller measures the mid-point of each $i_{DAB}$ plateau and provides the needed correction in the following switch-cycle. These measurements are quantized by the ADC. This quantization presents a minimum value of $I_{dc}$, $I_{dc,min}$, and subsequent minimum $B_{dc}$, $B_{dc,min}$, that can be sensed. This $B_{dc,min}$ is the minimum safety margin that can be tolerated by the controller for safe operation. Using a 12 bit, 1Ms/s serial interface ADC, 15mΩ sense resistor, and 200MHz differential amplifier, $I_{dc,min}=0.0206579$ A as given by

$$
\Delta I_{dc,min} = \frac{\Delta V_{quantized}}{15 \text{ m}\Omega} \times \text{Differential-Amplifier-Gain},
$$

(4.5)

where

- $\Delta V_{quantized} = 0.806$ mV,
- and the differential amplifier gain is 2.6.

The subsequent $B_{dc,min}=4$ mT as calculated by

$$
\Delta B_{dc,min} = \frac{n\Delta I_{dc,min}}{R_cA_e},
$$

(4.6)

where for the Power-Hub DAB transformer,

- the unsaturated core reluctance, $R_c = 256410 \text{ H}^{-1}$,
- and $A_e = 211 \text{ mm}^3$. 

A practical implementation of this controller requires a larger tolerance, as the averaging required to implement this system slows the controller response while material tolerances require additional margin.

Compared to the averaged current method, the value of $I_{dc,min}$ and $B_{dc,min}$ remain the same for the SPA as it uses the same circuit. Given a sufficiently large $\Delta t$, the SPA can measure a change in current greater than the ADC quantization due to the change in the slope of $i_{DAB}$ that occurs under saturation. As $\Delta m = 0.813 \, \text{A/µs}$ when $B = 0.38 \, \text{T}$, and assuming $\Delta t = 100 \, \text{ns}$, the slope approximation defined in Section 4.2 represents this slope as a difference in current of 0.0813 A. Therefore, the proposed SPA is able to detect when the transformer is at the cusp of saturation without the impact of ADC quantization as $\Delta I_{dc,min} \ll 0.0813 \, \text{A}$. This shows that the SPA requires a lower tolerance of safety margin for safe operation than the method of averaged winding currents.

### 4.5 SPA Corrective Action

Assuming $\Delta B \ll B_{sat}$, the proposed algorithm cannot measure the state, $B$, while $(B_{dc} + \Delta B) < |B_{sat}|$ as the core is not saturated and $\Delta m = 0$. In N97 material, little change occurs in the linearity of the $BH$ curve between the $B$ bounds of $\pm 0.32 \, \text{T}$. The lack of change in the slopes of $i_{DAB}$ can be seen in Fig. 4.4.

![Figure 4.4: Cadence simulation showing that no visible change in $i_{DAB}$ occurs until $(\Delta B + B_{dc}) > |B_{sat}|$.](image)

Figure 4.4: Cadence simulation showing that no visible change in $i_{DAB}$ occurs until $(\Delta B + B_{dc}) > |B_{sat}|$.

As measurements about the controlled state $B$, are not available for the entire set, two general control solutions can be achieved:

1. Using a PI controller, peak $B$ can be kept at one of the bounds of saturation. In practice, $B_{sat}$ is a point within the non-linear region of a ferrite material $BH$ curve.
\( \Delta m \) is not representative of the core \( B \) in the linear region of the \( BH \) curve. For multiple \( B \) values in the linear region of the \( BH \) curve, \( \Delta m = 0 \). Therefore, a non-zero setpoint must be chosen such that the PI controller can stabilize within one of the non-linear regions (where \( \Delta m \) is more closely representative of the core \( B \)).

2. Using a hysteretic controller, \( B_{dc} \) can be varied such that \( +B_{sat} > B > -B_{sat} \).

![Figure 4.5: (a) \( B \) and \( i_{DAB} \) after a step in \( \varphi \) of 0-0.314 rad, with SPA detection and a core operating with \( \Delta B \) of 0.34 T. (b) \( B \) and \( i_{DAB} \) after a step in \( \varphi \) of 0-0.314 rad, with SPA detection and a core operating with \( \Delta B \) of 0.2 T.]

In this thesis, a hysteretic controller with two possible \( \Delta D \) outputs is used due to its low Verilog complexity, and low FPGA demands. Once saturation is detected based on a set
\( \Delta m_{FPGA} \) threshold, the SPA applies a \( \Delta D \) to the pulse-width modulation of \( FB_{sat} \) to create the necessary corrective net volt-seconds, \( I_{dc} \) and \( B_{dc} \) in the transformer. With only two possible corrective actions, the transformer \( B \) oscillates between the saturation bounds, \( \pm B_{sat} \), as seen in Fig. 4.6. The frequency of oscillation depends on the \( \Delta B \) of the converter, and the controller bandwidth. Furthermore, transients can also impact this oscillation.

![Figure 4.6: Oscillations in the \( B \) waveform occur depending on how often \( B_{sat} \) is reached.](image)

Two different transformer designs, one with \( \Delta B = 0.34 \) T and the other with \( \Delta B = 0.2 \) T are simulated in Cadence with a fixed step controller using the SPA detection technique. Accurate transistor models are used in addition to a model of the transformer \( BH \) curve (including saturation but no core loss). A fixed offset is applied to a FB and the \( B \) and \( i_{DAB} \) waveforms are shown in Fig. 4.5.

As expected, the simulation shows that a controller using a constant correction in conjunction with the SPA detection causes the \( B \) to slowly oscillate between the bounds of saturation, with an average \( B \) of 0 T. With a \( \Delta B \) of 0.2 T, the controller successfully keeps \( |B| < |B_{sat}| \), as shown in Fig. 4.5(b). With a larger \( \Delta B \), Fig. 4.5(a) shows that more decisions are required from the controller and thus higher frequency oscillations occur due to the more frequent occurrence of saturation.

### 4.6 Start-Up Thermal Considerations

To prevent thermal shock as stated in Section 2.1.3, two soft-starting schemes were used in the charger. The duty-cycle was slowly increased to the desired 50% to prevent the core loss from heating the core rapidly. Given the thermal capacitance of the transformer, the maximum rate of temperature rise occurs from a low initial temperature. A conservative estimate for the ramp-up time of the duty-cycle soft-start scheme is made from experimental measurements of the transformer from a state of rest (the temperature
of the liquid chill-plate). The duty-cycle is applied symmetrically during this period as shown in Fig. 4.7.

![Diagram of B waveform](image)

Figure 4.7: The $B$ waveform is plotted with respect to the applied duty-cycle soft-start.

After 50% duty-cycle is achieved, the second soft-start technique increases the phase-shift and subsequent winding temperature.

### 4.7 Chapter Summary

The proposed SPA detects transformer saturation through the difference of slopes at the end of the positive and negative $i_{DAB}$ plateaus (particularly of $i_{DAB,batt}$). It applies a $\Delta D$ through hysteretic control of a DAB full-bridge to mitigate saturation. The slope measurements are performed using an ADC that operates at a sample rate twice that of the switching frequency without the use of expensive hall-effect sensors, thereby ensuring a low cost implementation. The validity of the SPA detection technique is shown through Cadence simulations using a model of the Power-Hub DAB transformer. A soft-start method was also presented to meet thermal considerations outlined in Section. 2.1.3.
Chapter 5

Experimental Results

This chapter describes the Power-Hub DAB prototype, and its specifications. Active air cooling is used for the MOSFETs and magnetic components in this Power-Hub revision. The SPA functionality is demonstrated through experimental measurements of the prototype $i_{DAB}$, transformer $B$ and controller commands. Experimental measurements are also shown with and without the SPA. The converter efficiency plot is presented with the SPA, including comparisons to existing DAB and resonant converters designed for on-board EV charging.

Figure 5.1: 6.6 kW Power-Hub Dual Active Bridge converter prototype.
Table 5.1: DAB Converter Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bus Voltage</td>
<td>380-480</td>
<td>Vdc</td>
</tr>
<tr>
<td>Battery Voltage</td>
<td>320-450</td>
<td>Vdc</td>
</tr>
<tr>
<td>Peak Power</td>
<td>6.6</td>
<td>kW</td>
</tr>
<tr>
<td>Transformer Core</td>
<td>ETD49</td>
<td></td>
</tr>
<tr>
<td>Material</td>
<td>N97</td>
<td>cm³</td>
</tr>
<tr>
<td>Volume</td>
<td>80</td>
<td></td>
</tr>
<tr>
<td>Turns ratio</td>
<td>1:1.08</td>
<td></td>
</tr>
<tr>
<td>Switching frequency</td>
<td>125</td>
<td>kHz</td>
</tr>
<tr>
<td>DAB inductor</td>
<td>10</td>
<td>µH</td>
</tr>
<tr>
<td>(between FBbus and transformer)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MOSFET</td>
<td>C3M0065090J</td>
<td></td>
</tr>
<tr>
<td>Controller</td>
<td>FPGA</td>
<td></td>
</tr>
<tr>
<td>ADC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sample Rate</td>
<td>1</td>
<td>Ms/s</td>
</tr>
<tr>
<td>Bits</td>
<td>12</td>
<td>bits</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>3.3</td>
<td>V</td>
</tr>
<tr>
<td>Operational Amplifier</td>
<td>10</td>
<td>MHz</td>
</tr>
<tr>
<td>Differential Amplifier</td>
<td>200</td>
<td>MHz</td>
</tr>
<tr>
<td>Gate Driver</td>
<td>Isolated Dual Gate Driver</td>
<td></td>
</tr>
<tr>
<td>Modes of operation</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Constant Current, Constant Voltage</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The DAB converter prototype shown in Fig. 5.1 is designed with the specifications written in Table 5.1. It is operated with a biased e-load at the battery terminal to simulate a battery connection. Additionally, active air cooling is applied to the cooling-plate below the PCB. The MOSFETs are thermally connected to the PCB through thermal vias, pad and paste, which are chosen to meet the required electrical insulation and thermal conductivity.
5.2 SPA Experimental Results

Experiments using of the Saturation Prevention Algorithm in the Power-Hub DAB, are conducted to validate

1. saturation detection,

2. DAB dynamic response,

3. soft-start procedure,

4. and continuous operation.

The converter efficiency is also measured at rated power under long-duration operation.

5.2.1 Saturation Detection

The DAB is operated with a $\Delta B$ of $\pm 0.37$ T at low power. The SPA is only used for saturation detection with no corrective actions. To test the controller response, a $\Delta D$ of $+0.072\%$ and $-0.072\%$ are applied from FB$_{bus}$ at two different instances in time to cause positive and negative saturation respectively, as shown in Fig. 5.2.

Compared to positive saturation, the $i_{DAB}$ waveform is less impacted by negative saturation as seen in Fig. 5.2(a). Despite the asymmetric impact, the SPA is able to detect both forms of saturation, as seen in Fig. 5.2(b). Measurements of the 12-bit samples of $i_{DAB}$ used to calculate $m_1$ and $m_2$ in the Power-Hub FPGA controller are presented in Fig. 5.2(b). With a positive $\Delta D$ and saturation, the measurements $i_{DAB,a,1}$ and $i_{DAB,b,1}$ diverge due to the increasing slope, $m_1$, as seen in Fig. 5.2(b). Similar divergence occurs for $i_{DAB,a,2}$ and $i_{DAB,b,2}$, for a negative $\Delta D$ and saturation. The $\Delta m_{FPGA}$ is calculated from these samples in the FPGA and is shown in Fig. 5.2(c). The SPA is able to determine that saturation caused by a $\Delta D$ of $+0.072\%$ is greater than $-0.072\%$ and requires corrective action as $|\Delta m_{FPGA}| > 20$ which implies that $B > 0.38$ T, as shown in Fig. 5.2(c).
Figure 5.2: (a) Measured Power-Hub DAB $i_{DAB}$ waveform with a $\pm 0.072\%$ duty cycle offset applied. (b) Measured 12-bit samples of the $i_{DAB,a,1}$, $i_{DAB,b,1}$ measurement pair, and the $i_{DAB,a,2}$, $i_{DAB,b,2}$ pair show the FPGA perception of the $m_1$ and $m_2$ slopes under saturation. (c) Measured 12-bit value of the $\Delta m_{FPGA}$ calculated in the FPGA.
5.2.2 DAB Dynamic Response to SPA Activation

The dynamic response of the DAB to the SPA activation is investigated. Prior to the SPA activation, large changes in slope, which are presented as spikes in current, are seen in the measured waveform of \( i_{DAB,batt} \) due to saturation, as seen in Fig. 5.3(a). To prevent damage during this time period, the experiment was conducted at approximately 50\% rated power (\( \sim 2.25 \) kW).

![Figure 5.3: Measured \( i_{DAB,bus} \) and \( i_{DAB,batt} \) waveforms. (a) Measured \( i_{DAB,batt} \) waveform presents large changes in slope (seen as large current spikes). \( i_{DAB,bus} \) is more immune to changes in slope. (b) Measured \( i_{DAB,batt} \) waveform with SPA activation. The DAB operation remains stable and does not present signs of saturation.](image)

The asymmetric DAB inductor placement causes the \( i_{DAB, bus} \) to be immune to large slope changes, as discussed in Section 3.1. After SPA activation, the spikes in \( i_{DAB} \) are
greatly reduced and saturation is mitigated, as seen in Fig. 5.3(b). The controller remains stable during the SPA enable transition.

5.2.3 Continuous Operation

To verify controller stability, the Power-Hub DAB is operated for 40 seconds at peak power. The data presented in this section is from 5.8 kW operation as 6.6 kW operation results in noise that impacts the data logging tools used to measure the $i_{DAB}$ samples represented in 12-bits. The $i_{DAB}$ current flowing on both sides of the transformer, and the $i_{batt}$ returning to the battery are measured. Transformer $B$ is also measured through the use of a wire loop around the transformer core, and an integrator that operates with sufficient bandwidth to track the $B$ oscillations due to the hysteretic control.

**Converter Waveforms**

As expected, the soft-start procedure discussed in Section 4.6 is able to increase the $\Delta B$ in the transformer at a constant rate to the steady-state operating condition, as seen in Fig. 5.4. This reduces the rate of temperature rise due to core loss.

![Converter Waveforms](image)

Figure 5.4: Measured steady-state operation of DAB with SPA at 5.8 kW. The $i_{DAB}$ in both transformer terminals, $B$ waveform of the transformer and the $i_{batt}$ are plotted. Saturation is shown to be mitigated.

As expected, $B$ oscillations due to the hysteretic control occur with a small amplitude ($\approx 30$ mT at $\approx 900$ Hz), as the steady-state $\Delta B$ of the transformer is very close to $B_{sat}$. Saturation is deemed to be controlled as there are no large spikes in the $i_{DAB,batt}$ waveform, as seen in Fig. 5.4. A closer look at the $i_{DAB}$ and $B$ waveforms in Fig. 5.5
reveal that the $\Delta D$ of the hysteretic controller is applied accurately. With the application of a constant $\Delta D$, a constant rise in $B_{dc}$ occurs until the bound of saturation is reached. The positive bound of saturation can be identified by the increase in current spikes on the positive $i_{DAB}$ plateau. Once detected, the controller applies an opposing $\Delta D$ to mitigate the saturation, decrease the $B_{dc}$, and continue the process.

![B oscillations due to hysteretic controller](image)

Figure 5.5: Measured $i_{DAB}$ and $B$ waveforms showing hysteretic controller oscillation.

**FPGA Control Parameter Values**

To validate the control response further, the 4 current samples taken by the ADC and represented in the FPGA during the 5.8 kW converter operation are measured and shown in Fig. 5.6
Figure 5.6: Measured 12-bit representations of the 4 required ADC samples. They were taken every two cycles during the 5.8 kW operation. \( i_{DAB,a,1-FPGA} \) and \( i_{DAB,b,1-FPGA} \) are the pairs used to calculate \( m_1 \), and \( i_{DAB,a,2-FPGA} \) and \( i_{DAB,b,2-FPGA} \) are used to calculate \( m_2 \).

The 2 slopes, \( m_1 \) and \( m_2 \), (Calculated in the FPGA from the 4 required ADC samples) are shown in Fig. 5.7. It is noted that the slopes track each other with the implementation of the SPA.

Figure 5.7: Measured FPGA value of the slopes, \( m_1 \) and \( m_2 \), recorded during the DAB 5.8 kW operation. \( m_1 \) and \( m_2 \) are shown to track one another.

The error, \( \Delta m_{FPGA} \) between the two slopes, \( m_1 \) and \( m_2 \), is shown in Fig. 5.8. With the SPA activated, the average error is stable and small. The spikes in error are a result of the hysteretic controller and the system inertia that needs to be reversed.
Chapter 5. Experimental Results

5.3 Converter Efficiency with SPA

The efficiency is measured over 40 seconds operations of the Power-Hub DAB. To achieve high accuracy, one multimeter is used to perform the necessary voltage and current measurements. With 3.3mΩ shunt resistors placed at the input and output of the converter, the Agilent 34401A multimeter is used to measure current.

To simulate the operating conditions of an on-board EV charger, the experiments are done with a bus and battery voltage ratio equal to that expected in the Power-Hub operation. To minimize conduction losses by ensuring flat $i_{DAB}$ plateaus, the bus terminal voltage tracks the fixed transformer turns ratio, for a battery voltage range of 350-450 V. For a battery voltage of 320 V, the bus is operated with 380 V, which is the lowest operable output voltage of the first stage inverter.

The converter efficiency at a 6.6 kW battery charge rate is similar to the expected value of 97% with a peak value of 96.8%, as shown in the measured efficiency curves of Fig. 5.9. The lower efficiency can be attributed to the higher $\Delta B$ operating point, chosen in Section 2.4 and the lack of a sophisticated transformer thermal management system (the transformer was not operated close to the optimal core loss temperature). The dc symmetry of the DAB ensures that the efficiency curves for converter discharge and charge are similar, if not identical.
Figure 5.9: Measured Power-Hub DAB efficiency under expected battery and bus voltage ratios. The battery and bus voltage ratios are expressed in the legend as $V_{\text{batt}}/V_{\text{bus}}$.

5.4 Benchmark Comparison

A comparison of the prototype DAB with comparable bi-directional converters is given in Table 5.2.

Table 5.2: DAB Benchmark Comparisons (All transformer volumes exclude required cooling system)

<table>
<thead>
<tr>
<th>Comparable</th>
<th>This Work: Power-Hub DAB 125kHz 6.6kW DAB</th>
<th>Comparison 1: [1] 120kHz 3.3kW DAB</th>
<th>Comparison 2: [2] 500kHz 6.6kW CLLC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transformer Volume</td>
<td>80 cm$^3$</td>
<td>170 cm$^3$</td>
<td>60 cm$^3$</td>
</tr>
<tr>
<td>Peak efficiency</td>
<td>96.8%</td>
<td>96.3%</td>
<td>97.8%</td>
</tr>
<tr>
<td>Switching device</td>
<td>SiC C3M0065090J, 65 mΩ</td>
<td>Si FCH76N60NF, 28 mΩ</td>
<td>GaN GS66516T, 25 mΩ</td>
</tr>
</tbody>
</table>
When compared against the GaN resonant converter of [2], the proposed transformer is relatively similar in volume yet operates at a much lower frequency, with cheaper SiC devices. Lower frequency leads to lower implementation costs. Furthermore, compared to [1], the Power-Hub DAB transformer operates at twice the power, relatively equal frequency, with half of the volume.

5.5 Chapter Summary

Experimental results with an inactive SPA are shown to cause large changes in slope and subsequently, large damaging current spikes. With an active SPA, saturation is controlled at a rated power of 6.6 kW. \( B \) waveform measurements of the transformer, show the expected performance of the hysteretic controller and the duty-cycle soft-start. Under the soft-start process, the transformer core \( \Delta B \) is increased at a slow rate to limit the rate of temperature rise. Due to the hysteretic controller, \( B \) is kept between the saturation bounds, as seen in the \( B \) and \( i_{DAB} \) measurements. Measurements of FPGA values representing the slopes at the positive and negative end of the \( i_{DAB} \) plateau confirm accurate saturation detection and correction.
References

vz modulation of single-phase single-stage bidirectional dab ac-dc converters,” IEEE 

Bandgap Device-Based Bidirectional On-Board Charger,” IEEE Journal of Emerging 
Chapter 6

Conclusions

6.1 Thesis Outcomes and Contributions

A Saturation Prevention Algorithm, SPA, for a Dual-Active-Bridge, DAB, converter has been presented in this work. The case for transformers operating close to their bounds of saturation is demonstrated. For the same loss, the smallest feasible transformer often needs to operate with a high $\Delta B$ in a converter with a high switching frequency. The lower safety margin that is caused by a high $\Delta B$ increases the risk of saturation and requires an active saturation mitigation solution.

The proposed SPA utilizes slope measurements to detect saturation, infer the core $B$ and take the necessary corrective action. The SPA is self-referenced and thus is not impacted by variations in the converter operating state. Compared to the prominent solution that controls the average current in both bridges, saturation detection from slope differences has a faster response, requires a lower safety margin, allows greater core density and lower cost. The SPA is demonstrated at rated power on a 6.6kW Power-Hub DAB. Efficiency results similar to the modeled values are presented in addition to benchmark comparisons and control validation. The primary contributions of this thesis are:

1. The demonstration of a reliable, low cost method to perform on-line slope measurement of the 125kHz trapezoidal transformer current in a 6.6kW DAB. The required sample rate is low, with approximately twice the converter switching frequency.

2. The integration of saturation detection into the power regulation circuitry of the DAB.

3. A SPA that enables transformer operation at the bounds of saturation and volume...
reduction.

4. A mathematical model representing the difference in slopes at the end of the positive and negative plateaus of the transformer current in a DAB due to saturation.

6.2 Future Work

Future work that can extend this thesis are presented below:

1. The use of a non-hysteretic controller to remove the $B$ oscillations shown Section 4.5 can be explored. The removal of $B$ oscillations decreases conduction loss and improves efficiency to a small degree (at 5.8 kW, the periodic action of the controller superimposes a 3 A, 900 Hz waveform on the steady state $i_{DAB}$). A lower frequency of oscillation will also remove the noise attributed to the transformer and controller from the human audible range.

2. A linearization of the controller around a fixed set-point can be derived to integrate this controller into larger control models. The fixed set-point can be chosen based on a particular converter loss optimization.

3. The effects of temperature and material tolerance on the shape of the $BH$ curve and subsequently the controller performance can be studied. This defines the generality of the proposed control approach.

4. The steady-state operation of the Power-Hub DAB and inverter in a closed environment with a liquid cooling-plate can be tested and characterized. This will validate the Power-Hub DAB and SPA at a fixed temperature near the optimal core loss temperature, as designed in the context of the Power-Hub on-board charger.
Appendices
Appendix A

MOSFET Thermal Analysis

Assuming an expected operating temperature of 70 °C, at a frequency between 50-150 kHz, the estimated losses per device was given by,

\[ P_{\text{perdevice}} = P_{\text{conduction}} + P_{\text{turn-off}} + P_{BD,\text{conduction}} = 13.136 - 17.136 \text{W}, \quad (A.1) \]

where

\[ P_{\text{conduction}} = R_{ds,\text{on}} I_{\text{conduction,RMS}} \frac{t_{\text{on}}}{T_{\text{sw}}} = 9.67 \text{ W}, \quad (A.2) \]

\[ P_{\text{turn-off}} = 40 \mu J \cdot f_{\text{sw}} = 2 - 6 \text{ W}, \quad (A.3) \]

\[ P_{BD,\text{conduction}} \] is the conduction loss of the MOSFET body-diode and

\[ P_{BD,\text{conduction}} = V_{\text{drive}} I_{\text{conduction,RMS}} t_{\text{dead-time}} f_{\text{sw}} = 1.466 \text{W}, \quad (A.4) \]

with,

- \( I_{\text{conduction,RMS}} = 14.66 \text{ A} \) based on a 6.6 kW battery charge at 450 V battery voltage
- \( R_{ds,\text{on}} = 90 \text{ mΩ} \)
- \( \frac{t_{\text{on}}}{T_{\text{sw}}} = \frac{1}{2} \)
- \( V_{\text{drive}} = 12 \text{ V} \)
- \( Q_{\text{drive}} = 30 \text{ nC} \)
Appendix A. MOSFET Thermal Analysis

- \( V_{\text{diode}} = 0.7 \) V
- \( t_{\text{deadtime}} = 200 \) ns

Through experimental measurements, the thermal resistance of the thermal vias employed in the proposed DAB PCB was measured to be 0.6 °C/W. The thermal circuit shown in Fig. A.1 was used to calculate the resulting semiconductor junction temperature, based on the device-to-case thermal resistance, \( R_{\theta,\text{junction,case}} \) from the datasheet [1], and the measured case-to-chill-plate thermal resistance, \( R_{\theta,\text{case,chill-plate}} \) of 0.6 °C/W. As the model predicts, a junction temperature close to the value assumed originally, the choice of semiconductor was deemed feasible.

![Thermal circuit](image)

Figure A.1: Thermal circuit representing the PCB and chill-plate connection to the semiconductor device. A chill-plate temperature of 40 °C was assumed.
Appendix B

Saturating $i_{DAB}$ Slope Calculation

The value of $\Delta m$ when $B=0.4$ T has been calculated below.

$$\frac{dR}{dt} = \frac{l}{A \mu_o} (-1) \mu_r^{-2} \frac{d\mu_r}{dt} + \frac{l}{\mu_o \mu_r} (-1) A^{-2} \frac{dA}{dt} + \frac{dl}{dt} \frac{l}{\mu_o \mu_r} A,$$

(B.1)

where the change in $l$ and $A$ due to saturation are neglected as saturation is not entered. (B.1) is simplified to,

$$\frac{dR}{dt} = \frac{l}{A \mu_o} (-1) \mu_r^{-2} \frac{d\mu_r}{dt}.$$

(B.2)

At $B = 0.4$ T the value of the variables in equation (B.2) are given by

$\frac{d\mu_r}{dt} = -2.85 \times 10^9$,

$\mu_r^{-2} = 386.879 \times 10^{-9}$,

$A = 211 \times 10^{-6}$ m$^2$,

$l = 114 \times 10^{-3}$ m,

$n^2 = 121$,

$R|_{B=0.4T} = \frac{l}{\mu_r \mu_o A} = 267424$ H$^{-1}$,

$i_M \approx 1.989$ A.

Given the above definitions and

$$|\Delta m| = \frac{1}{R_c} i_M \frac{dR}{dt} R_c,$$

(B.3)

it can be calculated that,

$|\Delta m| = 3523007.25$ A/s

or
Appendix B. Saturating $i_{DAB}$ Slope Calculation

$|\Delta m| = 3.523 \text{ A/}\mu\text{s}$
Appendix C

Saturating $i_{DAB}$ Slope Equation Derivation

The derivation for the expected current slope difference at a particular $B$ value is given in this appendix. Due to the negative feedback of a series DAB inductor, a changing $i_{DAB}$ slope is only be seen in the plateau of the current flowing through the transformer terminal without a connected inductor. The following variables are used in the derivation.

- $v_{batt}$ is the voltage applied by $FB_{batt}$ to the ac link.
- $i_{DAB,FB_{batt}}$ is the current in the transformer terminal connected to $FB_{batt}$.
- $i_{DAB,FB_{bus}}$ is the current in the transformer terminal connected to $FB_{bus}$.
- $R_c$ is the core reluctance.
- $i_M$ is the transformer magnetizing current.
- $n$ is the number of turns in the transformer winding. The transformer turns ratio is assumed to be unity in this derivation.

As the inductor is placed in between $FB_{bus}$ and the transformer, the voltage applied by $FB_{batt}$, determines the $B$ of the transformer as seen in

$$v_{batt} = n \frac{d}{dt} \left( n i_{DAB,FB_{batt}} - n i_{DAB,FB_{bus}} \right)$$

$$= n^2 \frac{d}{dt} \left( i_{DAB,FB_{batt}} - i_{DAB,FB_{bus}} \right) + n^2 \left( i_{DAB,FB_{batt}} - i_{DAB,FB_{bus}} \right) \frac{d}{dt} \frac{1}{R_c}$$

$$= n^2 \frac{d}{dt} \left( i_{DAB,FB_{batt}} \right) - n^2 \frac{d}{dt} \left( i_{DAB,FB_{bus}} \right) - \frac{n^2 i_M}{R_c} \frac{d}{dt} R_c. \quad (C.1)$$
APPENDIX C. SATURATING $i_{DAB}$ SLOPE EQUATION DERIVATION

The derivatives expressed above are calculated at the plateaus of the current waveforms. Therefore, each current can be expressed in terms of a plateau and a saturation component. The magnitude of the plateau current is equal in both $i_{DAB,FB\text{batt}}$ and $i_{DAB,FB\text{bus}}$. As the inductor is placed in the path of $i_{DAB,FB\text{bus}}$ its saturation component is zero. These simplifications of (C.1) result in

$$v_{\text{batt}} = \frac{n^2}{R_c} \frac{d}{dt} (i_{DAB,FB\text{batt},sat} + i_{DAB,FB\text{batt},plateau}) - \frac{n^2}{R_c^2} \frac{d}{dt} R_c$$

$$= \frac{n^2}{R_c} \frac{d}{dt} (i_{DAB,FB\text{bus},sat} + i_{DAB,FB\text{bus},plateau}) - \frac{n^2}{R_c^2} \frac{d}{dt} R_c \tag{C.2}$$

Rearranging (C.2) in terms of $i_{DAB,FB\text{batt},sat}$,

$$\frac{d}{dt} i_{\text{batt,FB\text{batt},sat}} = v_{\text{batt}} \frac{R_c}{n^2} + \frac{1}{R_c} i_M \frac{d}{dt} R_c. \tag{C.3}$$

To calculate $\Delta m$ the subscript 1 denotes the current in the positive plateau, and the subscript 2 denotes the negative plateau current waveform. The calculation of $\Delta m$ is given by,

$$\Delta m = \frac{d}{dt} i_{\text{batt,FB\text{batt},sat},1} - \frac{d}{dt} i_{\text{batt,FB\text{batt},sat},2}$$

$$= v_{\text{batt}} \frac{R_{c,1}}{n^2} + \frac{1}{R_{c,1}} i_{M,1} \frac{d}{dt} R_{c,1} - v_{\text{batt}} \frac{R_{c,2}}{n^2} - \frac{1}{R_{c,2}} i_{M,2} \frac{d}{dt} R_{c,2}. \tag{C.4}$$

At the bound of saturation, an approximation can be made that $R_{c,1} = R_{c,2}$. This simplifies the equation to

$$\Delta m = \frac{1}{R_{c,1}} i_{M,1} \frac{d}{dt} R_{c,1} - \frac{1}{R_{c,2}} i_{M,2} \frac{d}{dt} R_{c,2}. \tag{C.5}$$

Under a negative $B_{dc}$, $\frac{d}{dt} R_{c,1} = 0$ and $\Delta m$ is given by,

$$\Delta m \approx -\frac{1}{R_{c,2}} i_{M,2} \frac{d}{dt} R_{c,2}. \tag{C.6}$$

Under a positive $B_{dc}$, $\frac{d}{dt} R_{c,2} = 0$ and $\Delta m$ is given by,

$$\Delta m \approx \frac{1}{R_{c,1}} i_{M,1} \frac{d}{dt} R_{c,1}. \tag{C.7}$$
References