A Smart Gate Driver IC for Enhancement Mode GaN Power Transistor with Dead-time Correction

by

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Doctor of Philosophy

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University of Toronto

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Abstract

Researchers in power electronics have been optimizing silicon devices with novel structures and gate drivers to keep up with the growing demands for power management. However, the improvement has slowed down as silicon power devices approach their theoretical limits. The emergence of GaN power devices provides an avenue to meet the continuing demands for performance improvement.

GaN demonstrates material properties such as wider bandgap, higher electron mobility, and higher critical electrical field when compared to silicon. In particular, the AlGaN/GaN HEMTs exhibit great potential of lower on-resistance and smaller gate capacitance, leading to reduced conduction and switching losses. Their fast switching frequency (>10’s MHz) can further help to reduce the size of the passive components.

Driving enhancement mode (E-mode) GaN HEMT is similar to driving silicon power MOSFETs but with additional challenges. The optimum gate driving voltage for most E-
mode HEMTs is 6 V but the maximum allowed gate voltage is 7 V, leaving a narrow driving window. This restricts the maximum $dv/dt$ and $di/dt$ as little gate ringing can be tolerated. Consequentially, the active driving technique is often employed to suppress the gate ringing while maintaining the fast turn-on and turn-off transitions. Moreover, the fast switching requires precise dead-time control to avoid shoot-through current between the supply voltage and ground. However, excessively long dead-times lead to unwanted reverse conduction and additional power loss. Therefore, high precision detection circuits are important for dead-time correction as the load current changes.

In this thesis, a reverse conduction sensing circuit that can accommodate the large voltage swings at the switching node is designed to track the presence of reverse conduction. The proposed segmented gate driver IC for E-mode GaN power output stages, fabricated using TSMC’s 0.18 µm Gen-2 process, is equipped with dead-time correction for improving system efficiency and highly configurable gate drivers for ringing suppression. The one-step correction mode can optimize the dead-times for both the turn-on and turn-off edges within one switching cycle for switching frequencies of up to 10 MHz with 0.32 ns precision. This allows the power converters to maintain optimal conversion efficiency over a wide output current range.
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<th>Definition</th>
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<tr>
<td>2DEG</td>
<td>Two Dimensional Electron Gas (between AlGaN and GaN interface)</td>
</tr>
<tr>
<td>BV</td>
<td>Breakdown Voltage</td>
</tr>
<tr>
<td>D-mode</td>
<td>Depletion Mode (normally-on)</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital to Analog Converter</td>
</tr>
<tr>
<td>DLL</td>
<td>Delay Lock Loop</td>
</tr>
<tr>
<td>E-mode</td>
<td>Enhancement Mode (normally-off)</td>
</tr>
<tr>
<td>EMI</td>
<td>Electro-Magnetic Interference</td>
</tr>
<tr>
<td>HEMT</td>
<td>High Electron Mobility Transistor</td>
</tr>
<tr>
<td>IGBT</td>
<td>Insulated Gate Bipolar Transistor</td>
</tr>
<tr>
<td>LDO</td>
<td>Low Dropout Regulators</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>$R_{on,sp}$</td>
<td>Specific On-resistance (unit: mΩ⋅cm²)</td>
</tr>
<tr>
<td>$R_{ON}$</td>
<td>ON-resistance (unit: mΩ or Ω)</td>
</tr>
<tr>
<td>RTA</td>
<td>Rapid Thermal Annealing</td>
</tr>
<tr>
<td>S/H</td>
<td>Sample and Hold</td>
</tr>
<tr>
<td>SOA</td>
<td>Safe Operation Area</td>
</tr>
<tr>
<td>TDC</td>
<td>Time to Digital Converter</td>
</tr>
<tr>
<td>WGB</td>
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Chapter 1

Introduction

The concern of modern power electronics is to control electric power using power semiconductor devices [1]. Several basic functions can be achieved using switching converters. There are AC-DC rectifiers, AC-AC cyclo-converters, DC-DC converters, and DC-AC inverters, as shown in Figure 1.1 (a). Based on different application scenarios, a suitable topology is first selected, and a complete power electronic system is then designed accordingly. The design of the power system normally consists of the main converter circuitry and a controller that monitor the input or/and the output information to control the power devices, as represented in Figure 1.1 (b). The controller can be implemented as a self-contained integrated circuit (IC), typically called a power management IC (PMIC). The power converter circuitry usually contains multiple power devices either in discrete or integrated form.

For the past two decades, the demand in power management IC with high-level integration has increased, due to the popularity of personal computers and other portable consumer electronics. Figure 1.2 summarizes the rising number of transistors per die area [2]. This increasing transistor density leads to growth in power density for the modern VLSI (Very Large Scale Integration) chips. Therefore, the power converters for VLSIs are required to deliver more power. On the other hand, the rising demand in portable devices brings additional challenges in improving power efficiency, reducing printed circuit board (PCB) size, lowering the converter cost, and decreasing battery weight. These specific requirements encourage IC designers to integrate a wide range of analog circuits, digital circuits, DSPs, digital microprocessors onto one die. These different blocks need to be powered by multiple power rails (also called voltage islands), such as 0.8V, 1.0V, 1.8V,
3.3V, 5V, 12V, etc. These different voltage islands exist on the same chip. PMIC designs are required to be space efficient and power efficient.

(a) Major types of power conventions
(b) Power converter with controller

Figure 1.1: (a) Four major types of power conversion and (b) block diagram of a power converter consisting of the main circuitry and controller [1].

Figure 1.2: The trend in the number of transistors per chip area in the last two decades [2].

The three aspects that influence the design of PMICs are topology, controller, and power elements. An example of the power elements includes the recently emerged wide bandgap
gallium nitride (GaN) power transistors. GaN power transistors have found adaptation in fast-charging applications and in electric vehicles (EVs) because of their small size and high efficiency. Chapter 1 offers background information on buck converters and wide bandgap materials, followed by an outline of this research work. Chapter 2 proposes a dead-time detection method and Chapter 3 describes a designed gate driver IC. Chapter 4 presents the experimental results and Chapter 5 provides a conclusion and directions for future work.

As an introduction, this chapter first provides reviews on the DC-DC converters in Section 1.1. As the key elements in DC-DC converters, power transistors and their trade-offs are analyzed in Section 1.2. A brief comparison among silicon, GaN and SiC power transistors is also provided. Section 1.3 reviews the main gate driving challenges of GaN high electron mobility transistors (HEMTs). Section 0 provides an overview of the research work and the thesis objectives.

1.1 Point-of-Load Converters

Figure 1.3: Conceptual floor plan of an IC layout with 4 voltage islands powered by their dedicated converters [3].
The number of transistors per chip area continues to increase following Moore’s Law. On the other hand, the number of electronic products has also started to rise, driven by the development of the Internet of Things (IoT). In order to reduce the area of the printed circuit boards (PCB), system designers start to merge multiple ICs with different voltage ratings onto one chip with a single power supply, as indicated in Figure 1.3 [3]. The power management IC (PMIC) requirements have then become more challenging in terms of multiple voltage islands, transient load currents, and thermal management. The solution to power management includes a set of DC-DC converters for delivering power at the desired voltages. These converters referred to as the Point-of-Load (PoL) converters [4] are placed close to the loads for optimal power conversion efficiency.

1.1.1 Converter Topology and Operating Principle

One of the most widely used point-of-load (PoL) topologies is the buck converter [1], as demonstrated in Figure 1.4. The buck converter is used when an input voltage ($V_{IN}$) needs to be stepped-down to a lower desired value $v_{out}$ while delivering current $i_{LOAD}$ to its load. The basic electrical elements used in a buck converter are two switches, a filter inductor, and a filter capacitor. The high-side ($HS$) and low-side ($LS$) switches are turned on and off alternately. The main switch, labeled as $HS$, is usually implemented with power MOSFET. The secondary switch, labeled as $LS$, can be either a free-wheeling diode or another power MOSFET. The comparison between these two implementations are discussed at the end of this section. The common node between the two switches and the inductor $L$ is called the switching node, which is denoted as $SW$ in this thesis.

![Figure 1.4: The topology diagram of a buck converter.](image-url)
The steady-state waveforms of a buck converter under continuous conductor mode (CCM) are indicated in Figure 1.5. The switches are ideal, and both the ESL and ESR are neglected. Within one switching cycle $T_S$, the main switch ($HS$) is turned on for a percentage of the switching time, often called the duty cycle and denoted as $D$. The remaining portion of the switching cycle, where $HS$ is off and $LS$ is on, is denoted as $1 - D$ or $D'$. When the $HS$ switch is on, as indicated in Figure 1.5, the switching node ($SW$) is pulled up to the input voltage $V_{IN}$. The inductor voltage ($v_L$) during this phase is $V_{IN} - v_{OUT}$. When $LS$ is on and switching node ($SW$) is pulled down to ground, the voltage of the inductor becomes $-v_{OUT}$. This process repeats every period $T_S$, hence the switching frequency is defined as:

$$f_{SW} = \frac{1}{T_S} \quad (1.1)$$

The three assumptions required for solving the steady-state are Inductor Volt-Second Balance (IVSB), Capacitor Charge Balance (CCB), and the small ripple approximation. The IVSB is a phenomenon where the inductor current $i_L$ stays the same at the beginning and the end of one switching cycle. Therefore, the ramping up of the inductor voltage during $DT_S$ equals the drop of the inductor voltage during $D'T_S$. Based on IVSB, the relationship between $V_{IN}$ and DC component of $v_{OUT}$ (denoted as $V_{OUT}$) can be derived as:

$$\frac{(V_{IN} - V_{OUT})DT_S}{L} + \frac{(-V_{OUT})D'T_S}{L} = 0$$

$$\Rightarrow DV_{IN} - DV_{OUT} - (1 - D)V_{OUT} = 0$$

$$\Rightarrow DV_{IN} = V_{OUT} \quad (1.2)$$

The inductor ripple current $\Delta i_L$ can also be defined as:

$$\Delta i_L = \frac{1}{2} \frac{(V_{IN} - V_{OUT})DT_S}{L} = \frac{(V_{IN} - V_{OUT})D}{2Lf_{SW}} \quad (1.3)$$

where $L$ is the inductance and $f_{SW}$ is the switching frequency. Equation (1.3) implies that both increasing the inductance and switching frequency can reduce the ripple current. The benefit of having a small ripple current will be explained in the next section when the power losses are analyzed.
From the second assumption, Capacitor Charge Balance (CCB), the charge flowing into and out of the capacitor in one switching cycle cancel each other. The final output voltage has two components: the average $V_{OUT}$ and a small ripple superimposed factor $v_{ripple}$ as indicated in Figure 1.5. The charges flowing in ($q_1$) and flowing out ($q_2$) are represented by the shaded areas. Since the fluctuation of this charge flow is from the inductor ripple current, the ripple voltage can be defined as:

$$v_{ripple} = \frac{q_1 - q_2}{2C} = \frac{1}{2C} \cdot \frac{1}{2} \Delta i_L \frac{T_s}{2} = \frac{\Delta i_L}{8Cf_{sw}}$$  

(1.4)

where $C$ is the capacitance. Equation (1.4) also describes that the ripple voltage is inversely proportional to the switching frequency. CCB also implies that in steady-state,
the output voltage, $v_{out}$ keeps the same value at the start and at the end of each switching cycle. Therefore, the output current, $i_{LOAD}$ is equal to $i_L$ in steady-state.

As mentioned, the $HS$ switch is normally implemented with a power MOSFET but the $LS$ switch can either be a freewheeling diode operating in self-commutating (asynchronous) mode or an additional power MOSFET operating in synchronous mode, as illustrated in Figure 1.6. To compare these two implementations, the equivalent circuits and freewheeling efficiency are summarized in Table 1.1. When a diode is turned on, it is often modeled as a constant voltage drop $V_D$ and a serial resistance $R_D$. When a MOSFET is turned on, it is modeled as a serial resistor $R_{ON}$ since the power MOSFET often operates in the triode region. The voltages at the switching node during $LS$ conducting phase are expressed differently resulting in different freewheeling efficiencies.

![Figure 1.6: Different buck converter realizations using (a) freewheeling diode in an asynchronous mode and using (b) additional power MOSFET in synchronous mode.](image)

Table 1.1: Comparison between Diode and MOSFET as $LS$ Switches

<table>
<thead>
<tr>
<th>$LS$ switch</th>
<th>Equivalent circuit when $LS$ is on</th>
<th>Switching node $LS$ conduction</th>
<th>Freewheeling efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image" alt="Diode" /></td>
<td>$V_D$, $R_D$</td>
<td>$V_{SW,D} = V_D + i_L R_D$</td>
<td>$\eta_{FW} = \frac{V_{out}}{V_{out} + V_{SW,D}}$</td>
</tr>
<tr>
<td><img src="image" alt="MOSFET" /></td>
<td>$R_{ON}$</td>
<td>$V_{SW,FET} = i_L R_{ON}$</td>
<td>$\eta_{FW} = \frac{V_{out}}{V_{out} + V_{SW,FET}}$</td>
</tr>
</tbody>
</table>

For most of the applications, using MOSFET as the $LS$ switch is preferred, because the typical $V_{SW,FET}(0.2 \text{ V})$ is smaller than typical forward voltage drop of the diode ($V_{SW,D} = 0.7 \text{ V}$ for $pn$ junction diodes, and 0.3 to 0.4 V for Schottky diodes). The voltage difference generally allows the synchronous converter to operate at higher efficiency. However, there are some applications when the asynchronous converter is useful, such as when the load...
current is below 0.1 A [5]. This thesis targets the majority applications, and therefore the analysis of power losses will be based on synchronous mode converters.

1.1.2 Summary of Power Losses

In order to achieve optimized system operation, the trade-offs among different losses need to be studied. For a better understanding of the trade-offs, four major losses are evaluated: conduction loss, gate drive loss, switching loss, and body diode conduction loss. The mechanism of these losses has been analyzed systematically in [1, 6] and a brief review is provided in this section.

A Conduction loss

Conduction loss is the sum of resistive losses in all components and is dissipated as heat in the system. The passive components, including inductors \((L)\) and capacitors \((C)\), contain equivalent series resistance \((ESR)\) and are denoted as \(R_L\) and \(R_C\). The HS and LS transistors contribute to the conduction loss through their on-resistance \((R_{ON})\). The on-resistance of the transistor is estimated by the slope of its \(I-V\) relationship in the triode region and is a property of the power transistor. The generic conduction loss of all these components can be expressed as:

\[
P_{\text{cond}} = R_{\text{component}} \cdot I_{\text{RMS,component}}^2
\]

where \(R_{\text{component}}\) is the equivalent series resistance of a component and \(I_{\text{RMS,component}}\) is the root-mean-square (RMS) current flowing through a component.

Table 1.2 summarizes the equivalent models for four main components as well as their RMS current. When delivering a particular load current, the conduction losses in a power converter can be reduced in two ways. The first is to select different components with smaller series resistances. The second method is to adjust the ripple current \(\Delta i_L\) as it could greatly contribute to the RMS current of all components. As described in Equation (1.3), \(\Delta i_L\) is governed by the inductance and the switching frequency. Larger inductance normally means a longer coil winding, leading to a larger \(R_L\) and higher cost. Therefore, high-
frequency operation seems more reasonable for reducing the inductor size to maintain a smaller $\Delta i_L$.

Table 1.2: Conduction Loss Analysis of the Major Components

<table>
<thead>
<tr>
<th>Component</th>
<th>Loss Model</th>
<th>RMS Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inductor</td>
<td>$L$ $R_L$ $i_L$</td>
<td>$I_{rms,L} = \sqrt{I_{LOAD}^2 + \left(\frac{\Delta i_L}{\sqrt{3}}\right)^2}$</td>
</tr>
<tr>
<td>Capacitor</td>
<td>$C$ $R_C$ $i_C$</td>
<td>$I_{rms,C} = \sqrt{\frac{\Delta i_L}{\sqrt{3}}}$</td>
</tr>
<tr>
<td>HS FET</td>
<td>$R_{ON,HS}$ $i_L$</td>
<td>$I_{rms,HS} = \sqrt{D \cdot \left[I_{LOAD}^2 + \left(\frac{\Delta i_L}{\sqrt{3}}\right)^2\right]}$</td>
</tr>
<tr>
<td>LS FET</td>
<td>$R_{ON,LS}$ $i_L$</td>
<td>$I_{rms,LS} = \sqrt{D' \cdot \left[I_{LOAD}^2 + \left(\frac{\Delta i_L}{\sqrt{3}}\right)^2\right]}$</td>
</tr>
</tbody>
</table>

B Gate drive loss

The operation of a buck converter requires the HS MOSFET and LS MOSFET to be turned on and off alternately. Their gate capacitances are therefore charged and discharged, repeatedly at the switching frequency ($f_{SW}$). The power required to drive the transistors is called the gate drive loss. A gate driver is usually used for providing the power needed for this process. The gate drive loss, denoted as $P_{gate}$, is defined as [1]:

$$P_{gate} = Q_g \times \Delta V_{GS} \times f_{SW}$$  \hspace{1cm} (1.6)

where $V_{GS}$ is the gate to source voltage when the power MOSFET is on, and $Q_g$ is the total gate charge which is usually specified by the device manufactures. The $V_{GS}$ and $Q_g$ relationship is commonly expressed in a diagram similar to the one in Figure 1.7. It is desirable to have lower $Q_g$ value to minimize the gate drive loss as expressed in Equation (1.6). The factors that affect $Q_g$ are mainly the properties of the gate dielectric and fabrication techniques employed at the gate [7]. Most importantly, the total device area ($W \times L$) normally determines the total gate charge. Generally speaking, power MOSFETs with more fingers (wider channel width, $W$) exhibit smaller on-resistance but require more driving power.
Another major loss during the switching process is the power dissipation generated by the periodic turn-on and turn-off process. Due to the existence of parasitic capacitances, the transition times of a power MOSFET are not instantaneous. They are denoted as $t_{\text{turn-on}}$ and $t_{\text{turn-off}}$ in Figure 1.8. For hard switching, both the drain to source voltage ($V_{DS}$) and drain to source current ($I_{DS}$) change at finite rates. The waveforms in Figure 1.8 are simplified with the assumption of linear transition, but the actual switching waveforms contain a certain amount of ringing. The shaded areas $W_{\text{on}}$ and $W_{\text{off}}$, representing the overlaps between $V_{DS}$ and $I_{DS}$, are essentially the switching losses, derived as:
\[ P_{\text{switching}} = P_{sw, on} + P_{sw, off} \]

\[ \Rightarrow P_{\text{switching}} \approx \frac{1}{2} V_{IN} \cdot I_{DS} (t_{\text{turn-on}} + t_{\text{turn-off}}) \cdot f_{SW} \quad (1.7) \]

where the typical turn-on and turn-off times are often provided by the manufactures and can be adjusted by tuning the gate charging current, \( I_G \). Generally speaking, at the same voltage rating, power transistors with larger device areas require longer transition times [6].

D  Body diode conduction loss

Another major power loss is the body diode conduction loss. Figure 1.9 illustrates the alternating conduction in a half-bridge buck converter topology [9]. The high-side (HS) and low-side (LS) switches and their intrinsic body diode are as indicated. As discussed, the power transistors require minimum amounts of transition time for switching, therefore these two transistors cannot be on at the same time otherwise there will be shoot-through current from the input power supply (\( V_{IN} \)) to ground. One switch has to wait for an adequate amount of time to make sure the other switch is fully turned off. This blanking time when neither transistor is actively turned on is called the dead-time. Figure 1.10 and Figure 1.11 demonstrate two scenarios in which the dead-times are not optimized in a buck converter. When the dead-times are too short (Figure 1.10), the turn-on and turn-off transition could overlap leading to large shoot-through current. This causes extra power loss and potential reliability issues [10]. In the second case where the dead-times are excessively long (Figure 1.11), there will be periods when both the HS and LS switches are off. The converter starts to draw current from the body diode of the LS device and forces the switching node to be negative (typically the forward voltage of this body diode, denoted as \( V_F \)). This body diode conduction leads to extra power loss (\( P_{BD} \)) and an under-shoot voltage during the transition [11]. It can be expressed as:

\[ V_F \text{ is used for the body diode to distinguish from the forward voltage drop } V_D \text{ for the aforementioned freewheeling power diode.} \]
\[ P_{BD} \approx V_F \times I_{LOAD} \times (t_{dly,\text{on}} + t_{dly,\text{off}}) \times f_{SW} \] (1.8)

where \( t_{dly,\text{on}} \) represents the delay between the \( LS \) MOSFET turn-off and the \( HS \) MOSFET turn-on (rising edge of the switching node), and \( t_{dly,\text{off}} \) represents the delay between the \( HS \) MOSFET turn-off and the \( LS \) MOSFET turn-on (falling edge of the switching node).

Figure 1.9: Schematic of a half-bridge buck converter with different conducting phases.

Figure 1.10: Insufficient dead-time causes shoot-through current.

Figure 1.11: Excessive dead-time leads to body diode conduction [12].
1.1.3 Power Conversion Efficiency

The power conversion efficiency of a point-of-load (PoL) converter is defined as the ratio between the output power and the input power. The major losses that contribute to efficiency degradation are discussed in Section 1.1.2. The general expression of the conversion efficiency is defined as follows:

\[ \eta = \frac{P_{\text{out}}}{P_{\text{out}} + P_{\text{loss}}} \]  

(1.9)

\[ P_{\text{loss}} = P_{\text{cond}} + P_{\text{gate}} + P_{\text{SW}} + P_{\text{BD}} \]  

(1.10)

Table 1.3: Summary of Power Losses [13]

<table>
<thead>
<tr>
<th>Scenario</th>
<th>Conduction Loss</th>
<th>Gate Driven Loss</th>
<th>Switching Loss</th>
<th>Body Diode Conduction Loss</th>
</tr>
</thead>
<tbody>
<tr>
<td>Increase (f_{SW})</td>
<td>Decrease (smaller (\Delta i_L))</td>
<td>Increase</td>
<td>Increase</td>
<td>Increase</td>
</tr>
<tr>
<td>Decrease (f_{SW})</td>
<td>Increase (larger (\Delta i_L))</td>
<td>Decrease</td>
<td>Decrease</td>
<td>Decrease</td>
</tr>
<tr>
<td>Increase (W/L)</td>
<td>Decrease (smaller (R_{ON}))</td>
<td>Increase (larger (Q_g))</td>
<td>Increase (longer (t_{on/off}))</td>
<td>No significant effect</td>
</tr>
<tr>
<td>Decrease (W/L)</td>
<td>Increase (larger (R_{ON}))</td>
<td>Decrease (smaller (Q_g))</td>
<td>Decrease (shorter (t_{on/off}))</td>
<td>No significant effect</td>
</tr>
</tbody>
</table>

Both the peak power efficiency and the efficiency profile over a wide load current range are used for evaluating a converter. Among the four major power losses, conduction loss is mainly determined by the selection of components. Conduction loss also increases with increasing load current and ripple current. The other three losses, on the other hand, are determined by the switching frequency. Table 1.3 summarizes the qualitative trade-offs among four losses in a system, which are related to the properties of power transistors. The trade-offs in the selection of the power transistors are discussed in Section 1.2.
1.2 Realizations of the Power Switches

Power electronic devices used in switched mode power supplies (SMPS) require high voltage blocking and high current handling capabilities to efficiently process the conversion of electrical energy [14]. Three common categories of power devices are transistors, diodes, and thyristors. Modern power transistors include bipolar junction transistor (BJT), MOS field effect transistor (MOSFET), merged MOS-bipolar hybrid devices such as insulated-gate bipolar transistors (IGBTs) and wide bandgap (WBG) power transistors. This section starts with the trade-off analysis of silicon power transistors and provides discussion related to material limitation of silicon when compared to wide bandgap materials. The potential of wide bandgap power transistors is then analyzed by comparing SiC and GaN devices to silicon transistors. Since SiC and GaN technologies are applicable to different domains, they are both extensively researched. In this work, the focus is on the GaN power transistor applications.

1.2.1 Review of Silicon Power Devices

The first commercially available power transistor, the silicon bipolar junction transistor (BJT), was developed in the 1960s. It was later replaced by power MOSFETs in the 1970s because of their simpler MOS gate drive and faster switching speed. After the dominance of power MOSFETs, researchers kept on pushing the limit of silicon material by introducing the merged MOS-bipolar IGBT to take advantage of the benefits of the simple MOS gate drive and high current bipolar conduction in the 80s. This is followed by the introduction of the superjunction (SJ) concept in 1997 [15]. Today, IGBT and SJ are the two main pillars of the silicon power industry.

The major performance specifications of power devices are their breakdown voltage \( V_{BR} \) and \( R_{ON} \). The breakdown voltage is normally required to be at least 10% larger than the input supply voltage \( V_{IN} \). Designers are discouraged to choose power devices with \( V_{BR} \gg V_{IN} \), because devices with much large \( V_{BR} \) generally have higher \( R_{ON} \), leading to an increase
in conduction loss. As discussed in Section 1.1.3, power transistors contribute to conduction loss, gate drive loss, switching losses, and body diode conduction loss. The conduction loss can be reduced by using devices with small $R_{ON}$. The $R_{ON}$ is expressed in the following equation [16]:

$$R_{ON} = \frac{1}{WL\mu n C_{ox}(V_{GS}-V_{TH})}$$

(1.11)

where $\mu_n$ is the electron mobility of a material, $C_{ox}$ is the oxide capacitance, and $V_{TH}$ is the threshold voltage of the transistor. $R_{ON}$ can be reduced by increasing the width ($W$) of the power transistor. However, the resulted increase in $Q_g$ creates more switching loss. Therefore, it is more useful to evaluate the specific on-resistance ($R_{on,sp}$) of a transistor, which is defined as “$R_{ON} \times$ device area”. The widely-used Baliga figure of merit (FOM) [17-19] between specific on-resistance ($R_{on,sp}$) and breakdown voltage ($V_{BR}$) can be expressed as:

$$R_{on,sp} = \frac{4V_{BR}^2}{\varepsilon_0 \varepsilon_r E_{crit}}$$

(1.12)

where $\varepsilon_0$ refers to the permittivity of free space, $\varepsilon_r$ is the relative permittivity, and $E_{crit}$ is the critical electric field of material.

Figure 1.12: $R_{on,sp}$ versus $V_{BR}$ trends for silicon power transistors [20].
Device engineers would normally focus on minimizing the specific on-resistance for a particular breakdown voltage. The silicon material limit has been set as the guideline for researchers, as indicated in Figure 1.12. Power transistors are optimized to be as close to the limit lines as possible.

### 1.2.2 Advantages of Wide Bandgap Materials

There seems to be an implicit rule that a new device concept emerges every ten years in the power industry. However, the improvement in silicon power MOSFETs has slowed down since 2010, as the performance of silicon-based power electronics is approaching their limit in three aspects: on-resistance, switching speed, and junction temperature [21]. Since the early 2000s, gallium nitride (GaN) and silicon carbide (SiC) based power electronics have attracted significant attention due to their superior physical properties such as wider band gaps, higher electron mobility, and higher breakdown electrical field when compared to silicon [22]. In particular, GaN is a direct bandgap material used for lightening LED, and therefore the fabrication techniques for processing GaN have been extensively studied. Moreover, the development of GaN-on-Si growth techniques has promised low-cost manufacturing using CMOS compatible production lines. Table 1.4 compares the key material properties relevant to power transistor designs. As discussed in Section 1.2.1, the critical electric field and electron mobility determine the $R_{on,sp}$ for a particular breakdown voltage. GaN and SiC both offer better trade-off than silicon. In addition, their wide bandgap ($E_g$) also leads to lower intrinsic carrier concentrations ($n_i$), expressed as [23]:

$$n_i = \sqrt{N_C N_V e^{-\frac{E_g}{2kT}}} \tag{1.13}$$

where $N_C$ and $N_V$ are density of state for conduction band and valence band, $k$ stands for the Boltzmann constant, $T$ represents the junction temperature, and $E_g$ is the bandgap of a material. The intrinsic carrier concentration is a pre-factor of leakage current and is plotted as a function of temperature in Figure 1.13. For a fixed junction temperature, $n_i$ of GaN and SiC is orders of magnitude lower than that of silicon, allowing these wide bandgap materials to operate at a higher temperature than Si. Moreover, the high thermal
The conductivity of SiC allows the power density to be higher for a given maximum temperature.

Table 1.4: Physical Properties of Various Materials at 300 K [27]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Silicon</th>
<th>SiC</th>
<th>GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Band gap $E_g$ (eV)</td>
<td>1.12</td>
<td>3.25</td>
<td>3.44</td>
</tr>
<tr>
<td>Electron Mobility $\mu_n$ (cm²/Vs)</td>
<td>1400</td>
<td>700</td>
<td>1800 (2DEG)</td>
</tr>
<tr>
<td>Saturation Velocity $V_{sat}$ (10⁷ cm/s)</td>
<td>1.0</td>
<td>2.5</td>
<td>2.5</td>
</tr>
<tr>
<td>Critical Field $E_{crit}$ (MV/cm)</td>
<td>0.3</td>
<td>2.2</td>
<td>3.3</td>
</tr>
<tr>
<td>Thermal Conductivity $\sigma_T$ (W/cm·K)</td>
<td>1.3</td>
<td>3.8</td>
<td>1.3</td>
</tr>
</tbody>
</table>

Figure 1.13: Intrinsic carrier concentration as a function of temperature [23, 28].

Figure 1.14: Theoretical $R_{on,sp}$ versus $V_{BR}$ limits for Si, SiC and GaN [17].

The trade-offs between $R_{on,sp}$ and $V_{BR}$ for Si, SiC and GaN materials are plotted in Figure 1.14. Both the SiC and GaN theoretical limits are lower than the silicon limit (superjunction not plotted). For a particular breakdown voltage, the specific on-resistance ($R_{on,sp}$) of WBG devices can be orders of magnitude lower than silicon devices. This smaller $R_{on,sp}$ allows a great reduction in the device area to achieve the same $R_{ON}$ [24]. The reduced device area can further decrease the gate charge $Q_g$ which allows the device to be switched at higher switching frequency with lower switching loss [25]. However, the relatively low electron
mobility of SiC might limit its potential in high switching frequency applications. On the other hand, its high thermal conductivity and high maximum junction temperature allow operation with high power density under high temperatures. GaN offers higher electron mobility than silicon which allows fast switching frequency \( f_{SW} \) operation. As summarized in Table 1.3, fast \( f_{SW} \) can allow further reduction in the sizes of passive components \( (L \text{ and } C) \). With the aforementioned material properties, both SiC and GaN are therefore potential candidates for the next-generation power devices suitable for different high-performance applications [26]. Due to the fact that SiC fabrication processes are not compatible with most silicon-based equipment, they have a cost disadvantage at this stage of development.

1.2.3 Properties of Wide Bandgap Devices

Both GaN and SiC power transistors are valuable in their own rights. Figure 1.15 summarizes two application spectrums of various power transistors: power versus frequency and current versus voltage. SiC devices specialize in high power application but their switching frequency is limited due to its electron mobility. Typical applications of SiC include power supplies, electric trains, and transmission lines. Moreover, its high thermal conductivity also favors very high power operation. On the other hand, the GaN power devices are often used in 100 to 1000 V range with rated current under 100 A. The advantage of GaN is in high-frequency applications owing to the high mobility two-dimensional electron gas (2DEG) at the interface between AlGaN and GaN epitaxial layers.

There are two types of GaN transistors: depletion mode (D-mode, normally on) and enhancement mode (E-mode, normally off). Details of the D-mode transistor is included in the Appendix. This work focuses on E-mode high electron mobility transistor (HEMT). The \( p \)-GaN HEMT is the most widely commercially used structure as shown in Figure 1.16. A layer of \( p \)-type GaN is placed in the gate area using a selective epitaxial growth technique [30, 31]. The presence of the \( p \)-GaN layer can deplete the 2DEG channel underneath the gate due to the formation of a \( pn \) junction, as shown in Figure 1.16 (a). Therefore, this device is normally off without any gate bias. With a positive gate bias,
electrons are induced back into the channel, and therefore resuming the conduction path between the source and drain, as indicated in Figure 1.16 (b). The threshold voltage for this type of device is around 1.2 V which is relatively low for power applications [30, 31].

Figure 1.15: Applications of wide bandgap material SiC and GaN plotted as (a) power delivery versus switching frequency and (b) rated current versus rated voltage [29].

Figure 1.16: Cross-sectional diagrams of (a) a normally $p$-GaN gate HEMT and (b) its turn on mechanism.

1.2.4 GaN HEMT Applications

Gallium Nitride (GaN) power devices are being adopted for many power applications at a rapid pace. The world’s first commercial GaN power device has only been released less than one decade ago. The market size of GaN power electronics is projected to reach around $423 M by 2023 and its compound annual growth rate is 93% [32]. As illustrated in Figure
1.17, GaN is expected to provide solutions in many fields, including 45W fast-charging power adaptors for the smartphone market, the Electric Vehicle (EV) market, etc. Foundry services for GaN HEMTs are still limited: at this moment, only from TSMC, Episil, and X-fab.

Figure 1.17: GaN power electronics market projections with two scenarios [32].

GaN HEMTs start to appear in the modern hybrid electric vehicle (HEV) drive systems. The high-voltage GaN transistors (over 600 V) is competing against the current bipolar silicon devices in the 600 and 1200 V range in traction inverters. The main requirements for automotive power modules are low power loss, normally-off configuration, and temperature robustness. The superior material property of GaN has shown great advantage in specific on-resistance, far exceeding the silicon limit. The reduction of conduction loss can greatly improve the power conversion efficiency of the electric drivetrain. With the development of the E-mode HEMTs, the normally-off requirement is basically met. However, a few challenges, such as relatively low maximum gate voltage [33], still remain. More details on the gate driving challenges are discussed in Section 1.3.

GaN HEMTs also play an important role in the fast charger for smartphones. A reported 27-W charging mobile adapter is capable of delivering 5 hours of battery life for smartphones with only 5-minute charging time. The small size of this adapter is claimed to
be the state of art technology. GaN HEMTs are indeed well suited for improving the power density by reducing the size of passive devices due to their superior switching capability [34].

In addition to the aforementioned applications, GaN HEMTs are also found in consumer electronics. Major appliances include power over ethernet, wireless power transmission, LED lighting [35], etc. GaN HEMTs also find applications in power delivery sectors, power supplies, class D audio and aerospace applications [35, 36].

1.3 Gate Driving Challenges for GaN HEMTs

With the maturing GaN fabrication techniques, more and more GaN power HEMTs and dedicated gate drivers are becoming commercially available. A roadmap of GaN power integration is provided in Figure 1.18 with a list of the main GaN device vendors. Driving D-mode GaN in a cascode structure is similar to driving a conventional silicon power transistor, since the driver stills drives the gate of a silicon MOSFET, as illustrated in Figure 1.19. However, driving E-mode GaN HEMTs requires additional considerations. This section starts with the analysis of existing silicon drivers and a comparison between driving silicon MOSFETs and driving GaN HEMTs. Three main driving issues related to GaN are discussed in this section: gate voltage restriction, EMI regulation, and dead-time control challenges. This research work is motivated to provide potential driving solutions.
1.3.1 Gate Driver ICs for Silicon and GaN Power Transistors

The conventional silicon-based gate driver is normally optimized to provide 10 to 15 V $V_{GS}$ for silicon power transistors. The typical supply voltages of these drivers range from 8 to 18 V. Operating the existing silicon drivers at 5 V (GaN driving voltage) would reduce the efficiency of the driver itself. Moreover, gate ringing is a more severe issue for GaN HEMTs as their gate structures are more prone to breakdown when compared to silicon transistors. The turn-on and turn-off gate resistances are normally set differently for GaN and silicon devices, as shown in Figure 1.20. To compare the gate driver features for silicon and GaN power devices, two commercially available silicon-based drivers are chosen. Both drivers are designed as 100 V half-bridge drivers with similar output current and similar propagation delays. The drivers in comparison are designed by the same vendor [38, 39]. The major parameters of the two drivers are summarized in Table 1.5. These listed differences demonstrate the need for gate drivers tailored for GaN power HEMTs.
Table 1.5: Comparison between Gate Drivers for Si and GaN Power Devices

<table>
<thead>
<tr>
<th>Key differences</th>
<th>LM5109 for Silicon Power Transistors</th>
<th>LM5113 for GaN Power HEMTs</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>8 ~ 14 V</td>
<td>4.5 ~ 5.5 V</td>
</tr>
<tr>
<td>Separate on/off path</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>$HS$ recommended range</td>
<td>$-1 ~ 90$ V</td>
<td>$-5 ~ 90$ V</td>
</tr>
<tr>
<td>$HS$ slew rate</td>
<td>$&lt; 50$ V/ns</td>
<td>$50$ V/ns</td>
</tr>
<tr>
<td>$V_{DD}$ rising threshold</td>
<td>Typical 6.7 V</td>
<td>Typical 3.8 V</td>
</tr>
<tr>
<td>Output rise or fall times</td>
<td>15 ns</td>
<td>7ns, 1.5 ns</td>
</tr>
<tr>
<td>Minimum input PWM that changes the output</td>
<td>50 ns</td>
<td>10 ns</td>
</tr>
</tbody>
</table>

Figure 1.20: Application diagrams for (a) the LM5109 gate driver for silicon power transistors and (b) the LM5113 gate driver for GaN power HEMTs. Both driver ICs are silicon-based from Texas Instruments [38, 39].

1.3.2 Gate Voltage Restriction

As discussed, driving an E-mode GaN power HEMT is similar to driving an E-mode silicon power MOSFET except for a few new challenges [12, 37, 40]. Their rated gate driving voltages are between 5 V and 6 V but the maximum allowed gate voltages are 6 V or 7 V [9, 35, 41, 42]. Some commercially available GaN transistors listed in Table 1.6 only have a tolerance 1 V at the gate. This narrow gate driving window restricts the maximum $dv/dt$ and $di/dt$, as only very small ringing is allowed at the gate node before severe gate damage could occur, as indicated in Figure 1.21 labeled with the two major parasitic inductance $L_G$.
and $L_S$ [43-45]. Moreover, the threshold voltage of E-mode GaN HEMTs is relatively low (around 1.5 V), which also restricts the maximum $d\nu/dt$, as shown in Figure 1.21 (b). Therefore, a large gate resistance is needed for damping the gate ringing. However large gate resistance slows down the transistor turn-on and also increases the switching loss.[17].

![Diagram showing gate voltage and current relationships](image)

(a) A comparison between different $di/dt$.

![Diagram showing gate voltage and current relationships](image)

(b) A comparison between different $dv/dt$.

Figure 1.21: Potential (a) $di/dt$ and (b) $dv/dt$ issues for GaN power HEMTs.

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Rated $V_{BR}$ (V)</th>
<th>$V_{TH}$ (V)</th>
<th>Rated $V_G$ (V)</th>
<th>Maximum $V_G$ (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>EPC2023</td>
<td>30</td>
<td>1.4</td>
<td>5</td>
<td>6</td>
</tr>
<tr>
<td>EPC2035</td>
<td>60</td>
<td>1.4</td>
<td>5</td>
<td>6</td>
</tr>
<tr>
<td>EPC2037</td>
<td>100</td>
<td>1.4</td>
<td>5</td>
<td>6</td>
</tr>
<tr>
<td>EPC2034</td>
<td>200</td>
<td>1.4</td>
<td>5</td>
<td>6</td>
</tr>
<tr>
<td>GS61004B</td>
<td>100</td>
<td>1.3</td>
<td>6</td>
<td>7</td>
</tr>
<tr>
<td>GS66502</td>
<td>650</td>
<td>1.3</td>
<td>6</td>
<td>7</td>
</tr>
</tbody>
</table>

Table 1.6: List of Rated Gate Voltage and Maximum $V_G$
1.3.3 EMI Regulation

Another feature of driving E-mode GaN HEMTs is the very fast switching speed, owing to the small gate charging $Q_g$ factor (typical values range from 1.5 nC to 20 nC) [12]. Therefore, the transition times can be reduced to the nanosecond range. This leads to large $dv/dt$ and $di/dt$ transients, contradicting with the aforementioned gate ringing suppression requirement. Moreover, these short switching transitions would also cause electromagnetic interference (EMI) emission, as shown in Figure 1.22. There are several reported techniques for EMI mitigation, including frequency hopping [46, 47], adding gate resistance to slow down the transitions [48], and active driving with dynamic gate resistance [49-51]. The trade-offs for the design are among switching power loss, switching speed and EMI noises [9, 12, 37, 40, 41, 46-48, 50, 52, 53]. It could be useful to include $V_{GS}$ regulation, such as a segmented gate driver for dynamic gate resistance during the transition, in the gate driver design.

1.3.4 Dead-time Control

Another issue related to the high switching frequency ($f_{SW}$) of GaN power HEMTs is the control of dead-times. As $f_{SW}$ increases, the accuracy for reverse conduction detection needs to be improved and the introduction of dead-time needs to be much more precise [54]. An
optimized dead-time can avoid large shoot-through current, reduce switching noise, and mitigate body diode conduction which can improve the overall system efficiency.

![Diagram of LDMOS with body diode and GaN HEMT without body diode]

Figure 1.23: Comparing with a silicon LDMOS, the E-mode GaN HEMT lacks a built-in body diode.

Unlike its silicon counterparts, E-mode GaN power HEMTs do not have the intrinsic body diode [55-57], as shown in Figure 1.23. However, they could conduct current by a mechanism called self-commutated reverse conduction (SCRC)\(^2\) [12]. The key to this phenomenon is the symmetry of the device as shown in Figure 1.24. The channel can be turned on by a positive gate to source voltage \(V_{GS}\) that exceeds its threshold voltage \(V_{GS,TH}\) or a positive gate to drain voltage \(V_{GD}\) that exceeds its own threshold voltage \(V_{GD,TH}\). When an E-mode GaN HEMT is turned off \((V_G = V_S = 0)\) and in reverse bias, the drain to source voltage \(V_{SD}\) can be expressed as [12]:

\[
V_{SD} = V_{GD,TH} - V_{GS} + I_{SD}R_{SD,rev} \tag{1.14}
\]

where \(R_{SD,rev}\) is the channel resistance during reverse conduction and is typically larger than \(R_{ON}\). Figure 1.25 shows the typical reverse conduction characteristics for an E-mode HEMT [59]. When the dead-times are excessively long, both the silicon half-bridge and GaN half-

\(^2\) In this thesis, all the reverse conduction mentioned is referring to this mechanism unless otherwise specified.
bridge provide a current path \((i_{LOAD})\) through \(LS\) switch, as shown in Figure 1.26. The resulted voltage drop at the switching node for an E-mode GaN device (typically 2V – 5V [58], load current and \(V_{GS}\) variant) is larger than that of a silicon MOSFET (body-diode built-in voltage \(V_F\)), as compared in Figure 1.27. Therefore the switching power losses due to excessive dead-time could be higher for E-mode GaN devices [10], as indicated by Equation (1.8).

![Figure 1.24: The conceptual cross-sectional diagram of a \(p\)-GaN E-mode HEMT.](image)

![Figure 1.25: Typical reverse conduction behavior of an E-mode HEMT from GaN System. Inc. [59].](image)

![Figure 1.26: Comparison between (a) Si body diode conduction and (b) GaN reverse conduction.](image)

The simulated switching times for GaN power HEMTs as a function of load are shown in Figure 1.28 and listed in Table 1.7 [60]. A fixed dead-time cannot optimize the system efficiency over a wide load current range. As the switching frequency increases, the reverse conduction loss also increases and becomes more and more significant [61] compare to
silicon devices. Therefore, reverse conduction detection and dead-time correction are essential for improving the power efficiency of E-mode GaN converters.

Figure 1.27: Reverse conduction indicated by (a) the forward voltage ($V_F$) of the body diode in a silicon power transistor and (b) the load-dependent $V_{SD}$ value in a GaN power HEMT.

Figure 1.28: Simulated turn-on and turn-off times for a commercially available E-mode GaN HEMT.

Table 1.7: Simulation Parameters

<table>
<thead>
<tr>
<th>Simulation Environment</th>
</tr>
</thead>
<tbody>
<tr>
<td>GaN model</td>
</tr>
<tr>
<td>Input voltage</td>
</tr>
<tr>
<td>Gate resistances</td>
</tr>
<tr>
<td>$f_{SW}$</td>
</tr>
<tr>
<td>Duty cycle</td>
</tr>
</tbody>
</table>
1.4 Thesis Overview

The objective of this work is to design a gate driver for GaN power HEMTs with dynamic gate resistance for gate ringing suppression, EMI reduction, and dead-time correction. The realization of dynamic gate resistance requires segmented gate drivers with gate drive pattern control. The gate resistance is adjustable from 0.5 to 32 Ω and the control timing resolution is 500 ps. The realization of the dead-time correction requires reverse conduction detection using a SenseFET and a customized comparator. The timing accuracy is 500 ps.

The proposed silicon-based gate driver IC is intended for E-mode GaN HEMTs. This decision is largely due to the immaturity of the GaN IC technology and limited opportunity to submit GaN IC tape-outs. In fact, most drivers in the market are silicon based because of the same reason. In the work, the gate drivers are implemented with a segmented driver scheme. The notion of segmentation was used by our group to improve efficiency by switching in devices in parallel depending on the load profile. Here you are switching in resistors in the gate circuit to shape the gating waveform. The research focus is to modify the segment driver controller to facilitate high switching frequency and fast transition times with reduced control complexity. This segmented driver is intended to be co-packaged with an E-mode GaN power HEMT to reduce parasitic and PCB footprint.

This driver IC design also focuses on dead-time correction especially improving the accuracy of the detection of reverse conduction. Chapter 2 provides a literature review of three dead-time detection techniques, followed by the proposed clamping circuit technique for reverse conduction detection. The modified SenseFET detection mechanism is designed to accommodate the characteristic of E-mode GaN power HEMTs. The clamping method is verified by simulations and experiments with a discrete silicon device prior to the IC design and implementation.

3 The Smart Power Integration and Semiconductor Devices Research Group has worked on segmented driver ICs for IGBTs, LDMOS transistors, and cascode D-mode GaN HEMTs for over 10 years.
Chapter 3 provides the details of the IC design and different circuit blocks, including reverse conduction detection, digital processing, and gate driver with simulation results. The gate driver IC designed for the GaN power HEMT/SenseFET is fabricated using TSMC’s 0.18 µm BCD GEN2 process. Chapter 4 describes the experimental setup for the driver IC followed by the test results. The SenseFET is also tested and presented in this chapter. Finally, in Chapter 5, the conclusions and future work are presented.
Chapter 2

Detection of Reverse Conduction

This chapter reviews several detection methods for the reverse conduction in GaN and SiC power transistors. A novel clamping circuit is also proposed for this purpose. This chapter is organized as follows: Section 2.1 analyzes various methods for reverse conduction detection. Section 2.2 proposes a novel clamping circuit with a capacitive divider model and the corresponding verification via simulation. Section 2.3 presents the design and fabrication of the SenseFET. Finally, Section 2.4 provides a summary of this chapter.

2.1 Review of Existing Methods

Dead-time management has always been critical for the improvement of efficiency for power electronic circuits. Conventional silicon-based systems have demonstrated various techniques. Some CMOS-based detection techniques are unable to withstand the large negative undershoot voltage [57, 62] and are restricted by low input voltage with limited accuracy [61]. The operation of GaN-based converters with optimized dead-time has been reviewed in [56, 63, 64].

2.1.1 Switching Node Detection

The first method is the direct monitoring of the switching node for reverse conduction detection in a boost converter. This direct approach is highly accurate since the actual
reverse conduction causes overshoot voltage or undershoot voltage at the switching node (labeled as $V_X$ near $M_2$ in Figure 2.1).

Figure 2.1 shows the block diagram of a discrete boost converter where $V_X$ stands for the voltage at the switching node. When the boost converter is experiencing excessively long dead-times, overshoot appears at the switching node, noted as $V_{DS2}$ in the waveform (Figure 2.2). The signal $V_P$ is generated by a reverse conduction detection circuit, illustrated in Figure 2.3. This method scales down the switching node voltage $V_X$ and output voltage $V_{OUT}$ through a pair of resistive dividers. The overshoot voltage is then compared with the output voltage ($V_{OUT}$) and the comparator output represents the duration time of the excessive dead-time [63].

Figure 2.1: The block diagram for a switching node detection design [63].

Figure 2.2: The timing diagram for voltage and current of M1 and M2 [63].

Figure 2.3: The schematic diagram of the dead-time controller [63].

This method directly takes measurements from the switching node which should be the most accurate representation of the reverse conduction duration. However, the reverse
conduction signal is a negative pulse in the buck converter. This makes it challenging for integrating this sensor using conventional BCD or CMOS based technology.

2.1.2 Gate Signal Detection

The next detection method is an indirect approach. This method tries to extract the reverse conduction information from the gate signal at the output of gate drivers. Although this method requires more signal processing when compared to the direct approach mentioned above, it is useful for a high voltage system where the switching node could be at hundreds of volts. The indirect measurements might result in less accuracy in detecting the duration of the reverse conduction. However, the high voltage system is normally operating at a much lower switching frequency, where this inaccuracy can be better tolerated.

Figure 2.4: The schematic diagram of a buck converter with separate driver ICs for the HS and LS of a half-bridge [56].

Figure 2.4 shows the schematic diagram of the buck converter with 2 identical gate driver ICs manufactured with 0.35 µm 20 V BCD process. Each driver is equipped with a detector
that can sense the timing between the HS and LS gate signals. For example, when the LS transistor, Q2 is turned off, there is a small current passing the gate of the HS transistor, Q1. This current signifies the complete turn-off of Q2, as shown in Figure 2.5 (a). Once the Q1 (HS) transistor knows that the Q2 (LS) device has been turned off, it would turn on after a short but safe dead-time. The two gate drivers are not required to be on the same die for matching the gating signals as there is “communication” between the two drivers. Therefore, the gate driver can be implemented with a 20 V BCD process without the need to consider the high voltage at the switching node [56].

![Figure 2.5: Simulated voltage and current waveforms using a SiC JFET at 100 kHz showing the “cross-talk” when Q2 and Q1 turn off separately [56].](image)

The reported dead-time control range is 15 ns to 35 ns. The resolution of the dead-time adjustment remains unclear. It could be worthwhile testing at a higher frequency with E-mode GaN devices for this design. Overall, this method is a smart and versatile solution for adaptive dead-time control as it utilizes the inherent “cross-talk” between HS and LS.
2.1.3 Current SenseFET

The last method to be evaluated is an integrated half-bridge driver IC with on-chip dead-time management targeted for SiC half-bridge, as shown in Figure 2.6 [64]. The individual gate driver is implemented with its dead-time management block similar to the one mentioned above.

Different from the aforementioned work where the detector “listens” to the opposite gating signal, this detector is equipped with additional common drain SenseFETs ($M_{SH}$ and $M_{SL}$) in parallel with the main MOSFETs ($M_{MH}$ and $M_{ML}$). The source of this small SenseFET is connected to the driver IC as an indicator of body diode conduction [64]. This method has also been proven to be useful for silicon MOSFETs [65] and has been ported for driving wide bandgap devices. Although this gate driver is not targeted for E-mode GaN power transistors, it is interesting to evaluate this SenseFET detection technique.

The detailed IC implementation with the SenseFET connection is illustrated in Figure 2.7. During the body diode conduction phase (diode of $M_{MH}$), node D becomes lower than node S. The lowering of the voltage at node D would also turn on the body diode of the SenseFET, resulting in voltage drop at the CMPH node as shown in Figure 2.8. The comparator output of this node will then flag the reverse conduction for further correction (see Figure 2.7). It can be noticed that this SS signal can also be used for short-circuit protection with a slight modification of the comparator circuit [54].

There are several concerns to be addressed when porting this design from SiC to GaN power devices. The first one is the voltage level at SS when the built-in body diode is removed. Without the constant voltage drop, the voltage at node D (drain of the SiC transistor in Figure 2.7) could be $-5$ V (extracted from Figure 1.25) below node S, depending on the load condition. The negative voltage at node D will be reflected in the change at SS (or CMPH) node. The voltage of the CMPH node needs to be further analyzed to ensure that the comparators will not be force triggered. Moreover, the choices of $R_S$ might need to be adjustable to accommodate for different reverse conduction voltage.
Furthermore, a negative CMPH (i.e. \(-5\) V) node might not be suitable for a direct feed to the comparator as the gate of the input transistors (their gates) could be damaged. Another concern is the reported diode conduction is shortened to be less than 100 ns [64]. The final detection accuracy remains unknown and therefore this design might not be suitable for E-mode GaN power applications. A brief summary of the reviewed dead-time detection techniques is listed in Table 2.1.

![Diagram of SiC half-bridge power module](image1)

Figure 2.6: The reported SiC-MOSFETs integrated half-bridge driver [64].

![Diagram of circuit schematic](image2)

Figure 2.7: Circuit schematic of the “Gate driver IC” with an external SenseFET [64].
Figure 2.8: Timing diagram of the SiC-based SenseFET dead-time correction [64].

Table 2.1: Summary of the Proposed Dead-time Detection Methods

<table>
<thead>
<tr>
<th>Design</th>
<th>IET 2017</th>
<th>TPE 2016</th>
<th>TPE 2017</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>Discrete board</td>
<td>0.35 µm 20 V BCD</td>
<td>0.35 µm BICDMOS LVIC</td>
</tr>
<tr>
<td>Power switches</td>
<td>EPC2001 E-mode</td>
<td>E-mode GaN</td>
<td>SiC MOSFET</td>
</tr>
<tr>
<td>$f_{SW}$ (max)</td>
<td>2 MHz</td>
<td>100 kHz</td>
<td>100 kHz</td>
</tr>
<tr>
<td>Integrated</td>
<td>Discrete board</td>
<td>driver with detector</td>
<td>Driver with detector</td>
</tr>
<tr>
<td>$V_{in} - V_{out}$</td>
<td>10 V - 20V</td>
<td>45 V - 10V</td>
<td>250 V - 500 V</td>
</tr>
<tr>
<td>Dead-time</td>
<td>N/A</td>
<td>15 ns</td>
<td>0.1 µs</td>
</tr>
<tr>
<td>Dead-time detection</td>
<td>Switching node</td>
<td>Gate detection</td>
<td>Current SenseFET</td>
</tr>
</tbody>
</table>

2.2 Proposed Clamping Mechanism

As reviewed in Section 2.1, both the switching node detection method and the current SenseFET detection method directly track the reverse conduction. However, both methods rely on a resistive voltage divider to scale down the reverse conduction signal. It remains unknown whether the circuits would be functional when applied to a buck converter. In
this section, a novel application of the common drain SenseFET is proposed, the circuit model is then analyzed and finally, the simulated results are presented.

2.2.1  SenseFET Detection with Clamping Function

Traditional SenseFET applications focus on their current tracking ability for current-mode control and peak current detection. To get more accurate current readings, the gate of the SenseFET is turned on slower than the main power transistor by a fixed “blanking time”.

![Conceptual buck converter using the proposed SenseFET for tracking reverse conduction.](image)

The accuracy in current detection of the \( LS \) transistor is not the concern in this work. The SenseFET is used for tracking the duration of the reverse conduction in the \( LS \) GaN HEMT. Figure 2.9 presents a buck converter including the proposed SenseFET, which has its gate tied to a constant voltage \( V_{G,sense} \) and source feedback to the IC for detection. The SenseFET can either be a silicon \( n \)-type MOSFET or a GaN HEMT. Using a silicon \( n \)-type MOSFET provides a more versatile solution when an integrated SenseFET is not available. However, the larger \( Q_g \) of silicon leads to slower SenseFET response. Consequently, the silicon SenseFET results in larger detection errors than using an integrated GaN SenseFET.
The operation of the half-bridge with SenseFET on the low-side is analyzed in Figure 2.10. When the LS switch is in reverse conduction, current flows from ground to the switching node. The voltage at the switching node (SW) equal to \(-I_{DSR_{ON}}\) during this time. With a fixed positive gate voltage, the SenseFET is also turned on, forcing \(V_{\text{sense}}\) to be the same as the switching node. When the HS GaN HEMT is turned on, the switching node (SW) is pulled up to \(V_{IN}\). The SenseFET is then turned off due to the large negative \(V_{GD}\) voltage \((V_{G,Sense} – V_{IN})\). The source terminal of the SenseFET becomes floating and its voltage is defined by the capacitance at this node. The value that \(V_{\text{sense}}\) is defined as the “clamping voltage” and is discussed below.

![Figure 2.10: Working mechanism of the proposed SenseFET during HS and LS conduction.](image)

An equivalent capacitive divider model between the gate to source capacitance \((C_{GS})\), the gate to drain capacitance \((C_{GD})\) and the drain to source capacitance \((C_{DS})\) of the SenseFET is illustrated in Figure 2.11. The diagram is drawn with LS turned off and HS turned on. The SenseFET analyzed in this Section could be either a GaN HEMT or an external \(n\)-type silicon MOSFET and can be designed to be clamped at different voltage levels to accommodate a wide range of GaN HEMTs. The gate of the SenseFET can be tied to a constant value for higher tracking accuracy.

The objective of this SenseFET is to block the high voltage from the switching node while providing information related to the reverse conduction duration using a clamping mechanism. When the LS transistor is conducting, the SenseFET is also turned on. The
$V_{\text{sense}}$ node follows the switching node during this time. The $V_{\text{sense}}$ node is equal to the switching node during $LS$ conduction. When the $LS$ transistor is turned off, but the $HS$ transistor is not yet turned on (in dead-time), the switching node voltage decreases to a large negative value due to reverse conduction. $V_{\text{sense}}$ can track the reverse conduction in the window.

When the $HS$ transistor is turned on, the switching node is pulled up to high voltage. $V_{\text{sense}}$ is now represented by Equation (2.1) and clamped to a fixed value if $V_{IN}$ remains constant. The capacitive divider model can be simplified to Equation (2.2).

$$V_{\text{sense}} \approx \frac{1}{1 + \frac{C_{DS}}{C_{GS}}} \cdot V_{G,\text{sense}} + \frac{1}{1 + \frac{C_{GS}}{C_{DS}}} \cdot V_{IN} - V_{th} \quad (2.1)$$

$$V_{\text{sense}} \approx \frac{V_{G,\text{sense}} C_{GS} + V_{IN} C_{DS}}{C_{GS} + C_{DS}} - V_{th} \quad (2.2)$$

It needs to be pointed out that these aforementioned capacitances are not constant but voltage-dependent parameters. In the model derivation, this voltage dependency is neglected for simplicity. Therefore, this model needs to be verified in simulation using accurate device models.

Figure 2.11: Equivalent capacitive divider model for the SenseFET clamping circuit.
2.2.2 SenseFET Simulation

The SenseFET model is verified via LTSpice simulation using its built-in device models. This is because most GaN vendors provide LTSpice models of their products. The half-bridge uses the GaN power HEMT model provided by the manufacturers and the SenseFET is a *Fairchild BSS123* transistor [66]. The simulation test bench is designed to be the same as the configuration shown in Figure 2.9 with a constant input voltage of 70 V. While keeping $V_{IN}$ at 70 V, the clamping voltage is determined by the value of $V_{G,sense}$ as shown in Figure 2.12 (a). The test bench is then simulated under constant gate voltage but with increasing input voltage, as shown in Figure 2.12 (b). The simulated results and the calculated results (based on Equation 2.2) are compared.

![Figure 2.12: Clamping model verification by simulation using *GPI65015DFN* and *Fairchild BSS123* transistors. $V_{sense}$ is proportional to (a) $V_{G,sense}$ and (b) $V_{IN}$.](image)

The simulated results follow the general trend of the linear approximation with the assumption that the capacitances do not change with bias conditions. In reality, these capacitances are voltage dependent. For instance, $C_{DS}$ is dependent of the depletion width between the drain and body diode. When the drain voltage ($V_{IN}$) increases, the depletion width widens accordingly. Therefore, the actual $C_{DS}$ value is almost inversely proportional to the square root of $V_{DS}$ ($V_{IN}$) [67] and exhibits a “saturation” behavior as $V_{IN}$ increases. Moreover, when the model is simulated under three different gate bias voltages, the
clamping voltage \( (V_{\text{sense}}) \) rises slightly with \( V_{\text{IN}} \) in a monotonic relationship, as shown in Figure 2.13.

Figure 2.13: \( V_{\text{sense}} \) and \( V_{\text{IN}} \) characteristics stay valid under different gate biasing voltage.

2.3 SenseFET Design and Packaging

This section describes the layout of the GaN HEMT and the common drain SenseFET with separate gate and source nodes. The main transistor is rated 15 A and 100 V. The micrograph of the SenseFET is shown in Figure 2.14 with the corresponding circuit representation. The gate pad (G) is placed next to the sources and isolated from the high voltage drain (D). However, this placement shows poor current matching as the SenseFET is on the edge of the main power HEMT. In the original layout design, shown in the mask (Figure 2.15), The SenseFET is placed in the center of the power HEMT in a common center layout format. Due to the limited access to E-mode GaN technology and the delay of the in-house E-mode process development, the fabrication and layout of the SenseFET has been carried out by our collaborator. Only limited degrees of freedom was allowed in this design, and therefore, this SenseFET needs to be further optimized in the future.
Figure 2.14: A micrograph shows the SenseFET layout and its circuit representation.

Figure 2.15: The original layout with the SenseFET placed in the center of the main power HEMT for better matching.

Figure 2.16: Breakdown of the device loss for different types of package [68].

Figure 2.16 lists the breakdown of the device loss for different packages, with the land grid array (LGA) showing the best performance. However, in this design, the DFN-8 package carrier with a thermal pad is chosen as shown in Figure 2.17. This is a solder-friendly test package but it is much larger than the power HEMT with integrated SenseFET, resulting
in long bonding wires and extra power losses as a breakdown in [69]. The gate wires for this device are two long bond wires which add parasitic inductance to the gate.

Figure 2.17: The SenseFET wire bonding diagram for the DFN-8 package.

Figure 2.18: Measured $I_{DS} - V_{DS}$ characteristics for the main power GaN HEMT and the integrated SenseFET (HP4155A analyzer).

The packaged SenseFET is probed and characterized by an HP 4155A semiconductor analyzer for function verification, as plotted in Figure 2.18. The current limit for this tester is 100 mA. Therefore, the performance of the main power HEMT cannot be fully tested.

---

4 Selected by the collaborating company as this is their standard test package.
The two devices are both biased at $V_{GS} = 4$ V and the $I_{DS} - V_{DS}$ characteristics are measured. The resistance of the small SenseFET is extracted to be 26 Ω and the resistance for the main power HEMT is tested to be 0.5 Ω.

2.4 Chapter Summary

This chapter analyzed three reported reverse conduction detection methods suitable for dead-time adjustment and with comparison on their detection resolution and accuracy. Switching node detection is the most straight-forward method for reverse conduction detection but it is only demonstrated for a boost converter. The switching node for a buck converter can have a negative voltage swing, making it more difficult to be fully integrated.

A constant gate voltage clamping method is proposed in order to track the negative reverse conduction pulse while blocking the high voltage at the high-side conduction phase. The effectiveness of this clamping method has been verified by simulation using a MOSFET. In order to further improve the detection accuracy, an integrated GaN SenseFET is necessary.

The first version of the proposed SenseFET is fabricated using TSMC E-mode GaN technology with the help of our collaborators for functionality tests. The sense ratio is set to be 500:1 and verified by testing. The DFN-8 package is larger than necessary and adds extra inductance due to long wire bonding. Although the design of the SenseFET has a different layout than the intended symmetrical style, a clamping model compatible with both external silicon MOSFET and integrated GaN SenseFET has been developed and verified by simulation.
Chapter 3

Integrated Dead-time Control Gate Driver

This chapter describes the details of a gate driver IC designed for enhancement mode (E-mode) GaN power HEMTs with dead-time auto correction. As discussed in the previous chapter, the proposed clamping SenseFET circuit can be implemented using discrete silicon $n$-type MOSFET or discrete E-mode GaN transistor. However, discrete components increase the system complexity, cost, and size while introducing additional bond wire and packaging parasitic inductance. Therefore, an integrated GaN SenseFET has been designed. In order to drive this GaN HEMT half-bridge with the proposed reverse conduction detection method, an integrated half-bridge driver is designed to reduce the gating signal mismatch. Considering the fact that the driving voltage for E-mode GaN ranges from 5 V to 6.5 V, integrating the reverse conduction detecting function into an IC chip is feasible. However, the integrated reverse conduction detection circuit and gate driver design are challenging as they involve complicated mixed-signal processing, especially when detecting a negative pulse.

This chapter is organized to first provide an overview of the system-level design in Section 3.1. This chip is divided into four functional modules, including the reverse conduction detection circuit, digital processor, gate driver control and gate driver. Section 3.2 to 3.5 explains the operation of all four modules with simulation results. Section 3.6 is a summary of this chapter.
3.1 System Overview

The block diagram of the proposed gate driver chip is shown in Figure 3.1. This chip includes a pair of segmented E-mode GaN HEMT gate drivers, a digital processing block and a reverse conduction detection block. There are four voltage domains in this gate driver IC: 1.8 V for digital blocks; 3.3 V for the digital I/Os and the reverse conduction detection block; 5 V for the gate driver output stages and their control blocks; and up to 70 V high voltage diffusion well for the high-side gate drivers\(^5\). The reverse conduction detection block is directly connected to the SenseFET even with the presence of negative pulses.

---

\(^5\) The design of the 70 V level shifter is by X.X. Jiang (University of Alberta) as part of her Ph.D thesis.
The external SenseFET generates a clamped reverse conduction signal for the \( SENSE \) pin on-chip. The negative pulse signal is passed through a capacitor coupled signal line to the comparator. The detection comparator is designed with 5 V devices instead of 1.8 V devices because the clamping voltage is around 2 V to generate a stronger signal. The threshold voltage for GaN SenseFET is usually 1.4 V. It is safer to choose devices with slightly higher breakdown voltage. This detected pulse signal is then buffered and converted to 1.8 V before sending it to the time to digital converters (TDCs) where the signals are digitized into 8 binary bits. These binary signals can then be processed by an on-chip state machine to determine the gating signal for the next switching cycle.

The goal is to achieve optimum dead-times for this DC-DC converter to minimize the occurrence of reverse conduction. The two gating signals are then passed to the gate drivers after the signal buffers and the level shifters. The segmented gate drivers are designed with 5 V CMOS devices for this version.

### 3.2 Reverse Conduction Detection

The reverse conduction detection stage consists of a negative pulse conditioner, a digital conditioning inverter, and a control signal generator, as shown in Figure 3.2. The control signal generator provides bias for the entire block as well as the enable (\( EN \)) and sample and hold (\( S/H \)) control signals. The signal conditioning circuit is used to bring the negative \( SENSE \) pulse from around – 4 V to above 0 V such that the voltage level is compatible with the rest of the signal processing circuits. The final customized inverter block shapes the conditioned signal with the assistance of the control signal generator to reduce the delay time and improve the pulse width detection accuracy. The final output of this detection block is a 3.3 V digital signal. In order to send it to the next 1.8 V biased digital block (discussed in Section 3.3), a few digital buffers are used to interface between these two blocks.
3.2.1 Tunable Signal Conditioner

The signal conditioner is to shift a negative pulse to a positive pulse above $V_{SS}$ level while keeping the original pulse width. Since this negative pulse (or the undershoot voltage) represents the reverse conduction of the LS GaN HEMT, this negative voltage is typically in the range from $-1\ V$ to $-5\ V$ depending on load condition. Since GaN HEMTs have various reverse source to drain conducting resistance ($R_{SD,rev}$) as described in Equation (1.12) from Section 1.3.4, the negative voltage at the switching node could significantly vary among different transistors. Therefore, the amount of shifting is designed to be tunable to accommodate different transistors. The overall schematic of the level shifter is presented in Figure 3.3 and the sizes of transistors used in the signal conditioner are listed in Table 3.1. There are three inputs from the control signal block ($V_{BIAS}$, $V_{REF}$ and $S/H$) and one output ($V_o$) to the inverter block which will be explained in the next two sections.

There are 3 current mirrors ($T.M_1$, $T.M_2$, and $T.M_3$) referencing to the same bias controlled ($T.M_7$) by the signal $V_{BLAS}$. The aspect ratios (W/L) is designed to be $1\ \mu m/2\ \mu m$ to increase the output resistance ($R_{OUT}$) to reduce its sensitivity on their drain voltages [16]. The left two mirrors ($T.M_1$ and $T.M_2$) are designed to carry $5\ \mu A$. $C_1$ and $C_2$ are matched MIM caps to enhance the stability of these two branches [70]. Both capacitors are tied to the same reference node during the sample and hold period ($S/H = 1$). When $S/H$ is disabled, the $V_{SHIFT}$ is compared with the reference $V_{C2}$ by a pair of NMOS. The compared output $V_o$
will then be sent to a buffer. Another branch is the reference setting branch (50 µA). This branch is designed to set the desired $V_{REF}$. The top PMOS ($T.M_3$) defines the branch current, and the bottom NMOS ($T.M_{10}$, $T.M_{12}$, $T.M_{14}$, and $T.M_{16}$) are connected in diode configuration [71]. The current passing through this diode generates a $V_{GS}$ voltage. By increasing the number of fingers of this diode, the $V_{REF}$ decreases. The current distribution for different branches, main signals, and passive devices, and transistor aspect ratio (in µm) are as labeled in Figure 3.3 and Table 3.1.

![Figure 3.3: Schematic of the tunable signal conditioner.](image)

Table 3.1: Transistor Sizing for Tunable Signal Conditioner

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Type</th>
<th>W/L (µm)</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T.M_1$, $T.M_2$, $T.M_4$</td>
<td>PMOS</td>
<td>1/2</td>
<td>Current mirror</td>
</tr>
<tr>
<td>$T.M_3$</td>
<td>PMOS</td>
<td>10/2</td>
<td>Current mirror</td>
</tr>
<tr>
<td>$T.M_5$, $T.M_6$</td>
<td>NMOS</td>
<td>1/0.6</td>
<td>Cascode</td>
</tr>
<tr>
<td>$T.M_7$</td>
<td>NMOS</td>
<td>1/2</td>
<td>Voltage bias for mirror</td>
</tr>
<tr>
<td>$T.M_8$, $T.M_9$</td>
<td>NMOS</td>
<td>8/0.6</td>
<td>Switches</td>
</tr>
<tr>
<td>$T.M_{11}$, $T.M_{13}$, $T.M_{15}$</td>
<td>NMOS</td>
<td>5/0.6</td>
<td>Switches</td>
</tr>
<tr>
<td>$T.M_{10}$</td>
<td>NMOS</td>
<td>5/3</td>
<td>Diode connection</td>
</tr>
<tr>
<td>$T.M_{12}$</td>
<td>NMOS</td>
<td>8 fingers of 5/3</td>
<td>Diode connection</td>
</tr>
<tr>
<td>$T.M_{14}$</td>
<td>NMOS</td>
<td>4 fingers of 5/3</td>
<td>Diode connection</td>
</tr>
<tr>
<td>$T.M_{16}$</td>
<td>NMOS</td>
<td>2 fingers of 5/3</td>
<td>Diode connection</td>
</tr>
</tbody>
</table>
The timing diagram for two switching cycles is plotted in Figure 3.4. The sensed signal is sent to the SENSE pad connecting to capacitor $C_1$ (915.6 fF). During the sample and hold phase ($S/H = LS = 1$), the switching signal is brought to ground by the $LS$ switch (in reality, the $SW$ signal is not kept at ground level but slightly lower than ground). $C_1$ is charged to the voltage between $V_{SHIFT}$ and switching node. Moreover, $V_{SHIFT}$ and the $V_{REF}$ signals are also tied together by the NMOS switches ($T.M_8$ and $T.M_9$) with a large aspect ratio ($W/L = 8 \mu m/0.6 \mu m$) [72]. Therefore, the voltage across $C_1$ is approximately $V_{REF}$. When $LS$ is off ($S/H = LS = 0$) and $HS$ is yet to turn on (during the dead-time period), the sensed signal rapidly drops to negative but the charge in $C_1$ remains. Therefore,

$$V_{SHIFT} \approx V_{SENSE} + V_{REF} \quad (3.1)$$

Moreover, since $V_{SHIFT}$ is also limited by the cascaded current mirror, $V_{SHIFT}$ has a tendency to follow $V_{C2}$. Therefore, $V_{SHIFT}$ cannot go too negative for protecting other circuitry. The voltage across $C_1$ can be unstable and needs to be controlled to a range that is the least influential to the pulse width.

![Timing Diagram](image-url)

**Figure 3.4**: Sample and hold timing diagram explains the working mechanism of the signal conditioner.

Since $V_{REF}$ sets a reference level for the amount the negative voltage to be shifted, the value of $V_{REF}$ is determined by the number of fingers of the diode-connected NMOS ($T.M_{10}$, $T.M_{12}$, $T.M_{14}$, and $T.M_{16}$) at the $V_{REF}$ node. The diode-connected $n$-MOSFETs have the same W/L ratio (5µm/3µm) but with a binary-weighted number of fingers (1, 2, 4 and 8).
The larger fingers (2, 4 and 8) can be turned on and off separately by 3 NMOS switches (T.M\textsubscript{11}, T.M\textsubscript{13}, and T.M\textsubscript{15}). The tuning signals (B\textsubscript{2}, B\textsubscript{1}, and B\textsubscript{0}) can help adjust the size of the bottom NMOS diode by adding extra fingers for reducing the conducting resistance $R_D$, as explained in [73]:

\[ I_D = \left(\frac{W}{2L}\right) \mu_n C_{ox} (V_{GS} - V_{th})^2 (1 + \lambda_n V_{SD}) \]  \hfill (3.2)

\[ R_D \approx \frac{1}{g_m} \]  \hfill (3.3)

\[ R_D \propto \left(\frac{1}{\sqrt{W}}\right) \]  \hfill (3.4)

where $R_D$ is the conducting resistance of this diode-connected NMOS and is inversely proportional to the square root of the device width as expressed in equation (3.4). The device lengths are identical in this design. When the diode current is provided by the current mirror (50 µA), with an increasing number of fingers, the voltage across this diode decreases accordingly. Therefore, the reference voltage $V_{REF}$ can be adjusted to 8 levels to accommodate different GaN HEMTs. The simulated $V_{REF}$ voltage is shown in Figure 3.5. As more branches are enabled, the reference voltage decreases. The range of the reference voltage can be adjusted from 1.1 V to 1.8 V.

Figure 3.5: Tuning of $V_{REF}$ (referring to the $V_{REF}$ node in Figure 3.3) by changing the combinations of the finger widths.

Figure 3.6 compares the output of the voltage conditioner ($V_{SHIFT}$) with minimum and maximum reference voltage set by $B = 111$ and $B = 000$. The shifted voltage will then be passed through an inverter for digitization. It is important to select a suitable range for the
shifting voltage. The setting of $V_{REF}$ currently relies on manual calibration as proof of concept.

![Figure 3.6: Operation of the signal conditioner with minimum and maximum $V_{REF}$.](image)

### 3.2.2 Control Signal Generator

The schematic of the control signal generator is depicted in Figure 3.7. This module is designed with 5 V (0.35 µm) CMOS transistors to speed up the settling time of the signal conditioner. The input signals are the high-side ($HS$) and low-side ($LS$) gating signal from the dead-time generator and the output signals are $V_{BIAS}$, enable ($EN$) and sample and hold ($S/H$). The bias voltage is set by an external resistor connected to the I/O pad for $V_B$ in this version. The optimal bias current is 5 µA.

The $EN$ signal is enabled at the falling edge of either $HS$ or $LS$ gating signals and disabled a few nanoseconds after the rising edge of the gating signal. The delay time can also be tuned by the bias current of this system [74]. The $EN$ signal allows the signal conditioner results to be sent to the conditioning inverter and to mitigate false triggering caused by unwanted ringing at the switching node. The $S/H$ signal is a buffered $LS$ gating signal. The main purpose is to bring $V_{REF}$ to a pre-determined value during the $LS$ conduction phase of
the half-bridge. Therefore, the capacitors, $C_1$, and $C_2$ in Figure 3.3 would be pre-recharged to a voltage between the switching node and the level shifter reference node.

![Figure 3.7: Schematic of the control signal generator.](image)

![Figure 3.8: Simulated timing diagram for the control signal generator.](image)

A detailed timing diagram is presented to explain the operation of the signal conditioner and the comparator in the following sections. The simulated timing diagram is presented in Figure 3.8. The solid lines are the gating signals from the dead-time generator and the dashed lines represent the delayed gating signals. These four signals turn on the $EN$ signal twice every switching cycle for monitoring both the turn-on and turn-off transitions.
3.2.3 The Signal Conditioning Inverter Design

The conditioned signal $V_{SHIFT}$ is then passed to a customized inverter for generating digital pulse width. The enable signal ($EN$), discussed in Section 3.2.1, is kept low for keeping the $V_o$ node at $V_{DD}$ outside of the reverse conduction window in order to eliminate potential false detection caused by ringing at the switching node.

As shown in Figure 3.9, the sensing output ($Sense\_out$) also provides positive feedback to assist the inverter. Initially, the $Sense\_out$ signal is locked at 0 by $EN$. When the comparison starts, the $Sense\_out$ signal starts to rise to logic 1, which turns on the NMOS connecting $V_{SHIFT}$ and $V_o$. This loop adds hysteresis to the $Sense\_out$ signal to improve the immunity from sudden changes in $V_{SHIFT}$. The sizing information is listed in Table 3.2.

![Figure 3.9: The schematic of the inverter-based comparator and digital buffer.](image)

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Type</th>
<th>W/L (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>C.M1</td>
<td>PMOS</td>
<td>1/0.6</td>
</tr>
<tr>
<td>C.M2</td>
<td>NMOS</td>
<td>0.6/0.6</td>
</tr>
<tr>
<td>C.M3</td>
<td>PMOS</td>
<td>0.6/0.6</td>
</tr>
<tr>
<td>C.M4</td>
<td>NMOS</td>
<td>0.6/0.6</td>
</tr>
<tr>
<td>Buffer</td>
<td>PMOS</td>
<td>2/0.6</td>
</tr>
<tr>
<td>Buffer</td>
<td>NMOS</td>
<td>1/0.6</td>
</tr>
</tbody>
</table>

The transistor sizes for the inverter are set to the minimum. This choice might bring concern to matching issues in the layout. However, smaller transistors have smaller parasitic...
capacitances (for example, $C_{GD}$ and $C_{DS}$). Charging these smaller parasitic capacitances requires less time. With the fast charging and discharging, the Sense_out follows the reverse conduction signal closely, the propagation delay is hence minimized. Since the widths of the transistor $C.M_2$, $C.M_3$ and $C.M_4$ are reduced to 0.6 µm, such a small gate area might result in a larger mismatch between transistors [75]. However, as the response speed is the main concern in this design, with extensive simulations performed to analyze the trade-off between speed and mismatch, the current design exhibits the best result in terms of tracking accuracy. The signal buffer is implemented with two inverters with standard sizing (2 µm/0.6 µm for PMOS and 1 µm/0.6 µm for NMOS). Figure 3.10 illustrates an example of the simulation result for this comparator. Since the transistor sizing of this design is small, the performance will be largely influenced by the layout and process variations. Corner tests with different process parameters and operation temperatures are evaluated and discussed in the next section.

![Simulation Result](image)

Figure 3.10: A post-layout simulation results for the comparator.

### 3.2.4 Full Circuit Implementation

Figure 3.11 illustrates the final schematic view of the reverse conduction detection block. The sub-blocks mentioned above are labeled accordingly. Figure 3.12 presents the final
layout of this block. The total area used for this block is $115 \, \mu\text{m} \times 140 \, \mu\text{m}$, where the two capacitors occupy half of the block.

The reverse conduction detector is surrounded by its own isolating ring with one input pad (\textit{SENSE}) and one output pad (\textit{Sense_out}). Since this block is designed with 5-V CMOS and powered by 3.3 V, its output needs to be shifted down to 1.8 V for digital processing. The digital buffers are not shown in this diagram, but they are calibrated to maintain the same charging and discharging to avoid asymmetry between pull-up and pull-down speed.

Figure 3.11: Schematic of reverse conduction detector.
Figure 3.12: The layout for the reverse conduction detector (115 µm × 140 µm).

Post layout simulation for a 1 A, 48 V to 12 V buck converter is shown in Figure 3.13 to further explain the working principle of this reverse conduction detector. The negative reverse conduction at the switching node is tracked by the SenseFET and clamped at 1.78 V to protect the chip, as explained in Section 2.2. The input signal $V_{\text{SENSE}}$ is then shifted up by the on-chip signal conditioner, generating a $V_{\text{SHIFT}}$ signal. The amount of shifting can be adjusted by turning on the additional control bits ($B_2$, $B_1$, and $B_0$). The two outputs of the control signal generator $EN$ and $S/H$ are illustrated for demonstrating the control timing. The final logic output is shown on the bottom.

The zoom-in detection waveforms are shown on the right-hand side. To simplify the measurements, the input signal pulse is defined to be $-100$ mV lower than the voltage at the switching node during LS conduction. The pulse width of the digital output is defined as the mid-to-mid pulse width. By this definition, the detection timing accuracy is within 0.5 ns.
Figure 3.13: Post-layout simulation waveform for the reverse conduction detection block:

load current = 1A.

Figure 3.14: Radar diagram for evaluating the performance of the detection block under different process and temperature variations. $B = 000$, load current = 1 A.
As mentioned in Section 3.2.3, the small sizing of some transistors makes this detection block more easily influenced by process variation and operational temperature. Therefore, a corner test based on post-layout simulation has been carried out to evaluate the performance of the detector. In this simulation, the input reverse conduction pulses for both rising (red line) and falling edges (blue line) are around 3.25 ns for all 15 corners. The outputs of this detector block are various at different corners. The maximum error is smaller than 0.5 ns (corner Mff_libTemp-40). Moreover, if the output of this detector is too far from the expected value, the fine-tuning bit could be manually calibrated for improving the accuracy.

3.3 Digital Processing

The digital blocks in this chip include a serial scan chain [76] (SSC) for communicating with an external FPGA, a time to digital converter (TDC) for quantizing digital pulse width, a dead-time control for inserting dead-times at rising and falling edge of high-side gating signals and a state-machine for on-chip adaptive dead-time control.

![ON-chip digital blocks diagram](image)

Figure 3.15: The block diagram of the on-chip digital blocks.

Figure 3.15 presents the block diagram of the on-chip digital circuits. These digital blocks are controlled by a 128-bit SSC with read and write functions. A timing diagram of the
SSC is shown in Figure 3.16 as an example [77]. The detailed structure of this SSC is not discussed in this work as it is a common module for IC design [78, 79]. Since the scan speed is not a concern for this test version, there is no advanced functions added to the SC. This section will therefore only focus on the designs of TDC, dead-time control and the state-machine, sequentially.

![Conceptual block diagram and conceptual timing diagram of the scan chain.](image)

**3.3.1 Time to Digital Converter**

The time to digital converter (TDC) [80] is implemented with 128 delay cells, a delay lock loop (DLL) [81, 82] and a 128 to 7-bit decoder, as shown in Figure 3.17. When a pulse is sent to the input of the DLL, it is delayed by 320 ps per cell to a maximum number of 128 cells. The output of these 128 delay cells are sampled and held by the digital delay lock loop (DLL) for decoding. The schematic for a unit cell for the DLL is shown in Figure 3.18. The output of the DLL is passed through two D flip-flops (DFF) to improve system stability and reliability. The sampled delay cell outputs arrive at the decoder after two clock cycles (typical 10 ns/cycle) later. The decoder aims to count the number of ones from the DLL and output this number in binary. The detailed Boolean expression for this decoder is provided in the Appendix. Figure 3.19 shows the example of converting a 1 ns pulse into binary code and the output of decoder is 0000 011 which is equivalent to 0.96 ns. The linearity and resolution of this TDC largely depend on the delay cell (320 ps by design).
Although these 128 delay cells are identical, the routing mismatches and process variations could also affect the actual delay time per cell. It is expected that the accumulated error becomes larger for later cells, e.g. $D_{125}$, $D_{126}$, $D_{127}$, etc. Consequently, the TDC’s accuracy gets worse for a large input pulse than for a small input pulse, as shown in Figure 3.20. Figure 3.21 illustrates the final layout of this TDC, designed and completed manually.
following a binary tree style for better synchronization and signal matching. The total area used for one TDC is 460 µm × 280 µm, and there are two TDCs used in this system for measuring reverse conduction pulse at rising and falling edges, respectively. The clock signal is layout using a buffered clock tree for minimizing the skew and total power [83].

Figure 3.20: Post-layout simulation of the TDC performance.

3.3.2 Dead-time Control

The dead-time controller consists of two identical 8-bit controlled delay blocks. Figure 3.22 shows the block diagram of each controller similar to an inverter-based delay line described in [84]. The input signal $D_{IN}$ passes through 8 multiplexers controlled by $B_{[7:0]}$. 
Each delay cell can be bypassed by setting $B_{[7:0]}$ to 0. $B_0$ correlates to one unit-delay (320 ps) and $B_7$ correlates to 128 unit-delays (40.96 ns). By programming the 8 control bits, the delay for each delay block is 81.92 ns with a resolution of 320 ps, as shown in Figure 3.23.

![Figure 3.22: Block diagram of the binary-weighted delay block.](image)

Figure 3.22: Block diagram of the binary-weighted delay block.

![Figure 3.23: Post-layout simulation results of the 8-bit delay controller.](image)

Figure 3.23: Post-layout simulation results of the 8-bit delay controller.

The final $LS$ signal is determined by a delayed $Q$ signal (to avoid changing multiple signals at once), input signal and the delayed $LD$ signals. The final part of the timing diagram is shown in Figure 3.24. When either signal is low, the $LS$ signal stays low. Therefore, the dead-times are inserted on the rising edge and falling edge of the $LS$ gating signal and the $HS$ duty cycle remains the same with input. The final layout of the dead-time control, shown in Figure 3.25, is 270 μm by 160 μm. The largest blocks are the two identical delay
blocks. This dead-time controller is implemented with 2 V low voltage devices and is protected by the isolation ring.

![Diagram of the non-overlapping dead-time controller](image)

**Figure 3.24:** Final output from the non-overlapping dead-time controller.

![Diagram of the dead-time control layout](image)

**Figure 3.25:** Layout of the dead-time control. The two delay cell chain for controlling two dead-times are placed in symmetry to match the propagation delays.

### 3.3.3 Dead-Time Correction State Machine

The dead-time correction utilizes an on-chip state-machines that could finish the compensation within two clock cycles. Accounting for the signal buffering time and the reverse detection time, the maximum switching frequency is chosen to be 10 MHz, which
is equivalent to 10 digital cycle. The dead-times for the rising and falling edges can be corrected independently. The correction starts with a dead-time target setting \( D_t \) to set the targeted reverse conduction pulse and also to act as a safety point for overshoot protection. The target value can be set between 0 to 40.96 ns, controlled by 7 bits. The flow chart for the dead-time correction is shown in Figure 3.26.

![Flow chart of the one-step and gradual dead-time correction in an open-loop configuration.](image)

The state-machine first reads the digital output from the TDC (quantized reverse conduction pulse), \( T_{sense} \) and generates the corrected dead-time to reduce the reverse conduction to the targeted value. When \( T_{sense} \) is smaller than the target, the state-machine starts to add dead-time back by one unit delay. There are two correction modes, one step adjustment (100% correction) and partial correction with 3 choices: 12.5%, 25%, and 50%.

The operation is described by equation (3.5). The correction speed (represented by \( X\% \) is selected depending on the stability of the actual load condition. When the load current varies in a small range, the optimum dead-time is expected to vary within a small range.
Thus the adjustment amount could be set more aggressively (100%: one step) as the reverse conduction pulse stays in the same range. When the detected reverse conduction is a long pulse, the state machine can be adjusted to a gradual mode so that only a fraction of the dead-time is reduced. The detected pulse is then gradually corrected towards the target value.

\[ [n + 1]D_s = [n]D_s - [n](T_{\text{Sense}} - D_t) \times X\% \] 

The closed-loop discrete control for this gradual mode is designed as follows:

\[
\begin{align*}
T_{\text{Sense}} - D_t &\geq 9.6 \text{ ns} \rightarrow X = 12.5\% \\
9.6 \text{ ns} > T_{\text{Sense}} - D_t &\geq 4.8 \text{ ns} \rightarrow X = 25\% \\
4.8 \text{ ns} > T_{\text{Sense}} - D_t &\geq 1.0 \text{ ns} \rightarrow X = 50\% \\
1.0 \text{ ns} > T_{\text{Sense}} - D_t &\rightarrow X = 100\%
\end{align*}
\]

where the adjustment fraction is gradually increased as the reverse conduction pulse is compensated towards its pre-set target. Figure 3.27 shows the different correction speed programmed for the closed-loop control based on different input ranges. One example of the operation of both the one-step adjustment mode and the closed-loop gradual adjustment mode is presented in Figure 3.28.

![Figure 3.27: The correction speed setting based on different input ranges.](image)
In the one-step dead-time correction mode, the reverse conduction at the switching node is first detected and a digital pulse is generated for correction. The next switching cycle shows the reverse conduction has been correct towards 0 (most aggressive mode). For the gradual mode, the 6 ns pulse falls in the 25% bin, therefore only $6 \times 25\% = 1.5$ ns is corrected. The next detected pulse width is 4.2 ns which corresponds to 50% bin, and therefore 2.1 ns is deducted from the dead-time settings. The correction speed remains in the 50% bin for the next cycle until the detected pulse is reduced to 1 ns. The speed is then in the 100% bin and the 1 ns reverse conduction is corrected. To sum up, for long reverse conduction, the dead-time is corrected by a fraction at a time until it is finally eliminated.
3.3.4 Full Digital Implementation

The layout for the final digital block, including two TDCs, one dead-time control block, and two state machines, is illustrated in Figure 3.29. The layout of this version is manually performed as the synthesizing tools have not been configured probably at the time of the design. Therefore, the area efficiency of this digital block is relatively low. Most of this digital block, except for dead-time control and delay cells, needs to be improved with digital synthesizing for better efficiency. Another option is to include the SPRUCE CPU designed by our research group [85] for on-chip closed-loop PID control and real monitoring of this IC [86].

The detection block together with digital processing has been simulated to verify the effectiveness of the optimized dead-time control, shown in Figure 3.30. The optimized dead-time has less than 1 ns reverse conduction at the switching node. The on-chip dead-time correction system can keep track of the optimum dead-time operation over a wide range of load conditions.

![Diagram of digital block layout](image)

Figure 3.29: Top digital block uses a total area of 1000 µm × 800 µm.

---

There is a 6 month transition period to shift from Cadence Encounter to Innovus in our laboratory.
Figure 3.30: Post-layout simulation with fixed and adaptive dead-times. $V_{in} = 45$ V, $V_{out} = 10$ V, $I_{load} = 10$ A and $f_{SW} = 1$ MHz [40].

Figure 3.31: Efficiency post-layout simulation plot. $V_{in} = 45$ V, $V_{out} = 10$ V, $f_{SW} = 1$ MHz package losses, bond wire and PCB parasitics are not accounted for [40].
Figure 3.31 compares the efficiency of the fixed dead-time scheme and the adaptive dead-time scheme over a range of load conditions. The simulation, not including package, bonding or PCB losses, shows that the system efficiency could be optimized from fixed dead-time situations. When the load current is small, the required rise time and fall time are longer. Therefore, larger dead-time can avoid overshoot current and therefore is more suitable. During heavy load conditions, excessive dead-time leads to reverse conduction which could be the main source of power loss. Using the adaptive dead-time control scheme, the reverse conduction can be minimized and therefore enhancing the system efficiency across a wide range of load conditions.

Figure 3.32: Load step (1 to 10 A) simulation with fixed and adaptive dead-times. $V_{in} = 60 \text{ V}$, $V_{out} = 10 \text{ V}$, and $f_{SW} = 10 \text{ MHz}$. 
When the load condition changes, the rise and fall time of the switching node change accordingly, requiring the dead-time control to be re-evaluated under a load step condition. Figure 3.32 demonstrates the changes in the switching node waveform with a sudden increase in load current. Figure 3.32 (a) is set such that the rising edge has adaptive dead-time and falling edge has fixed dead-time. As load current increases under a load-step condition, the falling edge exhibits increased reverse conduction at switching node while the reverse conduction of the rising edge remains minimized. Figure 3.32 (b) demonstrates the effectiveness of the dead-time control for both edges under the same load step test.

### 3.4 Gate Driver Control

The block diagram of the segmented gate driver is illustrated in Figure 3.33. The gate driver includes two modules: the gate driver control for generating driving patterns and the 7-bit gate drivers with different gate resistances. Each driver can be programmed individually with an 8-bit pattern. The gate driver control will be discussed first in this section. The control block includes a current mirror for speed control, a pattern generator with pre-set patterns, a scan chain to change the pattern if required and pre-drivers for the output stages.

![Figure 3.33: Block diagram of the gate driver block: control and segmented driver.](image-url)
3.4.1 Delay Chain

The current controlled delay block is constructed with 12 identical unit delay cells. Each unit cell delays the input signal by an amount controlled by the difference in charging two current-starved inverters (CSI) [87], as shown in Figure 3.34.

When a gate signal arrives at the $IN$ pin, the delay of the first inverter is controlled by a bias current $I_B$. This signal is inverted again and sent to the $NEXT$ pin as the input for the next unit delay cell. This $NEXT$ signal is then buffered and then output to pin $OUT$. The layout for this cell is demonstrated in Figure 3.35. Figure 3.36 shows the timing diagram of the unit delay cell when the bias current is set to 13.5 µA as an example. The delay between $IN$ and $NEXT$ is around 650 ps, but this is not the unit delay value of this unit delay cell. The unit delay is measured as the difference between the two $OUT$ signals from two adjacent cells.

![Figure 3.34: The schematic of the unit delay cell.](image1)

![Figure 3.35: Layout of the unit delay cell.](image2)
As shown in Figure 3.37, The 12 unit-cells are connected in series and its current biasing is set by the same voltage bias. The first two and the last unit delay cells, marked in grey, are the dummy cells where their outputs are omitted. The output of the middle 9 unit-delay cells are used for creating the unit delay.

Figure 3.37: Block diagram of the delay chain used for gate driver control consisting of 12 unit-delay cells. This delay chain has 3 dummy outputs at both ends for layout matching purposes.

Figure 3.38: Unit delay decreases as the bias current increases.
Figure 3.38 plots the delay as a function of bias current. When the bias current increases, the first inverter is charged more quickly. The unit delay is inverse proportional to the bias current. The smallest delay time that can be set is around 500 ps. The optimum range to bias the current is between 10 µA and 20 µA where the delay versus bias current relationship is quasi-linear. These 9 delay-signals can then generate 8 time-intervals as listed in Figure 3.39. The pulse width of each interval is represented by $D$ and these intervals are expected to be the same width.

![Delay Chain](image)

Figure 3.39: The 9 delay cells generate eight time-intervals and the interval width is presented by $D$.

![Post-layout simulation results of the delay chain showing the input and 9 output signals](image)

Figure 3.40: Post-layout simulation results of the delay chain showing the input and 9 output signals.

The simulated output for one delay chain is illustrated in Figure 3.40. The output signals of the dummy cells are excluded leaving an uneven gap between $IN$ and OUT<1>. The delays between the adjacent outputs have been designed to be identical, but there are still variances among the delay times, as shown in Figure 3.41. The standard deviation (STD) among each delay cells ($D_{[1:8]}$) is calculated and plotted against increasing bias current. When the bias current is below 10 µA, the STD approaches 3%, and the accumulated error between $D_1$ and $D_8$ is 80 ps. This error should be tolerable as when the delay time is 3 ns,
the total transition times is 24 ns. When the bias current is above 15 µA, the standard deviation remains lower than 0.5% which meets the target of the design.

Figure 3.41: Error ($\Delta D$ from $D_4$) and standard deviation analysis for all the different delay cells, taking $D_4$ as the reference.

Figure 3.42: Post-layout simulation of the delay time for $D_4$ when the bias current is 13.5 µA.
Figure 3.42 demonstrates the radar graph for analyzing the delay cell at different corners of process variations. The bias current is 13.5 µA and the delay time of $D_4$ is extracted. The post-layout simulation shows that the offsets of $D_4$ under all 15 corners are around 0.3 ns. For the generation of the gate controlling pattern, the matching of different delay cells will affect the gating timing. On the other hand, the process variation can be compensated by tuning the biasing current.

### 3.4.2 Pattern Generator

There are 7 pattern generators used for generating the gating signals for the 7 gate drivers independently. The block diagram of one generator is shown in Figure 3.43. The output signals of the delay chain are then programmed by 8 customized control signals $SET_{[1:8]}$. When $SET_N = 0$, the corresponding interval $D_N$ is set to 0 and wise versa. Three examples of the pattern generator output are illustrated. The layout of one pattern generator is shown in Figure 3.44. The symmetry and compactness of the layout are essential for matching all the delay cells.

![Figure 3.43: Block diagram for one pattern generator with 3 examples.](image)
Figure 3.44: Layout of one pattern generator (80 µm × 64 µm).

Figure 3.45: The block diagram of the gate driver control with 7 delay chains and pattern generators.

The final gate driver control block includes 7 delay chains and 7 pattern generators, as shown in Figure 3.45. All the delay chains are biased by the same signal and are fed with the same gating signals. Each pattern generator is programmed by its individual $SET$ signals. There are 56 $SET$ signals required to program one driver control and there are two driver control blocks: for PMOS and NMOS, respectively. The gating signals for PMOS and NMOS are generated by a non-overlapping 2-phase clock generator, indicated in Figure 3.46. The biasing voltage $V_B$ can be adjusted by an external resistor soldering to pad $R_B$.

Figure 3.47 shows an example of the gate driver patterns generated for driver number 1 and 7. Both PMOS and NMOS signals are included for explaining the timing. Both drivers are programmed with $SET = 0101010$, therefore the gate patterns alternate between 1 and 0. The resolution of the interval is set to be 450 ps which is close to the limit of the timing
resolution. The diagram shows that the gate driving pattern 1 and 7 are synchronized. Inside each driver, a slight dead-time between the PMOS and NMOS is used to avoid overshooting within the drivers. The final layout of the pattern generator including a 120-bit scan chain for shifting 112 SET signals.

![Diagram of biasing circuitry and clock generator circuitry.](image)

**Figure 3.46:** The schematic diagrams for the biasing circuitry and the non-overlapping 2-phase clock generator circuitry.

![Timing diagram of gate driver patterns.](image)

**Figure 3.47:** A timing diagram of gate driver patterns generated for driver 1 and 7.

![Gate driver control block layout.](image)

**Figure 3.48:** Gate driver control block layout. The total area used is 1100 µm × 350 µm.
3.4.3 Segmented Drivers

A block diagram of the segmented gate driver is demonstrated in Figure 3.49. The 7 output segments for pull up and pull down resistance sets are designed from 1 Ω to 64 Ω. The targeted resistance values for each segment are documented in Table 3.3. In this case, no external gate resistors are needed for driving the E-mode GaN HEMT. The driver is configurable using the serial scan chain and the bias current. The scan chain determines the driving pattern for dynamic gate resistance and the bias current sets the switching speed.

![Block diagram for the segmented gate drivers and schematic of one driver segment.](image)

Figure 3.49: Block diagram for the segmented gate drivers and schematic of one driver segment.

### Table 3.3: Gate Driver Output Resistance for the Seven Segments

<table>
<thead>
<tr>
<th>Segment No.</th>
<th>Gate Resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>64 Ω</td>
</tr>
<tr>
<td>2</td>
<td>32 Ω</td>
</tr>
<tr>
<td>3</td>
<td>16 Ω</td>
</tr>
<tr>
<td>4</td>
<td>8 Ω</td>
</tr>
<tr>
<td>5</td>
<td>4 Ω</td>
</tr>
<tr>
<td>6</td>
<td>2 Ω</td>
</tr>
<tr>
<td>7</td>
<td>1 Ω</td>
</tr>
</tbody>
</table>
The gate driver is designed with voltage-driven topology, consisting of a chain of inverters with 7 driver segments [88]. The block diagram of one 7-bit segmented gate driver is shown in Figure 3.50. The PMOS and NMOS patterns are generated by the generator discussed above. The inverter chains are carefully sized in order to test desired driving strength for different E-mode GaN power HEMTs operated under a wide range of conditions (e.g., different input voltages). In this design, both the drivers and driver controls are designed with 5 V devices, therefore no level shifters are required for this design. The driving pattern design is presented in this section.

### 3.5 Driving Pattern Design

This section discusses different gate driving strengthen patterns and their effectiveness. First, the gate driver RLC circuit model is provided with the list of simulation test bench setup. The three driving patterns, including fixed driving strength and two dynamic driving patterns, are described. Their effectiveness is also compared.

#### 3.5.1 Gate Driver Model

The test bench for the segmented gate driver is a double pulse [85] set up as shown in Figure 3.51 and the parameters are listed in Table 3.4. The parasitic inductance for drain
and gate nodes are estimated by 1nH/mm for 1.2 mil bond wires. The gate inductance is estimated to be 2.5 nH including the PCB trace inductances and on-chip layout inductances.

The gate driver can be seen as a resistance, denoted as $R_G$, and the gate of the power transistor can be simplified to a capacitor, $C_{GS}$. With the presence of the parasitic inductance $L_G$, the gate driver and the power transistor form a second-order $RLC$ circuit as presented in Figure 3.52. In the RLC, circuit, the resonant frequency, $\omega_0$ and damping ratio, $\zeta$ are derived as in [71]:

$$\omega_0 = \frac{1}{\sqrt{L_G C_{GS}}}$$

$$\zeta = \frac{R_G}{2} \cdot \frac{C_{GS}}{L_G}$$

where the resonant frequency determines the frequency of the ringing oscillation and the damping ratio determines the speed of decaying in the amplitude of the oscillation.

If the resonant frequency is a fixed value, the damping ratio can be adjusted by the resistance. The step response of the output voltage, $V_{GS}$ in Figure 3.52 (b), is plotted in comparison of different damping ratios in Figure 3.53. Damping ratio smaller than 1 leads to large oscillation but faster-settling speed. A damping ratio greater than 1 leads to no oscillation in the step response but also slows down the transition. When driving a power

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**Table 3.4: Summary of the Test Bench Setup**

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>E-mode HEMT</td>
<td>EPC 2016 CL</td>
</tr>
<tr>
<td>$L_{Main}$</td>
<td>33 $\mu$H</td>
</tr>
<tr>
<td>$L_{Drain}$</td>
<td>0.5 nH + 10 m$\Omega$</td>
</tr>
<tr>
<td>$L_{Gate}$</td>
<td>2.5 nH</td>
</tr>
<tr>
<td>$V_{IN}$</td>
<td>70 V</td>
</tr>
<tr>
<td>$V_{Drive}$</td>
<td>5 V</td>
</tr>
<tr>
<td>Driver</td>
<td>7-bit segmented</td>
</tr>
<tr>
<td>Ramping pulse</td>
<td>2.5 $\mu$s</td>
</tr>
</tbody>
</table>
transistor, oscillation at the gate is not desirable because it would lead to more oscillation (also called ringing) elsewhere in the converter and often causes electromagnetic interference (EMI) issue. Particularly, in a GaN power converter, the large oscillation also introduces overshoot at the gate node of the output power transistors and needs to be mitigated for gate protection.

![Figure 3.52: The schematic of (a) gate driver and power transistor and (b) its simplified circuit representation.](image)

Figure 3.52: The schematic of (a) gate driver and power transistor and (b) its simplified circuit representation.

![Figure 3.53: Step response of the capacitor voltage with \(\omega_0 = 2\pi\) and different damping ratio \(\zeta\).](image)

Figure 3.53: Step response of the capacitor voltage with \(\omega_0 = 2\pi\) and different damping ratio \(\zeta\).
In the gate driver circuit, there are limited degrees of freedom in controlling the gate to source capacitance ($C_{GS}$) of a power transistor and the parasitic gate inductance ($L_G$) from the wire bonds. In order to control the damping ratio $\zeta$, the gate resistance $R_G$ is the more accessible parameter when compared to $C_{GS}$ and $L_G$. Therefore, the gate driver is divided into 7 segments, with different resistances. Each segment can be treated as a resistor that can be chosen for driving the power transistor. The layout of the gate driver is provided in Figure 3.54.

![Figure 3.54: Final gate driver block layout. The total area used is 1100 µm × 800µm.](image)

### 3.5.2 Fixed Driving Strength

The gate driver can be configured as a different gate resistance which affects the damping ratio. As an example, two segments with 8 Ω and 1Ω are used to drive the same power transistor. The step response of the gate to source voltage is shown in Figure 3.55 and the measurements of rise time and overshoot are shown in Figure 3.56.
Figure 3.55: Step response of the gate to source voltage $C_{GS}$ for a power transistor when driven by different gate driver segments.

(a) $R_G = 8 \, \Omega$

(b) $R_G = 1 \, \Omega$

Figure 3.56: Overshoot and rise time measurements of the step response for different gate driver segments.
Figure 3.57: Trade-off between overshoot and rise time with different gate resistance.

For the comparison between different gate resistances shown in Figure 3.56, the overshoot voltage and rise time are extracted. When the gate resistance is 8 Ω, the damping ratio is high and therefore no ringing is observed. The peak gate voltage maintains at 5 V which is safe for the gate, but the rise time is 15.3 ns. On the contrary, 1 Ω gate resistance reduces the damping ratio and therefore speeds up the transition (2.3 ns rise time) but causes large overshoot at the gate note which exceeds the maximum gate voltage of the GaN power transistor. The trade-off between overshoot and rise time are then examined with different gate resistance and plotted in Figure 3.57. With fixed gate resistance, the overshoot and rise time cannot be reduced at the same time.

### 3.5.3 Two-Stage Dynamic Driving Patterns

The dynamic gate driving method uses a large gate resistance in parallel with a small gate resistance, for instance, 1 Ω and 8 Ω from previous analysis. At the start of the transition, the gate driver is programmed to be 1 Ω to speed up the rise times. Near the end of the transition, the gate resistance is programmed to be 8 Ω to damp the ringing at the gate. This dynamic switching scheme can achieve a fast transition but without increasing the overshoot with the properly designed driving pattern. The step responses of dynamic driving and fixed driving are then compared in Figure 3.58.
Figure 3.58: Comparison of the gate voltage with different gate resistance configurations.

Figure 3.59: The waveforms of dynamic driving with 1 Ω and 8 Ω configuration.

Figure 3.60: Overshoot and rise time of dynamic driving.

A more detailed waveform for a two-stage dynamic driving pattern is provided in Figure 3.59. When the gate signal is sent to the gate driver, the driver is first configured to be 1 Ω for the $T_1$ amount of time and then switched to 8 Ω for in the middle of the turn-on process.
After $T_2$ amount of time, the gate driver resets to 1 Ω in preparation for the next switching cycle. The peak voltage for dynamic driving is reduced to 5.07 V while the rise time maintains 2.7 ns. This trade-off is better than the case with a fixed resistance.

![Fixed Gate Resistance](image)

Figure 3.61: Trade-off between overshoot and rise time for fixed driving and dynamic driving with different transition timing of 0.6 ns increment in $T_1$ and $T_2$.

With the same dynamic pattern (1 Ω - 8 Ω), the timing at which the gate configuration changes is also important for the trade-off. If $T_1$ is too long (using 1 Ω for most of the time), the effect of ringing damping is minimum and therefore there could still be ringing. If $T_1$ is too short (switching to 8 Ω too early), the rise time cannot be reduced, and more ringing might be introduced by the gate driver. Different timing has been simulated and compared in Figure 3.61 where both the $T_1$ and $T_2$ are incremented at a 0.6 ns step. There are some conditions where the dynamic driving is effective in reducing both overshoot and rise time. This dynamic driving scheme only changes the gate driving resistance once and therefore is called two-stage driving.
3.5.4 Analysis of Multi-stage Driving Patterns

The pattern generator has been designed to provide 8 transitions as described in Section 3.4.2, and therefore this gate driver can perform up to 8-stage driving if necessary. Therefore, it is useful to analyze the effectiveness of multi-stage driving and determine the optimum number of driving stage. To perform a fair comparison with the two-stage case (1 Ω – 8 Ω), the three-stage pattern is designed to switch from 1 Ω - 5.3 Ω - 8 Ω as shown in Figure 3.62. The driving pattern design methodology is the same as the two-stage case where 1 Ω is used for speeding up the turn-on and 5.3 Ω and 8 Ω are used for ringing damping.

The timing waveform is shown in Figure 3.63 and there are three timing windows labeled as $T_1$, $T_2$, and $T_3$. The overshoot voltage is damped to 5 V while the rise time is minimized.
to 2.7 ns. The overshoot and rise time trade-off between the two-stage (1 Ω - 8 Ω) and the three-stage driving (1 Ω - 5.3 Ω - 8 Ω) schemes are compared in Figure 3.65.

Both the two-stage and the three-stage driving demonstrate better trade-off than that of the fixed driving case. Both the transition times $T_1$ and $T_2$ for the two-stage driving are incremented by 0.6 ns. The three-stage transition times $T_1$, $T_2$, and $T_3$ are incremented by...
0.45 ns, 0.2 ns, and 0.45 ns, respectively. Therefore, the two-stage $\Delta(T_1 + T_2) = \Delta(T_1 + T_2 + T_3) = 1.2$ ns. As shown in the zoom-in trade-off plot in Figure 3.65 (b), the two-stage driving demonstrates higher sensitivity to timing, as both the rise-time and overshoot change a lot with changing timing. On the other hand, the three-stage driving shows higher resistance in timing as the change in both the overshoot and rise time is a smaller amount.

Figure 3.66: Trade-off comparison among 3 combinations of $R_G$ for three-stage driving.

The choices in the gate resistance at each stage are also influential to the trade-off. Aside from the 1 $\Omega$ - 5.3 $\Omega$ - 8 $\Omega$ combination, two other combinations 1 $\Omega$ - 2.28 $\Omega$ - 8 $\Omega$ and 1 $\Omega$ - 2.28 $\Omega$ - 5.3 $\Omega$ are investigated and the results are plotted in Figure 3.66. Comparing to the 1 $\Omega$ - 5.3 $\Omega$ - 8 $\Omega$ case, the other two combinations are more sensitive to timing in this particular set-up than 1 $\Omega$ - 5.3 $\Omega$ - 8 $\Omega$.

It seems that adding more stages in the dynamic driving can enhance the stability of the driver with respect to changing timing. The four-stage driving (1 $\Omega$ - 2.28 $\Omega$ - 5.3 $\Omega$ - 8 $\Omega$) is added into the comparison and the results are plotted in Figure 3.67. In comparison to three-stage, the four-stage shows less sensitivity to the changes in timing, but complexity in control and programming the gate driver increases. Moreover, the effort of looking for
the most suitable pattern for the four-stage case is also greater than that of the three-stage case. Therefore, it is recommended to choose between three-stage and four-stage driving but not to extend to five-stage or higher.

Figure 3.67: Trade-off comparison among different stages of driving.

3.6 Chapter Summary

The simulated power consumptions for the analog, digital and gate driver blocks are listed in Table 3.5. The chip performance could be further improved in two ways: a more compact package choice and the auto-routing/synthesis of the digital circuitry.

<table>
<thead>
<tr>
<th>Power Consumption</th>
<th>mW</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog Sensing Circuitry</td>
<td>2.29</td>
</tr>
<tr>
<td>Digital Dead-time Control (closed-loop enabled)</td>
<td>30.79</td>
</tr>
<tr>
<td>Gate Driver (one-side) $R_{OUT} = 0.5 , \Omega$ (all segments on)</td>
<td>289.1</td>
</tr>
<tr>
<td>Gate Driver (one-side) $R_{OUT} = 5 , \Omega$ (typical)</td>
<td>132.3</td>
</tr>
<tr>
<td>Gate Driver (one-side) 5-stage driving (optimized)</td>
<td>215.1</td>
</tr>
<tr>
<td>Gate Driver control Fixed driving (all segments on)</td>
<td>1.013</td>
</tr>
<tr>
<td>Gate Driver control 5-stage driving (optimized)</td>
<td>0.942</td>
</tr>
</tbody>
</table>
Figure 3.68: Micrograph of the gate driver IC, fabricated using TSMC’s 0.18 µm BCD GEN 2 process. The chip area is 5 mm × 3mm.

Figure 3.69: Bonding diagram of the gate driver IC chip in QFN 60.
The final gate driver chip occupies an area of 5 mm × 3 mm. The top-level layout blocks are labeled in the micrograph in Figure 3.68. This chip contains multi projects and therefore the top-side bond pads are not at the edge of this chip. The digital block is placed on the top left corner, as some of the digital I/O pads, such as controlling serial scan chain, are not required to be operated at high switching frequency. The parasitic of these bond wires does not affect the performance of this chip. The left pins are analog pins and the bottom and right edges are reserved for power outputs. The QFN 60 package is chosen for this gate driver IC due to the large chip size.

As shown in Figure 3.69, the bonding diagram of the packaged IC shows the short bond wires for power and analog pins (left, bottom and right edges) and long bond wires for the digital configuration I/Os on top.

This chapter presents the design of the proposed gate driver IC chip with an integrated dead-time controller and segmented driver. The simulation results of each module and their sub-blocks explain the design target and considerations of this chip. The driver is expected to perform on-chip dead-time control and segmented driving. However, due to one connection error, the segmented driving feature cannot be tested in this version. A new tape-out will be submitted to the next available shuttle run to fix this error. Chapter 4 will discuss the testing setup and testing results for this gate driver chip demonstrating all functions except for the segmented gate driving.
Chapter 4

Results and Discussion

This chapter presents the testing results of the designed gate driver IC chip. The experimental setup is described in Section 4.1. Section 4.2 demonstrates the functionality and discusses the test results for each block. Section 4.3 describes the SenseFET operational test and its performance in closed-loop dead-time correction. Section 4.4 provides a summary of the test results and issues encountered.

4.1 Experimental Setup

The fabricated IC is assembled in a QFN 60 package and soldered on a 2-layer PCB board as shown in Figure 4.1. The board is designed for testing both integrated and external SenseFETs for comparison purposes.

Furthermore, as mentioned in Section 3.4.3, the gate driver’s segment control block contains a mistake that could cause an overshoot in the gate voltage in certain situations and damage the driver. Therefore, the footprint for an external gate driver is reserved on the PCB for testing other on-chip functional blocks.

The test PCB board is designed to drive a half-bridge. The PCB includes multiple LDOs to supply different power rails on the IC, a 100 MHz oscillator to provide clock signal for the digital blocks, an FPGA connector to program the serial scan chains and 2 digital isolators to isolate the external FPGA from the power lines. Detailed descriptions of the major components are listed in Table 4.1. A picture of the final experimental setup is shown in Figure 4.2. Two oscilloscopes are used in order to monitor both the switching signals
and the digital status of the chip. The switching node is at 1 MHz to 10 MHz while the serial output is at 20 kHz range. The power HEMTs are 15-A rated devices.

![Figure 4.1: PCB board design for testing the QFN 60 packaged chip with different SenseFETs.](image1)

![Figure 4.2: Experimental test setup with an FPGA to control the serial scan chain for communication.](image2)
Table 4.1: Component List for the IC Test PCB

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
<th>No.</th>
<th>Model number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oscillator</td>
<td>100 MHz</td>
<td>1</td>
<td>SIT8008BI-21-33E-100G</td>
<td>Clock for digital</td>
</tr>
<tr>
<td>LDO</td>
<td>1.8 V</td>
<td>1</td>
<td>NCP1117ST18T3G</td>
<td>Power for digital</td>
</tr>
<tr>
<td>LDO</td>
<td>3.3 V</td>
<td>1</td>
<td>NCP1117ST33T3GOSCT</td>
<td>Power for analog</td>
</tr>
<tr>
<td>LDO</td>
<td>Adjustable</td>
<td>2</td>
<td>AZ1117H-ADJTRE1</td>
<td>Power for drivers</td>
</tr>
<tr>
<td>LDO</td>
<td>Adjustable</td>
<td>1</td>
<td>LDCL015MR</td>
<td>Power for sense gate</td>
</tr>
<tr>
<td>Isolator</td>
<td>5 KV</td>
<td>2</td>
<td>SI8650BD-B-IS</td>
<td>Protect FPGA</td>
</tr>
<tr>
<td>NMOS</td>
<td>240 V</td>
<td>1</td>
<td>ZVNL120A</td>
<td>Silicon SenseFET</td>
</tr>
<tr>
<td>Driver</td>
<td>4 A</td>
<td>1</td>
<td>LM5113SD/NOPB</td>
<td>Backup gate driver</td>
</tr>
<tr>
<td>HEMT</td>
<td>15 A</td>
<td>1</td>
<td>GPI6501510</td>
<td>E-mode GaN HEMT</td>
</tr>
<tr>
<td>SenseFET</td>
<td>15 A</td>
<td>1</td>
<td>Customized</td>
<td>Integrated SenseFET</td>
</tr>
</tbody>
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4.2 Functionality Test Results

The three major circuit blocks on the proposed gate driver IC are the dead-time control block, the reverse conduction detection block and the time to digital converter. Their testing results will be presented and analyzed in this Section.

4.2.1 Dead-time Control

In order to achieve a one-step dead-time correction for a synchronized buck converter, the duty cycle of the HS gate signal is designed to be stable while the dead-times are being adjusted. Therefore, the 2 phase non-overlapping clock generator is modified to provide a constant duty cycle as described in Section 3.3.2.

As shown in Figure 4.3, the HS and LS gating signals are presented at minimum dead-time and maximum dead-time settings. The duty cycle of the HS gating signal remains constant while the dead-time settings change on both edges. It is essential to minimize the potential distortion of the duty cycle introduced by dead-time adjustment, as the varying duty cycle can disturb the converter’s behavior by changing its output voltage and load condition.
The measured digital dead-time on both the rising and falling edges are plotted against the simulated value, as shown in Figure 4.4. Dead-times on both edges demonstrated constant offsets. The offset at the falling edge is intentionally inserted to compensate for the propagation delay from the level shifter to reduce the chance of shoot-through when both dead-times are set at 0. The offset at the rising edge could be due to the signal buffers.

The constant offsets of the dead-times are measured to be 4.2 ns and 0.8 ns, on the falling and rising edges, respectively. The actual resolution of the delay chain used in the dead-time controller is calculated to be 0.327 ns with the best curve fitting, slightly different from the post-layout simulation result 0.32 ns.

Figure 4.3: Measured dead-time control and high-side duty cycle. (a) The top graph is the minimum dead-time setting (b) The bottom graph is the maximum dead-time setting.
Figure 4.4 Measured dead-time control shows constant offsets.

Figure 4.5: Measured dead-time errors without the constant offsets are within a ±1 ns window.

Figure 4.6: Duty cycle distortion lies within 0.1% (1 ns) for full range dead-time control for 1 MHz switching.
4.2.2 Reverse Conduction Detector and TDC

The output of the reverse conduction detector is not connected to any I/O pad to avoid changing its load condition. Therefore, the comparator test can only be approached indirectly via the TDC as shown in Figure 4.7. A small negative pulse is first generated by the external FPGA and pulled down by a capacitor and resistor. The pulse is then shifted below ground level. The reverse conduction detection block measures this pulse and produces a digital pulse. This pulse is then quantized by the TDC and the final digital output representing the pulse width is read by the serial scan chain.

![Figure 4.7: Circuit configuration for the comparator test relies on the TDC](image)

One example of the comparator testing method is illustrated in Figure 4.8. The input generated by FPGA is measured to be 37 ns. This negative pulse is fed to the input of the comparator and the output of the TDC is read to be 1110110 which equals 118 in decimal. Each bit of the TDC is 0.32 ns, and therefore the output of the TDC is 37.76 ns.

Following a similar fashion, the comparator and TDC outputs are measured under different modes. The results of the two modes are plotted in Figure 4.9. When the test pulse is shorter than 15 ns, it is better to tune the signal conditioner to its minimum setting ($B = 000$) for maximum shifting amount which increases the sensitivity of the comparator. However, as
the pulse width increases, the error accumulated in the delay chain of the TDC starts to make the TDC output lower than expected. This issue needs to be fixed in the next design.

Figure 4.8: One example of the testing sequence is presented. The purple negative pulse is generated by FPGA and the serial output is read by the scan chain.

Figure 4.9: Comparator output for two different modes: $B = 000$ (referring to Figure 3.3) is more suitable for narrower pulse width and $B = 111$ is more suitable for wide pulse.
In the current design, if the reverse conduction pulse is known to be larger than 15 ns and it is not required to detect pulse width below 10 ns, the configuration control can be adjusted to a less sensitive mode ($B = 111$). The TDC output configured with minimum accuracy shows better linearity at wider reverse conduction pulse. An automated control algorithm can be implemented to shift between modes of the configurations.

Combining the results from the two comparator configurations mentioned above, the TDC output agrees with the theoretical result, as shown in Figure 4.10. The differential non-linearity (DNL) from the comparator mismatch and the TDC quantization errors are plotted in Figure 4.11. The final optimized TDC output exhibits an average error of 0.96 ns (3 bits). When the pulse width approaches the maximum range of the TDC (42 ns), the TDC output error increases to 1.28 ns (4 bits). When the pulse width is under 5 ns, the TDC output is within 0.66 ns (2 bit) which agrees with the assumption that most of the errors are from the accumulated errors of the delay chain used in the TDC.

![Figure 4.10: TDC output under optimized configurations. $B = 000$ for pulse width smaller than 15 ns and $B = 111$ covers pulse width greater than 15 ns.](image-url)
Figure 4.11: Comparator mismatch and TDC quantization error are within 4 bits (1.2 ns).

4.3 Integrated SenseFET

The effectiveness of the clamping circuit is verified experimentally using either an external silicon MOSFET as the SenseFET or an integrated GaN SenseFET. Two boards containing identical components except for the SenseFETs are tested. A comparison between the SenseFETs is first presented followed by the analysis of their performance in a closed-loop dead-time correction.

4.3.1 SenseFET Operation

The clamping voltage is plotted as a function of the input voltage \( V_{IN} \) and a function of gate voltage \( V_{G,sense} \), separately. Figure 4.12 (a) shows that for a constant gate voltage at 1.5 V, the detection voltage gradually increases with increasing input voltage, proportionally to the product of \( V_{IN} \) and drain to source capacitance \( (C_{DS}) \). The \( C_{DS} \) of a SenseFET is also a drain voltage dependent parameter which decreases as \( V_{IN} \) increases. Therefore, the detection voltage as a function of \( C_{DS} \) gradually saturates to a limited value. In Figure 4.12 (b), the detection voltage increases linearly as the gate voltage increases. The silicon SenseFET exhibits a lower clamping voltage possibly due to its larger \( C_{DS} \) and larger threshold voltage.
The tracking accuracies for both SenseFETs have been examined. The measurement of the negative pulse width is taken at the level of \(-100\) mV for both the switching node and the Sense nodes. Due to the larger capacitance of the silicon SenseFET, as mentioned above, its charging and discharging times are longer than the GaN power HEMT, leading to a greater variance in the measured reverse conduction pulse. The additional parasitic inductance resulted from the silicon packaging also contributes to the tracking offset. One example of the testing waveform from the oscilloscope is shown in Figure 4.13.

The tracking accuracy is summarized in Figure 4.14. The reverse conduction measured at the switching node exhibits a standard deviation of 500 ps, the tracking signals also carry this standard deviation. Both the silicon and GaN SenseFET measurement results show good agreement with the actual reverse conduction durations. However, the sensed reverse conduction duration from the silicon MOSFET shows a larger discrepancy when compared to its GaN counterpart. As a result, the GaN SenseFET shows better fitting to the expected value.
Figure 4.13: Tracking accuracy comparison between two SenseFETs with $V_{IN} = 5\,V$ and $V_{G,sense} = 2\,V$. (a) an external silicon SenseFET or (b) an integrated GaN SenseFET.

Figure 4.14: Sensed reverse conduction duration (with error bars) as a function of the actual reverse conduction.
4.3.2 Programmable Correction Mode

With the external silicon SenseFET, the additional parasitic inductance from packaging and its higher $C_{DS}$ capacitance leads to slower switching speed and contributes to tracking errors. When the one-step correction is performed on the silicon senseFET, this error could lead to large overshoots as shown in Figure 4.15. This issue can be mitigated by using a gradual correction mode and program a target dead-time value (referring to $D_T$ from Figure 3.26) as a safety margin.

Figure 4.15: Closed-loop dead-time correction with a silicon SenseFET demonstrates over-correction under one-step mode due to the error from the detection circuit.

Figure 4.16 demonstrates the GaN measurement results from the GaN integrated SenseFET test bench. The falling edge is programmed to perform gradual correction mode while the rising edge is set to one-step correction mode with some pre-et target $D_T$ as a comparison. In the gradual correction mode, the constant speed is set to be 12.5% leading to a slow correction requiring more than 10 switching cycles, as shown in Figure 4.16 (a). On the other hand, the rising edge highlighted in Figure 4.16 (b) is corrected within one switching cycle. In both cases, the overshoot voltage has been suppressed.
4.4 Chapter Summary

One main purpose of the chip is to maintain optimal dead-time with on-chip closed-loop correction while reducing shoot-through current and reverse conduction durations. This function allows the switch-mode power converters to work with optimal efficiency across various load conditions, as shown in Figure 4.17. The blue line represents the efficiency plot with a large dead-time (20.48 ns) showing that over-shoot current can be avoided at light load but could lead to power loss due to reverse conduction at heavy load. On the other hand, the red line presents the efficiency plot with short dead-time (4.8 ns) which
reduces the reverse-conduction at heavy load but causes shoot-through at small load conditions. The adaptive dead-time control, the system operates under the optimum condition for a range of load condition and maintain high working efficiency.

Figure 4.17: Measured power conversion efficiency for fixed and adaptive dead-times at

\[ V_{IN} = 20 \text{ V}, \quad V_{OUT} = 12 \text{ V}, \quad f_{SW} = 1 \text{ MHz} \] with all losses included.

Table 4.2: Chip Performance Summary

<table>
<thead>
<tr>
<th>Technology [µm]</th>
<th>0.18</th>
</tr>
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<tbody>
<tr>
<td>Chip Size</td>
<td></td>
</tr>
<tr>
<td>Total [mm×mm]</td>
<td>5×3</td>
</tr>
<tr>
<td>Digital [mm×mm]</td>
<td>1×0.8</td>
</tr>
<tr>
<td>Detection Circuitry [µm×µm]</td>
<td>115×140</td>
</tr>
<tr>
<td>Gate Driver Size [mm×mm]</td>
<td>1.1×0.8</td>
</tr>
<tr>
<td>E-mode GaN Maximum Switching frequency [Hz]</td>
<td>10×10^6</td>
</tr>
<tr>
<td>Tested Reverse Conduction Detection Accuracy [ns]</td>
<td>0.66</td>
</tr>
</tbody>
</table>

Simulated Propagation Delay @ \( V_{IN} = 70 \text{ V} \) (ns) |

<table>
<thead>
<tr>
<th></th>
<th>HS</th>
<th>LS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rising edge</td>
<td>11</td>
<td>5.6</td>
</tr>
<tr>
<td>Falling edge</td>
<td>13</td>
<td>6.1</td>
</tr>
</tbody>
</table>

A summary of the chip performance is listed in Table 4.2. The chip performance is mainly limited by the top layout synthesizing and the delay chain linearity from the TDC.
Chapter 5

Conclusions and Future Work

5.1 Conclusions

The overall focus of this thesis is to design a smart gate driver for enhancement mode (E-mode) GaN high electron mobility transistors (HEMTs). There are three main contributions in this thesis. The first one is the development of a SenseFET clamping circuit for reverse conduction sensing. A capacitive model is also derived, simulated and experimentally verified. The next contribution is the design of a smart gate driver IC with dead-time correction and segmented driving. The last contribution is the design of the integrated GaN SenseFET using the latest GaN IC techniques. As a pre-production ready GaN IC design, the modeling, routing, and layout are manually calibrated.

5.1.1 Detection of Reverse Conduction

The main contribution of this thesis is the presentation of a novel method to detect the occurrence of reverse conduction in E-mode HEMTs, as discussed in Section 2.2. This technique directly monitors the high voltage switching node using a novel clamping circuit during the reverse conduction when the high-side and low-side power transistors are both switched off. The clamping circuit is designed to track the reverse conduction while blocking the high input voltage at the switching node. The clamping level is determined by the type of E-mode HETMs and their intrinsic capacitances such as $C_{GS}$, $C_{DS}$, and $C_{GD}$. A simplified capacitive divider model is developed as a design guideline to determine the
clamping voltage. In Section 4.3, experiments demonstrated that the proposed technique with minor adjustments to account for the voltage dependent capacitances.

Different from previous reported reverse conduction sensing techniques for E-mode GaN HEMT, this technique can monitor the switching node during normal operation and reverse conduction. The SenseFET clamping circuit protects the detection circuit from the high supply voltage. Therefore, this technique can generate a signal that corresponds to the duration of the reverse conduction signals and continuously corrects for the optimum dead-time for the integrated gate driver. Discrete silicon MOSFETs can also be used as the voltage clamping SenseFET and is verified experimentally. However, the slower speed of the silicon SenseFET limits the detection accuracy of the reverse conduction and hence the correction for the optimum dead-time.

The proposed dead-time correction technique is compatible across different types of E-mode GaN HEMT and even power MOSFETs (as long as the clamping voltage for SenseFET is properly designed). It should be pointed out that the compatibility depends on the device capacitances, which is a reflection of the device optimization techniques. The clamping capacitive model needs to be customized for each device. In addition, since these capacitances are voltage dependent, the first order assumption may not hold and simulations are required to determine a suitable constant gate voltage for the SenseFET as demonstrated in Chapter 2. In addition, the conditioner can be tuned to achieve the best detection accuracy depending on the reverse conduction (or body diode conduction for MOSFET) characteristics.

5.1.2 Dead-time Correction

The proposed gate driver IC consists of two main functions: the dead-time correction and the dynamic gate driving. The dead-time correction technique requires a reverse conduction detector which is capable of tolerating negative input pulse. This function is designed and integrated into this IC with a tunable conditioner for the reference voltage adjustment as the reverse conduction characteristics vary among different E-mode HEMTs.
The proposed on-chip reverse conduction detector can successfully detect the negative pulse and generate a digital pulse that with less than 0.5 ns error.

The dead-time duration digitization system is first implemented using time to digital converter (TDC) constructed with delay chains. The delay uniformity among the cells is not the main target of the current design, and therefore only the basic functionality for testing is carried out. In Chapter 4, the experimental results show that for duration smaller than 15 ns, the delay chain error insignificant. However, for pulses approaching the 40 ns range, the non-linearity of the delay chain cannot be neglected as it affects the TDC accuracy.

The dead-time adjustment mode is controlled using an on-chip state machine. The dead-time can be user selected to a different speed, depending on the application. Instability due to overcorrection is achieved by setting a slower target dead-time value as a safety margin. With this correction system, a GaN-based buck converter demonstrates optimal dead-time operation over its full range of load conditions. It is also possible to program a multi-speed correction system using an external FPGA or switch to an on-chip integrated CPU in the future versions for more flexibility in controllability.

5.1.3 Gate Ringing Suppression

The dynamic gate driver is designed with 7 different gate resistances and 7 pairs of pattern generators for the dynamic gate resistance adjustment. Each pattern generator allows 8 distinct steps within one transition cycle which greatly improves the flexibility of the driver compares to our previously published work [37, 85, 90]. Moreover, the resolution for each step can be fined tuned by changing the bias current for the delay chain ranging from 500 ps. This adjustable resolution allows the dynamic gate driver to be used for different E-mode power HEMTs with a wide range of gate capacitances. A pre-determined optimal pattern has been designed. The goal is to only adjust the biasing current for suppressing gate ringing on different E-mode power HEMTs.
Different gate driving patterns have been programmed to suppress ringing without sacrificing the fast turn-on and turn-off transition speed of E-mode GaN power HEMTs. All the patterns are first simulated under the same biasing current, and the one with the best performance is selected. The biasing current is then tuned to investigate if there could be further performance improvement. Simulation results show the adjustment of biasing current could optimize the trade-off between transition time and gate ringing as discussed in Section 3.5.

5.2 Future Work

5.2.1 IC Improvement

Future work needs to focus on how to further improve the detection accuracy of the proposed reverse conduction detection. The first improvement is to employ an on-chip signal filter to avoid false triggering brought by the switching node ringing. In addition, the time to digital converter requires an improved delay chain. This delay chain could better quantize the detected pulse width. The next improvement should be the employment of on-chip LDOs for providing reference voltage and bias current. This could eliminate many unnecessary testing pins while providing more accurate bias.

Furthermore, the in-house developed SPRUCE CPU [85] could be incorporated in this chip to simply digital controls, including providing the clock signal for digital blocks and generating the gating signal from the DPWM block. This could save an off-chip ring oscillator, extra pins, and the need for an off-chip FPGA. Without many of the testing pins, the chip package could be greatly reduced from 5 mm $\times$ 3 mm to at least 2 mm $\times$ 3 mm (60% reduction in area). The length of the bond wires could be shortened leading to suppress EMI which large switching current.

The on-chip CPU also allows more complicated closed-loop control, signal monitoring with ADCs, and on-chip digital filtering as previously designed in [85]. The first edition
of the closed-loop control of dead-time has been implemented with 4 different correction speeds: 100%, 50%, 25%, and 12.5%. The current feedback can be programmed with one of the four speeds or as described in Equation (4.2) in order to provide a more tailored function for different applications.

5.2.2 Additional SenseFET Function

The proposed E-mode GaN SenseFET has only been used for dead-time detection. This SenseFET could also be used to drain current sensing. The layout of the integrated SenseFET should be improved as the current layout is not symmetrical and the gate node of this SenseFET should not be placed next to the high voltage drain pad. This current SenseFET could also be used for peak current detection as proposed in previous work [37] with current comparator and on-chip adjustable current DAC.

5.2.3 Incorporation of Active Gate Driving

Since the switching node ringing propagates to the clamping circuit. This could lead to possible false triggering in the detection block. The gate voltage ringing might also damage the gate of E-mode HEMTs with low maximum gate voltage tolerance. It is important to suppress the gate ringing with an active gate driving technique without slowing down the gate turn-on and turn-off switching time. The gate resistance can be changed to a small value at the start of the turning on sequence to speed up the switching and changed to a larger value near the end of the transition to damp the gate ringing.

The segmented gate driver with a programmable driving pattern has been designed and incorporated into the gate driver IC. However, this function is not available for this version. Moreover, the proposed gate driver is built using 5 V devices at the output stage in this version while the most efficient driving voltage for E-mode GaN HEMT is around 6 V for reducing $R_{on}$ but should not exceed 7 V for gate protection. The next design should incorporate LDMOS transistors with a higher breakdown voltage.
Figure 5.1: Segmented gate driver with dynamic driving strength co-packaged with E-mode GaN HEMT using 8 I/O pins and 1 ground thermal pad.

In the next version, this dynamic driving IC should also be co-packaged with the E-mode GaN power HEMT as shown in Figure 5.1 as an integrated module. The user can select the pre-programmed pattern and choose the suitable biasing current for overshoot suppression and switch loss reduction.
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Appendices

Appendix A. Layout Techniques for Large Devices

In GaN power HEMT design, the layout of large area multi-finger devices must be considered for device thermal stability, breakdown performance while suppressing leakage current and reducing on-resistance [91]. A commonly used multi-finger layout is shown in Figure. A.1. The source and drain fingers have comb-like shape, and the gate finger passes through the spaces between them.

Figure. A.1: Micrograph of a fabricated wafer sample. The source and drain metal fingers became dark brown color due to thermal annealing. The gate fingers are thin gold metal wires.

When scaling up the GaN HEMT, the defect density of the epi-wafer, the misalignment of the photolithography and non-uniformity of the metal lift-off process start affect the yield of the devices. Prior to design the actual SenseFET, a number of devices have first been designed and tested at TNFC in order to study the multi-finger behavior of an E-mode GaN device. Three layout techniques: leakage suppression, breakdown voltage enhancement, and on-resistance reduction have been investigated.
Appendix A.1. Leakage Suppression

When the W/L ratio of a HEMT increases from 25 to 5500 (220 times), the drain to source ($I_{DS}$) leakage current increases by more than 1000 times. In mesa isolated devices, the leakage path between drain and source could possibly come from three sources: the mesa edge leakage, the sidewall leakage, and the isolation leakage, as shown in Figure. A.2[92]. In an un-passivated (without SiN) device, the main leakage path is type-A leakage coming from contact between the gate metal and the mesa edge [93, 94]. As for the passivated device (with SiN), the leakage paths type-B and type-C dominate, where type B comes from the short circuit between SiN interface and the mesa side wall [92].

Figure A.2: Major leakage paths of a mesa isolated GaN device [92].

Since the current designed devices are all passivated, the gate mesa leakage might not increase too significantly. The remaining leakage paths are type-B and-C. With finger off mesa design, there is more type C leakage while with finger on mesa design, there is more type B leakage. Moreover, shrinking the mesa area can decrease the probability of
encountering epitaxial defects. Experiments have been conducted to identify the more dominate leakage path between type B and type C and potential methods to suppress it. After identifying all the possible leakage paths, the layout of the multi-finger device could then vary between two styles: gate fingers off the mesa Figure. A.3 (a) or gate fingers on mesa (b).

![Figure A.3](image)

Figure. A.3: Two 50-finger devices (W/L = 5500) have identical device parameters and placed side by side in the mask. (a) Left device (number 10): G/S/D fingers off the mesa and (b) right device (11): G/S/D fingers on the mesa.

For fair comparison, two of the tested layout styles are places side by side in the mask. Device 10 has a smaller mesa area such that the end of the gate pattern runs off the mesa, and device 11 has a larger mesa area such that all the source/drain and gate fingers are on the mesa. A few of these pairs are placed on different locations of the mask. The fabricated devices are tested, and their ON/OFF behaviors are shown in Figure. A.4 and Figure. A.5. The conducting current of both DUT types is around 60 mA as shown in Figure. A.6 and Figure. A.7. The leakage current of the off-mesa design is more stable compared to the on-mesa design. are show the threshold voltage, gate leakage and transconductance measurement for these two types of devices.

The devices with fingers of the mesa show a more stable gate and drain leakage current, from 10 to 100 µA. The devices with gate on the mesa show leakage current from 3 µA to 0.7 mA. Therefore, the gate “off-mesa” design shows a more stable leakage current behavior but not necessarily reduce the total leakage current. In the current design, “off mesa” is selected for a more stable leakage behavior.
Figure A.4: Measurement of 5 DUT 10 (fingers off mesa) ON/OFF characteristics.

Figure A.5: Measurement of 5 DUT 11 (fingers on the mesa) ON/OFF characteristics.
Figure. A.6: Measurement of the leakage current for four type 10 devices (finger off mesa).

Figure. A.7: Measurement of leakage current for five type 11 devices (finger on mesa).
Appendix A.2. Breakdown Enhancement

Breakdown voltage is a very important characteristic of power devices. Oval finger end style is a potential layout technique to prevent premature breakdown. The oval ratio is the deviation from a perfect semi-circle at the tip of the finger (ratio between the major axis and minor axis, $b/a$). The devices are designed to have the same parameters except for the oval ratio. The final areas of these devices are the same, as shown in Figure. A.8.

After testing these devices, it can be confirmed that a larger oval ratio can increase the breakdown voltage and suppress leakage current as shown in Figure. A.9. The increasing oval ratio can also reduce the leakage current.
On the other hand, the increased area between the gate and drain could also affect the on-resistance of the device. Therefore, the device on-resistance and breakdown voltage are plotted with an increasing oval ratio in Figure. A.10. The breakdown voltage keeps increasing due to the additional gate to drain distances ($L_{GD}$). On the other hand, the on-
resistance decreases slightly and then ramps up. The resistance drop could be from a better current flowing path when the oval ratio is small but rises again as the resistance introduced by increasing $L_{GD}$ dominates.

In order to analyze the trade-off between breakdown voltage and on-resistance, the figure of merit (FOM) of the tested device is plotted as shown in Figure A.11 and compared to silicon limit line with on-resistance converted into specific on-resistance ($R_{on,sp}$) by multiplying the device area. The trade-off points of the measured devices sets in between the silicon LDMOS limit line and the silicon theoretical limit line, as the oval ratio increases from 1 to 1.8. Therefore, in the actual SenseFET layout, the oval ratio should be designed to be 1.8 at the drain side.

![Figure A.11: Trade-off between $R_{on}$ and BV.](image)

**Figure A.11: Trade-off between $R_{on}$ and BV.**

### Appendix A.3. On-resistance Reduction

To further reduce the on-resistance for higher energy efficiency, the layout is designed to have wider fingers near the base and narrower near the tip. This taper angle design allows better source and drain metal conduction path and is expected to provide lower overall on-resistance.
The number of fingers is kept constant and the resulting device area increases accordingly as shown in Figure. A.12. Therefore, the taper angle cannot be increased without considering the additional area added to the device which also increases $R_{on,sp}$. A fabricated device with a 2-degree taper angle under a microscope is shown in Figure. A.13.

Figure. A.14 shows that an increase in taper angle has little impact on the leakage current or the breakdown voltage in particular. The main effect of the taper angle is the reduction of on-resistance ($R_{on}$) with the increase in taper angle, as shown in Figure. A.15. However, as a larger taper angle also leads to larger device area ($A$), then the specific on-resistance
\( R_{on,sp} = R_{on} \cdot A \) needs to be evaluated. Therefore, the taper angle should not be too large and needs to be carefully calibrated for an optimal trade-off point.

![Graph showing leakage current vs. taper angle]

Figure. A.14: Taper angle has no obvious effect on the leakage current but with a slightly enhanced BV.

![Graph showing Ron and Ron,sp vs. taper angle]

Figure. A.15: Taper angle decreases the \( R_{ON} \) but increases the \( R_{on,sp} \).
The FOM is plotted in Figure. A.16 and the optimal taper angle is either 2 or 3 degrees. Therefore, in the SenseFET layout design, the taper angle should be between 2 and 3 degrees.

![Figure. A.16: FOM figure as a function of taper angle (unit: degrees).](image)

**Appendix B. Development of GaN SenseFET**

Both depletion-mode (D-mode) and enhancement mode (E-mode) GaN power high electron mobility transistors (HEMTs) have metal gate stacks (typically nickel and gold Ni/Au) [95, 96]. One of the project objectives is to integrate a SenseFET into the GaN power HEMT in order to reduce package complexity and improve system performance. Therefore, it is worth investigating the general process of GaN HEMT and the common layout techniques to help with the design of the SenseFET structure.

A typical process flow for GaN power HEMTs and the corresponding masks used are described below. The cross-sectional views are not drawn to scale to better distinguish some of the small features. The AlGaN layer is first etched away to form the mesa isolation structure as shown in Figure. B.1. The ohmic contacts normally consist of a Ti/Al/Ni/Au metal stack [91, 97], followed by rapid thermal annealing (RTA) at 850 °C [95, 98] as shown in Figure. B.2. The gate metal stack Ni/Au is then deposited on top of the AlGaN
layer as shown in Figure. B.3. After Si₃N₄ passivation, the pad opening is formed, and the top pad metal is then deposited as shown in Figure. B.4.

Figure. B.1: Mesa etching process flow (a) wafer cleaning (b) mesa mask photolithograph.

Figure. B.2: Ohmic contact process flow (a) photolithography using negative photoresist (PR) (b) metal evaporation (c) lift-off and RTP.
Figure B.3: Schottky contact process flow (a) photolithography using negative PR (b) metal evaporation (c) lift-off.

Figure B.4: The remaining process flow (a) Si$_3$N$_4$ PECVD (b) Pad metal deposition.
Appendix C. GaN HEMT Fundamentals

This section will provide a discussion on the popular GaN High Electron Mobility Transistor (HEMT) applications in the power industry followed by a background introduction on GaN HEMTs through a comparison between intrinsic depletion-mode (D-mode) and enhancement-mode (E-mode) HEMTs.

Appendix C.1. Intrinsic Depletion-mode HEMTs

To further illustrate the working mechanism of the GaN HEMTs, its cross-sectional view is provided in Figure. C.1 (a). GaN HEMTs normally are 3-terminal devices without body contact. The source and drain are Ohmic contacts while the gate is a Schottky contact.

![GaN HEMT Structure](image)

Figure. C.1: The basic D-mode GaN HEMT structure and its energy-band diagram.

The conduction of GaN HEMTs relies on a sheet of two-dimensional electron gas (2DEG) located between AlGaN and GaN layers [23]. This sheet of electron gas is induced by the piezoelectric effect between two lattice-mismatched layers [99]. Figure. C.1 (b) shows the energy-band diagram of the device under the gate region along the vertical direction. The
sharp conduction band bending forms a valley, allowing electrons to be confined. As a result, the 2DEG is free to move along the x- and z-directions (pointing into the page).

Figure C.2: (a) Cross-sectional view of a HEMT and (b) its energy band diagram along AA’ cutline [100].

The inherent 2DEG provides an abundance of high mobility electrons resulting in a low resistive path between the source and drain electrodes [101]. Since the existence of 2DEG is intrinsic and if there are no special techniques used to disturb the 2DEG, the HEMT is a normally-on device. This normally-on transistor can be turned off by applying a negative voltage to the gate. The sheet of 2DEG under the gate region can thus be depleted (Figure. C.2). The D-mode HEMT exhibits an intrinsic negative threshold voltage. While the D-mode GaN HEMTs are the first to emerge in the power electronics industry, the development of “normally off” enhancement mode (E-mode) HEMT is rapidly progressing.

Appendix C.2. Enhancement-mode HEMTs

Enhancement mode (E-mode) HEMTs are more desirable for power electronic circuits due to their “normally-off” characteristics. This type of device can be turned on by applying a positive voltage to the gate electrode. Various techniques have been reported for producing
E-mode HEMTs. The fundamental mechanism of these techniques is to disrupt the 2DEG under the gate region with the absence of a gate voltage. Such techniques include MIS-HEMT, floating flash gate structure, fluoride-based plasma treatment, recessed gate structure, and a combination of these techniques (Figure. C.3).

The MIS-HEMT structure has an insulating layer with a high dielectric constant (high-κ) between the gate electrode and the AlGaN layer. This insulating layer can effectively block the gate leakage current. The quality and the selection of high-κ materials have a great impact on the device performance [105]. However, the presence of the insulator cannot completely disturb the 2DEG. The realization of enhancement mode relies on reducing the AlGaN thickness to reduce the 2DEG concentration.

The p-GaN structure has a layer of selectively epitaxial grown p-type GaN in the gate area [30, 31] in between the gate electrode and the AlGaN layer. The presence of p-GaN can deplete the 2DEG channel underneath the gate due to the formation of a pn junction, and
therefore this device is normally off without gate bias. With a positive gate bias, electrons are induced back into the channel and therefore resuming the conduction path between the source and drain. The threshold voltage for this type of device is around 1 V which is relatively low for power application [30, 31].

The fluoride-based plasma treatment method can adjust the threshold voltage without degrading channel conductivity or introducing extra photolithography steps. However, the plasma damage on the AlGaN layer can cause reliability issues: the shifts of the threshold voltage in the negative direction after the electrical stress test [108]. This threshold voltage drift is caused by the lack of practical technique to maintain the fluoride ions in the device [110].

The recessed gate HEMT has a selective AlGaN thickness reduction under the gate. Because the 2DEG concentration strongly depends on the thickness of the AlGaN layer, the 2DEG located in this thin AlGaN region is disrupted and thus normally-off characteristics can be achieved [104]. The key technical difficulty in this type of structure is the precise control of the reactive ion etching (RIE) while maintaining proper AlGaN morphology. The recessed gate can provide high transconductance, high saturation current, and high breakdown voltage while suppressing the occurrence of current collapse [105].

To sum up, Table. C.1 provides a comparison of the techniques. Combinations of these techniques have also been reported in order to provide improved performance and eliminate potential issues at the cost of increasing fabrication complexity. The $p$-GaN gate structure, among all techniques, appears to be the most favorable and reliable in the market right now.
Table. C.1: A Summary of Threshold Adjustment Techniques [102]

<table>
<thead>
<tr>
<th>Method</th>
<th>MIS structure</th>
<th>$p$-GaN</th>
<th>F-plasma</th>
<th>Recessed gate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Advantages</td>
<td>Low leaking current</td>
<td>Higher gate operational voltage</td>
<td>High Current density</td>
<td>Suppress current collapse, no extra material involved</td>
</tr>
<tr>
<td>Disadvantages</td>
<td>Current, degradation, controllability</td>
<td>Additional epitaxial growth</td>
<td>Controllability, reliability, AlGaN damage</td>
<td>AlGaN damage, controllability, gate leakage</td>
</tr>
<tr>
<td>Fabrication Difficulties</td>
<td>ALD</td>
<td>$p$-GaN growth</td>
<td>F-ion implant</td>
<td>RIE self-stop, recess depth control</td>
</tr>
</tbody>
</table>

Appendix C.3. D-mode Driving Challenges

D-mode devices can be driven either by applying negative voltage or cascode [112] with a low-voltage E-mode silicon LDMOS. The development of D-mode GaN HEMTs focuses on the cascode structure shown in Figure. C.4 rather than direct driving with negative voltage [12]. A power failure could cause the removal of the negative gate voltage, turning the device back on. This method might draw safety concerns.

![Figure. C.4: Device structure showing the cascode structure of GaN HEMT and LDMOS](image)

The cascode structure requires an E-mode MOSFET preferably an n-type LDMOS with a low voltage rating (around 20 V) to ensure low on-resistance. The source of the GaN HEMT is connected to the drain of the MOSFET and the gate of the HEMT is shorted to the source of the LDMOS. The gate signal is applied to the LDMOS. When the gate is on, both devices conduct the same current. The conduction loss comes from the sum of the $R_{ON}$ from both devices. Therefore, the LDMOS should be chosen with adequate current...
Conduction capability to minimize the conduction loss in order to enjoy the low $R_{ON}$ of the GaN HEMT.

When the gate of the LDMOS is turned off, the high voltage is blocked by both devices with a pre-determined voltage distribution. Therefore, it is important to make sure that the $V_m$ node (referring to Figure. C.4) has a high enough voltage to create a negative $V_{GS,GaN}$ for turning off the GaN HEMT but not too high such that $V_m$ exceeds the breakdown voltage the silicon LDMOS. An equivalent capacitive model is useful to determine the size of LDMOS for the desired $V_m$, as shown in Figure. C.5 [37].

![Figure C.5: Main parasitic capacitance in a cascode structure with its capacitive divider equivalent model [37].](image)

The capacitive divider model is determined by the drain to source capacitance $C_{DS,GaN}$ and $C_{DS,MOS}$, which is given by [37]:

$$V_m \approx V_{pdd} \cdot \frac{C_{ds,GaN}}{C_{ds,GaN} + C_{ds,MOS}} \quad (C.1)$$

Equation (C.1) implies that the capacitor matching will become a significant factor for the performance of the cascode module. Therefore, the choice of packaging also plays an important role for this structure. The bonding of the two dies (GaN and MOSFET) are normally connected inside one package to reduce wire inductance, as these inductances are
crucial for the switching performance of the cascode structure. A well-packaged structure can also ensure matching junction capacitance. There is currently one vendor (Texas Instrument) selling cascode modules on a large scale and only a couple of companies working on the gate drivers for cascode modules (VisiC [113]). Their driving methods are similar: driving the silicon LDMOS with conventional silicon MOSFET gate drivers. TI has moved one step ahead by integrating the gate driver IC and the GaN power device in one package [12].

The lack of dedicated D-mode GaN gate drivers leaves the driving challenges unresolved. As most gate drivers still require external pull-up and pull-down gate resistance, the trade-off between active ringing and transition speed is not optimized. Extra packaging and passive devices also add extra PCB space and parasitic which directly relate to cost increase and performance limitation. These challenges have received attention from many researchers and have been addressed a few times [37, 40, 52].
Appendix D. TDC Decoder Logic

This Appendix provides several schematics of the TDC decoder as a reference.

Figure. D.1: Block diagram for a 16 to 4 decoder.

Figure. D.2: Block diagram for a 64 to 6 decoder.
Figure. D.3: Block diagram for a 128 to 7 decoder.